MICRON TECHNOLOGY, INC.

MT9LD272 B(N), MT18LD472 B(N)
2, 4 MEG x 72 BURST EDO DRAM MODULES

BURST EDO DRAM MODULE

2, 4 MEG x 72

16, 32 MEGABYTE, 3.3V, ECC, BURST EDO

FEATURES

- 168-pin, dual-in-line memory module (DIMM)
- ECC pin-out
- Buffered and non-buffered versions
- Burst EDO order, interleave or linear, programmed by executing WCBR cycle after initialization
- High-performance CMOS silicon-gate process
- Single +3.3V ±5% power supply
- All inputs and outputs are LVTTL-compatible with 5V input/output tolerance
- Refresh modes: $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ (CBR) or $\overline{\text{RAS}}$ ONLY
  2,048-cycle refresh (11 row-, 10 column-addresses) [MT9LD272 B(N)]
  2,048-cycle refresh (11 row-, 11 column-addresses) [MT18LD472 B(N)]
- Four cycle Extended Data-Out (EDO) burst accesses

OPTIONS — MARKING

- Timing
  50ns access — -5
  60ns access — -6
  70ns access — -7
- Packages
  168-pin DIMM (gold) — G
- Buffered Inputs
  Buffered — B
  Non-Buffered — BN

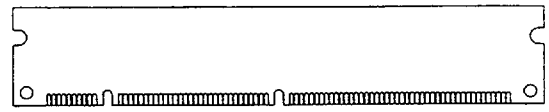
KEY TIMING PARAMETERS

SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{CAS}
-5	90ns	52ns	15ns	25ns	10ns	5ns
-6	110ns	60ns	16.6ns	28.2ns	11.6ns	5ns
-7	130ns	70ns	20ns	35ns	15ns	5ns

VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT9LD272G-xx B	2 Meg x 72 Burst EDO, Buffered
MT9LD272G-xx BN	2 Meg x 72 Burst EDO, Non-Buffered
MT18LD472G-xx B	4 Meg x 72 Burst EDO, Buffered
MT18LD472G-xx BN	4 Meg x 72 Burst EDO, Non-Buffered

PIN ASSIGNMENT (Front View)
168-Pin DIMM



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	$\overline{\text{OE2}}$	86	DQ36	128	RFU
3	DQ1	45	$\overline{\text{RAS2}}$	87	DQ37	129	NC
4	DQ2	46	$\overline{\text{CAS4}}$	88	DQ38	130	RFU
5	DQ3	47	RFU	89	DQ39	131	RFU
6	Vcc	48	$\overline{\text{WE2}}$	90	Vcc	132	$\overline{\text{PDE}}$
7	DQ4	49	Vcc	91	DQ40	133	Vcc
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	Vcc	101	DQ49	143	Vcc
18	Vcc	60	DQ24	102	Vcc	144	DQ60
19	DQ14	61	RFU	103	DQ50	145	RFU
20	DQ15	62	RFU	104	DQ51	146	RFU
21	DQ16	63	RFU	105	DQ52	147	RFU
22	DQ17	64	RFU	106	DQ53	148	RFU
23	Vss	65	DQ25	107	Vss	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	Vcc	68	Vss	110	Vcc	152	Vss
27	$\overline{\text{WE0}}$	69	DQ28	111	RFU	153	DQ64
28	$\overline{\text{CAS0}}$	70	DQ29	112	RFU	154	DQ65
29	RFU	71	DQ30	113	RFU	155	DQ66
30	$\overline{\text{RAS0}}$	72	DQ31	114	NC	156	DQ67
31	$\overline{\text{OE0}}$	73	Vcc	115	RFU	157	Vcc
32	Vss	74	DQ32	116	Vss	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	Vcc	126	B0	168	Vcc

GENERAL DESCRIPTION

The MT9LD272 B(N) and MT18LD472 B(N) are randomly accessed 16MB and 32MB solid-state memories organized in a x72 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 21/22 address bits, which are entered 11 bits (A0/B0-A10) at $\overline{RAS}$ time and 10/11 bits (A0/B0-A10) at $\overline{CAS}$ time. Two copies of address 0 (A0 and B0) are defined to allow maximum performance for 4-byte applications which interleave between two 4-byte banks. A0 is common to the DRAMs used for DQ0-DQ31, while B0 is common to the DRAMs used for DQ32-DQ63.

These DIMMs are burst access DRAM modules in which all READ and WRITE cycles occur in bursts of four. The bursts wrap around on a 4-byte boundary. This means only the two least significant bits of the $\overline{CAS}$ address are modified internally to produce each address of the burst sequence. The burst type, interleave or linear, is determined by executing a WCBR cycle (CBR cycle with $\overline{WE}$ LOW), with address A0/B0 set to either HIGH or LOW. A0/B0 LOW will program the device to execute linear bursts, A0/B0 HIGH will program the bursts to be interleave. For future compatability it is strongly recommended that the information (0010 $000x_B$) where x=A0/B0 is supplied on addresses A7-A0/B0 during the WCBR cycle. The WCBR cycle must be followed by a $\overline{RAS}$-ONLY or CBR REFRESH cycle to exit this programming mode.

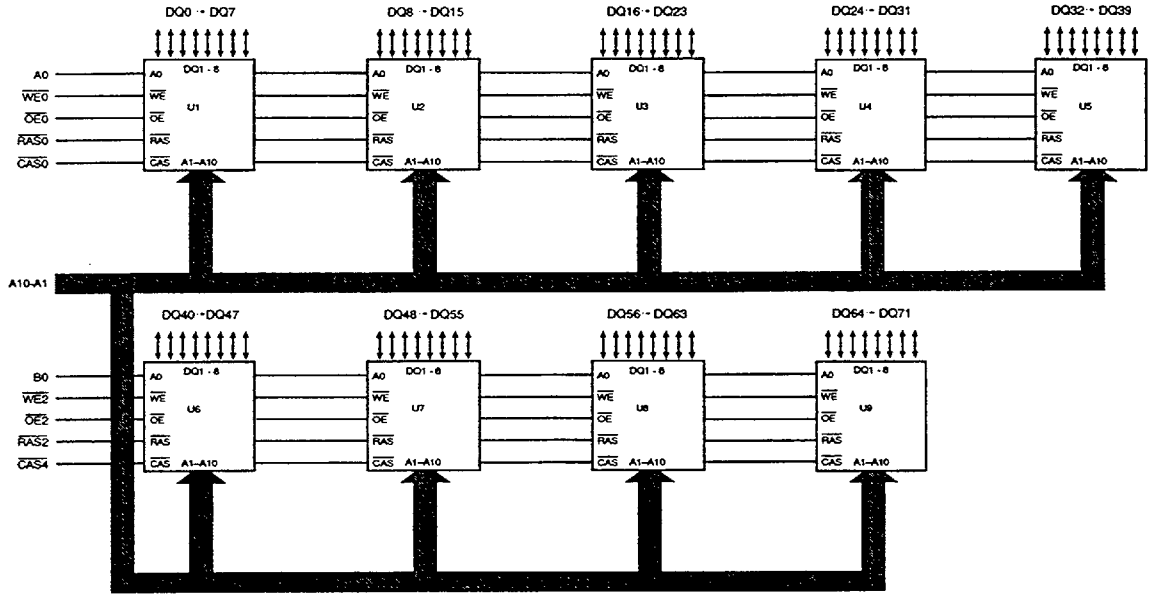
A READ or WRITE cycle is selected with the $\overline{WE}$ input during the first $\overline{CAS}$ LOW pulse of the burst. During the burst cycle the $\overline{WE}$ input must remain constant for the burst to continue. Transition of the $\overline{WE}$ input during a burst signals the burst to terminate and place the outputs in a High-Z state. After a terminated burst, the next falling edge of $\overline{CAS}$ will start a new burst access at the address present on the external address bus.

During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{CAS}$. $\overline{WE}$ must be LOW prior to $\overline{CAS}$ going LOW. This places the input/output pins in the High-Z state allowing the data-in (D) to be driven on the bus. $\overline{WE}$ must remain LOW during the burst operation for it to complete. $\overline{WE}$ going HIGH after ^tWCH from $\overline{CAS}$ LOW or before ^tWCS of the next $\overline{CAS}$ LOW terminates the burst operation and places the D/Q pins in the High-Z state.

During a READ cycle $\overline{WE}$ must be HIGH prior to $\overline{CAS}$ going LOW. $\overline{WE}$ must remain HIGH during the burst operation for it to complete. $\overline{WE}$ going LOW after ^tRCH from $\overline{CAS}$ LOW or before ^tRCS of the next $\overline{CAS}$ LOW terminates the burst operation and places the D/Q pins in the High-Z state.

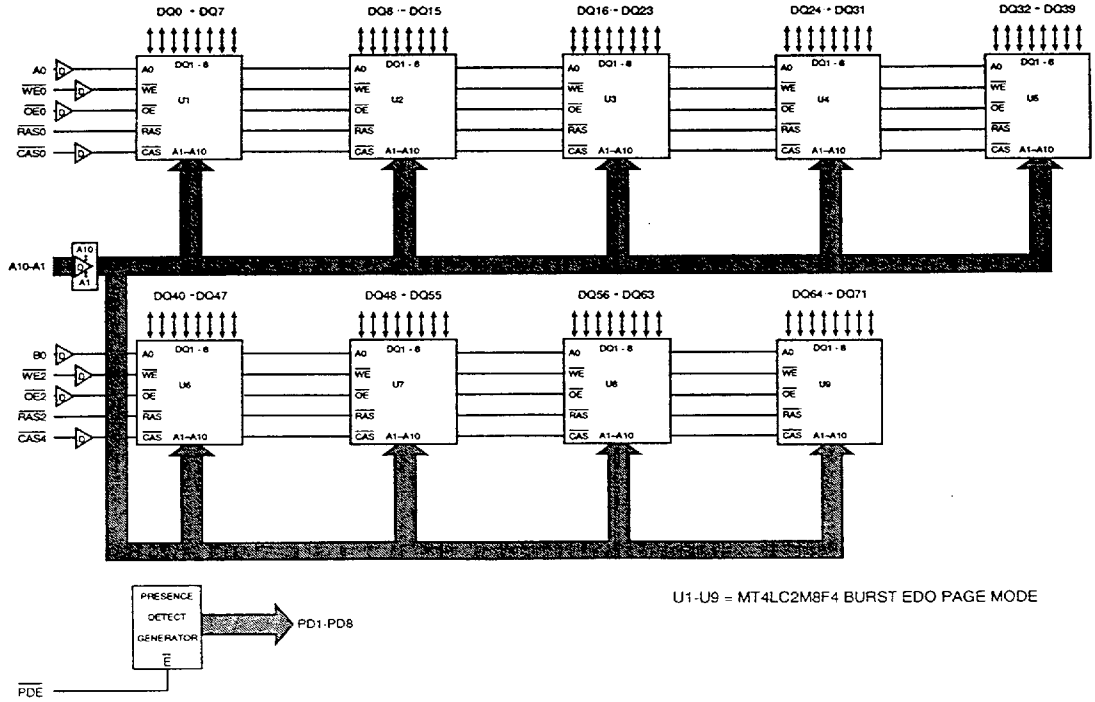
Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates burst operations in the selected row, resets the burst counter, closes that row and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next access during the $\overline{RAS}$ HIGH time.

FUNCTIONAL BLOCK DIAGRAM
MT9LD272 BN (16MB)



U1-U9 = MT4LC2M8F4 BURST EDO PAGE MODE

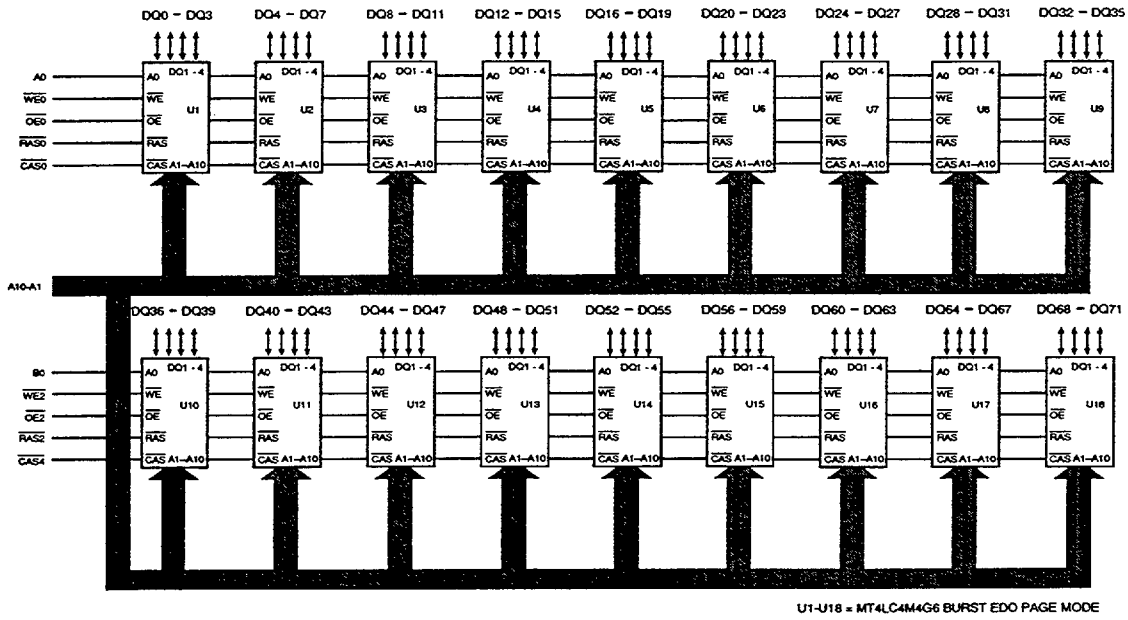
FUNCTIONAL BLOCK DIAGRAM
MT9LD272 B (16MB)



U1-U9 = MT4LC2M8F4 BURST EDO PAGE MODE

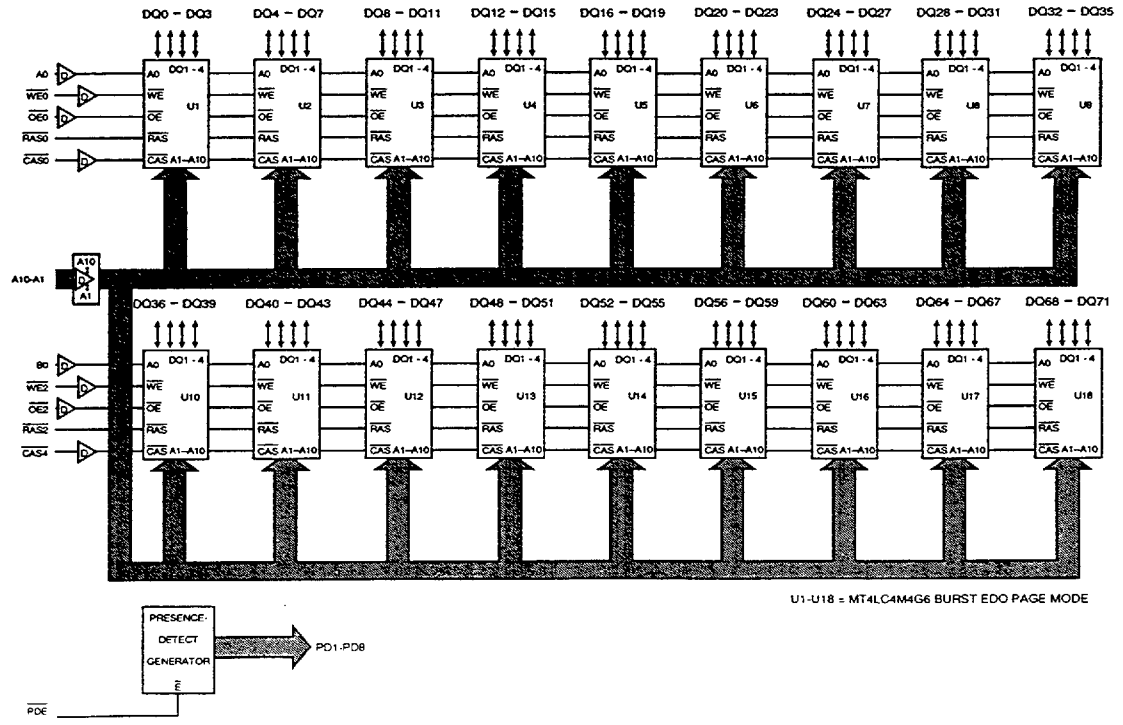
NOTE: 1. D = line buffers.

FUNCTIONAL BLOCK DIAGRAM
MT18LD472 BN (32MB)



U1-U18 = MT4LC4M4G6 BURST EDO PAGE MODE

FUNCTIONAL BLOCK DIAGRAM
MT18LD472 B (32MB)



U1-U18 = MT4LC4M4G6 BURST EDO PAGE MODE

NOTE: 1. D = line buffers.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	$\overline{RAS0}$, $\overline{RAS2}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to clock-in the 11 row-address bits. Two $\overline{RAS}$ inputs allow for one x72 bank or two x36 banks.
28, 46	$\overline{CAS0}$, $\overline{CAS4}$	Buffered Input	Column-Address Strobe: $\overline{CAS}$ is used to clock-in the 11 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles.
27, 48	$\overline{WE0}$, $\overline{WE2}$	Buffered Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. $\overline{WE0}$ controls DQ0-DQ35. $\overline{WE2}$ controls DQ36-DQ71. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	$\overline{OE0}$, $\overline{OE2}$	Buffered Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE0}$ controls DQ0-DQ35. $\overline{OE2}$ controls DQ36-DQ71. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-121, 126	A0-A10, B0	Buffered Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$. A0 is common to the DRAMs used for DQ0-DQ35 while B0 is common to the DRAMs used for DQ36-DQ71
2-5, 7-11, 13-17, 19-22, 52-53, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-106, 136-137, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ71	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ71 act as inputs to the addressed DRAM location. For READ access cycles, DQ0-DQ71 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	Buffered Output	Presence-Detect: These pins are read by the host system and tell the system the DIMM's personality. They will be either (1): NC (non-buffered) or driven to V_{OH} (buffered) or (0): Vss (non-buffered) or driven to V_{OL} (buffered).
29, 41-42, 47, 61-64, 111, 113, 115, 125, 128, 131, 145-148	RFU	—	RFU: These pins should be left unconnected (reserved for future use).
6, 18, 26, 40, 49, 59, 73, 133, 143, 157, 168	V_{CC}	Supply	Power Supply: +3.3V ± 5%

PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1, 12, 23, 32, 43, 54, 68, 78, 85, 96, 107, 116, 127, 138, 152, 162	Vss	Supply	Ground
83, 167	ID0, ID1	Output	ID bits: ID0 = DIMM type. ID1 = Refresh Mode. These pins will be either left floating (NC) or they will be grounded (Vss).
132	$\overline{PDE}$	Input	Presence-Detect Enable: $\overline{PDE}$ is the READ control for the buffered presence-detect pins. (B version only.)
24-25, 39, 50-51, 108-109, 112, 114, 122-123, 129, 130, 134-135, 150, 161	NC	—	No connect

EDO BURST MODE TRUTH TABLE

PRESENT STATE	RESULTING STATE	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES		DATA
						Row	Column	DQ0-71
Any	Idle	L→H	H	X	X	X	X	High-Z
Idle	Row Open	H→L	H	X	X	ROW	X	High-Z
Idle	CBR REFRESH	H→L	L	H	X	X	X	High-Z
Row Open	$\overline{RAS}$-ONLY REFRESH	L	H	X	X	ROW	X	High-Z
Row Open	READ burst	L	H→L	H	L	X	COL	Data-Out
Row Open	WRITE burst	L	H→L	L	X	X	COL	Data-In
READ burst	TERMINATE READ burst	L	H	H→L	X	X	X	High-Z
WRITE burst	TERMINATE WRITE burst	L	H	L→H	X	X	X	High-Z
Idle	PROGRAM burst type	H→L	L	L	X	A0[1]	X	High-Z
PROGRAM	EXIT PROGRAM MODE	H→L	L	H	X	X	X	High-Z
PROGRAM	EXIT PROGRAM MODE	L	H	X	X	ROW	X	High-Z

NOTE: 1. A WCBR cycle determines the burst sequence. A0/B0=LOW sets the burst sequence to linear, A0/B0=HIGH set the burst sequence to interleave. A8 through A10 are "don't cares." A7-A0/B0 should contain the sequence (0010 $000x_B$ where x=A0/B0) to ensure future compatability. A refresh cycle ($\overline{RAS}$ ONLY or CBR) must follow the WCBR cycle to exit the programming mode.

INTERLEAVE BURST SEQUENCE TABLE

	ADDRESSES USED		
OPERATION	A9 - A2	A1	A0/B0
First access, register external CAS address	A9 - A2	A1	A0/B0
Second access, (first burst address)	registered A9 - A2	registered A1	registered $\overline{A0/B0}$
Third access (second burst address)	registered A9 - A2	registered $\overline{A1}$	registered A0/B0
Fourth access (third burst address)	registered A9 - A2	registered $\overline{A1}$	registered $\overline{A0/B0}$

INTERLEAVE BURST ADDRESS TABLE

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X...X00	X..X01	X..X10	X..X11
X..X01	X..X00	X..X11	X..X10
X..X10	X..X11	X..X00	X..X01
X..X11	X..X10	X..X01	X..X00

LINEAR BURST ADDRESS TABLE

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X...X00	X..X01	X..X10	X..X11
X..X01	X..X10	X..X11	X..X00
X..X10	X..X11	X..X00	X..X01
X..X11	X..X00	X..X01	X..X10

PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	Module Organization	Row/Column Addresses	ID0	ID1	1	2	3	4	5	6	7	8
0MB	No module installed	x			1	1	1	1				
2MB 4MB	256K x 64/72 512K x 64/72	9/9 9/8			0	0 0	0 0	0 0				
4MB 8MB	512K x 64/72 1 Meg x 64/72	10/9 10/9			0	0 0	0 0	0 0				
8MB 16MB	1 Meg x 64/72 2 Meg x 64/72	10/10 10/10			0	0 0	1 0	0 0				
• 16MB	2 Meg x 64/72	11/10			1	0	0	1				
32MB	4 Meg x 64/72	11/11			1	0	0	1				
• 32MB	4 Meg x 64/72	12*/11*			1	1	0	1				
64MB	8 Meg x 64/72	12/11			0	0	1	0				
Page Mode		Fast Page Mode							0			
		EDO / BEDO							1			
Access Timing		80ns								0	0	
		70ns								0	1	
		60ns								1	1	
		50ns								0	0	
Refresh Control		Standard		Vss								
		Self		NC								
Data Width, Parity		x64 (No Parity)	Vss									
		x72 (Parity)	NC									
		x72, ECC	Vss									0
		x80, ECC	NC									0

NOTE: Vss = ground; 0 = Vss (non-buffered) or driven to V_{OL} (buffered); 1 = NC (non-buffered) or driven to V_{OH} (buffered).
* This addressing includes a redundant address to allow mixing of 12/10 and 11/11 DRAMs with the same presence-detect setting. The MT18LD472 B(N) uses 11/11 DRAMs.

CAPACITANCE

		MAX					
		NON-BUFFERED		BUFFERED			
PARAMETER	SYM	16MB	32MB	16MB	32MB	UNITS	NOTES
Input Capacitance: A1-A10	C_{I1}	51	96	9	9	pF	3
Input Capacitance: $\overline{WE0}$, $\overline{WE2}$, $\overline{OE0}$, $\overline{OE2}$, A0, B0	C_{I2}	29	49	9	9	pF	3
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}	34	58	34	58	pF	3
Input Capacitance: $\overline{CAS0}$, $\overline{CAS4}$	C_{I4}	24	40	9	9	pF	3
Input/Output Capacitance: DQ0-DQ71	C_{IO}	10	10	10	10	pF	3

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any I/O Pin Relative to Vss ..... -1V to +4.6V
Voltage on Inputs, NC or I/O pins
Relative to Vss ..... -1V to +5.5V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 11W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1) (V_{CC} = +3.3V ±5%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	3.13	3.47	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.0	5.5	V	2
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	2
INPUT LEAKAGE CURRENT	$\overline{CAS0}$, $\overline{CAS4}$	I_{I1}	-18	18	µA	
Any input 0V ≤ V_{IN} ≤ 6.5V	A1-A10	I_{I2}	-36	36	µA	
(All other pins not under test = 0V) for each package input	$\overline{WE0,2}$,$\overline{OE0,2}$	I_{I3}	-18	18	µA	
	$\overline{RAS0,2}$, A,B0	I_{I4}	-18	18	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V) for each package input	DQ0-DQ71	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)		V_{OL}		0.4	V	

			MAX				
PARAMETER/CONDITION	SYM	SIZE	-5	-6	-7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	16MB 32MB	18 36	18 36	18 36	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	16MB 32MB	4.5 9	4.5 9	4.5 9	mA	
OPERATING CURRENT: Closed Row Burst READ/WRITE Average power supply current; (^tPC = ^tPC [MIN]; 50% duty cycle on $\overline{RAS}$; Open Row, four Cycle Burst, Close Row)	I_{CC3}	16MB 32MB	990 1,980	900 1,800	810 1,620	mA	5
OPERATING CURRENT: Open Row Burst READ/WRITE Average power supply current (Alternating four cycle burst followed by four cycles of inactivity; ^tPC = ^tPC [MIN])	I_{CC4}	16MB 32MB	1,170 2,340	1,080 2,160	990 1,980	mA	5
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current $\overline{CAS}$ = V_{IH}; ^tRAS = ^tRAS [MIN]; ^tRP = ^tRP [MIN])	I_{CC5}	16MB 32MB	1,350 2,700	1,260 2,520	1,170 2,340	mA	4
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Cycling: ^tRAS = ^tRAS [MIN]; ^tRP = ^tRP [MIN])	I_{CC6}	16MB 32MB	1,350 2,700	1,260 2,520	1,170 2,340	mA	4, 6

NON-BUFFERED (BN) VERSION
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 7, 8, 9, 10, 15) (Vcc = +3.3V ±5%)

AC CHARACTERISTICS - NON-BUFFERED		-5		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from $\overline{CAS}$	tAA		25		28.2		35	ns	12
Column-address setup time	tASC	1.5		1.5		1.5		ns	
Row-address setup time	tASR	1.5		1.5		1.5		ns	
Burst terminate hold time	tBTH	3		3		3		ns	
Output disable from burst terminate	tBTHZ	7	13	7	13	7	13	ns	13, 16
Access time from $\overline{CAS}$	tCAC		10		11.6		15	ns	
Column-address hold time	tCAH	8.5		8.5		8.5		ns	
$\overline{CAS}$ pulse width	tCAS	5	10,000	5	10,000	5	10,000	ns	
$\overline{CAS}$ hold time (CBR or WCBR)	tCHR	15		15		15		ns	6
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		ns	13
Data Hold time from $\overline{CAS}$ LOW	tCOH	3		3		3		ns	
$\overline{CAS}$ precharge time	tCP	5		5		5		ns	
$\overline{CAS}$ precharge time (CBR or WCBR)	tCPN	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	10		10		10		ns	
$\overline{CAS}$ LOW to $\overline{RAS}$ HIGH (WRITE only)	tCRW	15		16.6		20		ns	
$\overline{CAS}$ setup time (CBR or WCBR)	tCSR	10		10		10		ns	6
Data-in hold time	tDH	5		5		5		ns	
Data-in setup time	tDS	3		3		3		ns	
Ouput Disable	tOD	4	10	4	10	4	15	ns	13
Ouput Enable access time	tOEA		10		12		15	ns	
Ouput Enable hold (only near $\overline{CAS}$)	tOEH	5		5		5		ns	
$\overline{OE}$ to output in Low-Z	tOELZ	3		3		3		ns	13
$\overline{OE}$ HIGH pulse width	tOEP	10		10		10		ns	
Ouput Enable setup (only near $\overline{CAS}$)	tOES	3		3		3		ns	
Output buffer turn-off delay	tOFF	4	10	4	10	4	15	ns	13
Burst EDO cycle time	tPC	15		16.6		20			
Access time from $\overline{RAS}$	tRAC		52		60		70	ns	
Row-address hold time	tRAH	8.5		8.5		8.5		ns	
$\overline{RAS}$ pulse width	tRAS	50	125,000	60	125,000	70	125,000	ns	
Random Read or Write cycle time	tRC	90		110		130			
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD1	15		16.6		20		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD2	40		46.6		55		ns	
Read command hold time	tRCH	5		5		5		ns	
Read command setup time	tRCS	3		4		5		ns	
Refresh period (1,024 cycles)	tREF		16		16		16	ms	
Refresh period (2,048 cycles)	tREF		32		32		32	ms	

NON-BUFFERED (BN) VERSION
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 7, 8, 9, 10, 15) (Vcc = +3.3V ±5%)

AC CHARACTERISTICS - NON-BUFFERED		-5		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		ns	
$\overline{RAS}$ hold time	tRSH	0		0		0		ns	
Transition time (rise or fall)	tT	1.5	50	1.5	50	1.5	50	ns	
Burst Terminate pulse width	tTP	6		6		8		ns	14
Write command hold time	tWCH	5		5		5		ns	
$\overline{WE}$ command setup time	tWCS	3		4		5		ns	
Ouput Disable from $\overline{WE}$ LOW	tWHZ	4	10	4	10	4	15	ns	13, 16
$\overline{WE}$ hold time (CBR or WCBR)	tWRH	10		10		10		ns	
$\overline{WE}$ setup time (CBR or WCBR)	tWRP	10		10		10		ns	

BUFFERED (B) VERSION
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 7, 8, 9, 10, 15) (Vcc = +3.3V ±5%)

AC CHARACTERISTICS - BUFFERED		-5		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from $\overline{CAS}$	tAA		30		33.2		40	ns	12, 19
Column-address setup time	tASC	3.5		3.5		3.5		ns	17
Row-address setup time	tASR	6.5		6.5		6.5		ns	19
Burst terminate hold time	tBTH	3		3		3		ns	
Output disable from burst terminate	tBTHZ	9	18	9	18	9	18	ns	13,16,21
Access time from $\overline{CAS}$	tCAC		15		16.6		20	ns	19
Column-address hold time	tCAH	13.5		13.5		13.5		ns	19
$\overline{CAS}$ pulse width	tCAS	5	10,000	5	10,000	5	10,000	ns	
$\overline{CAS}$ hold time (CBR or WCBR)	tCHR	13		13		13		ns	6, 18
$\overline{CAS}$ to output in Low-Z	tCLZ	5		5		5		ns	13, 17
Data Hold time from $\overline{CAS}$ LOW	tCOH	5		5		5		ns	17
$\overline{CAS}$ precharge time	tCP	5		5		5		ns	
$\overline{CAS}$ precharge time (CBR or WCBR)	tCPN	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	15		15		15		ns	19
$\overline{CAS}$ LOW to $\overline{RAS}$ HIGH (WRITE only)	tCRW	15		16.6		20		ns	
$\overline{CAS}$ setup time (CBR or WCBR)	tCSR	12		12		12		ns	6, 17
Data-in hold time	tDH	10		10		10		ns	19
Data-in setup time	tDS	1		1		1		ns	18
Ouput Disable	tOD	4	10	4	10	4	15	ns	13
Ouput Enable access time	tOEA		15		17		20	ns	19
Ouput Enable hold (only near $\overline{CAS}$)	tOEH	3		3		3		ns	18
$\overline{OE}$ to output in Low-Z	tOELZ	8		8		8		ns	13, 19
$\overline{OE}$ HIGH pulse width	tOEP	10		10		10		ns	
Ouput Enable setup (only near $\overline{CAS}$)	tOES	3		3		3		ns	
Output buffer turn-off delay	tOFF	6	15	6	15	6	20	ns	13, 21
Burst EDO cycle time	tPC	15		16.6		20		ns	
$\overline{PDE}$ to valid presence-detect data	tPD		10		10		10	ns	22
$\overline{PDE}$ inactive to presence-detect inactive	tPDOFF	2		2		2		ns	23
Access time from $\overline{RAS}$	tRAC		52		60		70	ns	
Row-address hold time	tRAH	6.5		6.5		6.5		ns	18
$\overline{RAS}$ pulse width	tRAS	50	125,000	60	125,000	70	125,000	ns	
Random Read or Write cycle time	tRC	90		110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD1	13		14.6		18		ns	18
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD2	38		44.6		53		ns	18
Read command hold time	tRCH	7		7		7		ns	17
Read command setup time	tRCS	5		6		7		ns	17
Refresh period (1,024 cycles)	tREF		16		16		16	ms	
Refresh period (2,048 cycles)	tREF		32		32		32	ms	

BUFFERED (B) VERSION
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 7, 8, 9, 10, 15) (Vcc = +3.3V ±5%)

AC CHARACTERISTICS - BUFFERED		-5		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{RAS}$ precharge time	^tRP	30		40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	5		5		5		ns	
$\overline{RAS}$ hold time	^tRSH	5		5		5		ns	19
Transition time (rise or fall)	^tT	1.5	50	1.5	50	1.5	50	ns	
Burst Terminate pulse width	^tTP	6		6		8		ns	14
Write command hold time	^tWCH	10		10		10		ns	19
$\overline{WE}$ command setup time	^tWCS	5		6		7		ns	17
Ouput Disable from $\overline{WE}$ LOW	^tWHZ	6	15	6	15	6	20	ns	13,16,21
$\overline{WE}$ hold time (CBR or WCBR)	^tWRH	8		8		8		ns	18
$\overline{WE}$ setup time (CBR or WCBR)	^tWRP	12		12		12		ns	17

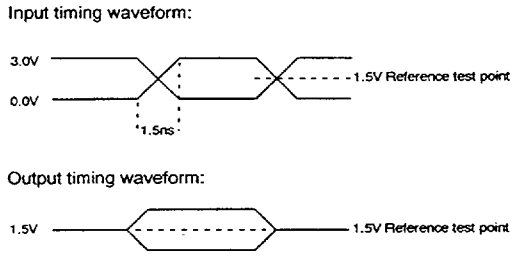


Figure 1
TIMING SPECIFICATIONS

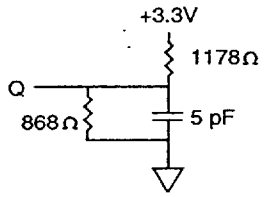


Figure 2
HIGH-Z OUTPUT LOAD

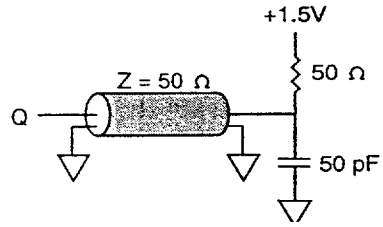


Figure 3
AC TIMING OUTPUT LOAD EQUIVALENT

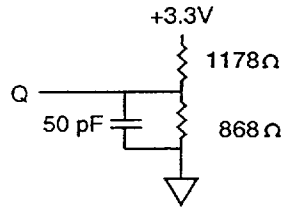
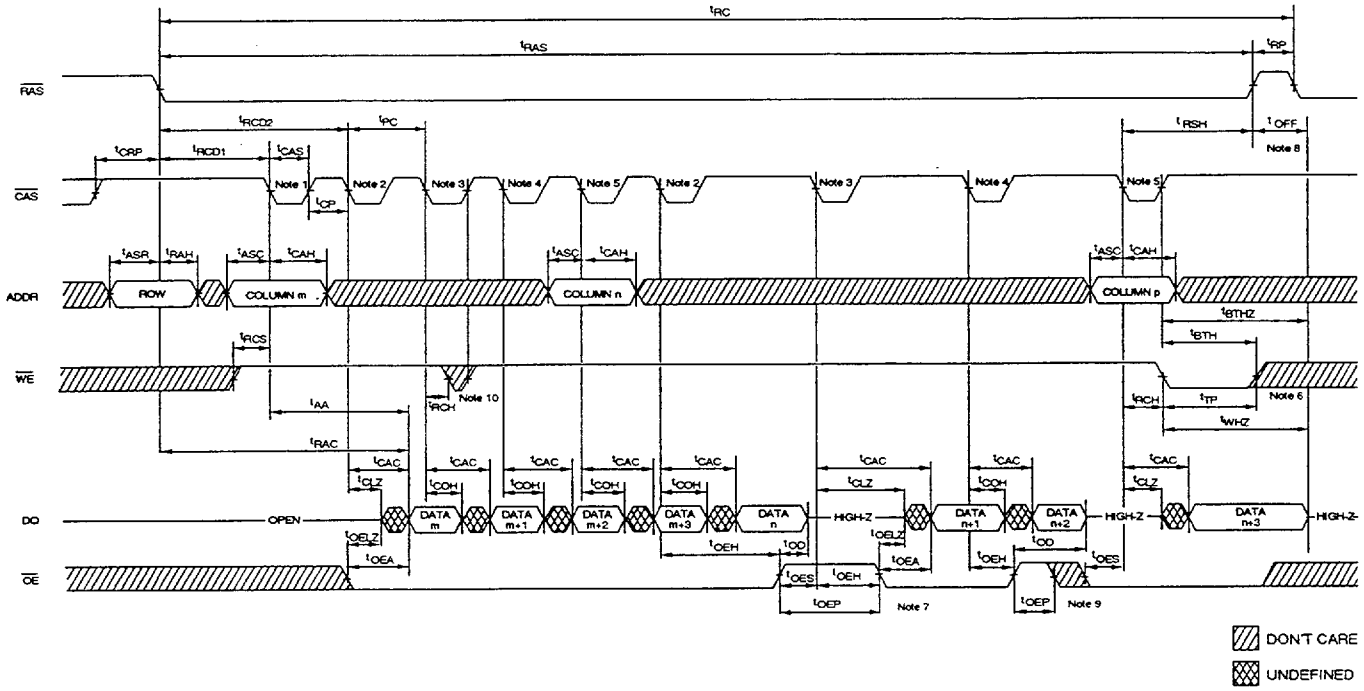


Figure 4
OUTPUT LOAD EQUIVALENT

NOTES

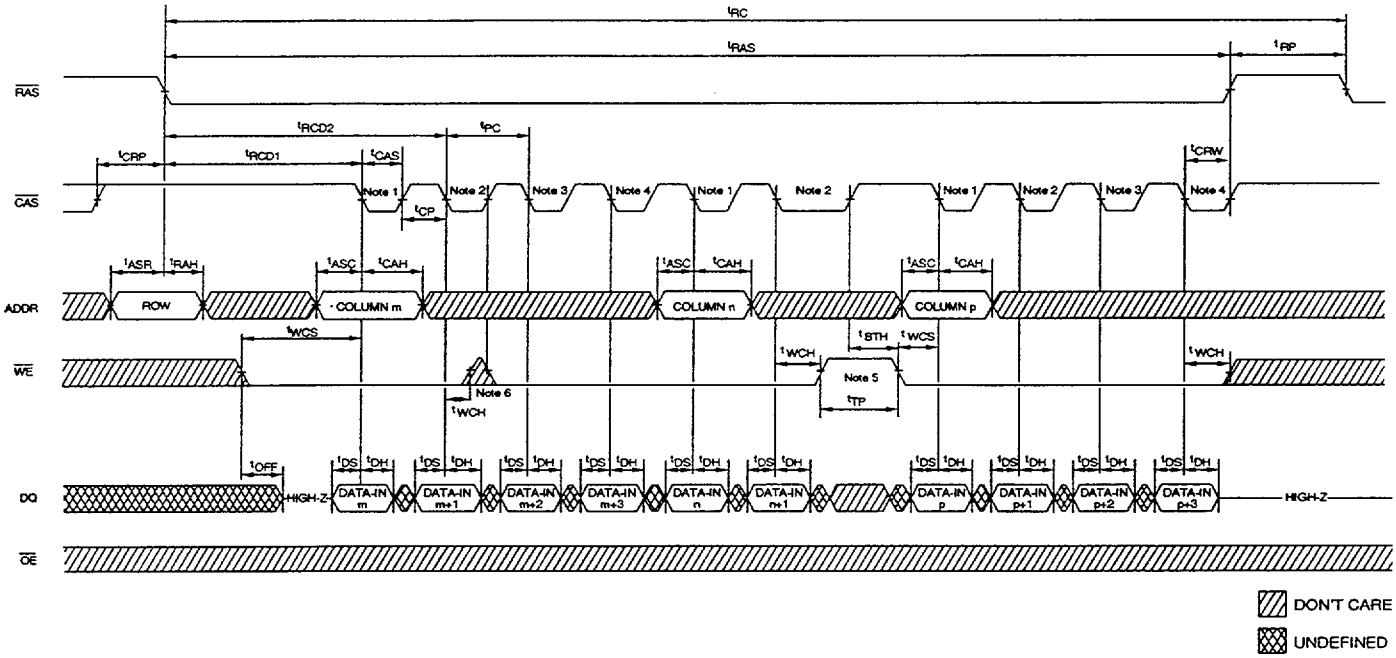
1. All voltages referenced to Vss.
2. Input Power-up: $V_{IH} \leq +5.5V$ and $V_{CC} \leq +3.13V$ for $t \leq 200ms$.
3. This parameter is sampled. $V_{CC} = 3.3V \pm 5\%$; $f = 1$ MHz.
4. I_{CC} is dependent on cycle rates.
5. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum ^tPC and 50 percent duty cycle. The outputs are open.
6. Enables on-chip refresh and address counters.
7. Initialization consists of an initial pause of 100µs after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH). This sequence must be executed before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded. A WCBR cycle must be executed to initalize the burst type, interleave or linear followed by a $\overline{RAS}$-ONLY or CBR REFRESH cycle.
8. AC characteristics assume $^tT = 1.5ns$.
9. All output timings are referenced to 1.5V and all input timings are referenced to 1.5V, unless otherwise specified. Inputs must be driven to the appropriate voltage levels indicated by the corresponding timing diagrams when AC specifications are measured, as shown in Figure 1.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. NC pins are assumed to be left floating and are not tested for leakage.
12. ^tAA is a calculated specification which is the sum of ^tPC and ^tCAC.
13. Output loading is specified with $C_L = 5pF$ as in Figure 2. Transition is measured ±200mV from steady state voltage. These parameters are sampled.
14. Applies only during burst termination operation.
15. AC output loading is specified with $C_L = 50pF$ as in Figure 3. Figure 4 is shown for reference. Transition is measured at the 1.5V reference level.
16. The DQs will continue to drive data out until both ^tBTHZ (MIN) and ^tWHZ (MIN) have been satisfied and will reach the High-Z state once both ^tBTHZ (MAX) and ^tWHZ (MAX) have been satisfied.
17. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
18. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
19. A +5ns timing skew from the DRAM to the module resulted from the addition of line drivers.
20. A -2ns (MIN) and a -5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
21. A +2ns (MIN) and a +5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
22. Measured with the specified current load and 100pf.
23. ^tPDOFF MAX is determined by the pull-up resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent DIMM position.
24. B version only.

BURST EDO READ CYCLE



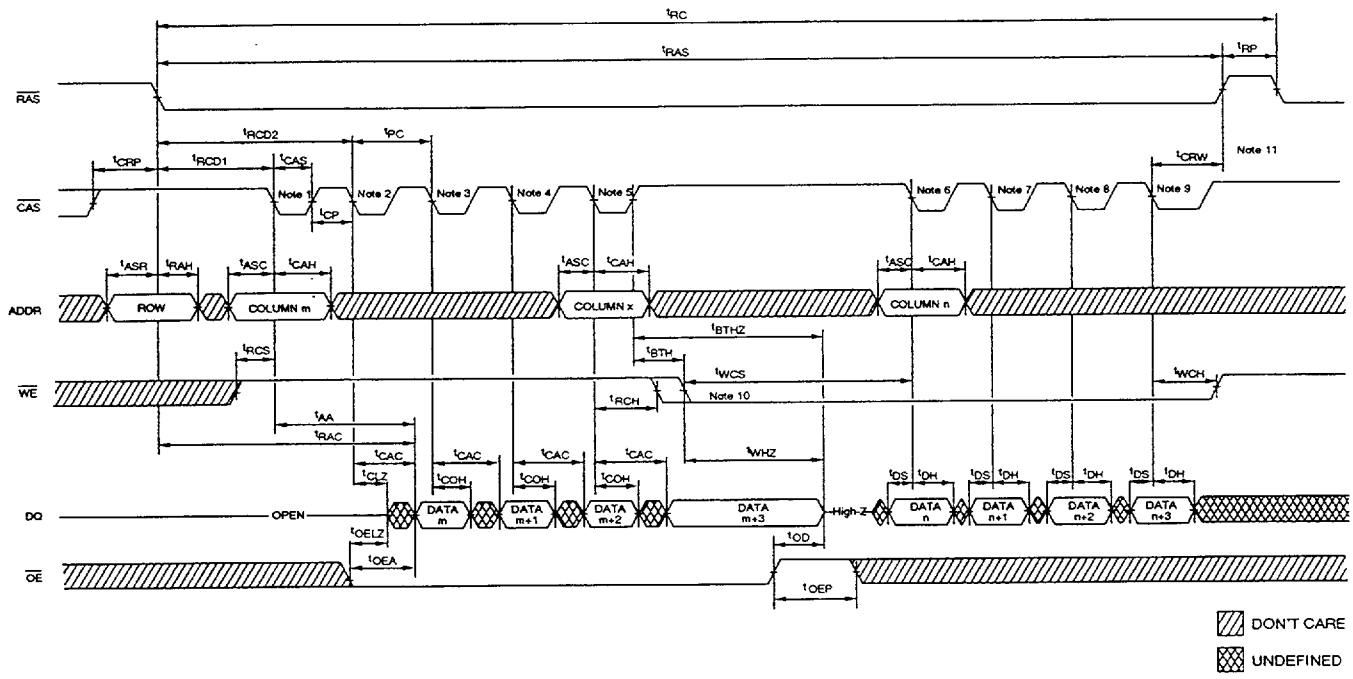
NOTE:
1. Latch column address; start READ cycle.
2. Output data 1; increment burst counter.
3. Output data 2; increment burst counter.
4. Output data 3; increment burst counter.
5. Output data 4; latch column address; start READ cycle.
6. $\overline{WE}$ transitioning LOW will terminate the burst and reset the burst counter provided ^{t}TP and ^{t}BTH are satisfied. The DQs will continue to drive data out until both ^{t}BTHZ (MIN) and ^{t}WHZ (MIN) have been satisfied and will reach the High-Z state once both ^{t}BTHZ (MAX) and ^{t}WHZ (MAX) have been satisfied.
7. Once $\overline{OE}$ transitions LOW after $\overline{CAS}$ transitions LOW, Note 9 applies if $\overline{OE}$ transitions back HIGH.
8. The combination of $\overline{RAS}$ and $\overline{CAS}$ HIGH close the row and place the DQs in the High-Z state. ^{t}OFF is measured from the last signal ($\overline{RAS}$ or $\overline{CAS}$) that transitions HIGH.
9. When $\overline{OE}$ transitions HIGH, the DQ pins are placed in the High-Z state and will remain in the High-Z state until another $\overline{CAS}$ LOW transition occurs, regardless of the state of $\overline{OE}$.
10. $\overline{WE}$ transitioning LOW and returning HIGH prior to $\overline{CAS}$ going HIGH will not terminate the burst.

BURST EDO WRITE CYCLE



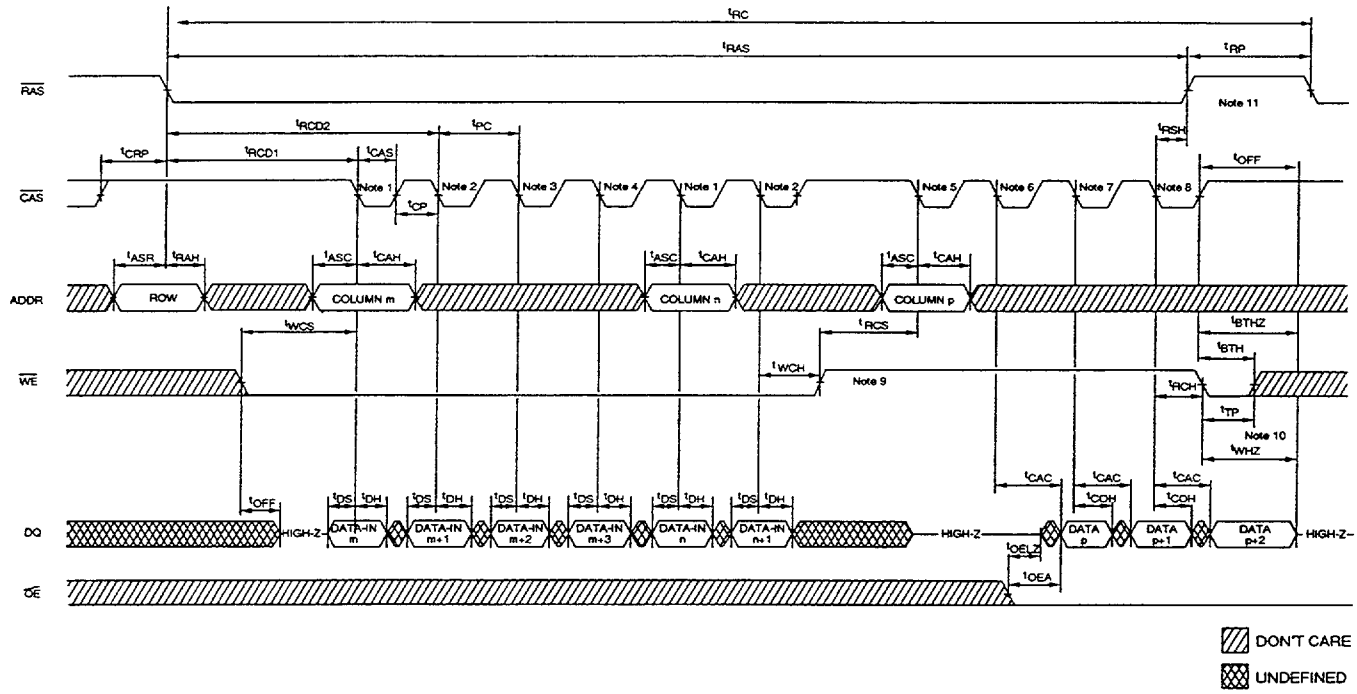
NOTE:
1. Latch column address; start burst WRITE cycle; write data 1.
2. Increment burst counter; write data 2.
3. Increment burst counter; write data 3.
4. Increment burst counter; write data 4.
5. $\overline{WE}$ transitioning HIGH will terminate the burst and reset the burst counter provided ^{t}TP and ^{t}BTH are satisfied.
6. $\overline{WE}$ transitioning HIGH and returning LOW prior to $\overline{CAS}$ going HIGH will not terminate the burst.

BURST EDO READ/WRITE CYCLE



NOTE:
1. Latch column address; start burst READ cycle.
2. Output data 1; increment burst counter.
3. Output data 2; increment burst counter.
4. Output data 3; increment burst counter.
5. Output data 4; latch column address; start burst READ cycle.
6. Latch column address; start burst WRITE cycle; write data 1.
7. Increment burst counter; write data 2.
8. Increment burst counter; write data 3.
9. Increment burst counter; write data 4.
10. $\overline{WE}$ transitioning LOW will terminate the burst and reset the burst counter provided ^{t}TP and ^{t}BTH are satisfied. ^{t}TP is met by the READ burst being terminated by a WRITE burst. The DQs will continue to drive data out until both $^{t}BTHZ$ (MIN) and ^{t}WHZ (MIN) have been satisfied and will reach the High-Z state once both $^{t}BTHZ$ (MAX) and ^{t}WHZ (MAX) have been satisfied.
11. The combination of $\overline{RAS}$ and $\overline{CAS}$ HIGH close the row and place the DQ pins in the High-Z state.

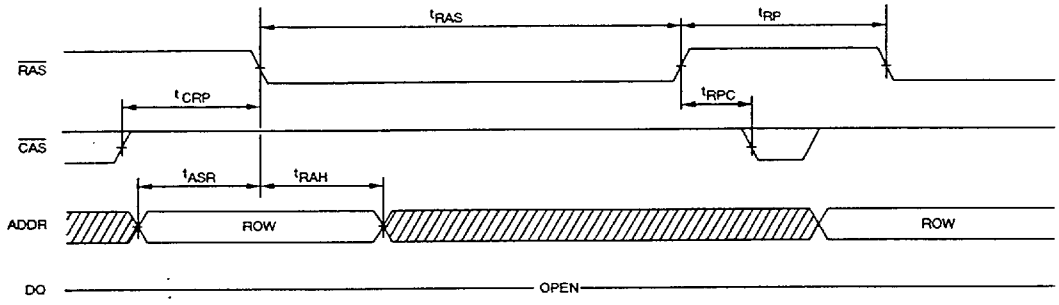
BURST EDO WRITE/READ CYCLE



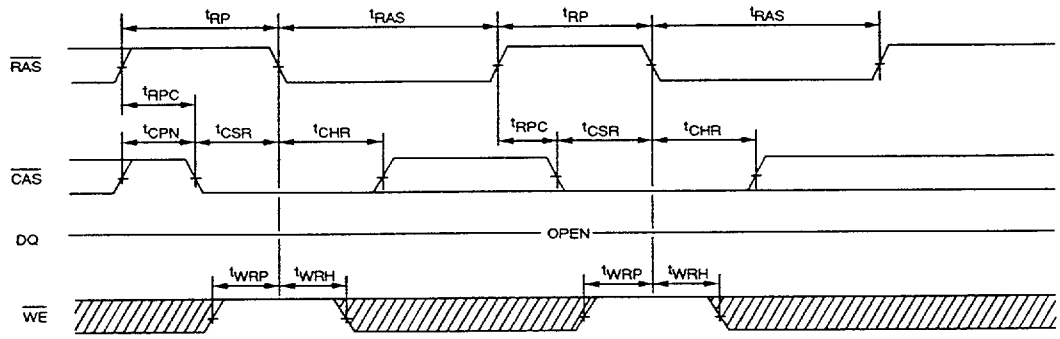
NOTE:

1. Latch column address; start burst WRITE cycle; write data 1.
2. Increment burst counter; write data 2.
3. Increment burst counter; write data 3.
4. Increment burst counter; write data 4.
5. Latch column address; start burst READ cycle.
6. Output data 1; increment column address.
7. Output data 2; increment column address.
8. Output data 3; increment column address.
9. $\overline{WE}$ transitioning HIGH will terminate the burst and reset the burst counter. The ^{t}BTH time is not required as it is satisfied by ^{t}RCS; ^{t}TP is met by the WRITE burst being terminated by a READ burst.
10. $\overline{WE}$ transitioning LOW will terminate the burst and reset the burst counter provided ^{t}TP and ^{t}BTH are satisfied. The DQs will continue to drive data out until both ^{t}BTHZ (MIN) and ^{t}WHZ (MIN) have been satisfied and will reach the High-Z state once both ^{t}BTHZ (MAX) and ^{t}WHZ (MAX) have been satisfied.
11. The combination of $\overline{RAS}$ and $\overline{CAS}$ HIGH close the row and place the DQ pins in the High-Z state. ^{t}OFF is measured from the last signal ($\overline{RAS}$ or $\overline{CAS}$) that transitions HIGH.

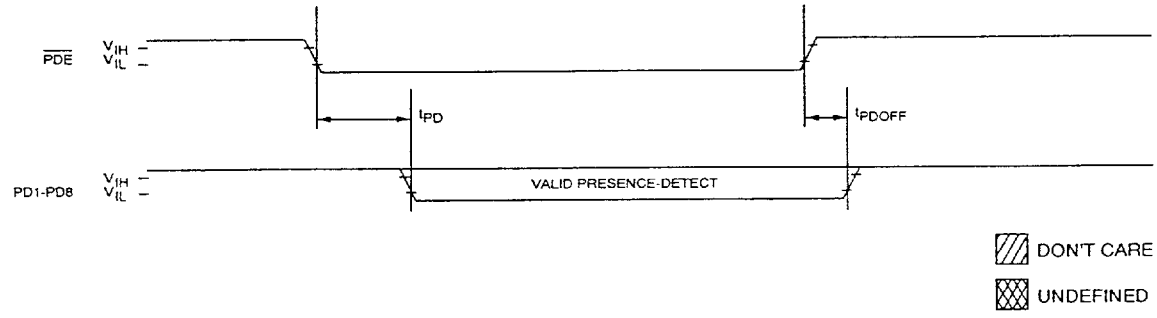
RAS-ONLY REFRESH CYCLE



CBR REFRESH CYCLE

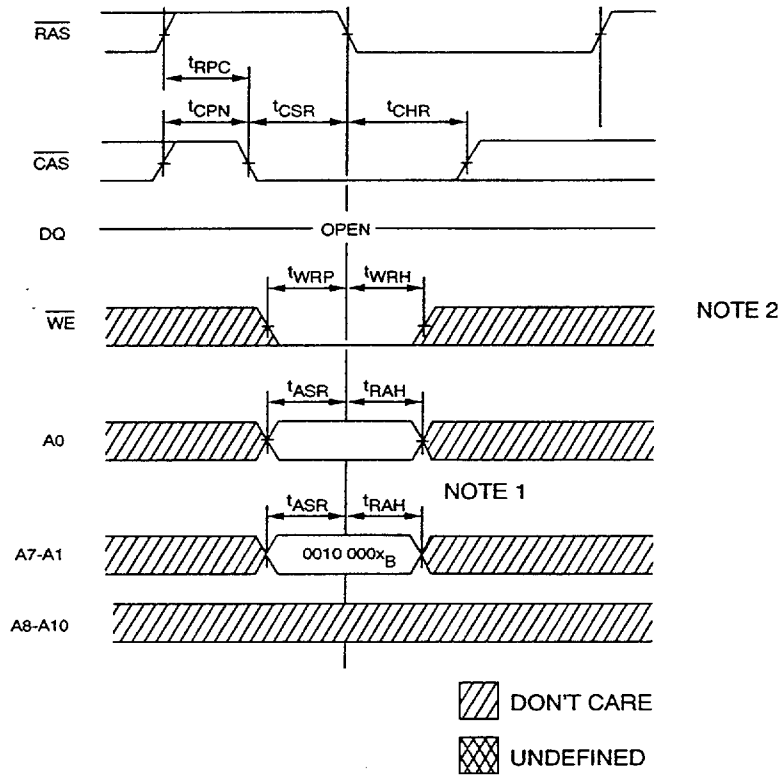


PRESENCE-DETECT READ CYCLE [24]



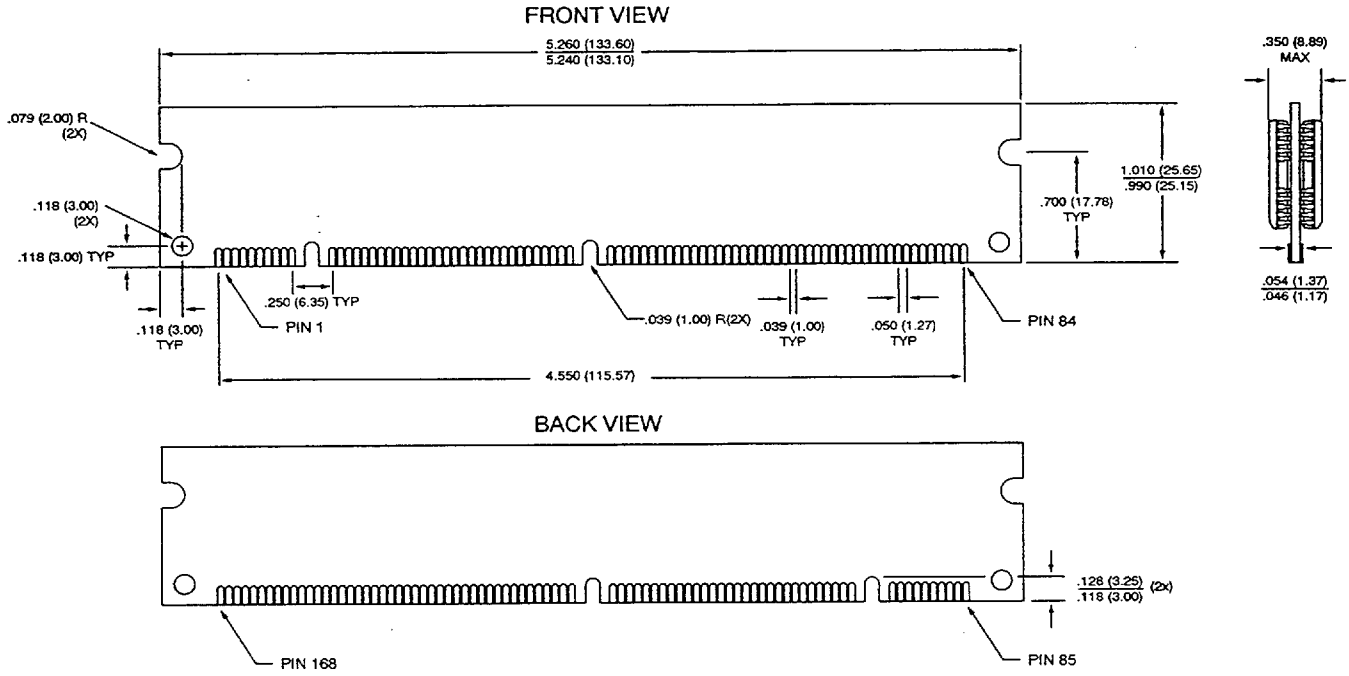
NOTE: 1. CBR REFRESH is recommended for all new designs to insure compatibility with future generation DRAMs. Micron and JEDEC recommend CBR REFRESH as the preferred method of refresh for the 64 Meg DRAM generation and beyond.
2. PD pins must be pulled HIGH at next level of assembly.

WCBR PROGRAM CYCLE



NOTE:
1. A0/B0 LOW sets the burst sequence to linear bursts. A0/B0 HIGH sets the burst sequence to interleave bursts. Addresses A8 through A10 are "don't cares." Addresses A7-A0 should contain the state of (0010 $000x_B$ where x=A0/B0) to ensure future compatability. The burst sequence will remain set until the device power is interrupted or another WCBR cycle is executed.
2. A $\overline{RAS}$-ONLY or CBR REFRESH cycle must be executed after the WCBR cycle to exit the programming mode.

168-Pin DIMM



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.