

LH534000B

CMOS 4M (512K × 8 / 256K × 16)
Mask-Programmable ROM

FEATURES

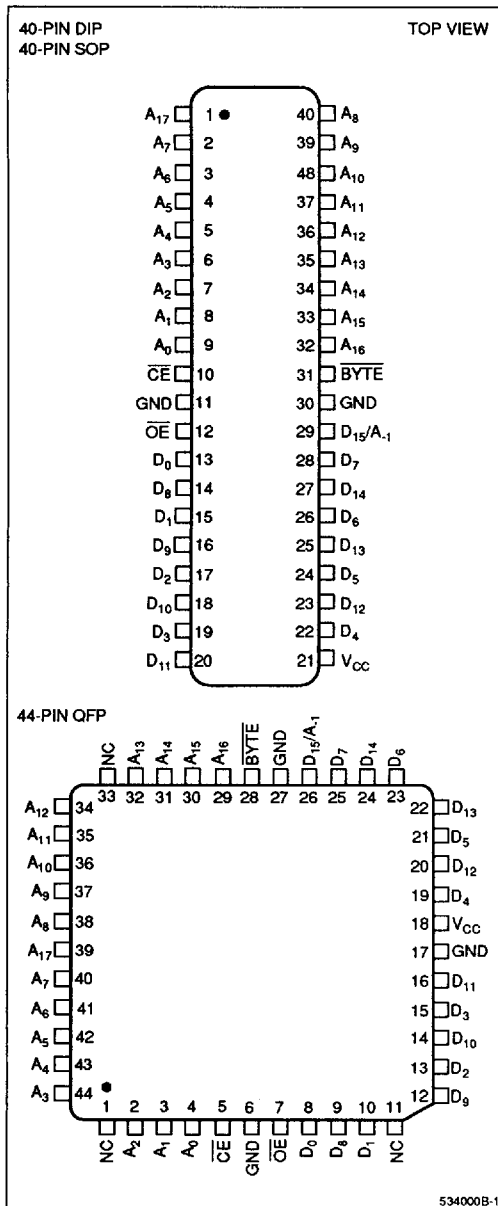
- Memory organization selection:
524,288 × 8 bit (byte mode)
262,144 × 16 bit (word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 200 ns (MAX.)
- Low-power consumption:
Operating: 275 mW (MAX.)
Standby: 550 μ W (MAX.)
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs

- Single +5 V power supply
- Packages:
40-pin, 600-mil DIP
40-pin, 525-mil SOP
48-pin, 12 × 18 mm² TSOP (Type I)
44-pin, 14 × 14 mm² QFP
44-pin, 10 × 10 mm² QFP
- X16 word-wide pinout

DESCRIPTION

The LH534000B is a 4M bit mask-programmable ROM with two programmable memory organizations of byte and word modes. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS





SIGNAL	PIN NAME	NOTE
A ₁	Address input (BYTE mode)	1
A ₀ - A ₁₇	Address input	
D ₀ - D ₁₅	Data output	
$\overline{CE}$	Chip enable input	

SIGNAL	PIN NAME	NOTE
$\overline{\text{OE}}$	Chip enable input	
$\overline{\text{BYTE}}$	Byte/word mode switch	
V _{CC}	Power supply (+5 V)	
GND	Ground	

1. D₁₅/A-1 pin becomes LSB address input (A-1) when the bit configuration is set in byte mode, and data output (D₁₅) when in word mode. BYTE input pin selects bit configuration.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	BYTE	A ₁	MODE	D ₀ - D ₇	D ₈ - D ₁₅	SUPPLY CURRENT
H	X	X	X	Non selected	High-Z		Standby (<i>I</i> _{SB})
L	H	X	X	Non selected	High-Z		Operating (<i>I</i> _{CC})
L	L	H	Inhibit	Word	D ₀ - D ₇	D ₈ - D ₁₅	Operating (<i>I</i> _{CC})
L	L	L	L	Byte	D ₀ - D ₇	High-Z	Operating (<i>I</i> _{CC})
L	L	L	H	Byte	D ₈ - D ₁₅	High-Z	Operating (<i>I</i> _{CC})

NOTES:

1. X = H or L
2. The input state of **BYTE** must not be changed during operation. The **BYTE** pin must be set to either HIGH or LOW.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V _{CC}	-0.3 to +7.0	V	1
Input voltage	V _{IN}	-0.3 to V _{CC} +0.3	V	
Output voltage	V _{OUT}	-0.3 to V _{CC} +0.3	V	
Operating temperature	T _{opr}	0 to +70	°C	
Storage temperature	T _{stg}	-55 to +150	°C	

NOTE:

1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V _{IL}		-0.3		0.8	V	
Input 'High' voltage	V _{IH}		2.2		V _{CC} +0.3	V	
Output 'Low' voltage	V _{OL}	I _{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V _{OH}	I _{OH} = -400 μA	2.4			V	
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}			10	μA	
Output leakage current	I _{LO}	V _{OUT} = 0 V to V _{CC}			10	μA	1
Operating current	I _{CC1}	t _{RC} = 200 ns			50	mA	2
	I _{CC2}	t _{RC} = 1 μs			45		
	I _{CC3}	t _{RC} = 200 ns			45	mA	3
	I _{CC4}	t _{RC} = 1 μs			40		
Standby current	I _{SB1}	$\overline{CE} = V_{IH}$			3	mA	
	I _{SB2}	$\overline{CE} = V_{CC} - 0.2 V$			100	μA	

NOTES:

1. $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$
2. $V_{IN} = V_{IH}/V_{IL}$, $\overline{CE} = V_{IL}$, outputs open
3. $V_{IN} = (V_{CC} - 0.2 V)$ or 0.2 V, $\overline{CE} = 0.2 V$, outputs open

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

AC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0\text{ to }+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200			ns	
Address access time	t_{AA}			200	ns	
Chip enable access time	t_{ACE}			200	ns	
Output enable delay time	t_{OE}			80	ns	
Output hold time	t_{OH}	10			ns	
CE to output in High-Z	t_{CHZ}			80	ns	1
OE to output in High-Z	t_{OHZ}			80	ns	

NOTE:

1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE ($V_{CC} = 5\text{ V} \pm 10\%$, $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

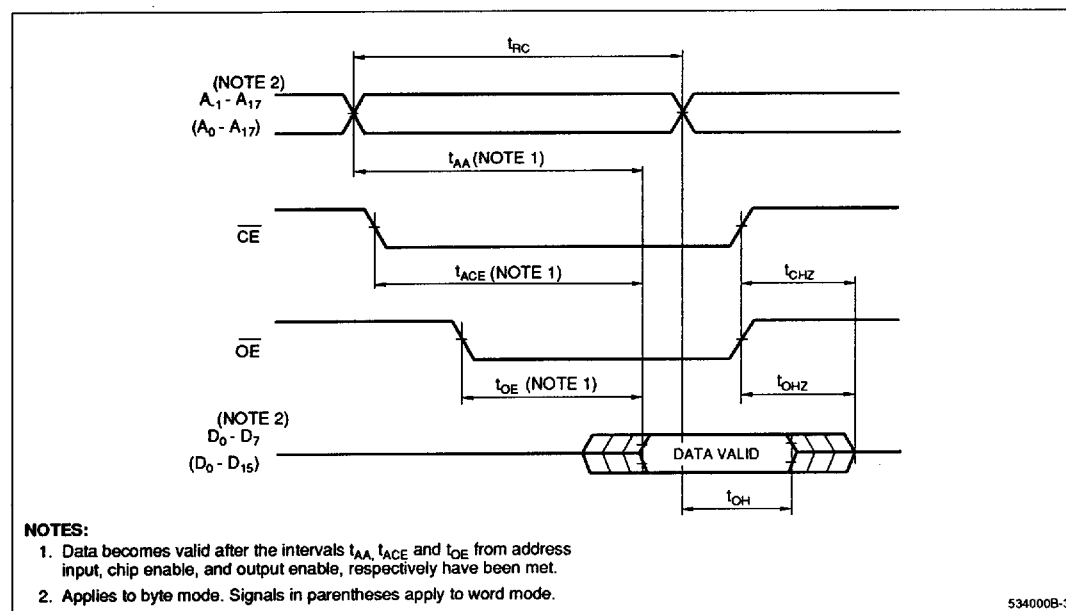


Figure 4. Timing Diagram

ORDERING INFORMATION

<u>LH534000B</u>	<u>X</u>	<u>- ##</u>	
Device Type	Package	Speed	
		20 200	Access Time (ns)
			{ D 40-pin, 600-mil DIP (DIP40-P-600)
			{ N 40-pin, 525-mil SOP (SOP40-P-525)
			{ T 48-pin, 12 x 18 mm ² TSOP (TSOP48-P-1218: Type I)
			{ Z 44-pin, 10 x 10 mm ² QFP (QFP44-P-1010)
			{ M 44-pin, 14 x 14 mm ² QFP (QFP44-P-1414)
			CMOS 4M (512K x 8 or 256K x 16) Mask Programmable ROM
Example: LH534000BD-20 (CMOS 4M (512K x 8) Mask Programmable ROM, 200 ns, 40-pin, 600-mil DIP)			

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