

DESCRIPTION

The HY5117404A is the new generation and fast dynamic RAM organized 4,194,304 x 4-bit. The HY5117404A utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY5117404A to be packaged in a standard 24/26 pin plastic SOJ, TSOP-II and Reverse TSOP-II.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 5V $\pm 10\%$ tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- Low power dissipation
Max. battery back-up 2.75mW (SL-part)
Max. CMOS standby 2.2mW (SL-part)
5.5mW
Max. TTL standby 11.0mW
Max. operating

Speed	Power
60	660mW
70	550mW
80	495mW

- Single power supply of 5V $\pm 10\%$
- TTL compatible inputs and outputs
- Fast access and cycle time

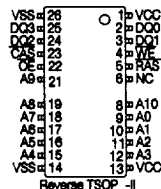
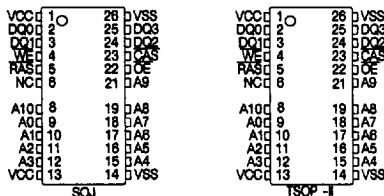
Speed	t _{RAC}	t _{CAC}	t _{HPC}
60	60ns	15ns	25ns
70	70ns	18ns	30ns
80	80ns	20ns	35ns

- Extended Data Out Operation
- Multi-bit test capability
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden refresh and Self Refresh capability
- 2048 refresh cycles / 256ms (SL-part)
2048 refresh cycles / 32ms

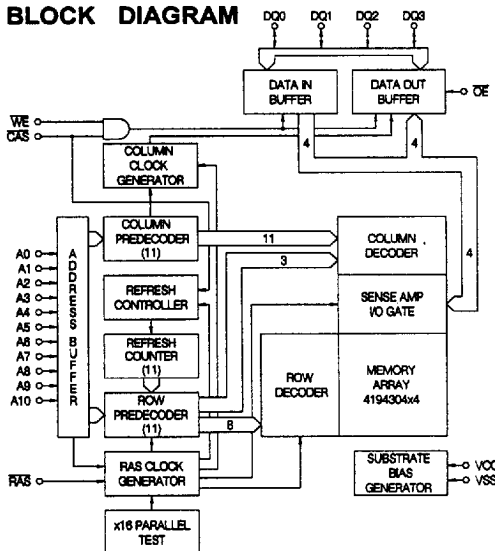
PIN DESCRIPTION

RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
A0-A10	Address input
DQ0-DQ3	Data Input/Output
Vcc	Power (+5V)
Vss	Ground

PIN CONNECTION



BLOCK DIAGRAM



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1AD38-10-MAY95

ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 125	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
VCC	Voltage on Vcc Relative to Vss	-1.0 to 7.0	V
Ios	Short Circuit Output Current	50	mA
PD	Power Dissipation	1.0	W
TSOLDER	Soldering Temperature • Time	260 • 10	°C • sec

NOTE: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Power Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	Vcc+1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE: All Voltage are referenced to Vss.

DC CHARACTERISTICS

(TA=0°C to 70°C, VCC=5V±10%, VSS=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pins)	$V_{SS} \leq V_{IN} \leq V_{CC}+1.0$, All other pins not under test = V_{SS}		-10	10	μA	
ILO	Output Leakage Current (High impedance State)	$V_{SS} \leq V_{OUT} \leq V_{CC}$ $RAS \& CAS = V_{IH}$		-10	10	μA	1
ICC1	Vcc Supply Current, Operating	RAS, CAS Address cycling $t_{RC} = t_{RC}(\text{min.})$	60 70 80	- - -	120 100 90	mA	
ICC2	Vcc Supply Current, Operating.	$RAS \& CAS = V_{IH}(\text{min.})$, other inputs $\geq V_{SS}$		-	2	mA	1
ICC3	Vcc Supply Current, RAS-only refresh	$t_{RC} = t_{RC}(\text{min.})$	60 70 80	- - -	120 100 90	mA	1
ICC4	Vcc Supply Current, EDO mode	$RAS = V_{IL}$, CAS Address cycling $t_{HPC} = t_{HPC}(\text{min.})$	60 70 80	- - -	100 90 80	mA	
ICC5	Vcc Supply Current, CMOS Standby	$RAS = CAS = V_{CC}-0.2V$	SL-part	- -	1 0.4	mA	1
ICC6	Vcc Supply Current, CAS-before-RAS refresh	RAS, CAS Cycling $t_{RC}=t_{RC}(\text{min.})$	60 70 80	- - -	120 100 90	mA	
ICC7	Vcc Supply Current, Battery Back up (SL-part only)	$t_{RC} = 125\mu s$ $CAS = CBR$ cycling or 0.2V $OE \& WE = V_{CC}-0.2V$, $A0-A10 = V_{CC}-0.2V$ or 0.2V $DQ0-DQ3 = 0.2V, V_{CC}-0.2V$ or open	$t_{RAS} \leq 300ns$ $t_{RAS} \leq 1\mu s$	- -	300 500	μA	
ICC8	Vcc Supply Current Self Refresh (SL-part only)	$RAS \& CAS \leq 0.2V$ $OE \& WE \& A0-A10 = V_{CC}-0.2V$ or 0.2V, $DQ0-DQ3 = V_{CC}-0.2V, 0.2V$ or open		-	300	μA	
VOL	Output Low Voltage	$I_{OL} = 4.2mA$		-	0.4	V	
VOH	Output High Voltage	$I_{OH} = -5mA$		2.4	-	V	

NOTE :

- ICC1, ICC3, ICC4 and ICC6 depend on output loading and cycle rates. Specified values are obtained with the output open. In ICC1, ICC3, ICC6, address can be changed only once or less while $RAS = V_{IL}$. In ICC4, address can be changed only once or less during a EDO mode cycle (t_{HPC}).

AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted.) VOH=2.0V, VOL=0.8V

#	SYMBOL	PARAMETER	HY5117404AJ/T/RSJ/SLT/SLR						UNIT	NOTE
			- 60		- 70		- 80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	155	-	180	-	200	-	ns	
3	tHPC	EDO Mode cycle Time	25	-	30	-	35	-	ns	
4	tHPRWC	EDO Mode Read-Modify-write Cycle Time	75	-	85	-	95	-	ns	
5	tRAC	Access Time form RAS	-	60	-	70	-	80	ns	4,5
6	tCAC	Access Time from CAS	-	15	-	18	-	20	ns	4,5
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,5
8	tCPA	Access Time from CAS Precharge	-	35	-	40	-	45	ns	4
9	tCLZ	CAS to Output Low Impedance	3	-	3	-	3	-	ns	4
10	tOFF	Output Buffer Turn-off Delay from CAS	3	15	3	18	3	20	ns	6
11	tT	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	
12	tRP	RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (EDO Mode)	60	200K	70	200K	80	200K	ns	
15	tRSH	RAS Hold Time	15	-	18	-	20	-	ns	
16	tCSH	CAS Hold Time	45	-	50	-	55	-	ns	
17	tCAS	CAS Pulse width	11	10K	14	10K	17	10K	ns	
18	tRCD	RAS to CAS Delay	20	45	20	50	20	60	ns	5
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	17	40	ns	5
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	7
21	tCP	CAS Precharge Time	10	-	12	-	14	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold time	10	-	10	-	12	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	10	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	50	-	55	-	60	-	ns	
27	tRAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	8
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	8
31	tWCH	Write Command Hold Time	10	-	10	-	15	-	ns	9
32	tWCR	Write Command Hold Time from RAS	50	-	55	-	60	-	ns	
33	tWP	Write Command Pulse Width	10	-	10	-	15	-	ns	9
34	tRWL	Write Command to RAS Lead Time	15	-	18	-	20	-	ns	
35	tCWL	Write Command to CAS Lead Time	15	-	18	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	10
37	tDH	Data-In Hold Time	10	-	10	-	10	-	ns	10
38	tDHR	Data-In Hold Time Referenced to RAS	50	-	50	-	55	-	ns	
39	tREF	Refresh Period (2048)	-	32	-	32	-	32	ms	13
		SL-part	-	256	-	256	-	256		
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	11

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY5117404AJ/T/R/SLJ/SLT/SLR						UNIT	NOTE
			- 60		- 70		- 80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	40	-	45	-	50	-	ns	12
42	tRWD	RAS to WE Delay Time	80	-	95	-	105	-	ns	12
43	tAWD	Column Address to WE Delay Time	50	-	60	-	65	-	ns	12
44	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	
47	tCPT	CAS Precharge Time (CBR Counter Test)	20	-	25	-	25	-	ns	
48	tROH	RAS Hold Time Referenced to OE	10	-	10	-	10	-	ns	
49	tOEA	OE Access Time	-	15	-	18	-	20	ns	
50	tOED	OE to Data Delay	15	-	18	-	20	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from OE	3	15	3	18	3	20	ns	6
52	tOEH	OE Command Hold Time	15	-	18	-	20	-	ns	
53	tCPWD	WE Delay Time from CAS Precharge	55	-	65	-	75	-	ns	
54	tRHCP	RAS Hold Time from CAS Precharge	35	-	40	-	45	-	ns	12
55	tWRP	WE to RAS Precharge Time(CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	WE to RAS Hold Time(CBR Cycle)	10	-	10	-	10	-	ns	
57	tWTS	Write Command Set-up Time (Test Mode In)	10	-	10	-	10	-	ns	
58	tWTH	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
59	tRASS	RAS Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	μs	
60	tRPS	RAS Precharge Time (Self Refresh Cycle)	90	-	110	-	130	-	ns	
61	tCHS	CAS Hold Time (Self RefreshCycle)	- 50	-	- 50	-	- 50	-	ns	
62	tDOH	Output Data Hold Time	5	-	5	-	5	-	ns	
63	tREZ	Output Buffer Turn Off Delay Time from RAS	3	15	3	18	3	20	ns	6,14
64	tWEZ	Output Buffer Turn Off Delay Time from WE	3	15	3	18	3	20	ns	6
65	tWED	WE to Data Delay Time	15	-	18	-	20	-	ns	
66	tOEP	OE High Pulse Width	5	-	8	-	10	-	ns	
67	tWPE	WE Pulse Width (EDO Cycle)	5	-	8	-	10	-	ns	
68	tOCH	OE to CAS Hold Time	0	-	0	-	0	-	ns	
69	tCHO	CAS Hold Time to OE	5	-	8	-	10	-	ns	

AC CHARACTERISTICS IN TEST MODE

NOTE 13

#	SYMBOL	PARAMETER	HY5117404AJ/T/R/SLJ/SLT/SLR						UNIT	NOTE
			- 60		- 70		- 80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	115	-	135	-	155	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	160	-	185	-	215	-	ns	
3	tHPC	EDO Mode Cycle Time	30	-	35	-	40	-	ns	
4	tHPRWC	EDO Mode Read-Modify-Write Cycle Time	80	-	90	-	100	-	ns	
5	tRAC	Access Time from RAS	-	65	-	75	-	85	ns	4,5
6	tCAC	Access Time from CAS	-	20	-	23	-	25	ns	4,5
7	tAA	Access Time from Column Address	-	35	-	40	-	45	ns	4,5
8	tCPA	Access Time from CAS Precharge	-	40	-	45	-	50	ns	4
13	tRAS	RAS Pulse Width	65	10K	75	10K	85	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	65	200K	75	200K	85	200K	ns	
15	tRSH	RAS Hold Time	20	-	25	-	25	-	ns	
16	tCSH	CAS Hold Time	50	-	55	-	60	-	ns	
17	tCAS	CAS Pulse Width	20	10K	23	10K	25	10K	ns	
27	tRAL	Column Address to RAS Lead Time	35	-	40	-	45	-	ns	
41	tCWD	CAS to WE Delay Time	45	-	50	-	55	-	ns	
42	tRWD	RAS to WE Delay Time	90	-	100	-	110	-	ns	
43	tAWD	Column Address to WE Delay Time	60	-	65	-	70	-	ns	
49	tOEZ	OE Access Time	-	20	-	23	-	25	ns	
50	tOED	OE to Data Delay	20	-	20	-	25	-	μs	
52	tOEH	OE Command Hold Time	20	-	23	-	25	-	ns	

NOTE:

1. An initial pause of 200 μ s is required after power-up followed by any 8 refresh ($\overline{\text{RAS}}$ only $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh) cycle before proper device operation is achieved.
2. If $\overline{\text{RAS}}=\text{Vss}$ during power-up, the HY5117404A could begin an active cycle. These condition results in higher current than necessary which is demanded from the power supply during power-up. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ track with Vcc during power-up or be held at a valid Vih in order to minimize the power-up current.
3. $\text{Vih}(\text{min.})$ and $\text{Vil}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between $\text{Vih}(\text{min.})$ and $\text{Vil}(\text{max.})$, and are assumed to be 3ns for all inputs.
4. Measured at $\text{Voh}=2.0\text{V}$ and $\text{Vol}=0.8\text{V}$ with a load equivalent to 2 TTL loads and 100pF.
5. These parameters define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either trch or trrh must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and $\overline{\text{WE}}$ leading edge in Read-Modify-Write cycles.
8. twcs , trwd , tcwd , tawd and tcpwd are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $\text{twcs} \geq \text{twcs}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $\text{trwd} \geq \text{trwd}(\text{min.})$, $\text{tcwd} \geq \text{tcwd}(\text{min.})$, $\text{tawd} \geq \text{tawd}(\text{min.})$, and $\text{tcpwd} \geq \text{tcpwd}(\text{min.})$, the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the $\text{trcd}(\text{max.})$ limit insures that $\text{trac}(\text{max.})$ can be met. $\text{trcd}(\text{max.})$ is specified as a reference point only. If trcd is greater than the specified $\text{trcd}(\text{max.})$ limit, then access time is controlled by tcac .
10. Operation within the $\text{trad}(\text{max.})$ limit insures that $\text{trac}(\text{max.})$ can be met. $\text{trad}(\text{max.})$ is specified as a reference point only. If trad is greater than the specified $\text{trad}(\text{max.})$ limit, then access time is controlled by taa .
11. $\text{tref}(\text{max.})=256\text{ms}$ is applied to SL-Parts (HY5117404ASLJ, HY5117404ASLT and HY5117404ASLR).
12. A burst of 2048 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles must be executed within 64ms(256ms for SL-part) after exiting self refresh.
13. These specifications are applied to the test Mode.
14. If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going.
15. $\text{tasc} \geq \text{tcp}$ (min.), Assume $\text{tT}=2\text{ns}$

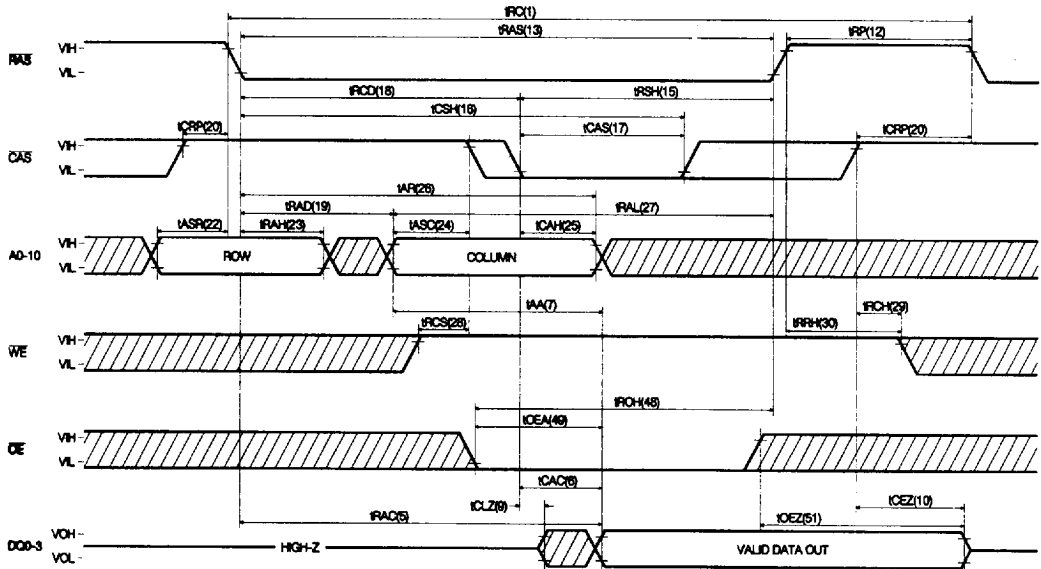
CAPACITANCE

($\text{TA}=25^\circ\text{C}$, $\text{Vcc}=5\text{V}\pm 10\%$, $\text{Vss}=0\text{V}$, $\text{f}=1\text{MHz}$, unless otherwise noted.)

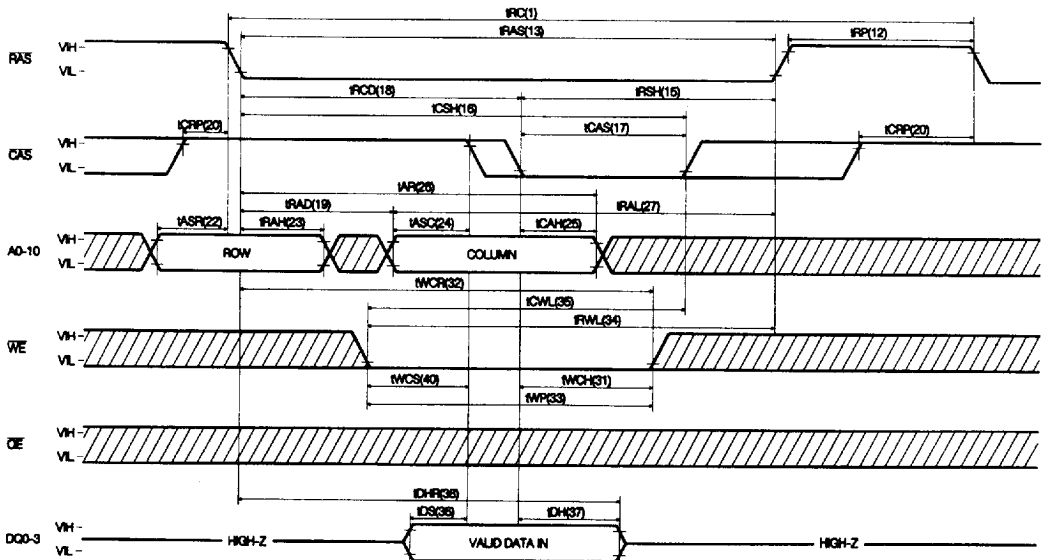
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A10)	-	5	pF
CIN2	Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	-	7	pF
CDQ	Data Input/Output Capacitance (DQ0-DQ3)	-	7	pF

TIMING DIAGRAM

READ CYCLE



EARLY WRITE CYCLE



The timing diagram illustrates the relationship between several control and data signals over time. The signals shown are:

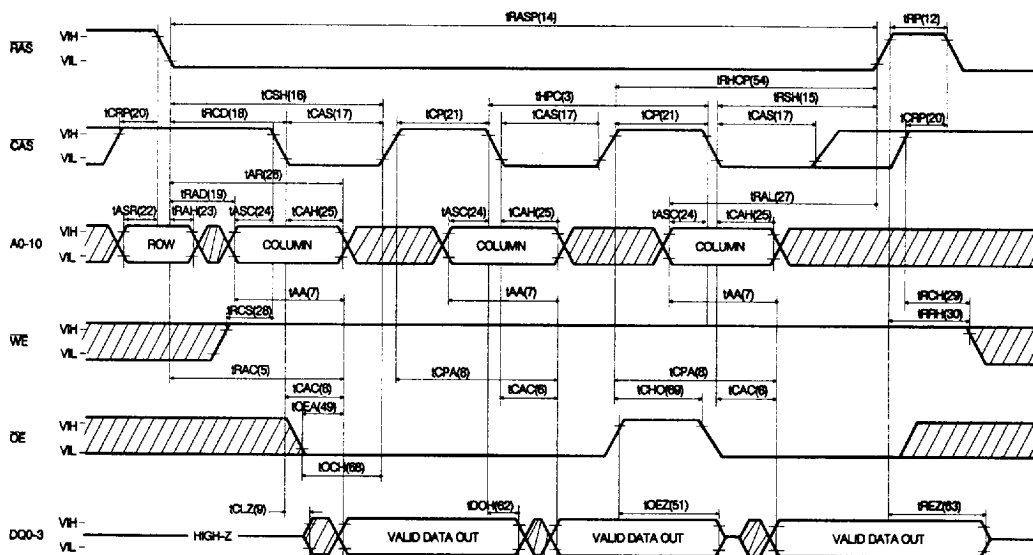
- RAS**: Row Address Strobe. High impedance (HIZ) before and after its pulse.
- CAS**: Column Address Strobe. High impedance (HIZ) before and after its pulse.
- A0-10**: Address bus. Shaded regions indicate valid periods for ROW and COLUMN operations.
- WE**: Write Enable. Active-low signal, shaded during write operations.
- OE**: Output Enable. Active-low signal, shaded during output operations.
- DQ0-3**: Data bus. Shaded regions indicate HIGH-Z state and VALID DATA periods.

Key timing parameters labeled in the diagram include:

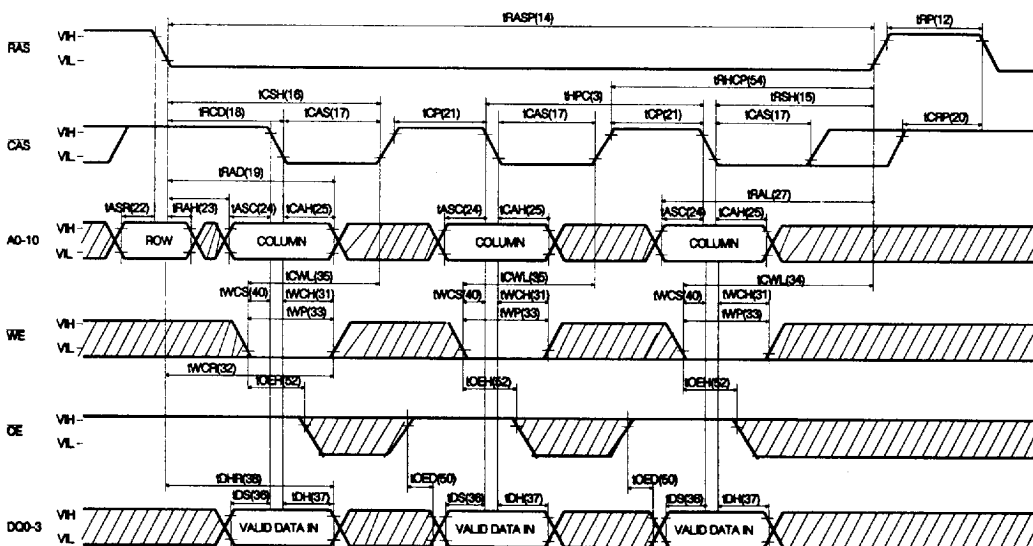
- $t_{RC}(1)$, $t_{RP}(12)$
- $t_{RCD}(18)$, $t_{CSH}(16)$, $t_{FSH}(19)$
- $t_{CPR}(20)$, $t_{CAS}(17)$
- $t_{RAD}(19)$, $t_{APR}(26)$, $t_{FAL}(27)$
- $t_{ASPR}(22)$, $t_{RAH}(23)$, $t_{ASC}(24)$, $t_{CAH}(25)$
- $t_{CWL}(35)$, $t_{RWL}(34)$
- $t_{WPR}(33)$, $t_{OEH}(32)$
- $t_{OED}(50)$, $t_{DS}(39)$, $t_{DH}(37)$

[illegible]

EDO MODE READ CYCLE



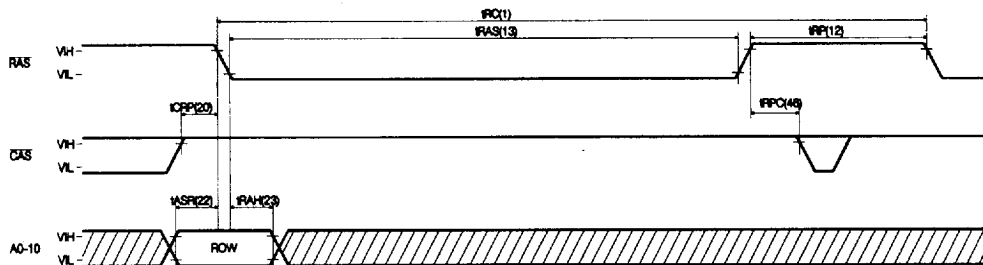
EDO MODE EARLY WRITE CYCLE



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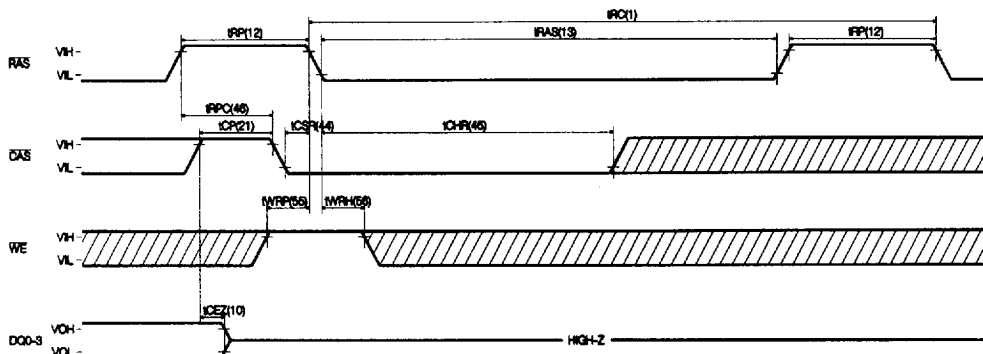
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RAS-ONLY REFRESH CYCLE



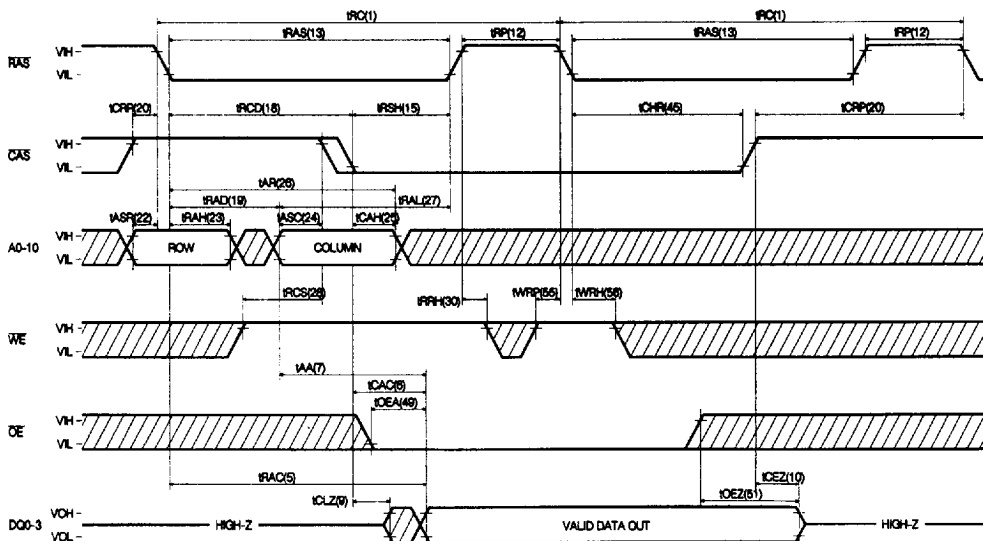
NOTE : OE and WE = "H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE



NOTE : A0-10 and OE = "H" or "L"

HIDDEN REFRESH CYCLE (READ)



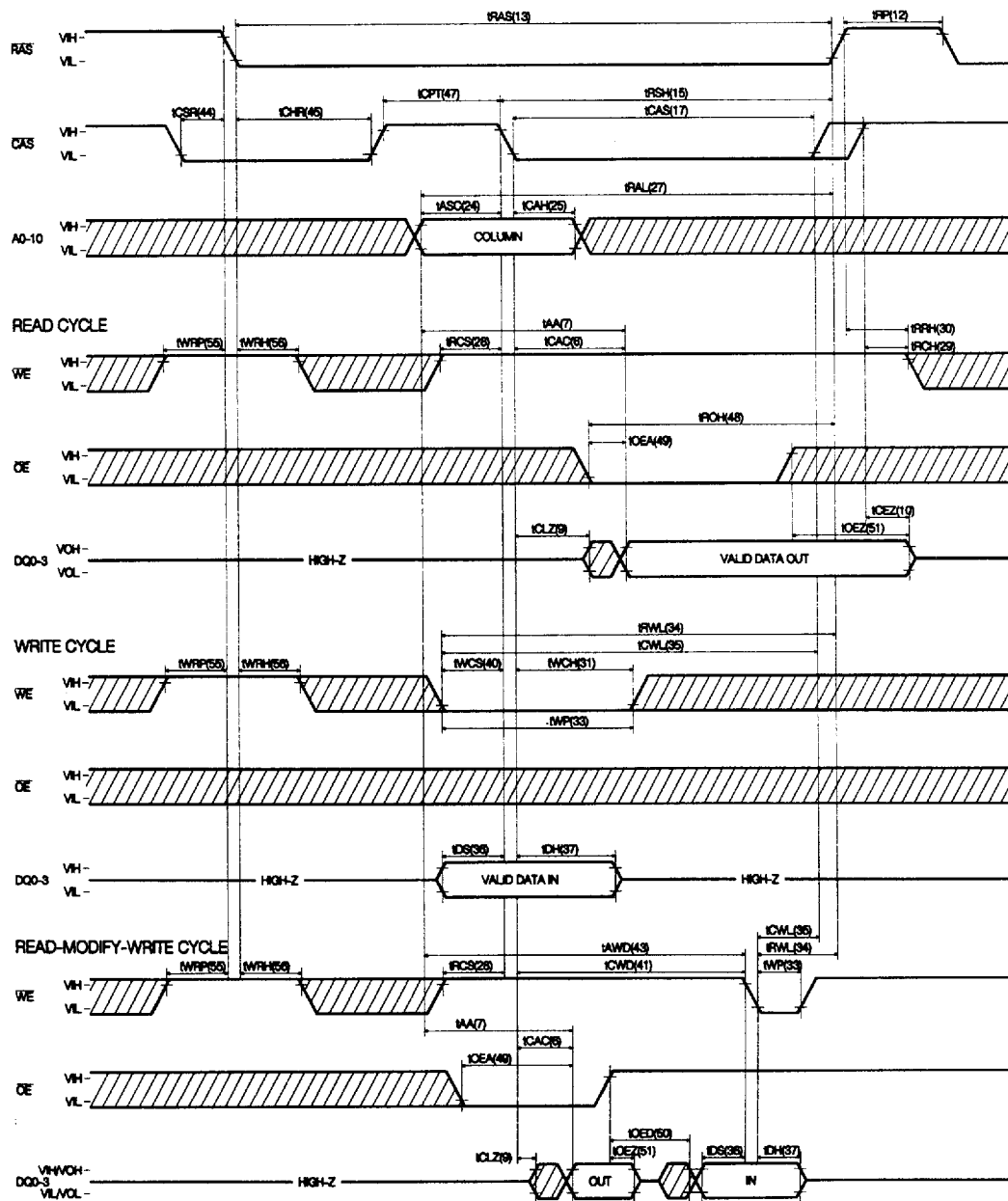
The timing diagram illustrates the relationship between several signals and their timing parameters:

- RAS:** Shows high (VH) and low (VL) states. Key parameters include $t_{RAS}(13)$, $t_{RC}(1)$, $t_{RP}(12)$, $t_{ICPP}(20)$, $t_{ICD}(18)$, $t_{FSH}(15)$, $t_{ICRH}(45)$, and $t_{ICPP}(20)$.
- CAS:** Shows high (VH) and low (VL) states. Key parameters include $t_{AR}(26)$, $t_{RAD}(19)$, $t_{RAH}(23)$, $t_{ASC}(24)$, and $t_{CAH}(25)$.
- AO-10:** Shows high (VH) and low (VL) states. Key parameters include $t_{ASR}(22)$, t_{ROW} , t_{COLUMN} , $t_{CAH}(25)$, $t_{WCS}(40)$, $t_{WCH}(31)$, $t_{WPR}(33)$, $t_{WPR}(55)$, and $t_{WRH}(56)$.
- WE:** Shows high (VH) and low (VL) states. Key parameters include $t_{WCR}(32)$.
- OE:** Shows high (VH) and low (VL) states. Key parameters include $t_{DHR}(38)$, $t_{DS}(36)$, and $t_{DH}(37)$.
- DQ0-3:** Shows high (VH) and low (VL) states. Key parameters include $t_{DHR}(38)$, $t_{DS}(36)$, and $t_{DH}(37)$.

The timing diagram illustrates the sequence of events for a memory access cycle. The RAS signal is active (low) for a duration of $t_{PR}(12)$ ns, followed by a period of $t_{RAS}(59)$ ns. The CAS signal is active (low) for a duration of $t_{CPR}(44)$ ns, followed by a period of $t_{CHS}(61)$ ns. The DQ0-3 signals are active (low) for a duration of $t_{CEZ}(10)$ ns, followed by a period of $t_{RPC}(46)$ ns. The diagram also shows the relationship between the RAS and CAS signals, with $t_{RPC}(46)$ ns being the time from the start of the RAS pulse to the start of the CAS pulse.

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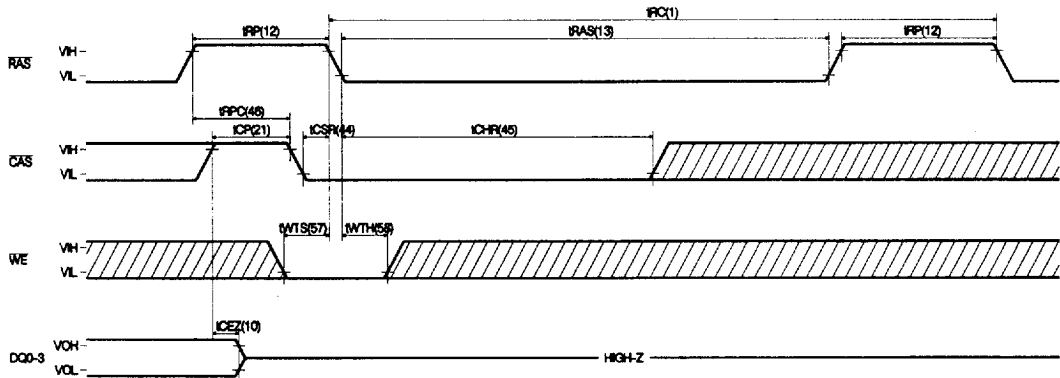
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



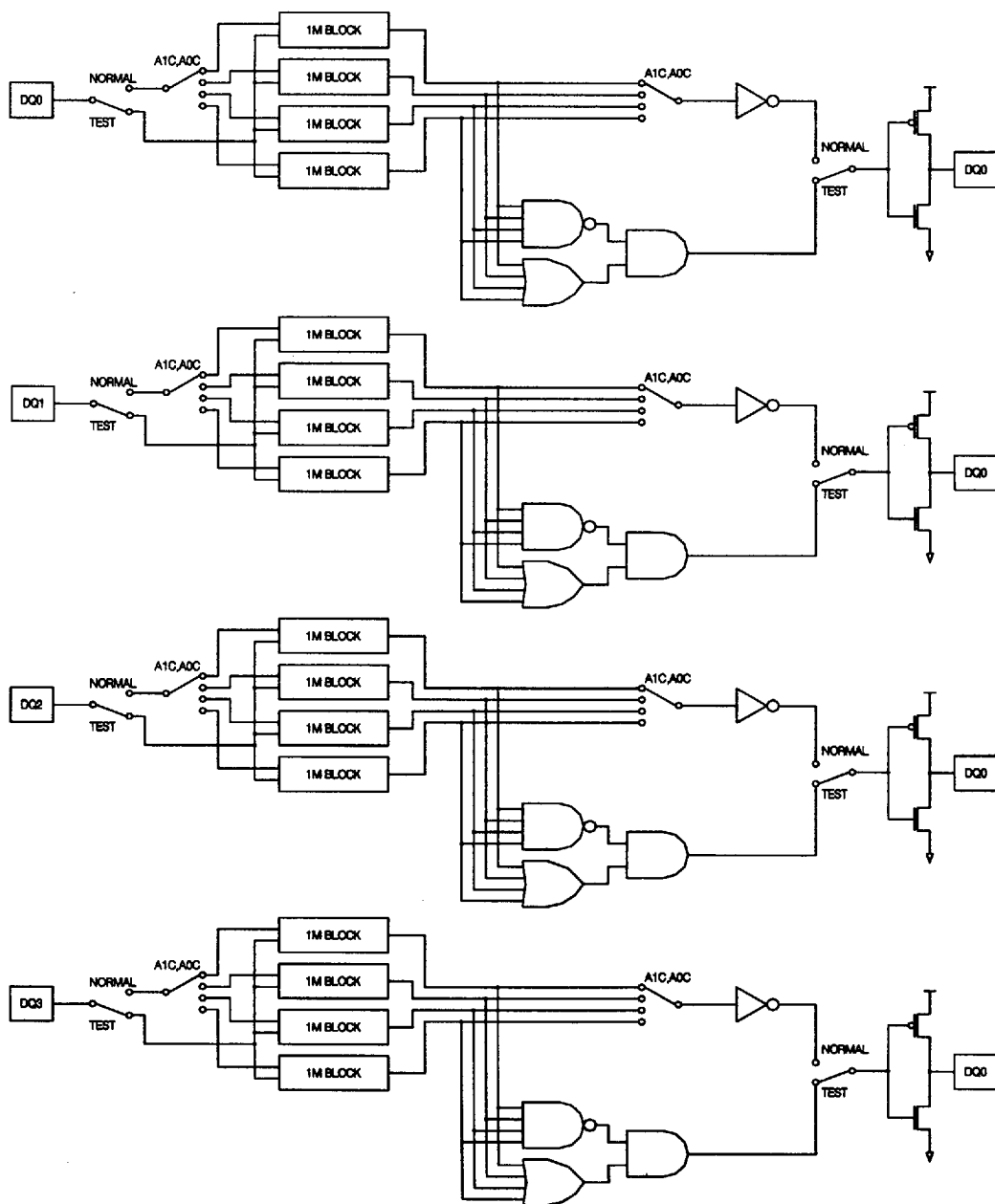
TEST MODE

The HY5117404A is a DRAM organized 4,194,304 x 4-bit. It is internally organized 1,048,576 x 16-bit. In Test Mode, data are written into 16 sectors (Each is composed of 1M bits) in parallel and retrieved the same way. Column address A0 and A1 are not used. If upon reading, 4-bit data from 4 sectors connected to one DQ pin are equal (all "1"s or "0"s), the DQ pin indicates a "1". If they are not equal, the DQ pin indicates a "0". Belowing shows the timing diagram of the HY5117404A enter Test Mode. In Test Mode, the 4M x 4 DRAM can be tested as if it were a 1M x 4 DRAM. **WE**, CAS-before-RAS cycle (Test Mode In Cycle) puts the HY5117404A into Test Mode and CAS-before-RAS or RAS-only refresh cycle puts it back into Normal Model. In Test Mode, **WE**, CAS-before-RAS cycle shall be used for the refresh operation. The Test Mode function reduces test time (1/4 in case of N test pattern).

TEST MODE IN CYCLE



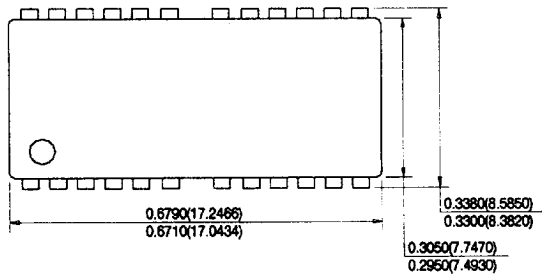
BLOCK DIAGRAM IN TEST MODE



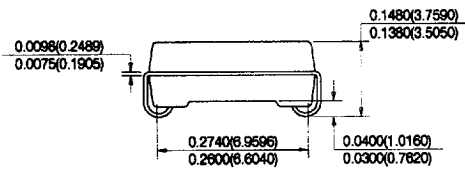
4675088 0004499 263

PACKAGE INFORMATION

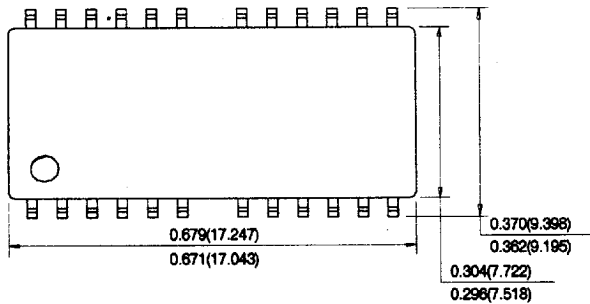
300 mil 24/26 pin Small Outline J-form Package (J)



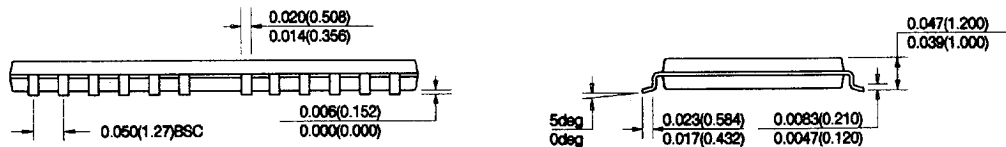
UNIT : INCH(mm)



300 mil 24/26 pin Thin Small Outline Package (T) (R)



UNIT : INCH(mm)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE
HY5117404AJ	60/70/80		SOJ
HY5117404ASLJ	60/70/80	SL-part	SOJ
HY5117404AT	60/70/80		TSOP-II
HY5117404ASLT	60/70/80	SL-part	TSOP-II
HY5117404AR	60/70/80		TSOP-II(R)
HY5117404ASLR	60/70/80	SL-part	TSOP-II(R)