HEWLETT PACKARD

1300 nm LED Transceiver for ATM, SONET/SDH 622 Mb/s and General Purpose 155 - 650 Mb/s

Technical Data

HFBR-5208

Features

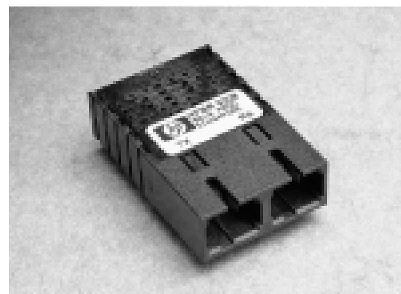
- **1300 nm LED-based Transceiver for 155 to 650 Mb/s Links of 500 m in 62.5/125 µm**
- **Compliant with ATM Forum 622.08 Mb/s Physical Layer Specification (AF-PHY-0046.000)**
- **Compliant with ANSI Broadband ISDN - Physical Layer Specification T1.646-1995**
- **Compliant with Specifications Proposed to ANSI T1E1.2 Committee for Inclusion in SONET Physical Layer Specifications (T1E1.2/96-002)**
- **Industry Standard 1 x 9 Package Style**
- **Integral Duplex SC Connector Compliant with TIA/EIA and IEO Building Wiring Standards**
- **Single +5 V Power Supply Operation and PECL Logic Interfaces**
- **Wave Solder and Aqueous Wash Process Compatible**
- **Designed and Manufactured in an ISO 9000 Certified Facility**

Applications

- **General Purpose Low Cost MMF Links at 155 to 650 Mb/s**
- **ATM 622 Mb/s MMF Links from Switch-to-Switch or Switch-to-Server in the End-User Premise**
- **Private MMF Interconnects at 622 Mb/s SONET STS-12/SDH STM-4 Rate**

622 Mb/s Product Family

- **HFBR-5208**
  1300 nm LED Based Transceiver in 1 x 9 Package for 500 m Links in 62.5/125 µm MMF Cables
- **HFBR-5207**
  1300 nm LED Based Transceiver with Integral Clock and Data Recovery in 2 x 9 Package for 500 m Links in 62.5/125 µm MMF Cables
- **HFCT-5207/HFCT-5217**
  1300 nm Laser Based Transceiver with Integral Clock and Data Recovery in 2 x 9 Package for Links in Single Mode Fiber Cables
  HFCT-5207 - 15 km
  HFCT-5217 - 40 km



- **HFCT-5208/HFCT-5218**
  1300 nm Laser Based Transceiver in 1 x 9 Package for Links in Single Mode Fiber Cables
  HFCT-5208 - 15 km
  HFCT-5218 - 40 km
- **HFBR-5205**
  1300 nm LED Based Transceiver in 1 x 9 Package for 155 Mb/s Links at 2 km in 62.5/125 µm MMF Cables

Description

General

This 1300 nm LED based transceiver is intended to provide low cost 622 Mb/s Multimode Fiber (MMF) interconnects for the emerging ATM switch-to-switch and switch-to-server applications within a customer premise.

Transmitter Section
The transmitter section of this transceiver is similar to 1300 nm LED transceivers in use at the 155 Mb/s rate today. It consists of a 1300 nm InGaAsP LED in an optical subassembly (OSA) which mates to the fiber cable. The LED OSA is driven by a custom, silicon bipolar IC which converts differential PECL logic signals, ECL referenced to a +5 V supply, into an analog LED drive current.

Receiver Section
The receiver starts with an InGaAs PIN photodiode mounted together with a custom, silicon bipolar transimpedance pre-amplifier IC in an OSA. This OSA is mated to a custom, silicon bipolar circuit providing post amplification and quantization and optical signal detection.

The custom, silicon bipolar circuit includes a Signal Detect circuit which provides a PECL logic high output upon detection of a usable input optical signal level. This single ended PECL output is designed to drive a standard PECL input through normal 50 Ω PECL load.

Applications Information

Typical BER Performance of Receiver versus Input Optical Power Level
The HFBR-5208 transceiver can be operated at Bit-Error-Ratio conditions other than the required BER = 1 x 10^{-10} of the 622 MBd ATM Forum 622.08 Mb/s Physical Layer Standard. The typical trade-off of BER versus Relative Input Optical Power is shown in Figure 1. The Relative Input Optical Power in dB is referenced to the Input Optical Power parameter value in the Receiver Optical Characteristics table. For better BER condition than 1 x 10^{-10} , more input signal is needed (+dB). For example, to operate the HFBR-5208 at a BER of 1 x 10^{-12} , the receiver will require an input signal approximately 0.6 dB higher than the -26 dBm level required for 1 x 10^{-10} operation, i.e. -25.4 dBm.

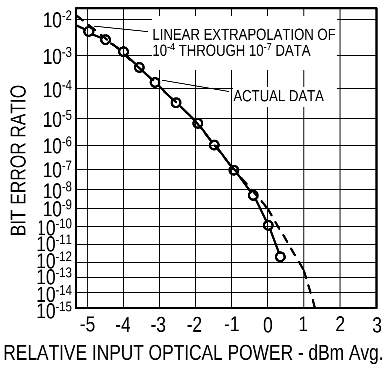


Figure 1. Relative Input Optical Power - dBm Average.

An informative graph of a typical, short fiber transceiver link performance can be seen in Figure 2. This figure is of Relative Input Optical Power versus Sampling Time Position within the receiver output data eye-opening. The given curves are at a constant bit-error-ratio (BER) of 10^{-10} for four different signaling rates, 155 Mbd, 311 Mbd, 622 Mbd and 650 Mbd. These curves, called “tub” diagrams for their shape, show the amount of data eye-opening time-width for various receiver input optical power levels. A wider data eye-opening provides more time for the clock recovery circuit to operate within without creating errors. The deeper the tub is indicates less input optical power is needed to operate the receiver at the same BER condition. Generally, the wider and deeper the tub is the better. The relative receiver input optical power amount (dB) is referenced to the absolute level (dBm avg.) given in the Receiver Optical Characteristics table. The 0 ns sampling time position for this Figure 2 refers to the center of the Baud interval for the particular signaling rate. The Baud interval is the reciprocal of the signaling rate in Mbd. For example, at 622 Mbd the Baud interval is 1.61 ns, at 155 Mbd the Baud interval is 6.45 ns. Test conditions for this tub diagram are listed in Figure 2.

The HFBR-5208 receiver input optical power requirements vary slightly over the signaling rate range of 20 Mbd to 700 Mbd for a constant bit-error-ratio (BER) of 10^{-10} condition. Figure 3 illustrates the typical receiver relate input optical power varies by $\leq$0.7 dB over this full range. This small sensitivity variation allows the optical budget to remain nearly constant for designs that make use of the broad signaling rate range of the HFBR-5208. The curve has been normalized to the input optical power level (dBm avg.) of the receiver for 622 Mbd at center of the Baud interval with a BER of 10^{-10}. The data patterns that can be used at these signaling rates should be, on average, balanced duty factor of 50%. Momentary excursions of less or more data duty factor than 50% can occur, but the overall data pattern must remain balanced. Unbalanced data duty factor will cause excessive pulse-width distortion, or worse, bit errors. The test conditions are listed in Figure 3.

Recommended Circuit Schematic
When designing the HFBR-5208 circuit interface, there are a few fundamental guidelines to follow. For example, in the Recommended Circuit Schematic, Figure 4, the differential data lines should be treated as 50 ohm Microstrip or

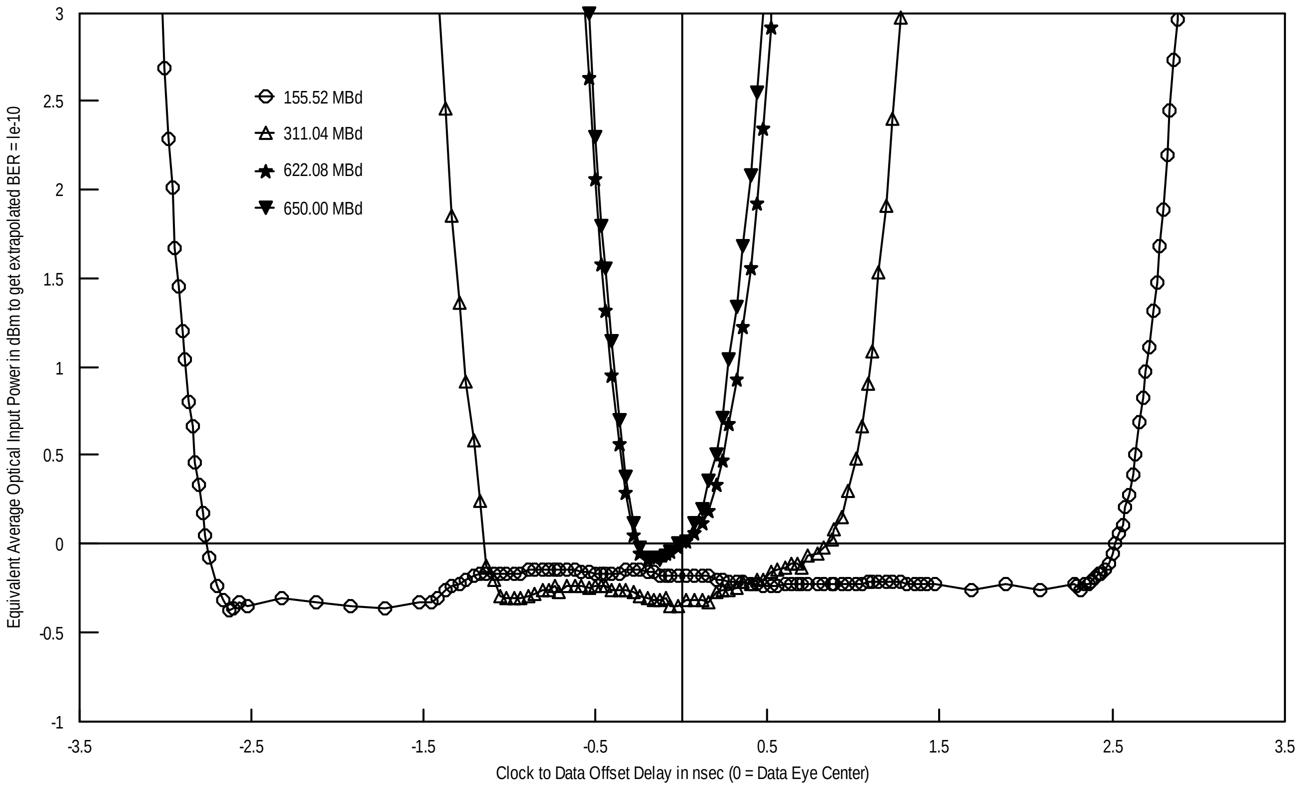


Figure 2. Relative Input Optical Power as a function of sampling time position. Normalized to center of Baud interval at 622 Mbd. Test Conditions +25°C, 5.25 V, PRBS 2^{23}-1, τ_r/τ_f = 0.9 ns.

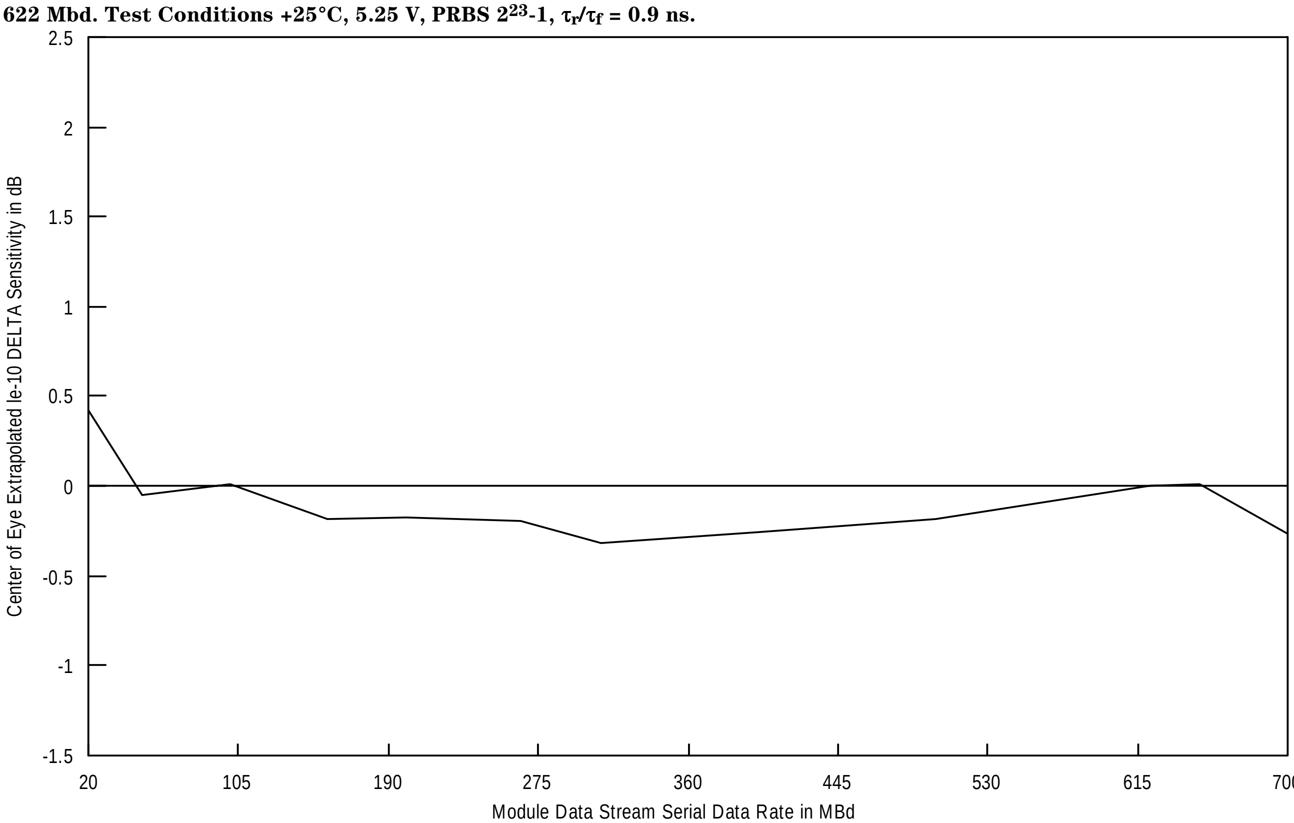
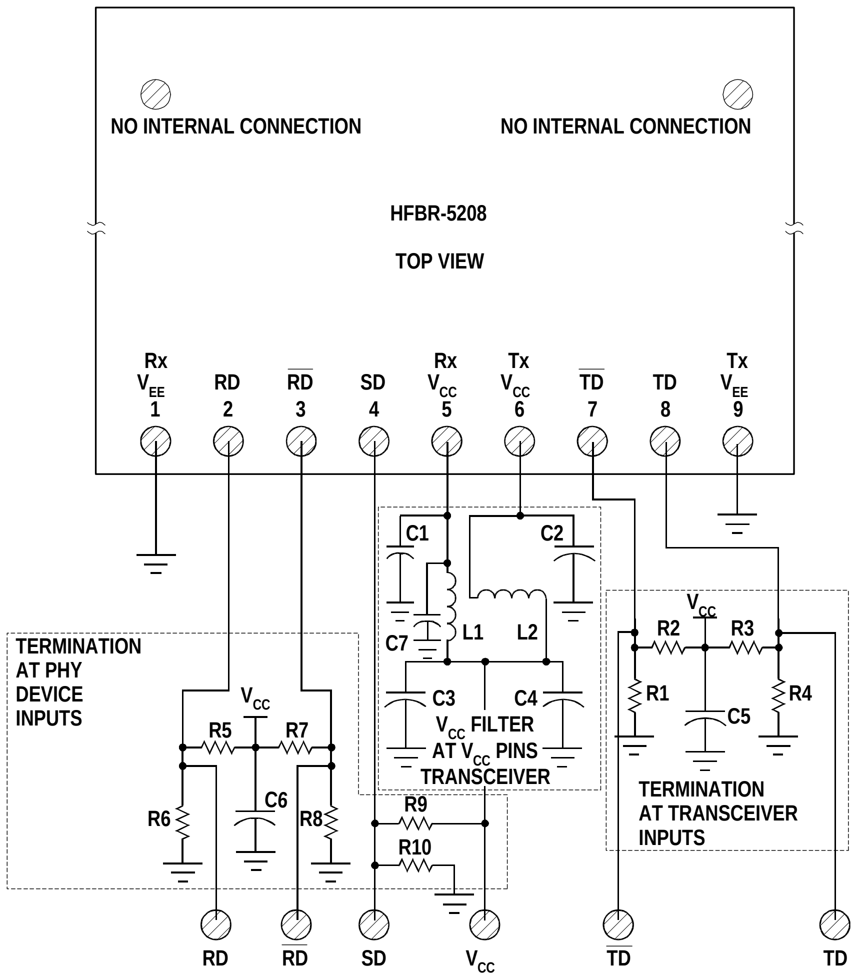


Figure 3. Relative Input Optical Power as a function of data rate normalized to center of Baud interval at 622 Mbd. Test Conditions +25°C, 5.25 V, PRBS 2^{23}-1, τ_r/τ_f = 0.9 ns.

stripline transmission lines. This will help to minimize the parasitic inductance and capacitance effects. Proper termination of the differential data signal will prevent reflections and ringing which would compromise the signal fidelity and generate unwanted electrical noise. Locate termination at the received signal end of the transmission line. The length of these lines should be kept short and of equal length to prevent pulse-width distortion from occurring. For the high-speed signal lines, differential signals should be used, not single-ended signals. These differential signals need to be loaded symmetrically to prevent unbalanced currents from flowing which will cause distortion in the signal.

Maintain a solid, low inductance ground plane for returning signal currents to the power supply. Multilayer plane printed circuit board is best for distribution of V_{CC}, returning ground currents, forming transmission lines and shielding. Also, it is important to suppress noise from influencing the fiber-optic transceiver performance, especially the receiver circuit. Proper power supply filtering of V_{CC} for this transceiver is accomplished by using the recommended separate filter circuits shown in Figure 4. These filter circuits suppress V_{CC} noise of 50 mV peak-to-peak or less over a broad frequency range. This prevents receiver sensitivity degradation . It is recommended that surface-mount components be used. Use tantalum capacitors for the 10 µF capacitors and mono-lithic, ceramic bypass capacitors for the 0.1 µF capacitors. Also, it is recommended that a surface-mount coil inductor of 1 µH be used. Ferrite beads can be used to replace the coil inductors when using quieter V_{CC} supplies, but a coil inductor is recommended over a ferrite bead. Coils with a low, series dc resistance (<0.7 ohms) and high, self-resonating frequency are recommended. All power supply components need to be placed physically next to the V_{CC} pins of the receiver and transmitter. Use a good, uniform ground plane with a minimum number of holes to provide a low-inductance ground current return path for the power supply currents.



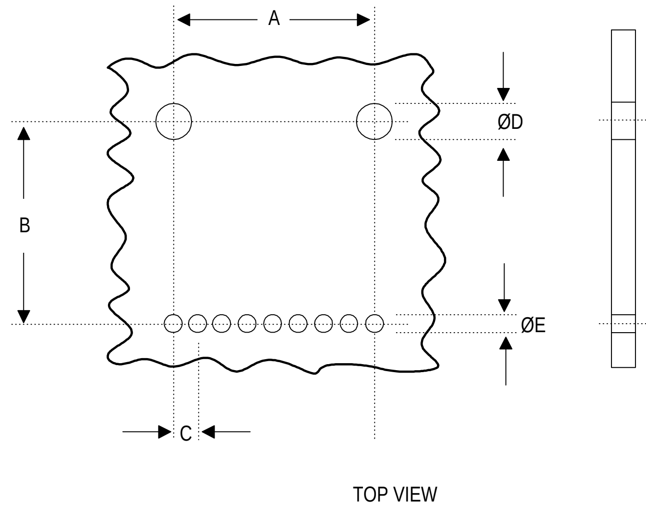
NOTES:
THE SPLIT-LOAD TERMINATIONS FOR ECL SIGNALS NEED TO BE LOCATED AT THE INPUT OF DEVICES RECEIVING THOSE ECL SIGNALS. RECOMMEND MULTI-LAYER PRINTED CIRCUIT BOARD WITH 50 OHM MICROSTRIP SIGNAL PATHS BE USED.
R1 = R4 = R6 = R8 = R10 = 130 OHMS
R2 = R3 = R5 = R7 = R9 = 82 OHMS
C1 = C2 = C3 = C5 = C6 = 0.1 µF.
C4 = 10 µF.
C7 = 10 µF (Optional).
L1 = L2 = 1 µH COIL OR FERRITE INDUCTOR.

Figure 4. Recommended Circuit Schematic

In addition to these recommendations, Hewlett-Packard's Application Engineering staff is available for consulting on best layout practices with various vendors serialiser/deserialiser, clock generator.

Evaluation Circuit Boards
Evaluation circuit boards implementing this recommended circuit design are available. Contact your local HP sales representative to arrange for access to one if needed.

Operation in -5.2 V Designs
For applications that require -5.2 V dc power supply level for true ECL logic circuits, the HFBR-5208 transceiver can be operated with a V_{CC} = 0 V dc and a V_{EE} = -5.2 V dc. This transceiver is not specified with an operating, negative power supply voltage. The potential compromises that can occur with use of -5.2 V dc power are that the absolute voltage states for V_{OH} and V_{OL} will be changed slightly due to the 0.2 V difference in supply levels. Also, noise immunity may be compromised for the HFBR-5208 transceiver because the ground plane is now the V_{CC} supply point. The suggested power supply filter circuit shown in the Recommended Circuit Schematic figure should be located in the V_{EE} paths at the transceiver supply pins. Direct coupling of the differential data signal can be done between the HFBR-5208 transceiver and the standard ECL circuits. For guaranteed -5.2 V dc operation, contact our local Hewlett-Packard Component Field Sales Engineer for assistance.



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	20.32	-	-	0.8	-
B	-	20.32	-	-	0.8	-
C	-	2.54	-	-	0.1	-
ØD	1.8	-	2.0	0.071	-	0.079
ØE	0.7	-	0.9	0.028	-	0.036

Figure 5. Recommended Board Layout Pattern

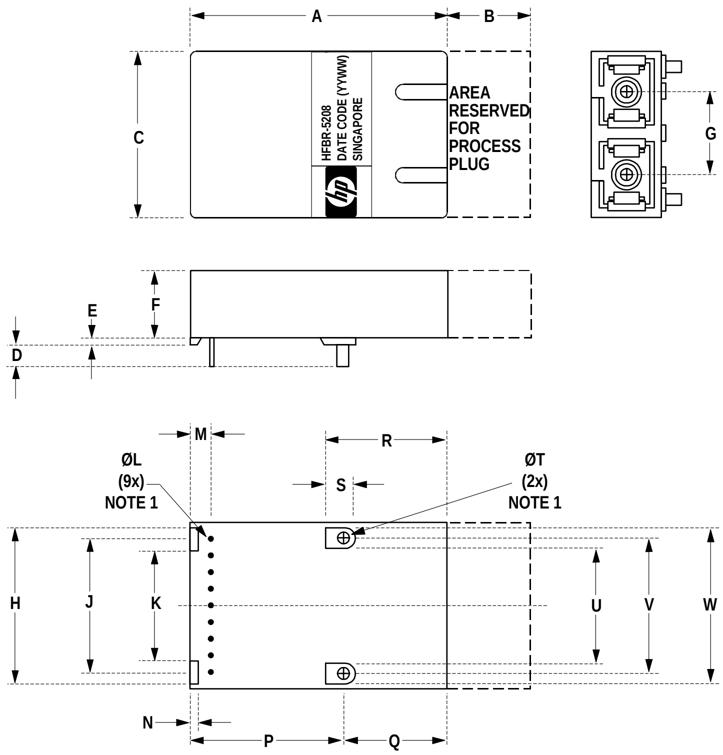
Recommended Solder and Wash Process

The HFBR-5208 is compatible with industry-standard wave or hand solder processes.

HFBR-5000 Process Plug
The HFBR-5208 transceiver is supplied with a process plug, the HFBR-5000, for protection of the optical ports with the Duplex SC connector receptacle. This process plug prevents contamination during wave solder and aqueous rinse as well as during handling, shipping or storage. It is made of high-temperature, molded, sealing material that will withstand +80°C and a rinse pressure of 50 lb/in 2 .

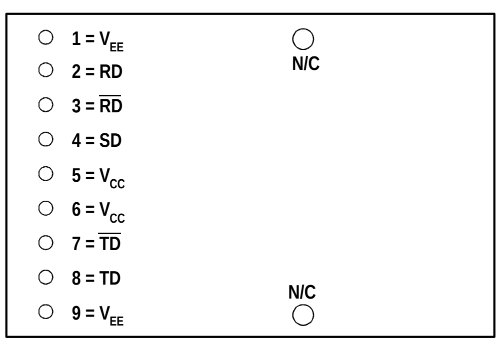
Recommended Solder Fluxes and Cleaning/Degreasing Chemicals
Solder fluxes used with the HFBR-5208 fiber-optic transceiver should be water-soluble, organic solder fluxes. Some recommended solder fluxes are Lonco 3355-11 from London Chemical West, Inc. of Burbank, CA, and 100 Flux from Alphametals of Jersey City, NJ.

Recommended cleaning and degreasing chemicals for the HFBR-5208 are alcohols (methyl, isopropyl, isobutyl), aliphatics (hexane, heptane) and other chemicals, such as soap solution or naphtha. Do not use partially halogenated hydrocarbons for cleaning/degreasing. Examples of chemicals to avoid are 1,1.1 trichloroethane, ketones (such as MEK), acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride or N methylpyrolldone.



NOTE 1: THE SOLDER POSTS AND ELECTRICAL PINS ARE PHOSPHOR BRONZE WITH TIN/LEAD OVER NICKEL PLATING.

DIMENSIONS ARE IN MILLIMETERS (INCHES).



TOP VIEW

Dim.	Millimeters			Inches			Dim.	Millmeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.		Min.	Typ.	Max.	Min.	Typ.	Max.
A			39.12			1.540	M		2.92			0.115	
B		12.70			0.500		N		0.87			0.034	
C			25.40			1.000	P		23.24			0.915	
D		3.30			0.130		Q		15.88			0.625	
E		0.75			0.030		R		18.52			0.729	
F			10.35			0.407	S		4.14			0.163	
G		12.70			0.500		ØT		1.27			0.050	
H		23.55			0.927		U		17.32			0.682	
J		20.32			0.800		V		20.32			0.800	
K		16.70			0.657		W		23.32			0.918	
ØL		0.46			0.018								

Figure 6. Package Outline Drawing and Pinout

Regulatory Compliance

These transceiver products are intended to enable commercial system designers to develop equipment that complies with the various regulations governing certification of Information Technology Equipment. See the Regulatory Compliance Table for details. Additional information is available from your Hewlett-Packard sales representative.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas.

The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the duplex SC connector receptacle is exposed to the outside of the equipment chassis, it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high-speed transceivers from Hewlett-Packard will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

The HFBR-5208 EMI has been characterized without a chassis enclosure to demonstrate the robustness of the parts integral shielding. Performance of a system containing these transceivers within a well designed chassis is expected to be better than the results of these tests with no chassis enclosure.

Immunity

Equipment utilizing these HFBR-5208 transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers, with their integral shields, have been characterized without the benefit of a normal equipment chassis enclosure and the results are reported below. Performance of a system containing these transceivers within a well-designed chassis is expected to be better than the results of these tests without a chassis enclosure.

Regulatory Compliance - Targeted Typical Specifications

Feature	Test Method	Targeted Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.4	Class 2 (>2000 V)
Electrostatic Discharge (ESD) to theDuplex SC Receptacle	Variation of IEC 801-2	Typically withstand at least 25 kV without damage when the Duplex SC Connector Receptacle is contacted by a Human Body Model probe.
Electromagnetic Interference (EMI)	FCC Class B CENELEC EN55022 Class B (CISPR 22B) VCCI Class 2	Typically provide a 4 dB margin to FCC Class B and a 1 dB margin to the other noted standard limits when tested with the transceiver mounted to a circuit card without a chassis enclosure at frequencies up to 1 GHz. An ATM scrambled pattern is assumed. Margins above 1 GHz are dependent on customer board and chassis design.
Immunity	Variation of IEC 801-3	Typically show no measurable effect from a 10 V/m field swept from 10 MHz to 1 GHz applied to the transceiver when mounted to a circuit card without a chassis enclosure.

The HFBR-5208 LED transmitters are classified as IEC 825-1 Accessible Emission Limit (AEL) Class 1. AEL Class 1 LED devices are considered eye safe.

Table 1. Pinout Table

Pin	Symbol	Functional Description
Mounting Studs		The mounting studs are provided for transceiver mechanical attachment to the circuit boards, they are embedded in the nonconductive plastic housing and are not tied to the transceiver internal circuit. They should be soldered into plated-through holes on the printed circuit board.
1	V_{EER}	Receiver Signal Ground Directly connect this pin to receiver signal ground plane.
2	RD+	Receiver Data Out Terminate this high-speed, differential, PECL output with standard PECL techniques at the follow-on device input pin.
3	RD-	Receiver Data Out Bar Terminate this high-speed, differential, PECL output with standard PECL techniques at the follow-on device input pin.
4	SD	Signal Detect Normal optical input levels to the receiver result in a logic "1" output. Low optical input levels to the receiver result in a fault condition indication shown by a logic "0" output. If Signal Detect output is not used, leave it open-circuited This Signal Detect output can be used to drive a PECL input on an upstream circuit, such as, Signal Detect input or Loss of Signal-bar.
5	V_{CCR}	Receiver Power Supply Provide =5 v dc via the recommended transmitter supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCR} pin.
6	V_{CCT}	Transmitter Power Supply Provide =5 v dc via the recommended transmitter supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCT} pin.
7	TD-	Transmitter Data In Bar Terminate this high-speed, differential, Transmitter Data intput with standard PECL techniques at the transmitter input pin.
8	TD+	Transmitter Data In Terminate this high-speed, differential, Transmitter Data intput with standard PECL techniques at the transmitter input pin.
9	V_{EET}	Transmitter Signal Ground Directly connect this pin to the transmitter signal ground plane.

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Storage Temperature	T_S	-40		+85	°C	
Lead Soldering Temperature	T_{SOLD}			+260	°C	
Lead Soldering Time	t_{SOLD}			10	sec.	
Supply Voltage	V_{CC}	-0.5		7.0	V	
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Transmitter Differential Input Voltage	V_D	See Table Below		1.6	V	Note 1
Output Current	I_D			50	mA	
Relative Humidity	RH	0		95	%	

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Ambient Operating Temperature	T_A	0		+70	°C	
Supply Voltage	V_{CC}	4.75		5.25	V	
Power Supply Rejection	PSR		50		mV pp	Note 2
Transmitter Data Input Voltage - Low	V_{IL}-V_{CC}	-1.810		-1.475	V	Note 3
Transmitter Data Input Voltage - High	V_{IH}-V_{CC}	-1.165		-0.880	V	Note 3
Transmitter Differential Input Voltage	V_D	0.3		See Table Above	V	
Data Output Load	R_{DL}		50		Ω	Note 4
Signal Detect Output Load	R_{SDL}		50		Ω	Note 4

Notes:

1. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs without damaging the ESD protection circuit.
2. Tested with a 50 mV p-p sinusoidal signal in the frequency range from 500 Hz to 450 MHz imposed on the V_{CC} supply with the recommended power supply filter in place, see Figure 4. Typically less than a 0.25 dB change in sensitivity is experienced.
3. Compatible with 10K, 10KH and 100K ECL and PECL output signals.
4. The outputs are terminated to V_{CC} - 2 V.

Transmitter Electrical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 4.75 to 5.25 V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Supply Current	I_{CCT}		150	200	mA	Note 5
Power Dissipation	P_{DIST}		0.75	1.05	W	
Data Input Current - Low	I_{IL}	-350	0		µA	
Data Input Current -High	I_{IH}		16	350	µA	

Receiver Electrical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 4.75 to 5.25 V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Supply Current	I_{CCR}		113	177	mA	
Power Dissipation	P_{DISR}		0.37	0.77	W	Note 6
Data Output Voltage - Low	$V_{OL} - V_{CC}$	-1.950	-1.80	-1.620	V	Note 7
Data Output Voltage - High	$V_{OH} - V_{CC}$	-1.045	-0.96	-0.740	V	Note 7
Data Output Rise Time	t_R	0.2	0.3	0.51	ns	Note 8
Data Output Fall Time	t_F	0.2	0.3	0.51	ns	Note 8
Signal Detect Output Voltage - Low	$V_{OL} - V_{CC}$	-1.950	-1.80	-1.620	V	Note 7
Signal Detect Output Voltage - High	$V_{OH} - V_{CC}$	-1.045	-0.96	-0.740	V	Note 7
Signal Detect Assert Time (Off to On)	t_{SDA}		30	100	µs	Note 9
Signal Detect Deassert Time (On to Off)	t_{SDD}		100	350	µs	Note 10

Notes:

5. The I_{CC} value is held nearly constant to minimize unwanted electrical noise from being generated and conducted or emitted to neighboring circuitry.
6. Power dissipation value is the power dissipated in the receiver itself. It is calculated as the sum of the products of V_{CC} and I_{CC} minus the sum of the products of the output voltages and load currents.
7. These outputs are compatible with 10K, 10KH and 100K ECL and PECL inputs.
8. These are 20% - 80% values.
9. The Signal Detect output will change from logic “0” to “1” within 100 µs of a step transition in input optical power from no light to -26 dBm.
10. The Signal Detect output will change from logic “1” to “0” within 350 µs of a step transition in input optical power from -28 dBm to no light.

Transmitter Optical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 4.75 to 5.25 V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Output Optical Power 62.5/125 µm. NA = 0.275 fiber	P_O (BOL) P_O (EOL)	-19 -20	-17	-14 -14	dBm avg.	
Output Optical Power 50/125 µm. NA = 0.20 fiber	P_O (BOL) P_O (EOL)		-21.5 -22.5	-14 -14	dBm avg.	
Output Optical Power at Logic "0" State	P_O ("0")		-60		dBm avg.	
Optical Extinction Ratio		10	46		dB	
Center Wavelength	λc	1270	1330	1380	nm	
Spectral Width - FWHM	σ		136	200	nm	Note 11
Optical Rise Time	t_R		0.7	1.25	ns	Note 12
Optical Fall Time	t_F		0.9	1.25	ns	Note 12
Overshoot			1.0	25	%	
System Jitter Contributed by the Transmitter	SJ		0.04	0.23	ns p-p	
Random Jitter Contributed by the Transmitter	RJ		0.0	0.10	ns p-p	

Notes:

11. The relationship between FWHM and RMS values for spectral width can be derived from the assumption of a Gaussian shaped spectrum which results in RMS = FWHM/2.35.
12. These are 10-90% values.

Receiver Optical Characteristics

(T_A = 0°C to +70°C, V_{CC} = 4.75 to 5.25 V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Input Optical Power	P_{IN}	-26		-14	dBm avg.	Note 13
Input Operating Wavelength	λ	1270		1380	nm	
System Jitter Contributed by the Receiver	SJ			0.30	ns p-p	
Random Jitter Contributed by the Receiver	RJ			0.48	ns p-p	
Signal Detect - Asserted	P_A	P_D +1.0 dB	-30	-28	dBm avg.	
Signal Detect - Deasserted	P_D	-45	-32.4		dBm avg.	
Signal Detect - Hysteresis	P_A - P_D	1.0	-2.4		dB	

Notes:

13. This specification is intended to indicate the performance of the receiver section of the transceiver when the input power ranges from the minimum level (with a window time-width) to the maximum level. Over the range the receiver is guaranteed to provide output data with a Bit Error Ratio (BER) better than or equal to 1 x 10^{-10}
    - At the Beginning of Life (BOL)
    - Over the specified operating temperature and voltage ranges
    - Input is at 622.08 Mbd, 2^{23}-1 PRBS data pattern with 72 “1”s and 72 “0”s inserted per the CCITT (now ITU-T) recommendation G.958 Appendix 1.
    - Receiver worst-case output data eye-opening (window time-width) is measured by applying worst-case input systematic (SJ) and random jitter (RJ). The worst-case maximum input SJ = 0.5 ns peak-to-peak and the RJ = 0.15 ns peak-to-peak. Since the random jitter contribution is very small and difficult to produce exactly, only the maximum systematic jitter is produced and used. The corresponding receiver test window time-width must meet the requirement of 0.31 ns or larger. This worst-case test window time-width results from the following jitter equation:
      Minimum Test Window Time-Width = Baud Interval - Tx SJ max. - Rx SJ max. - Rx RJ max.
      Respectively, Minimum Test Window Time-Width = 1.608 ns - 0.50 ns - 0.30 ns - 0.48 ns = 0.328 ns.
      This is a test method that is within practical test error of the worst-case 0.31 ns limit.
    - Transmitter operating with a 622.08 Mbd, 311.04 MHz square wave input signal to simulate any cross talk present between the transmitter and receiver sections of the transceiver.

www.hp.com/go/fiber

For technical assistance or the location of your nearest Hewlett-Packard sales office, distributor or representative call:

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