HD66350T (TFT Driver)

256-level Grayscale TFT for XGA/SXGA/UXGA Systems

HITACHI

ADE-207-297(Z)
Preliminary
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Description

The HD66350T is a TFT-LCD source driver LSI suitable for XGA, SXGA, and UXGA systems. It receives 8-bit-per-pixel digital display data, and generates and outputs voltages for 256 grayscales. The output circuit includes an operational amplifier, and is capable of alternate output of 256 positive-polarity grayscale voltages and 256 negative-polarity grayscale voltages on individual output pins (dot inversion drive).

Users can select 384 or 402 outputs. For XGA and SXGA, respectively, eight and ten 384-output LSIs are used. For UXGA, twelve 402-output LSIs are used.

Features

- High-speed operation
  - Operating clock: 65 MHz (Vcc = 3.0 to 3.6 V) and 50 MHz (Vcc = 2.5 to 3.0 V)
- Operational power-supply voltage range
  - V_{CC} = 2.5 to 3.6 V
  - V_{LCD} = 10 to 15.5 V
- LCD drive voltage
  - Low-voltage side: 0.1 to $V_{LCD}/2 - 0.2$ (V)
  - High-voltage side: $V_{LCD}/2 + 0.2$ to $V_{LCD} - 0.1$ (V)
- LCD drive outputs
  - 384/402 outputs can be selected:
    Eight 384-output LSIs for XGA,
    Ten 384-output LSIs for SXGA, and
    Twelve 402-output LSIs for UXGA
- Data inversion function
  - Each port has a data inversion pin (a total of two pins), which reduces the power consumption of the data buses.

Hitachi semiconductor

- Multicolor display
  — The HD66350T receives 8-bit-per-pixel digital display data, and selects and outputs a display voltage from 256 grayscale voltages, enabling a maximum of 16,770,000 display colors (full colors) when using R/G/B color filters.

- 48 data bits (8 grayscale code bits × RGB × 2 ports)

- High-voltage asymmetric drive
  — The wide dynamic range of 15.3 V and the ability to output positive-polarity and negative-polarity voltages make it unnecessary to provide a counter-electrode alternating current. Also, since both positive-polarity and negative-polarity voltages are generated by an externally provided reference power supply, gamma compensation is possible according to the characteristics of the liquid crystal.

- Dot inversion drive
  — The voltage can be alternated between positive polarity and negative polarity on individual output pins, allowing a dot-by-dot inversion drive even with a single-sided layout configuration. This provides a high-quality display with little crosstalk.

- Low-output voltage deviation of ±3 mV

- Operational amplifier
  — The output circuit includes an operational amplifier.

- Bidirectional shift

- Package
  — TCP (customized package dimensions)

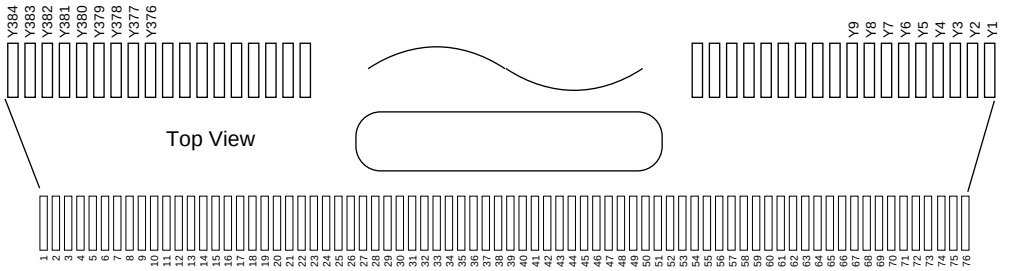
- Supported systems
  — XGA (1024 × 768 dots), SXGA (1280 × 1024 dots), and UXGA (1600 × 1200 dots)

- Applications

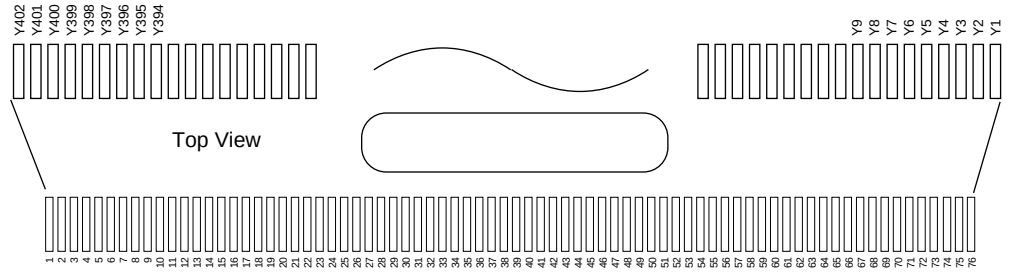
  — Portable PCs and monitors

Pin Arrangement

• 384-output LSI



• 402-output LSI



1 EIO2	21 D34	41 V2	61 D16
2 D57	22 D33	42 V1	62 D15
3 D56	23 D32	43 V0	63 D14
4 D55	24 D31	44 GND	64 D13
5 D54	25 D30	45 TEST2	65 D12
6 D53	26 VCC	46 TEST	66 D11
7 D52	27 OS	47 CL2	67 D10
8 D51	28 SHL	48 CL1	68 D07
9 D50	29 FSL	49 M	69 D06
10 D47	30 STPLS	50 POL1	70 D05
11 D46	31 ODD/EVN	51 POL2	71 D04
12 D45	32 V9	52 D27	72 D03
13 D44	33 V8	53 D26	73 D02
14 D43	34 V7	54 D25	74 D01
15 D42	35 V6	55 D24	75 D00
16 D41	36 V5	56 D23	76 EIO1
17 D40	37 V_{LCD}	57 D22	
18 D37	38 AGND	58 D21	
19 D36	39 V4	59 D20	The TCP package dimensions are
20 D35	40 V3	60 D17	not standardized.

Figure 1 Pin Arrangement

Internal Block Diagram

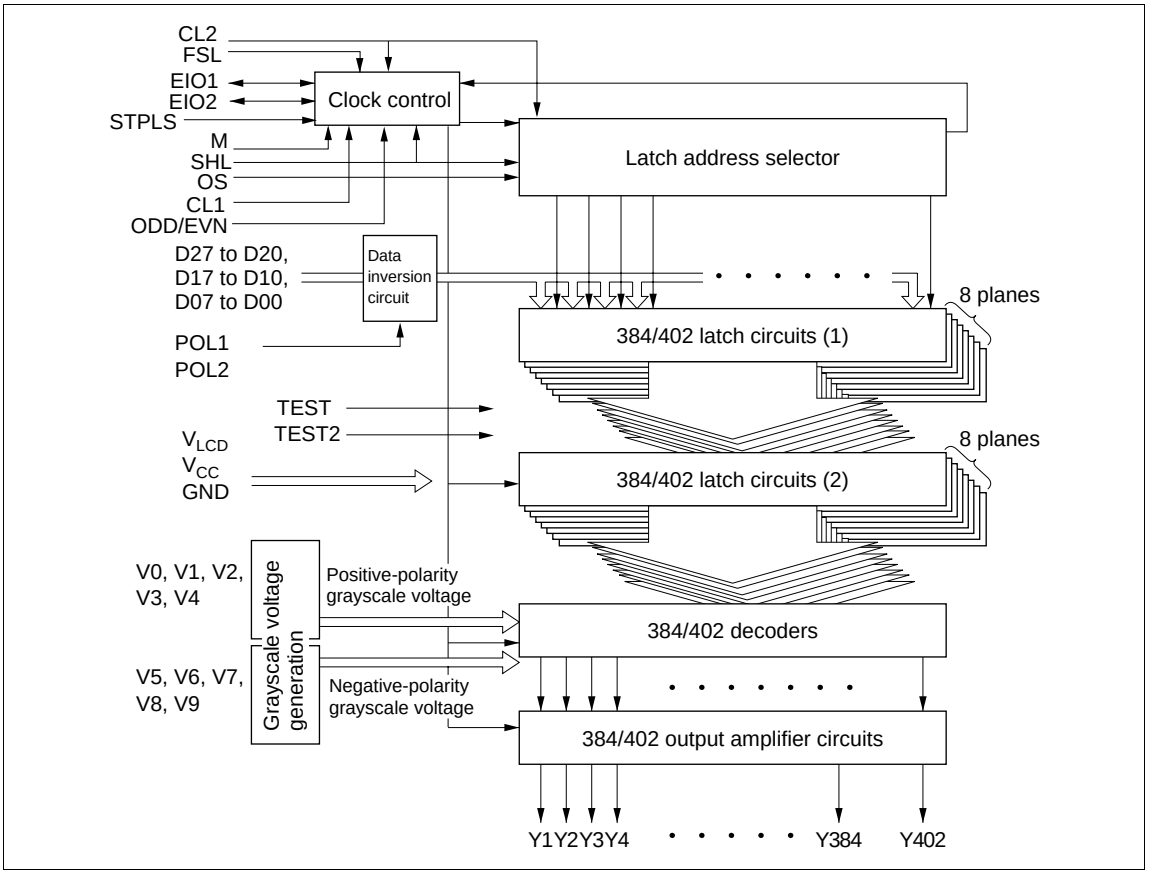


Figure 2 Block Diagram

1. Clock control unit

   Generates the chip-enable signals (EIO2, EIO1) and controls internal timing signals.

2. Data inversion circuit

   Uses the POL1 and POL2 signals to perform data polarity inversion (POL = 1) or non-inversion (POL = 0) processing of input display data.

3. Latch address selector

   Generates latch signals for sequentially latching the input display data. Setting the OS pin enables the operation of the 384-output driver (OS = 0) or 402-output driver (OS = 1).

4. Latch circuits (1)

   402 × 8-bit latch circuits that sequentially latch 6-output × 8-bit input display data.

5. Latch circuits (2)

   Perform latching, in synchronization with CL1, of the 402 × 8-bit data latched by latch circuits (1).

6. Decoders

Decode the 8-bit data and select the liquid-crystal application voltages.

7. Grayscale voltage generation unit

Performs resistance- and capacitance-division of the external input voltage, and generates 256 positive-polarity grayscales and 256 negative-polarity grayscales.

8. Output amplifier circuits

Output the grayscale voltage that has been selected for each output and buffered in the operational amplifier.

Pin Functions

Table 1 Pin Functions

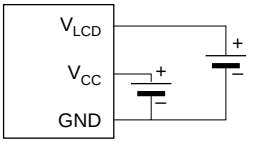
Signal Name	Quantity	Input/Output	Function
V_{LCD}	1	Power supply	 V_{LCD} – GND: Driver-circuit power supply V_{CC} – GND: Logic-circuit power supply
V_{CC}	1	Power supply	
GND/AGND	2	Power supply	
V9 to V5	5	Power supply	Reference power supply for generating the liquid-crystal application voltage. Supplies a voltage in the range VLCD/2 + 0.5 to VLCD – 0.1 V to pins V0–V4, and a voltage in the range 0.1 V to VLCD/2 – 0.5 to pins V5–V9.
V4 to V0	5		
CL1	1	Input	Data of one line is transferred to the latch at the rising edge of this clock, and the liquid-crystal application voltage is output at the falling edge. One pulse must be input in each horizontal period.
CL2	1	Input	Display data is latched at the rising edge of this clock. For the 384-output LSIs, after the start pulse input, the start pulse output goes high at the rising edge of the 63rd (66th) clock, and this becomes the start pulse of the next-stage driver. The 65th (68th) clock of the first-stage driver is the start-pulse latch clock of the next-stage driver. After the start pulse input, display data latching is halted automatically when 66 (69) clock pulses are input. (Values in parentheses are for the 402-output LSIs.)
POL1, POL2	1	Input	Data-polarity inversion signal to reduce power consumption of data bus lines in the interface. When POL1 or POL2 is high, display data is inverted in the driver. When POL1 or POL2 is low, display data is input without inversion in the driver. The POL1 signal controls the polarity of 24 data (D00 to D27). The POL2 signal controls the polarity of 24 data (D30 to D57). When POL1 or POL2 is not used, this pin must be either high or low.
D57 to D50, D47 to D40, D37 to D30, D27 to D20, D17 to D10, D07 to D00	48	Input	Inputs 8-bit (grayscale data) × 6-pixel display data. Dx0 is the LSB, and Dx7 is the MSB.

Table 1 Pin Functions (cont)

Signal Name	Quantity	Input/Output	Function
EIO1, EIO2	2	Input/output	Chip-enable signals. Input/output switching is controlled by the SHL signal. When these signals are used as inputs, display data latching is performed when the input goes high. When these signals are used as outputs, a low-to-high transition is made at the rising edge of the 63rd (66th) clock of the CL2 signal, and the next-stage driver is activated. (Values in parentheses are for the 402-output LSIs.) SHL = V_{CC}: EIO1 = Input, EIO2 = Output SHL = GND: EIO1 = Output, EIO2 = Input
M	1	Input	Current-alternating signal, controlling the liquid-crystal alternating-current drive. The M signal is input after provision of a setup time with respect to the rise of the CL1 signal. Positive-polarity (V0–V4) and negative-polarity (V5–V9) output voltages are generated as shown below according to the polarity of the latched M signal. M = 0: Odd output pins (Y1,Y3,..,Y383): Positive-polarity liquid-crystal application voltage is output; Even output pins (Y2,Y4,..,Y384): Negative-polarity liquid-crystal application voltage is output M = 1: Odd output pins (Y1,Y3,..,Y383): Negative-polarity liquid-crystal application voltage is output; Even output pins (Y2,Y4,..,Y384): Positive-polarity liquid-crystal application voltage is output
OS	1	Input	Pin for switching the number of outputs. When OS is low, this LSI operates as a 384-output product. When OS is high, this LSI operates as a 402-output product. Since this pin performs 50-kΩ pull-down processing within the chip, it must be opened or low when used as the 384-output product. When this pin is used as the 402-output product, it must be high.
FSL	1	Input	Pin for switching the operating speed. When it is used in the range of 40 to 65 MHz, input high level. When it is used in the range of 30 to 40 MHz, input low level. Since this pin performs 50-kΩ pull-down processing within the chip, it can be opened when it is used in the range of 30 to 40 MHz.
STPLS	1	Input	Input the same signal as the start pulse, which is input in the first-stage IC, to the STPLS pin in all drivers. This pin is required for high-speed operation.
ODD/EVN	1	Input	When this pin is used for 402-output operation (OS = high), use the first, third, or fifth pin as low level in the order of fetched data. Use the second, fourth, or sixth pin as high level. This pin is required for 402-output operation. When this pin is used for 384-output operation (OS = low), set this pin to low in all drivers. Since this pin performs 50-kΩ pull-down processing within the chip, it can be opened.

Table 1 Pin Functions (cont)

Signal Name	Quantity	Input/Output	Function
Y1 to Y402	402	Output	Signal lines for output of liquid-crystal application voltages. For the 384-output LSI, 18 invalid outputs can be selected to not lead to the TCP.
TEST, TEST2	2	Input	Test pins. Set these pins to low. Since these pins perform 50-kΩ pull-down processing within the chip, use them opened or low.
SHL	1	Input	Controls display-data shift direction. • 384-output LSI (OS is low or opened).

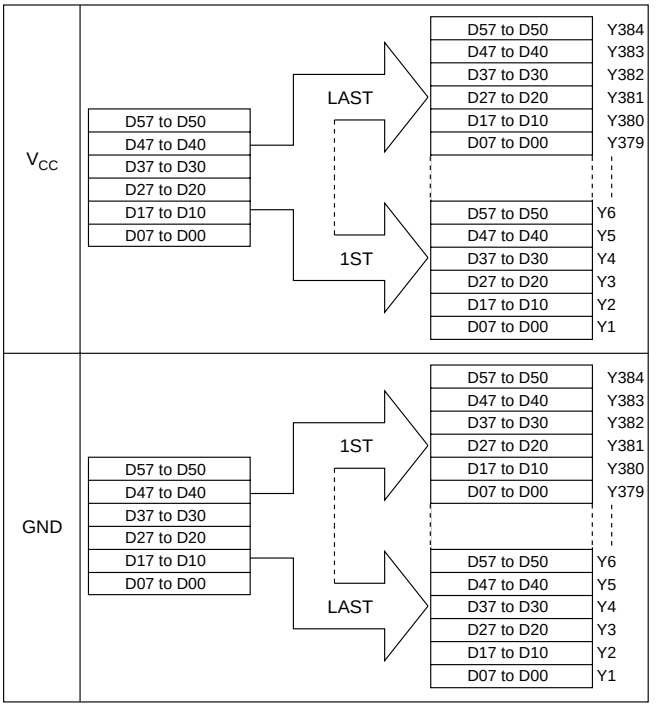
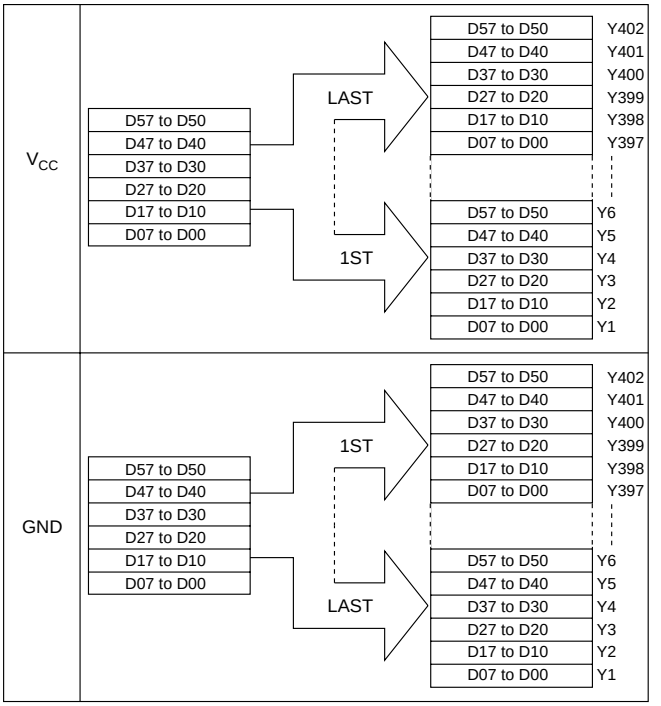


Table 1 Pin Functions (cont)

Signal Name	Quantity	Input/Output	Function
SHL	1	Input	• 402-output LSI (OS is high).



System Overview

Figure 3 is a block diagram of the configuration of an XGA (1024 × 768) compatible TFT color panel with the HD66350Ts. The HD66350T latches 8-bit data for each dot, selects a level from the 256 positive-polarity or negative-polarity liquid-crystal application voltages generated internally, and outputs that voltage.

By configuring pixels using R/G/B color filters, a full-color display of approximately 16,770,000 colors can be achieved.

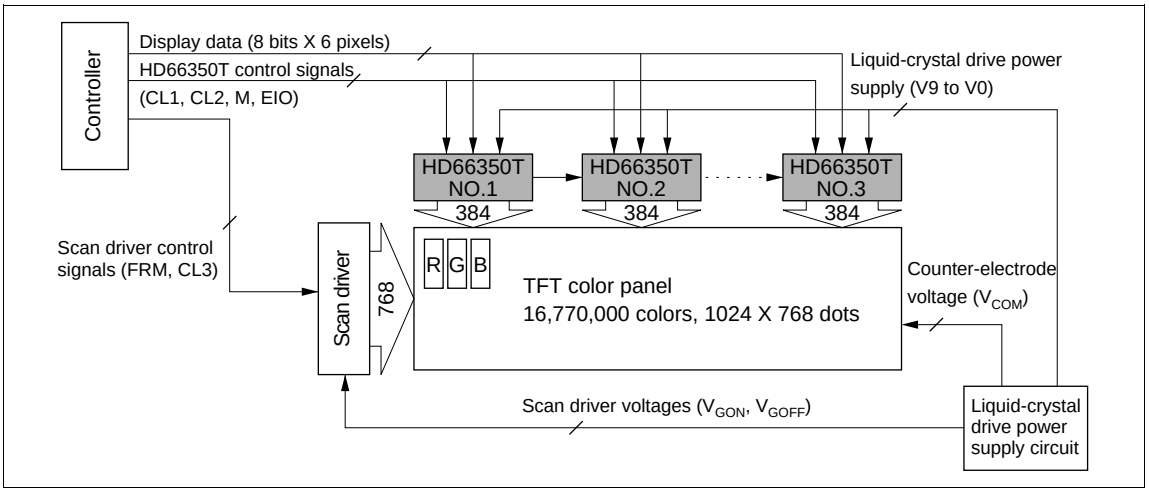


Figure 3 System Block Diagram

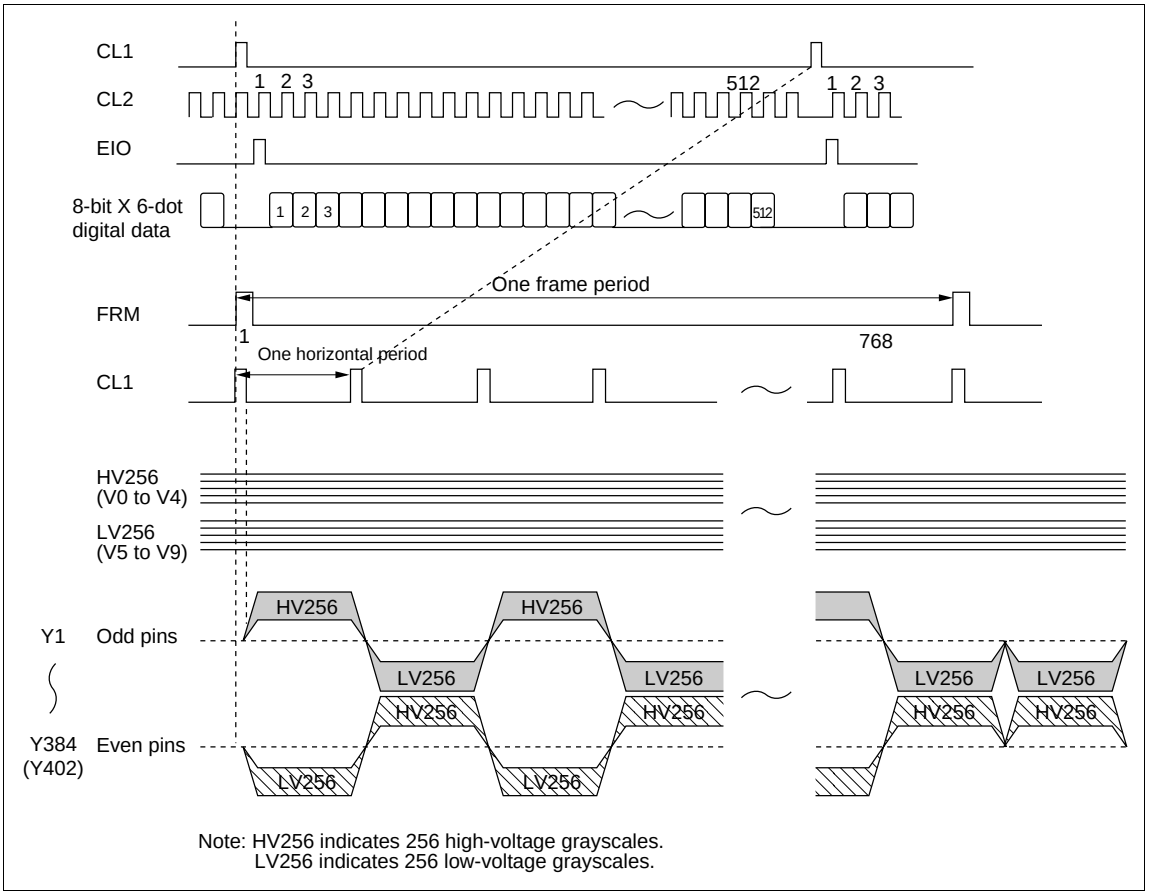


Figure 4 Timing Chart (Example of a Dot-inversion Drive System)

Operation Timing

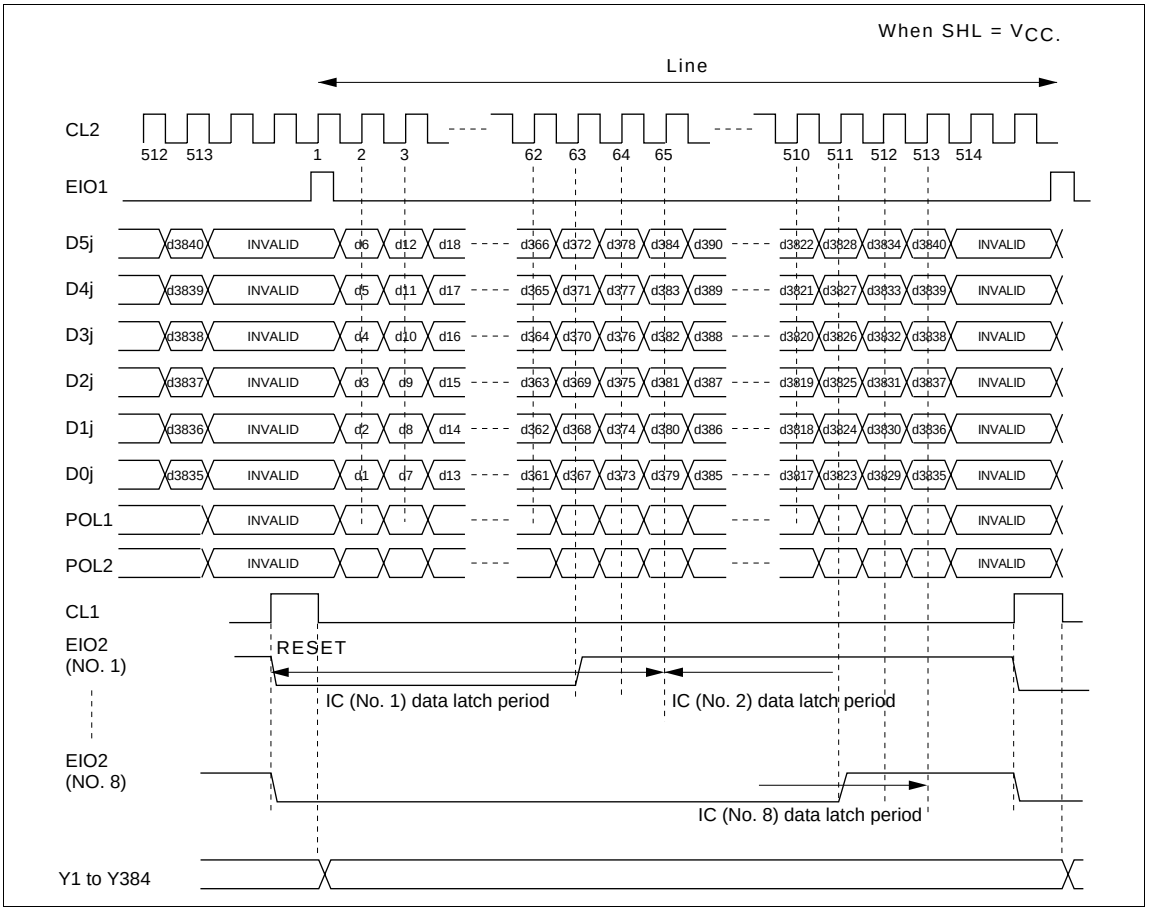


Figure 5 Operation Timing

The high level of the enable-input signal (when SHL = V_{CC}: EIO1) is latched at the rising edge of the data-latch clock signal CL2, and data latching begins after one CL2 signal cycle. Data of 8 bits × RGB × 2 pixels, i.e. 6 outputs, are simultaneously latched at the rising edge of the CL2 signal. At the rising edge of the 63rd clock pulse of the CL2 signal, the enable-output signal (when SHL = V_{CC}: EIO2) is driven high, and the operation is automatically halted (the standby state is entered) when latching of data for 384 outputs is completed. By connecting the EIO2 pin to the next-stage EIO1 pin, the next-stage IC is activated in the same way. All the IC enable-output signals are reset at the rising edge of the CL1 signal.

The data-latch clock signal CL2 does not require a clock-halted period. At least two clocks must be added to the necessary CL2 clocks (512 clocks for XGA) in each horizontal period.

M Signal and Data Input

This example shows the relationship between the data input, M signal, and output level, with dot-by-dot inversion and frame inversion. The HD66350T driver must hold the M signal during the high-level period of CL1. The grayscale-voltage selection circuits for high and low voltages are operated according to the M signal level at the rise of CL1, and the grayscale voltages are output at the following rising edges of CL1.

To provide stable output operation of the buffer amplifier, the output is placed in the high-impedance state in the high-level period of CL1.

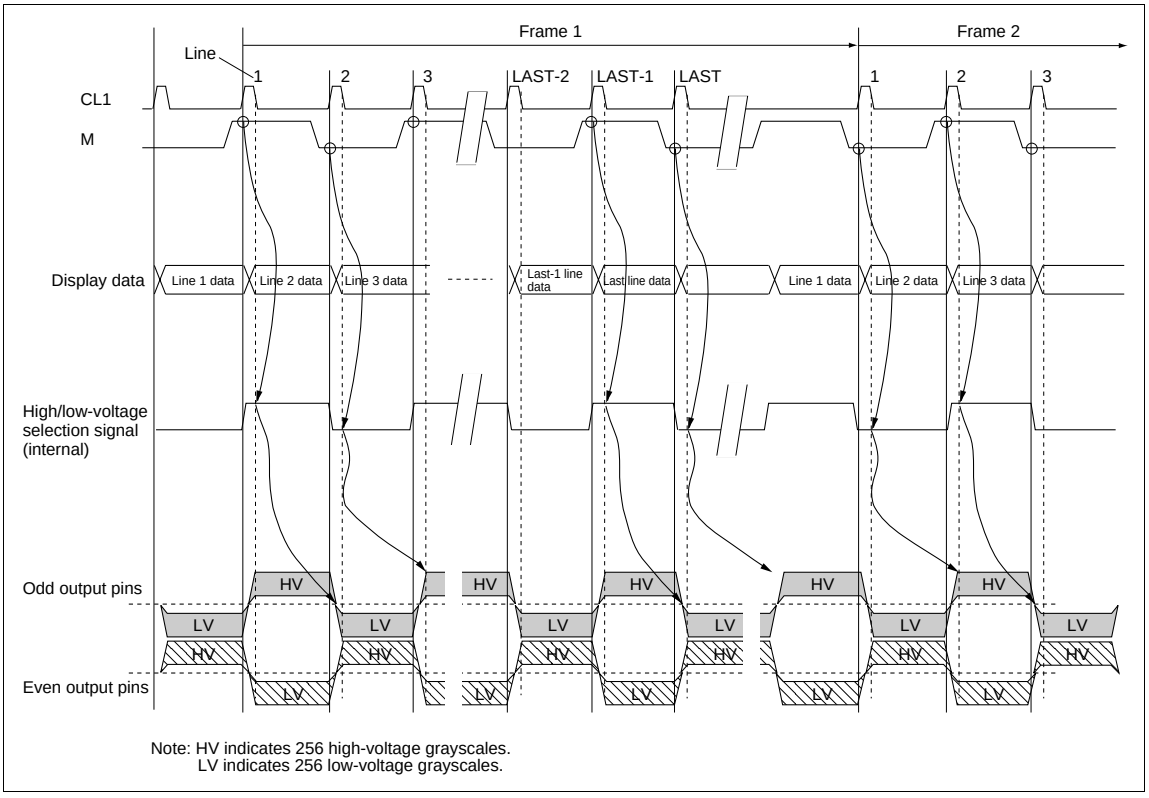


Figure 6 Relationship between the M Signal and Data Input

Pin-by-pin Inversion Drive

With regard to the inversion standard voltage for individual adjacent odd and even output pins, the HD66350T can generate 256-level positive-polarity and negative-polarity grayscale voltages. In addition, the liquid-crystal alternating-current drive can be controlled by switching the polarity of the M signal. (See the Pin Functions section.)

In this way, when HD66350Ts are arranged on either the upper or lower side of a TFT LCD panel, a dot inversion drive can be used in which grayscale voltages of different polarities are applied to individual adjacent dots by switching the M signal on each CL1 clock, reducing the crosstalk which adversely affects image quality, and thus achieving a high-quality display.

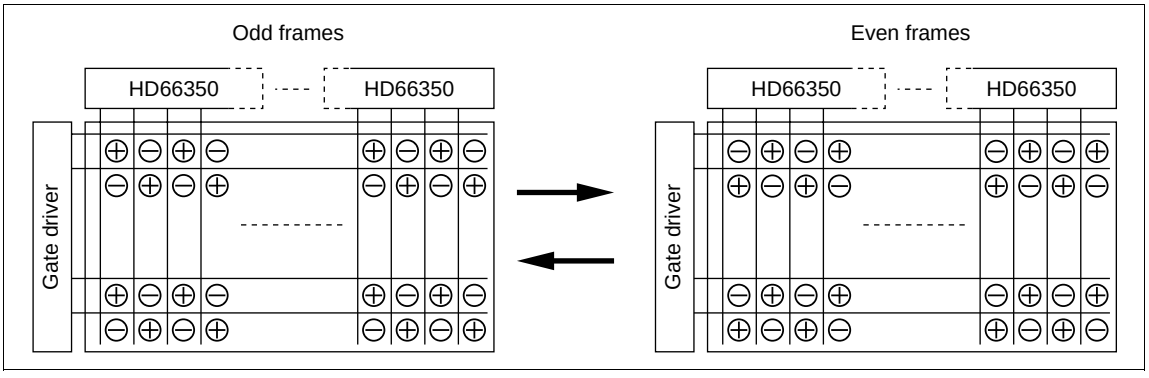


Figure 7 Dot Inversion Drive

When the M signal switches on each CL1n clock, the following n-raster-row inversion drive can be used on each horizontal dot and vertical n-raster-row.

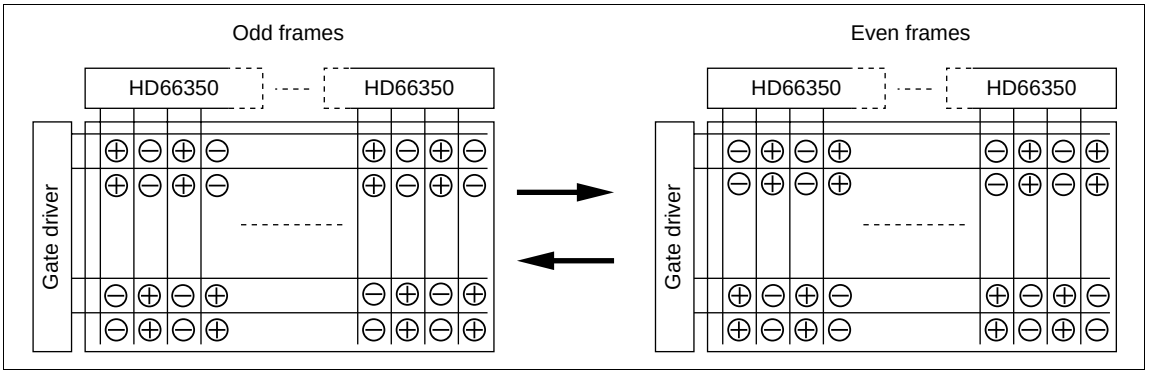


Figure 8 n-raster-row Inversion Drive

When the M signal switches on each FLM signal, the following frame inversion drive can be used on each horizontal dot and vertical frame.

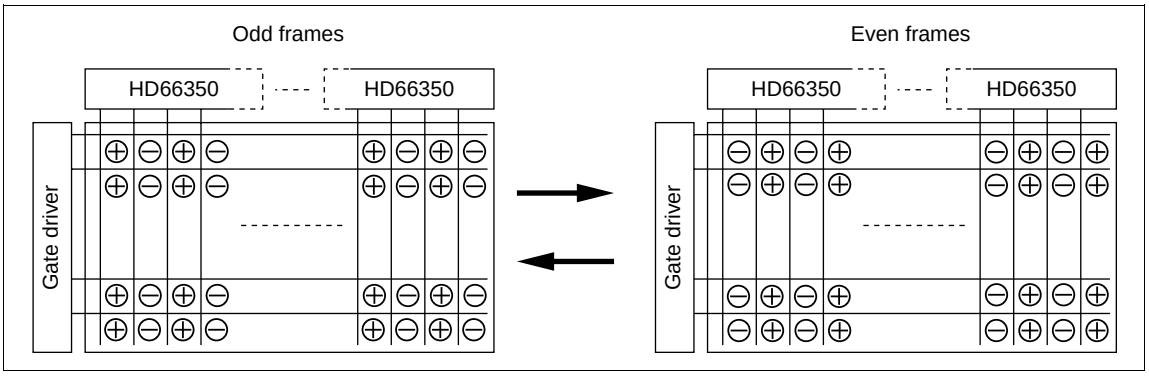


Figure 9 Frame Inversion Drive

System Application

Figure 10 shows system applications for XGA-, SXGA-, and UXGA-sized TFT color panels with the HD66350Ts.

For the XGA or SXGA size, the dot clock frequency is halved by the timing converter and data are transferred to the drivers. For the UXGA size, after the dot clock frequency is halved, data are transferred to odd and even drivers in parallel with the frequency halved again. Since one horizontal period is shorter for the UXGA size, the screen can be divided into upper and lower screens for the purpose of transferring data if the display panel has a large TFT load capacitance.

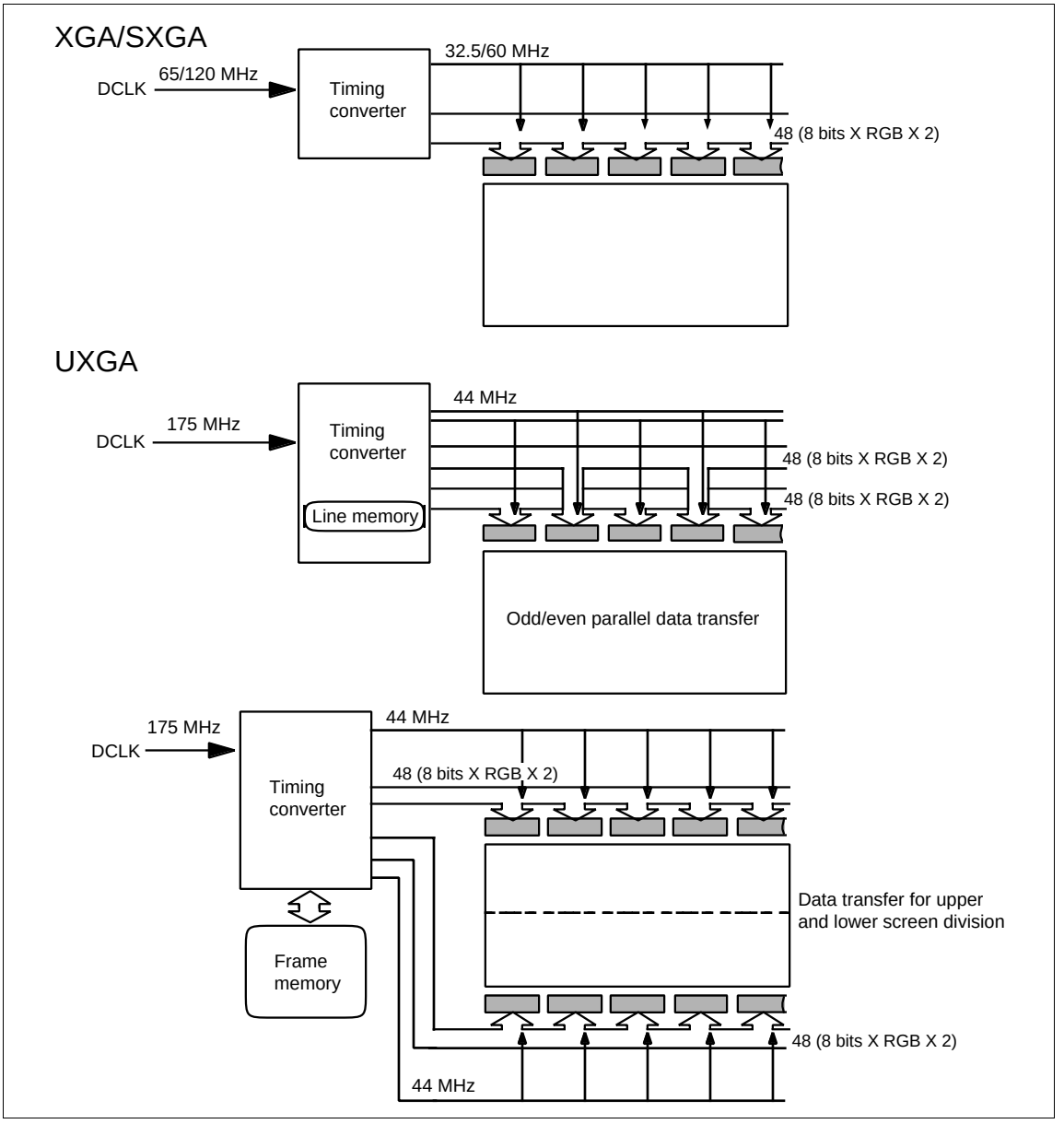


Figure 10 System Applications

Display Data and Output Voltage

With input of a 10-level liquid-crystal power supply and 8-bit digital data, the HD66350T outputs 256 grayscale voltage levels on the high-voltage side and 256 grayscale voltage levels on the low-voltage side.

Tables 2 and 3 show the relationship between the input voltages of the liquid-crystal power supply, digital codes, and output voltages.

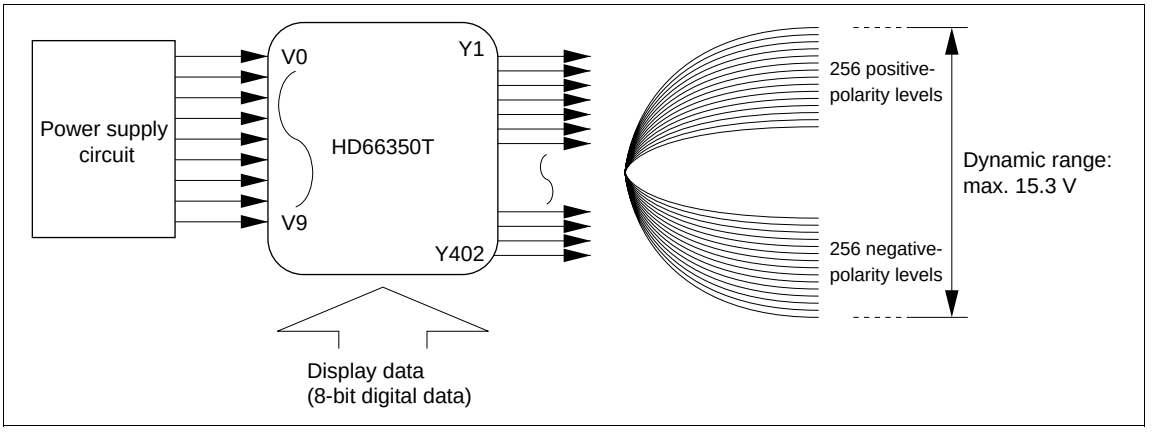


Figure 11 Selection of the LCD Drive Output Level

Ladder Resistance Values (Reference Values)

	Resistance Name	Resistance Value
V0,V9	R0	600
	R1	516
	R2	450
	R3	390
	R4	339
	R5	300
	R6	270
	R7	255
V1,V8	R8	240
	R9	240
	R10	240
	R11	240
	R12	243
	R13	252
	R14	261
	R15	264
V2,V7	R16	270
	R17	285
	R18	300
	R19	315
	R20	330
	R21	354
	R22	366
	R23	390
V3,V6	R24	420
	R25	480
	R26	540
	R27	600
	R28	660
	R29	720
	R30	900
	R31	1200
V4,V5	Total	13230

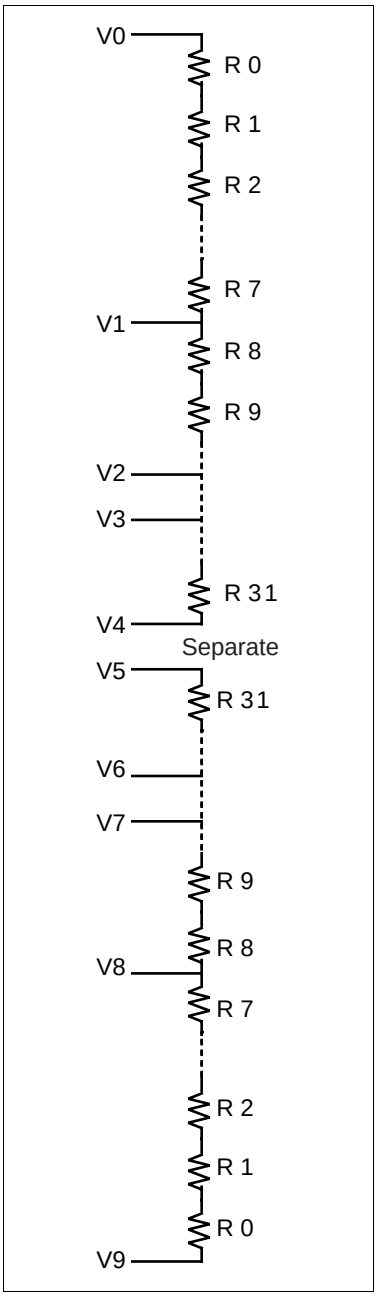


Figure 12 Ladder Resistance

Table 2 256 Positive-polarity Grayscale Levels

Display Data									256 Positive-polarity Grayscale Levels
Code	Di7	Di6	Di5	Di4	Di3	Di2	Di1	Di0	
00h	0	0	0	0	0	0	0	0	V0
01h	0	0	0	0	0	0	0	1	
02h	0	0	0	0	0	0	1	0	
03h	0	0	0	0	0	0	1	1	Divided into eight levels
04h	0	0	0	0	0	1	0	0	
05h	0	0	0	0	0	1	0	1	
06h	0	0	0	0	0	1	1	0	
07h	0	0	0	0	0	1	1	1	
08h	0	0	0	0	1	0	0	0	V0-(V0-V1)X600/3120
⋮									Divided into eight levels
10h	0	0	0	1	0	0	0	0	V0-(V0-V1)X1116/3120
⋮									Divided into eight levels
18h	0	0	0	1	1	0	0	0	V0-(V0-V1)X1566/3120
⋮									Divided into eight levels
20h	0	0	1	0	0	0	0	0	V0-(V0-V1)X1956/3120
⋮									Divided into eight levels
28h	0	0	1	0	1	0	0	0	V0-(V0-V1)X2295/3120
⋮									Divided into eight levels
30h	0	0	1	1	0	0	0	0	V0-(V0-V1)X2595/3120
⋮									Divided into eight levels
38h	0	0	1	1	1	0	0	0	V0-(V0-V1)X2865/3120
⋮									Divided into eight levels
40h	0	1	0	0	0	0	0	0	V1
⋮									Divided into eight levels
48h	0	1	0	0	1	0	0	0	V1-(V1-V2)X240/1980
⋮									Divided into eight levels
50h	0	1	0	1	0	0	0	0	V1-(V1-V2)X480/1980
⋮									Divided into eight levels
58h	0	1	0	1	1	0	0	0	V1-(V1-V2)X720/1980
⋮									Divided into eight levels
60h	0	1	1	0	0	0	0	0	V1-(V1-V2)X960/1980
⋮									Divided into eight levels
68h	0	1	1	0	1	0	0	0	V1-(V1-V2)X1203/1980
⋮									Divided into eight levels
70h	0	1	1	1	0	0	0	0	V1-(V1-V2)X1455/1980
⋮									Divided into eight levels
78h	0	1	1	1	1	0	0	0	V1-(V1-V2)X1716/1980
⋮									Divided into eight levels
80h	1	0	0	0	0	0	0	0	V2

Table 2 256 Positive-polarity Grayscale Levels (cont)

Display Data									256 Positive-polarity Grayscale Levels
Code	Di7	Di6	Di5	Di4	Di3	Di2	Di1	Di0	
80h	1	0	0	0	0	0	0	0	V2
⋮									Divided into eight levels
88h	1	0	0	0	1	0	0	0	V2-(V2-V3)X270/2610
⋮									Divided into eight levels
90h	1	0	0	1	0	0	0	0	V2-(V2-V3)X555/2610
⋮									Divided into eight levels
98h	1	0	0	1	1	0	0	0	V2-(V2-V3)X855/2610
⋮									Divided into eight levels
A0h	1	0	1	0	0	0	0	0	V2-(V2-V3)X1170/2610
⋮									Divided into eight levels
A8h	1	0	1	0	1	0	0	0	V2-(V2-V3)X1500/2610
⋮									Divided into eight levels
B0h	1	0	1	1	0	0	0	0	V2-(V2-V3)X1854/2610
⋮									Divided into eight levels
B8h	1	0	1	1	1	0	0	0	V2-(V2-V3)X2220/2610
⋮									Divided into eight levels
C0h	1	1	0	0	0	0	0	0	V3
⋮									Divided into eight levels
C8h	1	1	0	0	1	0	0	0	V3-(V3-V4)X420/5520
⋮									Divided into eight levels
D0h	1	1	0	1	0	0	0	0	V3-(V3-V4)X900/5520
⋮									Divided into eight levels
D8h	1	1	0	1	1	0	0	0	V3-(V3-V4)X1440/5520
⋮									Divided into eight levels
E0h	1	1	1	0	0	0	0	0	V3-(V3-V4)X2040/5520
⋮									Divided into eight levels
E8h	1	1	1	0	1	0	0	0	V3-(V3-V4)X2700/5520
⋮									Divided into eight levels
F0h	1	1	1	1	0	0	0	0	V3-(V3-V4)X3420/5520
⋮									Divided into eight levels
F8h	1	1	1	1	1	0	0	0	V3-(V3-V4)X4320/5520
F9h	1	1	1	1	1	0	0	1	
FAh	1	1	1	1	1	0	1	0	
FBh	1	1	1	1	1	0	1	1	
FCh	1	1	1	1	1	1	0	0	Divided into eight levels
FDh	1	1	1	1	1	1	0	1	
FEh	1	1	1	1	1	1	1	0	
FFh	1	1	1	1	1	1	1	1	V4+1/8X(V3-V4)X1200/5520
									V4

Table 3 256 Negative-polarity Grayscale Levels

Display Data									256 Negative-polarity Grayscale Levels
Code	Di7	Di6	Di5	Di4	Di3	Di2	Di1	Di0	
00h	0	0	0	0	0	0	0	0	V9
01h	0	0	0	0	0	0	0	1	
02h	0	0	0	0	0	0	1	0	
03h	0	0	0	0	0	0	1	1	Divided into eight levels
04h	0	0	0	0	0	1	0	0	
05h	0	0	0	0	0	1	0	1	
06h	0	0	0	0	0	1	1	0	
07h	0	0	0	0	0	1	1	1	
08h	0	0	0	0	1	0	0	0	V9-(V9-V8)X600/3120
⋮									Divided into eight levels
10h	0	0	0	1	0	0	0	0	V9-(V9-V8)X1116/3120
⋮									Divided into eight levels
18h	0	0	0	1	1	0	0	0	V9-(V9-V8)X1566/3120
⋮									Divided into eight levels
20h	0	0	1	0	0	0	0	0	V9-(V9-V8)X1956/3120
⋮									Divided into eight levels
28h	0	0	1	0	1	0	0	0	V9-(V9-V8)X2295/3120
⋮									Divided into eight levels
30h	0	0	1	1	0	0	0	0	V9-(V9-V8)X2595/3120
⋮									Divided into eight levels
38h	0	0	1	1	1	0	0	0	V9-(V9-V8)X2865/3120
⋮									Divided into eight levels
40h	0	1	0	0	0	0	0	0	V8
⋮									Divided into eight levels
48h	0	1	0	0	1	0	0	0	V8-(V8-V7)X240/1980
⋮									Divided into eight levels
50h	0	1	0	1	0	0	0	0	V8-(V8-V7)X480/1980
⋮									Divided into eight levels
58h	0	1	0	1	1	0	0	0	V8-(V8-V7)X720/1980
⋮									Divided into eight levels
60h	0	1	1	0	0	0	0	0	V8-(V8-V7)X960/1980
⋮									Divided into eight levels
68h	0	1	1	0	1	0	0	0	V8-(V8-V7)X1203/1980
⋮									Divided into eight levels
70h	0	1	1	1	0	0	0	0	V8-(V8-V7)X1455/1980
⋮									Divided into eight levels
78h	0	1	1	1	1	0	0	0	V8-(V8-V7)X1716/1980
⋮									Divided into eight levels
80h	1	0	0	0	0	0	0	0	V7

Table 3 256 Negative-polarity Grayscale Levels (cont)

Display Data									256 Negative-polarity Grayscale Levels
Code	Di7	Di6	Di5	Di4	Di3	Di2	Di1	Di0	
80h	1	0	0	0	0	0	0	0	V7
⋮									Divided into eight levels
88h	1	0	0	0	1	0	0	0	V7-(V7-V6)X270/2610
⋮									Divided into eight levels
90h	1	0	0	1	0	0	0	0	V7-(V7-V6)X555/2610
⋮									Divided into eight levels
98h	1	0	0	1	1	0	0	0	V7-(V7-V6)X855/2610
⋮									Divided into eight levels
A0h	1	0	1	0	0	0	0	0	V7-(V7-V6)X1170/2610
⋮									Divided into eight levels
A8h	1	0	1	0	1	0	0	0	V7-(V7-V6)X1500/2610
⋮									Divided into eight levels
B0h	1	0	1	1	0	0	0	0	V7-(V7-V6)X1854/2610
⋮									Divided into eight levels
B8h	1	0	1	1	1	0	0	0	V7-(V7-V6)X2220/2610
⋮									Divided into eight levels
C0h	1	1	0	0	0	0	0	0	V6
⋮									Divided into eight levels
C8h	1	1	0	0	1	0	0	0	V6-(V6-V5)X420/5520
⋮									Divided into eight levels
D0h	1	1	0	1	0	0	0	0	V6-(V6-V5)X900/5520
⋮									Divided into eight levels
D8h	1	1	0	1	1	0	0	0	V6-(V6-V5)X1440/5520
⋮									Divided into eight levels
E0h	1	1	1	0	0	0	0	0	V6-(V6-V5)X2040/5520
⋮									Divided into eight levels
E8h	1	1	1	0	1	0	0	0	V6-(V6-V5)X2700/5520
⋮									Divided into eight levels
F0h	1	1	1	1	0	0	0	0	V6-(V6-V5)X3420/5520
⋮									Divided into eight levels
F8h	1	1	1	1	1	0	0	0	V6-(V6-V5)X4320/5520
F9h	1	1	1	1	1	0	0	1	
FAh	1	1	1	1	1	0	1	0	
FBh	1	1	1	1	1	0	1	1	
FCh	1	1	1	1	1	1	0	0	Divided into eight levels
FDh	1	1	1	1	1	1	0	1	
FEh	1	1	1	1	1	1	1	0	
FFh	1	1	1	1	1	1	1	1	V5+1/8X(V6-V5)X1200/5520
									V5

Input Data and Output Voltages

The HD66350T outputs grayscale voltages of different polarities at the odd and even output pins with respect to the LCD counter-electrode voltage. As an example, figure 13 shows the relationship between the input data and output voltages when VLCD – 0.1 ≥ V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VLCD/2 + 0.2, and VLCD/2 – 0.2 ≥ V5 ≥ V6 ≥ V7 ≥ V8 ≥ V9 ≥ 0.1 V.

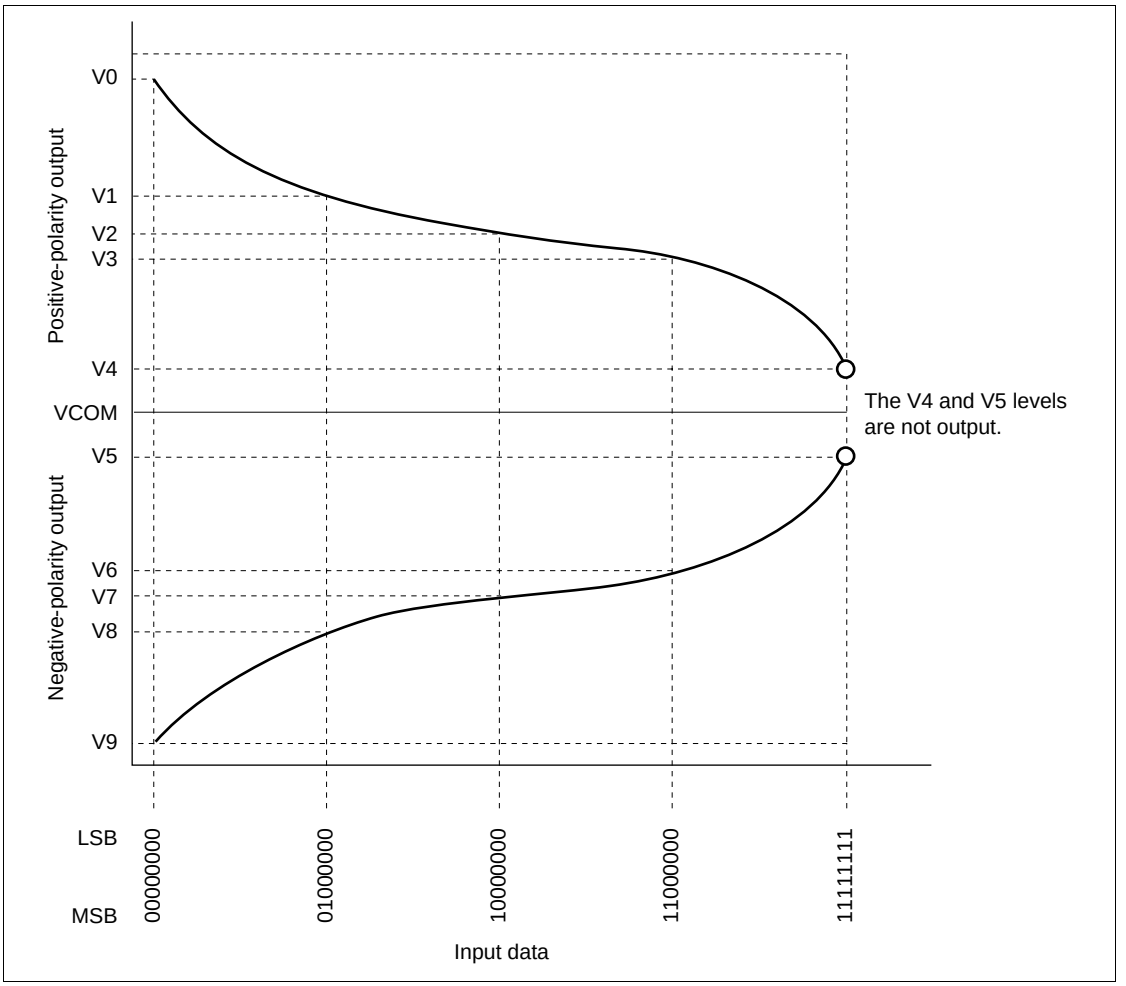


Figure 13 Relationship between Input Data and Output Voltages

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Notes
Power supply voltage	Logic circuit (low voltage)	V_{CC}	–0.3 to +5.0	V	1
	LCD drive circuit (high voltage)	V_{LCD}	–0.3 to +17	V	1
Input voltage (high voltage)		Vt1	–0.3 to V_{LCD} + 0.3	V	1, 2
Input voltage (low voltage)		Vt2	–0.3 to V_{CC} + 0.3	V	1, 3
Storage temperature		Tstg	–55 to +110	°C	

If the LSI is used beyond the above maximum ratings, it may be permanently damaged. It should always be used within its specified operating range for normal operation to prevent malfunction or degraded reliability.

Notes: 1. Value when GND = 0 V and AGND = 0 V.

2. Applies to the CL1, CL2, SHL, Dxx, M, POL1, POL2, OS, TEST, TEST2, STPLS, FSL, and ODD/EVN input pins, and the EIO1 and EIO2 input/output pins when used as input.

3. Specifies the voltage to be input to the LCD drive power supply pins.

   The following relationships must be observed: VLCD ≥ V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VLCD/2 + 0.2, and VLCD/2 – 0.2 ≥ V5 ≥ V6 ≥ V7 ≥ V8 ≥ V9 ≥ 0.

Recommended Operating Ranges

Item		Symbol	Ratings	Unit	Notes
Power supply voltage	Logic circuit (low voltage)	V_{CC}	+2.5 to +3.6	V	1
	LCD drive circuit (high voltage)	V_{LCD}	+10.0 to +15.5	V	1
γ compensation power supply voltage (high voltage)		Vt1U	$V_{LCD}/2$ + 0.2 to V_{LCD}	V	1
γ compensation power supply voltage (low voltage)		Vt1L	0 to $V_{LCD}/2$ – 0.2	V	1
Driver output voltage		Vout	0.1 to V_{LCD} – 0.1	V	1
Max. clock frequency		Fmax	65	MHz	
Operating temperature		Topr	–30 to +75	°C	

Note: 1. Value when GND = 0 V and AGND = 0 V.

Electrical Characteristics

DC Characteristics (Conditions (unless otherwise specified): V_{CC} – GND = 2.5 V to 3.6 V, V_{LCD} – GND = 10.0 V to 15.5 V, Ta = –30°C to +75°C)

Item	Symbol	Applicable Pin	Min.	Typ.	Max.	Unit	Conditions	Not
Input high-level voltage (1)	V_{IH1}	CL1, SHL, TEST, M, EIO1(I),	$0.8 \times V_{CC}$		V_{CC}	V		
Input low-level voltage (1)	V_{IL1}	EIO2(I), Dij, POL1, POL2, OS, and ODD/EVN	0		$0.2 \times V_{CC}$	V		
Input high-level voltage (2)	V_{IH2}	CL2	$0.8 \times V_{CC}$		V_{CC}	V		
Input low-level voltage (2)	V_{IL2}		0		$0.2 \times V_{CC}$	V		
Output high-level voltage	V_{OH}	EIO1(O) and EIO2(O)	V_{CC} – 0.4			V	I_{OH} = –0.4 mA	
Output low-level voltage	V_{OL}				0.4	V	I_{OL} = 0.4 mA	
Input leakage current (1)	IL1	CL1,CL2,SHL, TEST, Dij, M, POL1, POL2, OS, and ODD/EVN	–5		+5	µA		
Input leakage current (2)	IL2	EIO1(I) and EIO2(I)	–10		+10	µA		
γ compensation power supply voltage current	Iref	V0, V5		1.0	2.0	mA	V0–V4 = 7 V V5–V9 = 7 V	
		V4, V9	–2.0	–1.0		mA		
Output voltage deviation	ΔV0	Y1 to Y402	—	±3	±8	mV	Input data 00 to FF	1
Average output voltage dispersion	ΔV_{Δ}	Y1 to Y402	—	±10	—	mV	Input data 00 to FF	2
Logic unit consumptive current	I_{CC}	V_{CC}	—	4	TBD	mA	V_{CC} = 3.3 V V_{LCD} = 15 V f_{CL1} = 83 kHz	3
Driver unit consumptive current	I_{LCD}	V_{LCD}	—	6	TBD	mA	(1 horizontal period = 12 µs) f_{CL2} = 60 MHz	
Input capacitance 1	C1	Input pins except EIO1 and EIO2	—	5	10	pF	Ta = 25°C, Vin = 0 V, f = 1 MHz	
Input capacitance 2	C2	EIO1 and EIO2	—	10	20	pF		

Notes: 1. The output voltage deviation is the difference in adjacent output voltages for the same display data (within the chip).

2. The average output voltage dispersion is the difference in average output voltage between chips; the average output voltage is the average voltage within the chip for the same display data. The average output voltage dispersion is a reference value.

3. With outputs unloaded, and excluding the current flowing in V0–V9. The specification applies to the display pattern (from among solid black, solid white, and dot check patterns) with the largest current.

AC Characteristics (Conditions (unless otherwise specified): V_{CC} – GND = 3.0 V to 3.6 V, V_{LCD} – GND = 10.0 V to 15.5 V, Ta = –30°C to +75°C, Tr = Tf = 2 ns)

Item	Symbol	Applicable Pins	Min.	Typ.	Max.	Unit	Conditions	Notes
Clock cycle time	Trate	CL2	15			ns		
Clock low-level width	Tcwl	CL2	5			ns		
Clock high-level width	Tcwh	CL2	5			ns		
Data setup time	Tds	Dij and CL2	4			ns		
Data hold time	Tdh	Dij and CL2	2			ns		
Start pulse setup time	Tss	EIO1, EIO2, and CL2	–1			ns		
Start pulse hold time	Tsh	EIO1, EIO2, and CL2	7			ns		
POL setup time	Tps	POL1, POL2, and CL2	–1			ns		
POL hold time	Tph	POL1, POL2, and CL2	7			ns		
CL1 high-level width	Tcl1wh	CL1	3			µs		
Data invalid period	Tinv	CL1 and CL2	1			CLK		
Last data timing	Tldt	CL1 and CL2	2			CLK		
Time between CL1 start pulses	Tcl1-eio	CL1, EIO1, and EIO2	20			ns		
M setup time	Tms	M and CL1	–5			ns		
Start pulse delay time	Tsd	EIO1, EIO2, and CL2		15	28	ns	CL = 25 pF	
Driver output delay time (load condition)	Tdd	CL1 and Y1 to Y402		6.0	9	µs	V_{LCD} = 15 V 95% write	1

Note: 1. The specification applies to the following conditions.

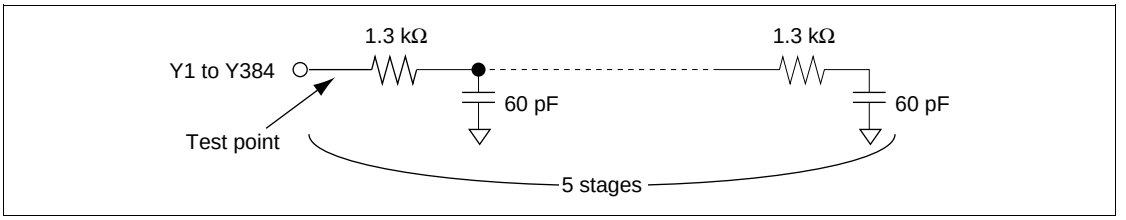


Figure 14 Load Conditions

Switching Characteristic Waveforms

The CL2 high-level width and low-level width are specified by ViH = 0.8 × V_{CC} and ViL = 0.2 × V_{CC}. Other timings are specified by ViH and ViL = 0.5 × V_{CC}.

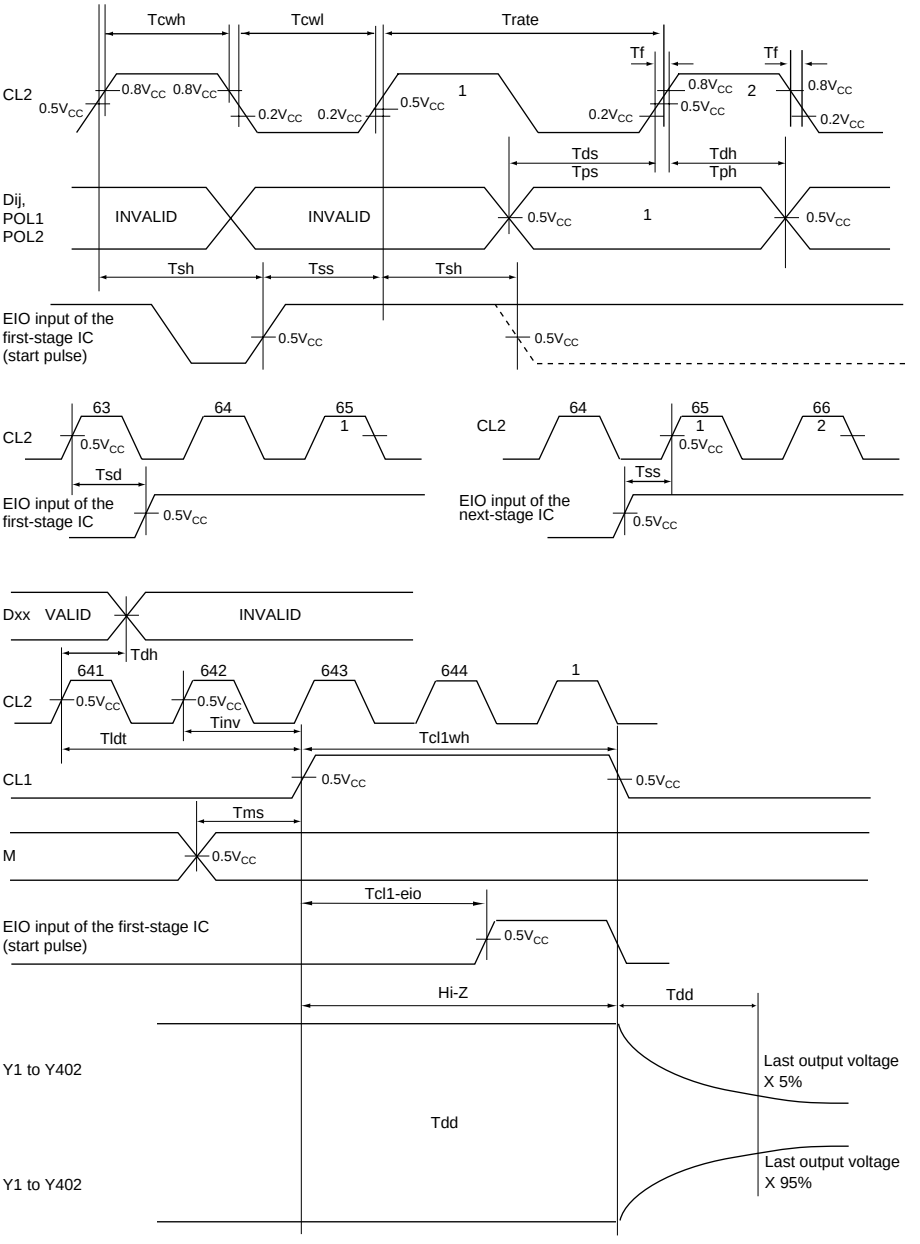


Figure 15 Switching Characteristic Waveforms

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