A DIVISION OF CIRRUS LOGIC

CS7665

Digital Color-Space Processor for CCD Cameras

Features

- ITU-601 Compliant Image Formatting
- ITU-656 and SMPTE-125/M Transport
- Provides Separate HREF and VREF (or alternately VSYNC) Signals
- I^2C Control Interface
- Limited Secondary I^2C Bus Master
- Automatic White Balance
- Programmable Gamma Correction
- 4:5 Square-Pixel Interpolation
- Advanced Color Anti-Aliasing Filter
- Programmable Luma Gain and Saturation Control
- Fully Programmable Color Separation Matrix Coefficients
- Supports Images up to 1024 pixels wide, with no limitation on Vertical Size

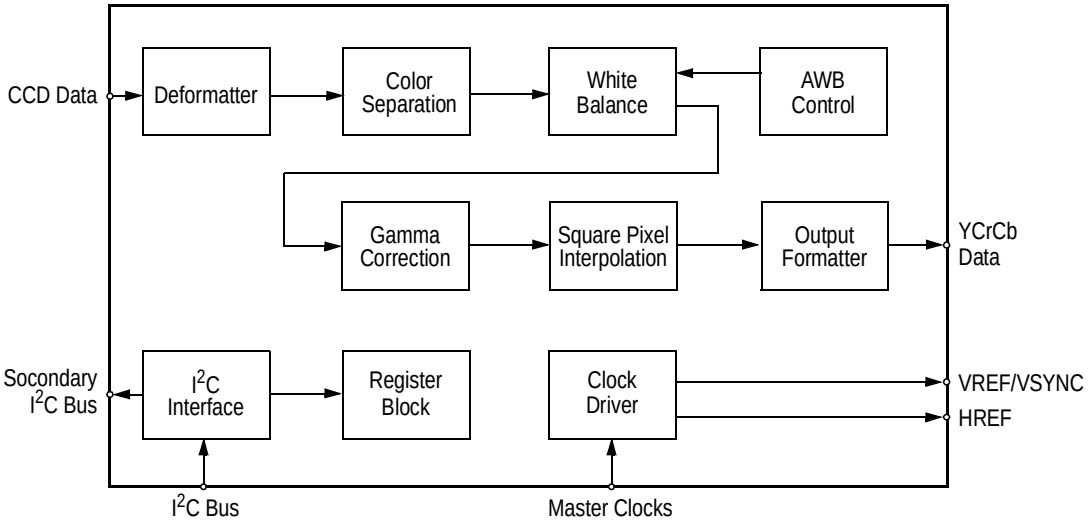
Description

The CS7665 is a low-power Digital Color-Space Processor for CCD cameras. It provides all necessary digital image processing for standard four-color interline transfer CCD imagers. The CS7665 processes the MYCG CCD imager data into YCrCb formatted component digital video. Internal processing includes color separation, automatic white balance, user programmable gamma correction curves, square pixel interpolation, and output formatting. The CS7665 employes an advanced color anti-aliasing filter which prevents both incorrect color and "color noise" that can undermine compression based systems. The CS7665 digital output is ITU-601 compliant and supports both ITU-656 and SMPTE-125/M transport. Additionally, HREF and VREF (or VSYNC) output pins are provided to support older analog video encoders and the current ZV-Port definition. The CS7665 can support horizontal line widths of up to 1024 pixels. It has no limitations on the number of lines it can support in the vertical direction.

The CS7665 is designed to work directly with the CS7615 CCD Imager Analog Processor.

ORDERING INFORMATION

CS7665-KQ	0° to +70° C	64-pin TQFP (10 mm x 10 mm x 1.4 mm)



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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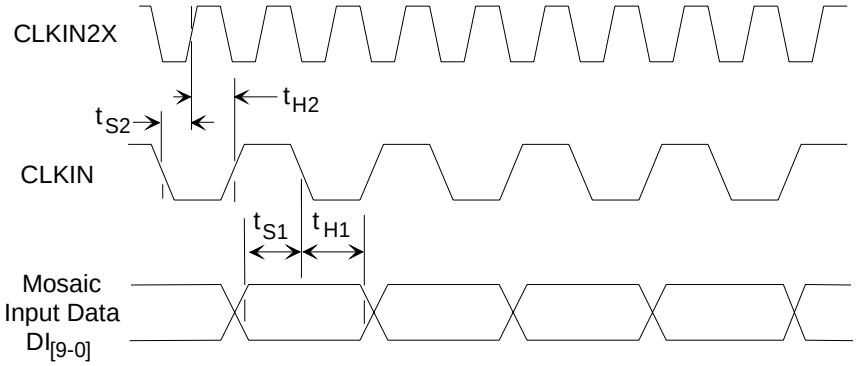
DIGITAL CHARACTERISTICS: (Test conditions: T_A=25°C ; V_{DD}=5V; Output load=30pf; Input Levels: logic 0=0V, logic 1=V_{DD}.)

Parameter	Symbol	Min	Typ	Max	Units
ILogic Inputs					
High-Level Input Voltage	V_{IH}	V_{DD}-0.8			V
Low-Level Input Voltage	V_{IL}			0.8	V
Input Leakage Current	I_{IN}			10.0	µA
Input Pin Capacitance	C_{DI}		10		pF
Input Clamp Voltage			-0.7		V
Logic Outputs					
High-Level Output Source Current @ V_{OH} = V_{DD}-0.4V	I_{OH}	2			mA
Low-Level Output Sink Current @ V_{OL} = 0.4V	I_{OL}	2			mA
High-Z Leakage Current	I_Z			10.0	µA

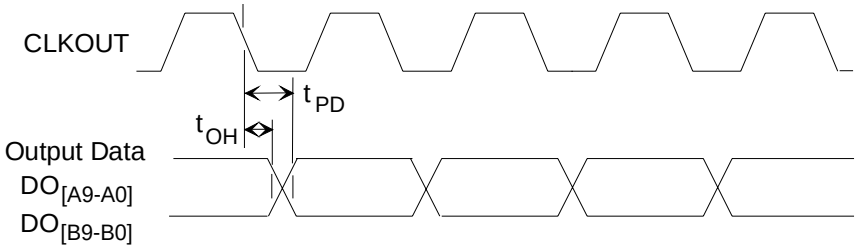
SWITCHING CHARACTERISTICS: (Test conditions: T_A=25°C ; V_{DD}=5V; Output load=30pf; Input Levels: logic 0=0V, logic 1=V_{DD}.)

Parameter	Symbol	Min	Typ	Max	Units
Digital Input					
CLKIN2X Frequency Range (Note 1)	f_{CLK2X}			30	MHz
Input Data setup time, $DI_{[9-0]}$	t_{S1}	5			ns
Input Data hold time, $DI_{[9-0]}$	t_{H1}	5			ns
Digital Output					
Channel A/B Digital Data Output Clock: Interleaved Data Parallel Data	f_{CLKOUT}			30 15	MHz MHz
Channel A/B Output Hold Time	t_{OH}		0		ns
Channel A/B Output Propagation Delay	t_{PD}		1.9	5	ns
Digital Output Rise Time with 30 pF load	t_R		15		ns
Digital Output Fall Time with 30 pF load	t_F		15		ns

Notes: 1. CLKIN, f_{CLK}, is f_{CLK2X}/2 in non-interpolated mode and f_{CLK2X}*2/5 in interpolated mode.



Input Timing Diagram



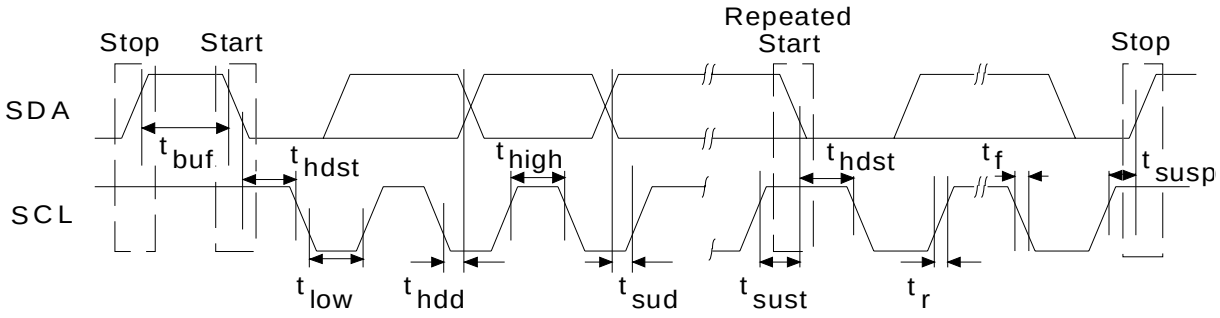
Output Timing Diagram

POWER CONSUMPTION: (Test conditions: T_A=25ºC ; V_{DD}=5V; Output load=no load; Input Levels: logic 0=0V, logic 1=V_{DD}.)

Parameter	Symbol	Min	Typ	Max	Units
Normal Mode	I_{DD}			80	mA
Low Power Mode	I_{DD}			7	mA

CONTROL PORT CHARACTERISTICS: (Test conditions: T_A=25ºC ; V_{DD}=5V; Input Levels: logic 0=0V, logic 1=V_{DD}.)

Parameter	Symbol	Min	Typ	Max	Units
SCL Clock Frequency	f_{SCL}			100	kHz
Bus Free Time Between Transmissions	t_{buf}	4.7			µs
Start Condition Hold Time	t_{hdst}	4.0			µs
Clock Pulse Width: High Low	t_{high} t_{low}	4.0 4.7			µs µs
Setup Time for Repeat Start Condition	t_{sust}	4.7			µs
SDAIN Hold TIme from SCL Falling	t_{hdd}	0			µs
SDAIN Setup TIme from SCL Rising	t_{sud}	0.25			µs
SDAOUT and SCL Rise Time	t_r	TBD			µs
SDAOUT and SCL Fall Time	t_f	TBD			µs
Setup Time for Stop Condition	t_{susp}	4.0			µs



I^2C Timing Diagram

RECOMMENDED OPERATING CHARACTERISTICS:

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Ground to Ground Voltage Differential				10	mV
Digital Input Rise/Fall Time				10	ns
CLKIN Level Setup to CLKIN2X Rising (non-interpolated) CLKIN Level Hold after CLKIN2X Rising (non-interpolated)	t_{S2} t_{H2}	8 8			ns ns
Digital Input Voltage Range		0		V_{DD}	V
Operating Temperature Range	T_A	0		70	°C

ABSOLUTE MAXIMUM RATINGS:

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	V_{DD}	-0.3	7.0	V
Digital Input Voltage Range		GND-0.3	V_{DD}+0.3	V
Sustained Digital Output Current			50	mA
Forced Digital Output Voltage		GND-0.3	V_{DD}+0.3	V
Output Short Circuit Current				mA
Operating Temperature Range	T_A	0	70	°C
Lead Solder Temperature (10sec duration)			+260	°C
Storage Temperature Range		-65	+160	°C

Note: Specifications are subject to change without notice.

GENERAL DESCRIPTION

Overview

The CS7665 forms the heart of a four chip digital CCD Camera. The four chips include the CCD imager, the CS7615 CCD digitizer, the CS7665 color space processor, and a vertical drive interface-chip for the CCD imager. Most four-phase CCD imagers (and their associated vertical drives) can be used with the CS7615 digitizer and the CS7665 processor to form a simple and cost-effective YCrCb output format digital camera. The CS7615 and CS7665 together support imager formats ranging from 175x175 pixels up to 1000x1000 pixels. Timing control is located in the CS7615 analog processor, while the CS7665 synchronizes itself to the CS7615 data stream by decoding the timing queues embedded in the CS7615 data stream. Alternately, the CS7665 accepts horizontal and vertical timing signals on pin inputs. The block diagram in figure 1 illustrates a typical system interconnect.

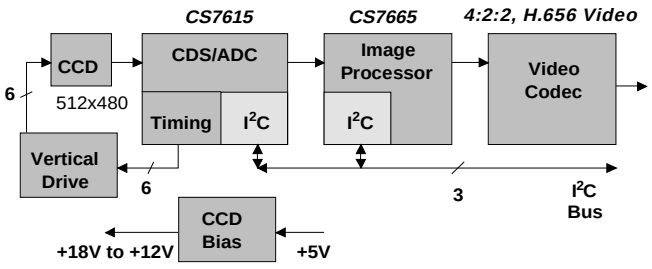


Figure 1. Typical 4-Chip Digital CCD Camera

The CS7665 is a CCD camera color separation and color-space processor designed to process the four-color mosaic CCD imager data into ITU-601 compliant full-motion 4:2:2 YCrCb digital component video. The CS7665 timing control is based on the main pixel clock (from the CS7615), and provides formatted component digital video compliant with SMPTE-125 and ITU-656 transport protocols.

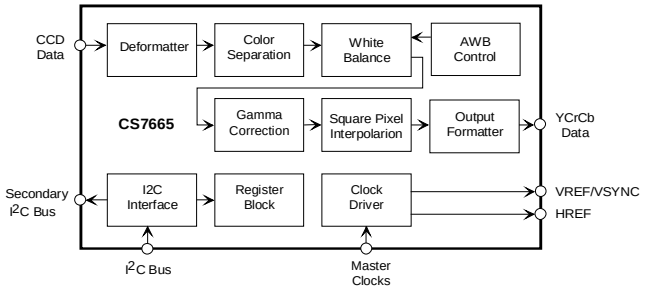


Figure 2. CS7665 Block Diagram

The CS7665 provides the color separation matrixing of standard MYCG chroma block data from industry standard four-color CCD imagers, via the CS7615 quantizer. Gamma correction and white balance adjustments functions are also included in the CS7665. The YCrCb (luminance and chrominance) data is output at the CCD pixel rate in 20-bit format, or at twice the pixel rate in 10-bit format (see discussion on Digital Output Formats). The YCrCb output data from the CS7665 conforms to the ITU-601/656 component digital video recommendation with embedded synchronization (see Embedded EAV and SAV discussion). External horizontal and vertical synchronization signals are also provided to support the older transport protocols made popular by Philips, as well as the PC-Card Zoom-Video standard being used in notebook computers.

The CS7665 incorporates an internal horizontal 4:5 scaler which may be turned on to increase the horizontal pixel count of the popular 512 horizontal pixel class of imagers to deliver digital video signal with 640 horizontal pixels, supporting the ubiquitous 640x480 image format.

The CS7615 and CS7665 chip set support a wide range of imager formats up to 1000x1000 pixels, while incorporating an output format that follows

the ITU-601 Component Digital Video recommendation. The ITU-601 document primarily specifies horizontal resolutions of 720 active horizontal pixels (which is required for broadcast television compatibility). Many of today's digital video receivers are capable of operating with a wide range of video image formats. Even though these digital video receivers allow image formats not specified in the ITU-601/656 recommendation, all of these receivers expect the basic ITU-601/656 protocol to be followed in terms of data sequence and timing queues. This is the case with the CS7665, where all output formats follow the ITU-601/656 recommendation even if the image formats differ in horizontal and vertical pixel dimensions.

The 640 Pixel Horizontal Line

The following discussion assumes that a 512 horizontal pixel class imager has been selected for the camera, and that the internal 4:5 horizontal scaler has been enabled. Many other imager/scaler combinations are possible, but the digital video format would not be significantly different than the 640x480 case described here.

Transmitted during each active line are 1280 multiplexed luminance and chrominance values (640 luminance, 320 chrominance Cr, and 320 chrominance Cb values). Eight of the remaining 280 interface clock intervals are used to transmit synchronizing information. The first of these 1560 interface clock intervals is designated line 0 word 0 for the purpose of reference only. The 1560 sample words per total line are therefore numbered 0 through 1559. Intervals 0 through 1279, inclusive, contain video data.

The interface clock intervals occurring during digital blanking are designated 1280 through 1559. Intervals 1280 through 1283 are reserved for the end-active-video (EAV) timing reference. Intervals 1556 through 1559 are reserved for the start-of-active-video (SAV) timing reference. Figure 3 indicates the values of the timing reference signals (F, V, H) for an entire frame of interlaced video. Please note the scan lines are numbered 1 through 525 consecutively in the time domain (spatially they are interlaced). Table 2 defines the 1560 samples of a single scan line of video.

Embedded ITU-656 EAV and SAV Timing

The lines in figure 3 are numbered 1 through 525. Video data is not present on lines 1 to 19 or 264 to 282, which constitute the vertical blanking periods. The vertical blanking is in full line increments, where Y samples are set to 10h, while Cb and Cr samples are set to 80h. The interval starting with EAV and ending with SAV is the digital horizontal synchronization, which occurs on every line.

It is implicit that the timing reference signals are contiguous with the video data and continue through the vertical blanking interval. Each timing reference signal consists of the four-word sequence in table 1. The first three words are a preamble, followed by a fourth word indicating a) even field (field 2) identification, b) state of vertical blanking, and c) state of horizontal blanking. Table 2 details the timing reference format. The protected bit states are dependent on the F, V, and H bits according to table 3.

	Value	Description
First Byte	FFh	Fixed
Second Byte	00h	Fixed
Third Byte	00h	Fixed
Fourth Byte	xyh	See Table 3

Table 1. Timing Reference Signal

Word	Data Content		Pixel	Notes
1280	1111	1111	640	EAV
1281	0000	0000		EAV
1282	0000	0000		EAV
1283	1FV1	P3P2P1P0	641	EAV
1284	1000	0000	642	Fro pixels 642 to 777 Cr = Cb = 80h Y = 10h
1285	0001	0000		
1286	1000	0000		
1287	0001	0000	643	
1552	1000	0000	776	
1553	0001	0000		
1554	1000	0000		
1555	0001	0000	777	
1556	1111	1111	778	SAV
1557	0000	0000		SAV
1558	0000	0000		SAV
1559	1FV0	P3P2P1P0	779	SAV
0	Cb0		0	Start of Digital Video
1	Y0			For VBLANK line 1 to 19 and 264 to 283 Cr = Cb = 80h Y = 10h
2	Cr0			
3	Y1		1	
4	Cb2		2	
5	Y2			
6	Cr2			
7	Y3		3	
2n	Cbn		n	For active pixels 20 through 263 and 283 to 525 for n=even from pixels 0 to 638
2n + 1	Yn			
2n + 3	Crn			
	Yn+1		N+1	
1272	Cb636		636	
1273	Y636			
1274	Cr636			
1275	Y637		637	
1276	Cb638		638	
1277	Y638			
1278	Cr638			
1279	Y639			End of Digital VIdeo

Table 2. Detail of Scan Line for 640x480 Image

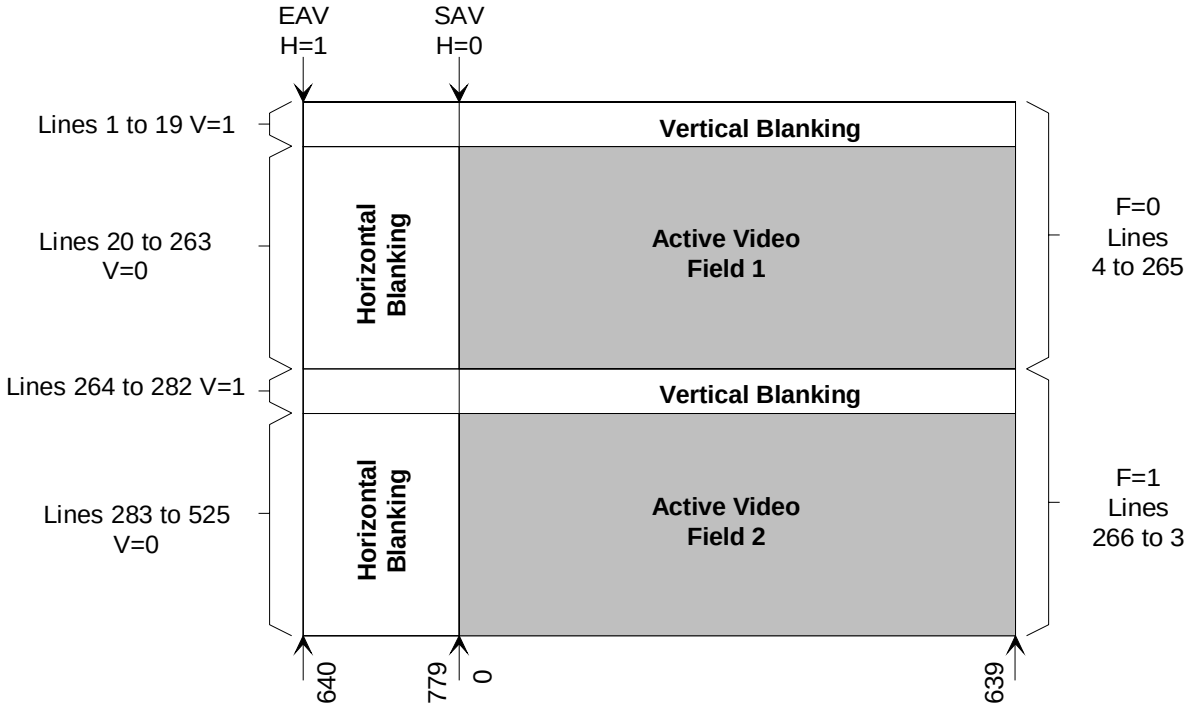


Figure 3. Horizontal and Vertical Timing States

Protected State Bits - In table 3 and 4, H, V, and F bits provide all the necessary timing and state information. Bits 0 to 3 provide error detection and correction information. The protection bits allow for correction of single-bit errors and detection of two-bit errors. The F or field bit indicates which of the interlaced fields is active, the first/odd field which contains 262 lines, or the second/even field which contains 263 lines.

Bit Position	Word 1281 and 1556	Word 1281 and 1557	Word 1282 and 1558	Word 1283 and 1589	Description
7	1	0	0	1	Fixed
6	1	0	0	F	F = 0 during Field 1/ODD F = 1 during Field 2/EVEN
5	1	0	0	V	V = 0 during Active Video V = 1 during Vertical Blanking
4	1	0	0	H	H = 1 at end of Active Video H = 0 at start of Active Video
3	1	0	0	P3	see Protected Bits State Table 4
2	1	0	0	P2	see Protected Bits State Table 4
1	1	0	0	P1	see Protected Bits State Table 4
0	1	0	0	P0	see Protected Bits State Table 4

Table 3. EAV and SAV Timing Reference Signal Detail.

Bit 7	Bit 6 (F)	Bit 5 (V)	Bit 4 (H)	Bit 3 (P3)	Bit 2 (P2)	Bit 1 (P1)	Bit 0 (P0)
1	0	0	0	0	0	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	0	1	1
1	0	1	1	0	1	1	0
1	1	0	0	0	1	1	1
1	1	0	1	1	0	1	0
1	1	1	0	1	1	0	0
1	1	1	1	0	0	0	1

Table 4. EAV and SAV Protected Bit States Detail.

Individual Timing and Synchronization Signals

In addition to the embedded EAV and SAV timing signals, the CS7665 provides individual synchronization output signals which are employed by many video encoder circuits. These synchronization signals are typically used to interface the H.656 digital video stream to other components and subsystems. The individual synchronization signals include HREFOUT and VREFOUT.

HREFOUT

HREFOUT is an active-high signal indicating when active pixel data is being transmitted on $DO_{A[0-9]}$ or $DO_{B[0-9]}$. HREFOUT is low when non-active picture data is being transmitted during horizontal blanking. Depending on the mode of operation, the HREFOUT signal follows either the HREFIN signal or the HREF defined by the EAV and SAV code.

VREFOUT/VSYNC

VREFOUT is an output signal that is active high when the CS7665 is putting out active video lines. The active-low portion of this signal defines the vertical blanking period. Alternately, when the ZV mode bit in register 06h is set, this output behaves as a VSYNC signal appropriate for ZV ports. The VSYNC signal is active-high during the first six horizontal line period of every field. The transition in VSYNC signal lags the HREF signal's rising edge during odd field and leads the rising edge of HREF during even field.

Digital Output Formats

The CS7665 outputs data in a 20-Bit wide format at the output pixel clock rate. Alternately, the data can be multiplexed in a 10-bit format at a 2x output pixel clock rate. Figures 4 and 5 detail the clock and data relationships. The output data transitions on the falling edge of the clock, such that the rising edge of the clock can be used to latch the data into subsequent circuitry.

The CS7665 delivers 4:2:2 component digital video output data in YCrCb format. The digital outputs can be configured for 10-bit interleaved Y and CrCb data, or for 20-bit parallel operation. The INTERL bit of the *Operational Control Register 06h* determines which output format is active. Logic 0 places the CS7665 in interleave mode with output data on channel "A." Logic 1 places the CS7665 in non-interleaved mode where luminance data is output on channel "A" and chrominance data is output on channel "B."

In 20-bit wide mode, the luminance information is output on $DO_{A[0-9]}$ and the chrominance information is output on $DO_{B[0-9]}$.

	Parallel INTERL = 1	Interleaved INTERL = 0
DOA[0-9]	10-Bit Luminance Data	Interleaved 10-Bit Luminance Data and 10-Bit Chrominance Data
DOB[0-9]	10-Bit Chominance Data	High-Z
CLKOUT	Pixel Rate	2x Pixel Rate

Table 5. INTERL Controlled Output Formats

The CS7665 supports both 8-bit and 10-bit operation as per the ITU H.656 recommendation. The H.656 recommendation defines the primary data path as 8-bits wide with two additional fractional bits that can be used to form a 10-bit data path. If only 8-bits of output data are used, it is very important to MSB align the CS7665 and the data path. This is essential to properly pass the image data and synchronization signals to the next component.

Internal Horizontal 4:5 Scaler

The internal horizontal 4:5 scaler is used to bridge between "broadcast based" image formats (like the common 512 horizontal pixel imagers) and "computer based" image formats (as with the 640x480 VGA standard). The 4:5 data rate scaler will convert the standard 512 horizontal pixel width CCD imager used for cam-corders into the VGA 640x480 format. The scaler is enabled/disabled via the INTERP pin on both the CS7665 and the CS7615 (if that device is used in the system.) The filtering done in the scaler should not generate any noticeable image artifacts.

CLKIN and CLKIN2X Input Timing

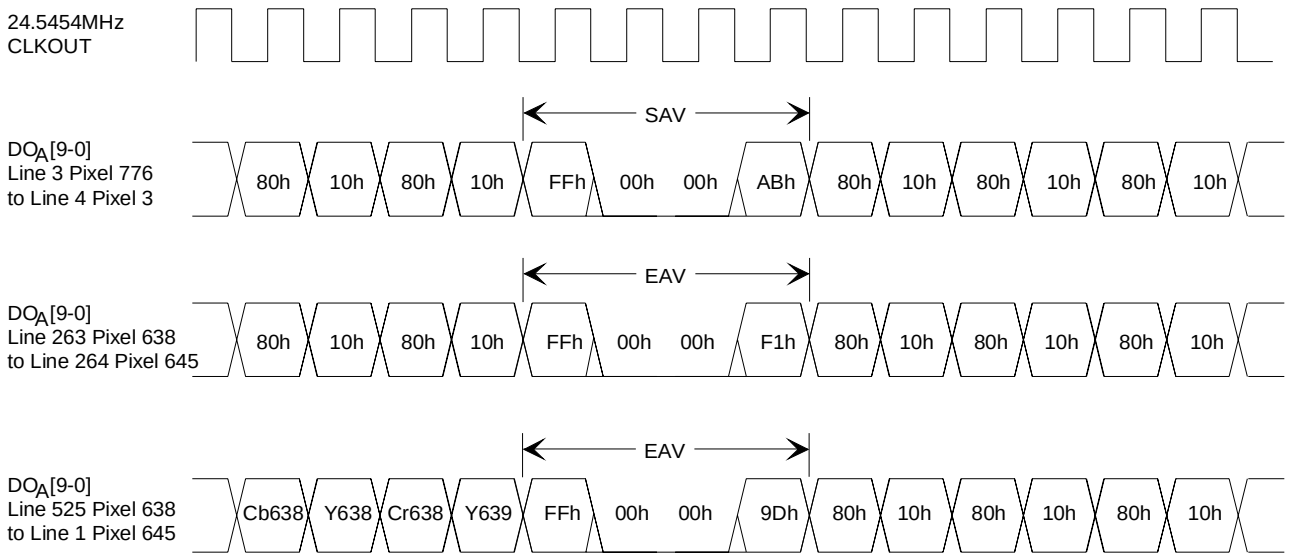
The CLKIN, pin 55, will always require a primary pixel rate clock source. CCD manufacturers generally specify a pixel clock frequency that is compatible with one of the analog encoders that can be used with a given imager. If an analog encoder is used in the camera to generate an analog output, the pixel clock frequency expected by the encoder must be matched precisely. Digital display systems, such as those based on VGA graphics adaptor cards and Zoom Video systems, are generally not sensitive to pixel clock frequency, and will tolerate a wide range of pixel and frame rates.

Specific pixel-rate clock frequencies for analog encoders include 14.31818 MHz for 768H imagers, the primary ITU-601 13.5 MHz for 720H imagers, and down to 12.272727MHz clock rates for 640H VGA format imagers.

The CLKIN2X, pin 56, will either require a 5/2x CCD pixel rate clock when the internal 4:5 scaler is enabled or a 2x times the 1x CCD pixel rate clock in non-interpolation mode.

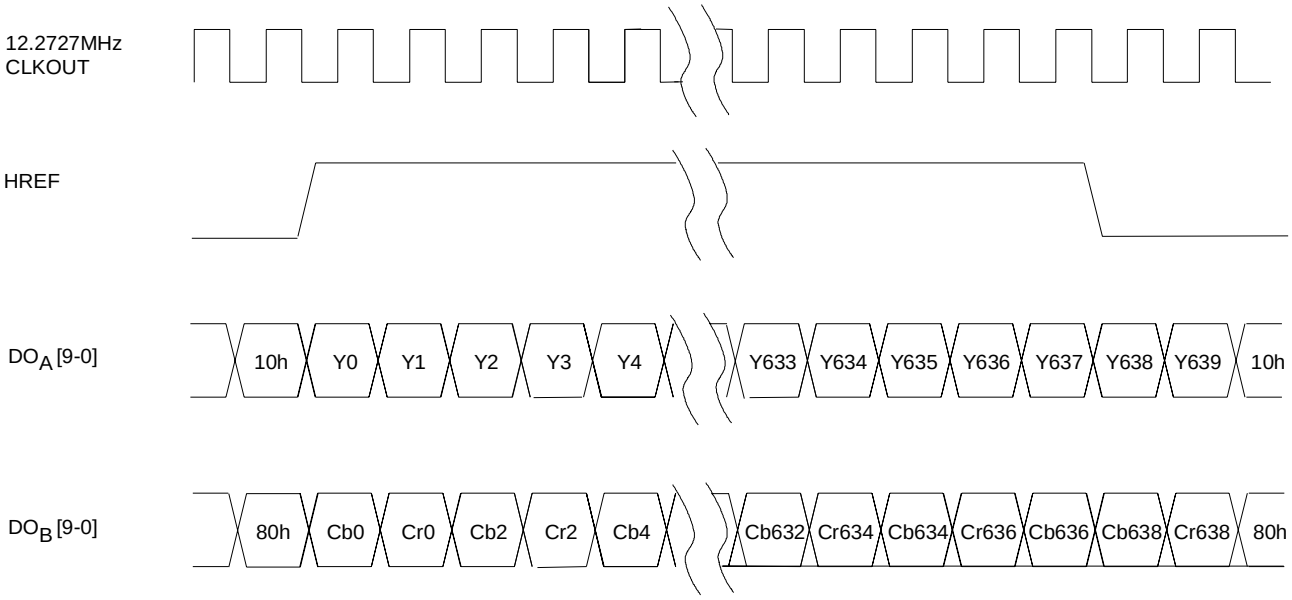
CLKOUT

CLKOUT follows the output data rate. In the non-interleaved mode the clock output is at the output luma sample rate whereas in the interleaved mode the clock output is at 2x the output luma sample rate.



NOTE: EAV, SAV, and Blanking data values are based on the 8 MSB's of the output data, the two LSBs are considered fractional.

Figure 4. 2x Pixel Clock, 10-Bit interleaved Output Format for 640x480 Image Format.



NOTE: EAV, SAV, and Blanking data values are based on the 8 MSB's of the output data, the two LSBs are considered fractional.

Figure 5. 1x Pixel Clock, 20-Bit Parallel Output for a 640x480 Image.

INTERNAL PROCESSING

The internal operation of the CS7665 can be separated into several distinct blocks. The following section provides an overview of how these blocks operate and interact.

Input Data Format and Chroma Separator

The CS7665 accepts up to 10-bit MYCG image data from the CCD digitizer, CS7615, or other suitable CCD analog processing unit. The CS7665 internally converts the four-color CCD MYCG interlaced image data into the various color space formats. These include RGB and YUV, as well as YCrCb. The individual image adjustments are performed in the most appropriate color space representation. Ultimately the image is converted to YCrCb format for outputting data.

Luminance Edge Enhancement and Color Saturation Control

Edge enhancement is performed in YCrCb color space and is a complement to the spatial anti-aliasing filtering performed in the chroma separator.

Color Saturation Control

Color saturation control is via the Red Saturation and the Blue Saturation control register addresses 0Ah and 0Bh.

White Balance and Gamma Correction

The red and blue color balances can be adjusted through the I^2C control port. During the AWB (automatic white balance) sequence the red level is adjusted to minimize the (Y-R) difference component; similarly the blue level is adjusted to minimize the (Y-B) color difference component. The red balance is accessed through register 08h, and the blue balance is accessed through register 09h.

INTERNAL REGISTER STRUCTURE AND USER INTERFACE

The user interface describes the user's external view of the CS7665 and the basic control operations. These areas include digital data output modes and organization, timing and synchronization signals, I^2C interface, and miscellaneous controls.

The CS7665 has two I^2C ports: (i) a slave I^2C port called the primary I^2C port, and (ii) a secondary I^2C port with limited I^2C master capabilities. The primary I^2C port allows an external controller to control the CS7665. It is assumed the external controller will also directly control any other I^2C slave devices on the camera board. This is the normal I^2C operation mode of CS7665. The secondary I^2C port, on the other hand, may be used to control all the other slave devices on a camera board through CS7665 only. This feature is useful when the external I^2C controller is used to control multiple cameras. When used in this configuration the 4BYTEMODE pin of CS7665 must be tied high and the device is operated in four-byte mode.

Operating CS7665 in Normal I^2C Configuration

In normal mode the CS7665 is connected as a slave device to an external I^2C controller through the primary I^2C port. The connection is done via a two-wire serial bus. Other I^2C devices on the camera may also share the same serial bus. The external controller communicates with the I^2C devices by sending and receiving short packets of 8-bit words in accordance with the I^2C protocol. Each device on the I^2C bus has unique 8-bit write and 8-bit read station addresses. The two addresses of the device differ only in the LSB. The packets contain the station address of the target device, the desired register address, and data.

There are three packet formats: WRITE format, ADDRESS SET format, and READ format. Each packet is addressed to a device by the station address. The LSB of the station address is the data direction bit. This bit is set LOW in the WRITE and ADDRESS SET packets, and it is set HIGH for READ packets. The receiver can read and write to non-existent registers within the selected device.

WRITE operations will have no effect; READ operations will return a value of 00h.

Station Address

The CS7665 default station address is 34h for writes and 35h for reads. The station address can be changed by writing a new base station address to internal I^2C register FFh.

Write Operations

The WRITE format consists of a three-byte packet. The first byte is the station address with the data direction bit set LOW to indicate a write. The second byte is the device register address (0..255). The third byte is the register data (0..255). No extra bytes should be sent.

Byte Sequence	WRITE Format Packet Detail
First Byte	Station Address with LSB Set LOW
Second Byte	Device Register Address (0..255)
Third Byte	Register Data (0..255)

Table 6. WRITE Format Packet

Address Set Operation

The ADDRESS SET format consists of a two-byte packet which sets the address of a subsequent READ operation. The first byte of the Station Address with the LSB (data direction bit) set LOW to indicate a write operation. The second byte is the register address (0..255). The ADDRESS SET format is the same as the WRITE format, without the register data.

Byte Sequence	ADDRESS SET format Packet Details
First Byte	Station Address with LSB Set LOW
Second Byte	Device Register Address (0..255)

Table 7. ADDRESS SET Format Packet Operation

Read Operations

The READ operation consist of two or more bytes of packet. The first byte is the station address with the LSB (data direction bit) set HIGH indicating a read operation. The addressed device then sends one or more bytes back from the register last addressed by the previous WRITE operation, or ADDRESS SET operation.

Byte Sequence	READ Format Packet Details
First Byte	Station Address with LSB set HIGH; Source Device then Returns One Byte of Register Data (0..255)
Second Byte	Returned data from CS7665

Table 8. READ Format Packet.

Operating CS7665 in Four-Byte I^2C Configuration

In this configuration the external controller talks only to CS7665 through the primary I^2C interface. All the other slave devices on the camera board are tied to the secondary I^2C port of CS7665. WRITE and READ packets only are defined in four-byte mode. Independent address set operation to slave devices on secondary I^2C bus is not allowed in four-byte mode. Four-Byte-Mode is active when the 4BYTEMODE pin is logic high.

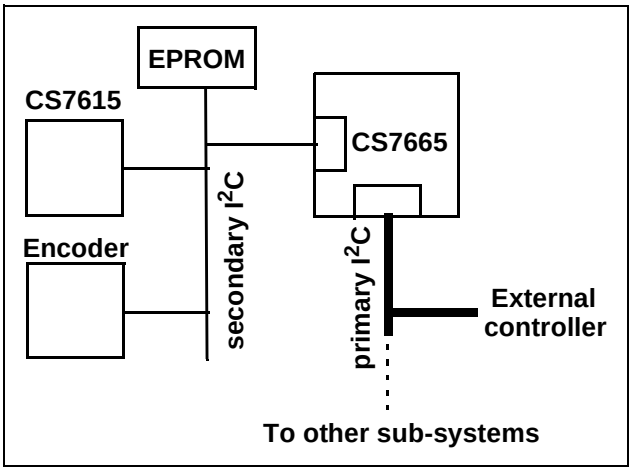


Figure 6. I^2C configuration showing primary and secondary I^2C busses.

Write Operations in Four-byte mode:

All WRITE operations from external controller, through the CS7665, to any slave device must use the four-byte mode; his includes writing to CS7665 itself. The external controller sends a four-byte WRITE command to CS7665 which initiates a WRITE operation to the destination slave device and sets the I2CBUSY bit in status register. External controller can poll the status register to check if CS7665 has completed the command.

CS7665 has a one command buffer which allows the external controller to queue one additional command while the current command is still being executed. If more than one command is sent before the I2CBUSY bit is cleared CS7665 saves only the last command and executes it after the current one is completed. Commands that involve writing or reading only to CS7665 registers are not put in the queue and are executed immediately without affecting any transactions going on in the master I^2C interface.

Any attempt by the external I^2C controller to write to CS7665 registers while CS7665 is busy initializing from EPROM will be ignored. However, reads from CS7665 are allowed.

If during a READ or WRITE operation to a slave device CS7665 fails to receive an acknowledge bit the execution of the command is aborted and the NODEV bit in the status register is set high. This bit remains set unless it is explicitly cleared by writing to it or a new command is written to CS7665.

Byte Sequence	WRITE Format Packet Detail
First Byte	Station Address of CS7665 with LSB Set LOW
Second Byte	Station Address of target slave device with LSB Set LOW
Third Byte	Device Register Address (0..255)
Fourth Byte	Register Data (0..255)

Table 9. Four-byte WRITE Format Packet

Read Operation

The READ operation in four-byte mode first requires a three-byte READ-TRIGGER packet to CS7665. The first byte is the station address of CS7665 with LSB set. The second byte is the target slave device's station address with the LSB (data direction bit) set HIGH. The third byte is the register address (0..255).

Byte Sequence	READ-TRIGGER format Packet Details
First Byte	CS7665 Station Address with LSB Set LOW
Second Byte	Target device Station Address with LSB Set HIGH
Third Byte	Device Register Address (0..255)

Table 10. READ-TRIGGER packet in four-byte mode

The READ-TRIGGER packet initiates a READ operation by CS7665 from the target slave device on the secondary I^2C bus. The status register on CS7665 may be checked to see if the read operation has been completed. I2CBUSY bit in status register 01h is set to zero when the operation is completed.

On completion of read from the target device, CS7665 places the read data in a Slave Data Hold register at address 19h. The external controller can read this data through the primary I^2C port. This requires first performing an ADDRESS SET operation to set the address to 19h and then sending a one-byte station address indicating read to CS7665. The data from register 19h is then returned by CS7665.

Byte Sequence	WRITE Format Packet Detail
First Byte	Station Address of CS7665 with LSB Set LOW
Second Byte	Station Address of CS7665 with LSB Set LOW
Third Byte	Slave Data Hold reg. address 19h

Table 11. Address Set for Slave Data Hold register in Four-byte mode

Byte Sequence	READ Format Packet Details
First Byte	CS7665 Station Address with LSB set HIGH.
Second Byte	Returned data from register 19h of CS7665

Table 12. READ Format Packet.

Initializing Slave Devices on Secondary I^2C bus from an EPROM.

An EPROM may be attached to the secondary I^2C bus for initialization purposes. A reset to CS7665 initiates a download of register values from the EPROM into any of the slave devices on the secondary I^2C bus. The EPROM is assumed to be at station address A0h. If during initialization, CS7665 does not receive an acknowledge bit from the EPROM, all transactions with the EPROM are aborted and NODEV status bit is set in status register at address 01h.

At the end of reset period, the CS7665 fetches three bytes from the EPROM. These three bytes represent destination station address, register address, and data. CS7665 then writes the data into the specified register of the destination station. After completing this process CS7665 reads the next three bytes from the EPROM. The number of registers to be read and initialized from the EPROM is loaded into a two-byte COUNT register in CS7665. The top six bytes in the EPROM must specify the number of triple-bytes to be read from the EPROM. The maximum number of triple-bytes allowed in the EPROM space is 2 kbytes/3.

While the CS7665 is downloading from the EPROM, the INITACT bit is set in the status register of CS7665. All attempts to write to CS7665 registers by the external controller will be ignored during this time.

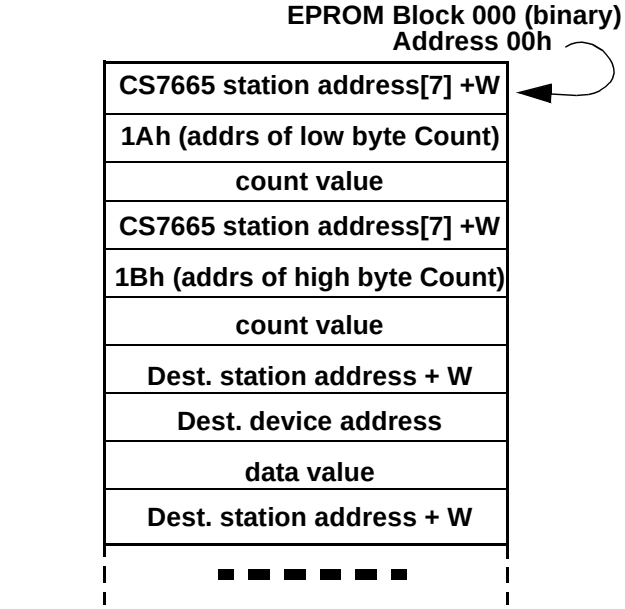


Figure 7. Map of EPROM table for initialization of registers

A typical map of the EPROM table is shown in Figure 7. The only exception to this organization is data for the CS7665 gamma table. The data for the gamma table is organized as shown in figure 8.

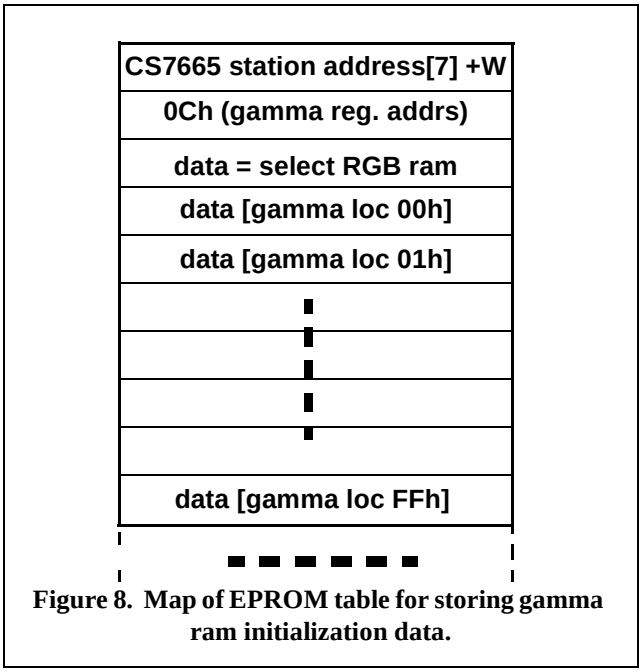


Figure 8. Map of EPROM table for storing gamma ram initialization data.

Master Reset Register (00h)

7	6	5	4	3	2	1	0
MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
-	-	-	-	-	-	-	W

MR0 Setting bit MR0 to logic high will initiate a CS7665 master reset equivalent to executing an external reset using the Reset pin. All registers will be placed in their default state, and the download of any external EPROM present on the secondary I^2C bus will be initiated. The bit is self-cleared.

Status Register (01h)

7	6	5	4	3	2	1	0
res	res	res	res	INiTACT	I2CBUSY	NODEV	EVNFLD
-	-	-	-	R	R	R	R

EVNFLD Logic high indicates even field of interline-transfer CCD. Logic low indicates odd field of interline-transfer CCD. This bit provides a course means of synchronizing to the field rate.

NODEV Logic high indicates that the addressed slave device on the secondary I^2C bus did not respond.

I2CBUSY Logic high indicates that the CS7665 secondary I^2C master is busy accessing the addressed slave device.

INITACT Logic high indicates the CS7665 master is busy initializing registers from the external I^2C EPROM on the secondary I^2C bus (if present).

Digital Gain Register (03h)

7	6	5	4	3	2	1	0
res	res	res	DG4	DG3	DG2	DG1	DG0
-	-	-	R/W	R/W	R/W	R/W	R/W

DG0..DG4 Controls the digital gain applied to the Y (Luminance) signal after the RGB to YCrCb converter block. The range of gains are from 0 to 31/8 in increments of 1/8. A gain of 0, indicates no brightness.

Feature Control Register (05h)

7	6	5	4	3	2	1	0
res	res	res	CHROFF	LUMOFF	GAMON	AWB	res
-	-	-	R/W	R/W	R/W	R/W	-

AWB The Automatic White Balance procedure is initiated by pointing to a white scene and setting this bit high. The bit will return a logic high while the AWB procedure is in progress. Setting this bit low will have no effect. This bit will always be read as a “0” when the AWB is not in progress.

GAMON The gamma correction from the gamma ram look up table is applied to the video signal in R-G-B space when this bit is set high. The gamma ram is a fully user programmable, 256 entry look up table.

LUMOFF Setting LUMOFF bit high disables the luma peaking filter.

CHROFF Setting the CHROFF bit high disables the chroma low-pass filter for minimizing color aliasing.

Operational Control Register (06h)

7	6	5	4	3	2	1	0
res	ZV	INTERL	INREF	OE	POSPIX	EBLU	OBLU
-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

OBLU Logic high causes the first line after VREF of the odd field to be processed as a BLUE line. Logic low causes the first line of the odd field to be processed as a RED line.

EBLU Logic high causes the first line after VREF of the even field to be processed as a BLUE line. Logic low causes the first line of the even field to be processed as a RED line.

POSPIX Logic “1” causes the first pixel of the first line to be treated as a positive pixel in the color separation block. Logic “0” causes the first pixel to be treated as a negative pixel. Try toggling this bit if the colors appear “reversed”.

OE The Output Enable Bit operates in conjunction with the external Output Enable Pin, as illustrated in table 13.

OE Bit	OE Pin	Digital Outputs
0	0	Enabled
0	1	High-Z
1	0	High-Z
1	1	Enabled

Table 13. OE Pin and Bit Operation

INREF Logic “1” causes CS7665 to accept HREF input and VREF input pins as the reference inputs signals. EAV and SAV codes in the CCD data stream are ignored. Logic “0” causes the internal de-formatter to decode and follow the embedded EAV and SAV codes sent from the CCD digitizer (as with the CS7615).

INTERL Logic “0” places the digital outputs in interleaved mode with alternate Y and CrCb data on the $DO_{[A0..A9]}$ 10-Bit output. Logic “1” places the digital outputs in parallel mode with Y data on $DO_{[A0..A9]}$ and CrCb on the $DO_{[B0..B9]}$ outputs.

ZV A Logic “1” causes VREFOUT pin to output a VSYNC signal compatible with ZV port specifications as well as many composite video encoders.

Red Balance Register (08h)

7	6	5	4	3	2	1	0
RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0

RB0..RB7 The Red Balance register controls the red contribution to the R-Y chrominance signal. When the register value is 00h, the red contribution is minimized; when the register value is FFh, the red contribution is maximized. When the AWB correction is in progress, this register value is adjusted such that the absolute magnitude of the R-Y signal is minimized.

Blue Balance Register (09h)

7	6	5	4	3	2	1	0
BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0

BB0..BB7 The Blue Balance register controls the blue contribution to the B-Y chrominance signal. When the register value is 00h, the blue contribution is minimized; when the register value is FFh, the blue contribution is maximized. When the AWB correction is in progress, this register value is adjusted such that the absolute magnitude of the B-Y signal is minimized.

Red Saturation Register (0Ah)

7	6	5	4	3	2	1	0
RS7	RS6	RS5	RS4	RS3	RS2	RS1	RS0

RS0..RS7 The Red Saturation register value controls the amplitude of the R-Y chrominance signal. When the register value is 00h, the amplitude of the R-Y is minimized; when the register value is FFh, the amplitude of the R-Y is maximized.

Blue Saturation Register (0Bh)

7	6	5	4	3	2	1	0
BS7	BS6	BS5	BS4	BS3	BS2	BS1	BS0

BS0..BS7 The Blue Saturation register value controls the amplitude of the B-Y chrominance signal. When the register value is 00h, the amplitude of the B-Y is minimized; when the register value is FFh, the amplitude of the B-Y is maximized.

Gamma Correction Register (0Ch)

Writing to the gamma register (0Ch) selects the R, G, and/or B ram. Continuing data writes without sending a stop bit after the register write results in writes to the ram locations starting with 00h and continuing to FFh. Reads from register 0Ch function in a similar way. NOTE: All three gamma rams may be selected for simultaneous writes, but read should be done one ram table at a time.

7	6	5	4	3	2	1	0
GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0
-	-	-	-	-	-	-	-

GC0 Logic “1” selects BLUE gamma ram for subsequent access.

GC1 Logic “1” selects GREEN gamma ram for subsequent ram access.

GC2 Logic “1” selects RED gamma ram for subsequent ram access.

GC0..GC7 Provide R/W access to ram after gamma ram table has been selected.

Test Control A Register (0Eh)

7	6	5	4	3	2	1	0
TCA7	TCA6	TCA5	TCA4	TCA3	TCA2	TCA1	TCA0
Reserved							

Test Control B Register (0Fh)

7	6	5	4	3	2	1	0
TCB7	TCB6	TCB5	TCB4	TCB3	TCB2	TCB1	TCB0
Reserved							

YR Coefficient Register (10h)

7	6	5	4	3	2	1	0
YR7	YR6	YR5	YR4	YR3	YR2	YR1	YR0
-	-	-	-	-	-	-	-

Color separation and color space conversion coefficient.

CrR Coefficient Register (11h)

7	6	5	4	3	2	1	0
CrR7	CrR6	CrR5	CrR4	CrR3	CrR2	CrR1	CrR0
-	-	-	-	-	-	-	-

Color separation and color space conversion coefficient.

CbR Coefficient Register (12h)

7	6	5	4	3	2	1	0
CbR7	CbR6	CbR5	CbR4	CbR3	CbR2	CbR1	CbR0
-	-	-	-	-	-	-	-

Color separation and color space conversion coefficient.

YG Coefficient Register (13h)

7	6	5	4	3	2	1	0
YG7	YG6	YG5	YG4	YG3	YG2	YG1	YG0
-	-	-	-	-	-	-	-

Color separation and color space conversion coefficient.

CrG Coefficient Register (14h)

7	6	5	4	3	2	1	0
CrG7	CrG6	CrG5	CrG4	CrG3	CrG2	CrG1	CrG0
-	-	-	-	-	-	-	-

Color separation and color space conversion coefficient.

CbG Coefficient Register (15h)

7	6	5	4	3	2	1	0
CbG7	CbG6	CbG5	CbG4	CbG3	CbG2	CbG1	CbG0
-	-	-	-	-	-	-	-

Color separation and color space conversion coefficient.

YB Coefficient Register (16h)

7	6	5	4	3	2	1	0
YB7	YB6	YB5	YB4	YB3	YB2	YB1	YB0
-	-	-	-	-	-	-	-

Color separation and color space conversion coefficient.

CrB Coefficient Register (17h)

7	6	5	4	3	2	1	0
CrB7	CrB6	CrB5	CrB4	CrB3	CrB2	CrB1	CrB0
-	-	-	-	-	-	-	-

Color separation and color space conversion coefficient.

CbB Coefficient Register (18h)

7	6	5	4	3	2	1	0
CbB7	CbB6	CbB5	CbB4	CbB3	CbB2	CbB1	CbB0
-	-	-	-	-	-	-	-

Color separation and color space conversion coefficient.

Slave Data Hold Register (19h)

7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

When an external I^2C controller initiates a register read from a slave device on the secondary I^2C bus through CS7665, the returned data is placed in this register. The external controller may then read the data from the Slave Data Hold register.

EPROM Count Low Byte Register (1Ah)

7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

Lower byte of the number of triple-bytes to be read from EPROM upon reset of CS7665.

EPROM Count High Byte Register (1Bh)

7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

Upper byte of the number of triple-bytes to be read from EPROM upon reset of CS7665.

Version (Major) Register (1Ch)

7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

The major version register in CS7665 rev. A is assigned the value FFh. With each major revision the value is decreased by 1.

Version (Minor) Register (1Dh)

7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

The minor version register in CS7665 rev. A is assigned the value 00h. With each minor revision the value is increased by 1.

Low Power Register (20h)

7	6	5	4	3	2	1	0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
-	-	-	-	-	-	-	R/W

PD0 Setting bit PD0 to “1” will place the CS7665 in low power mode.

Test Enable Register (21h)

7	6	5	4	3	2	1	0
TE7	TE6	TE5	TE4	TE3	TE2	TE1	TE0
Reserved							

Station Address Register (FFh)

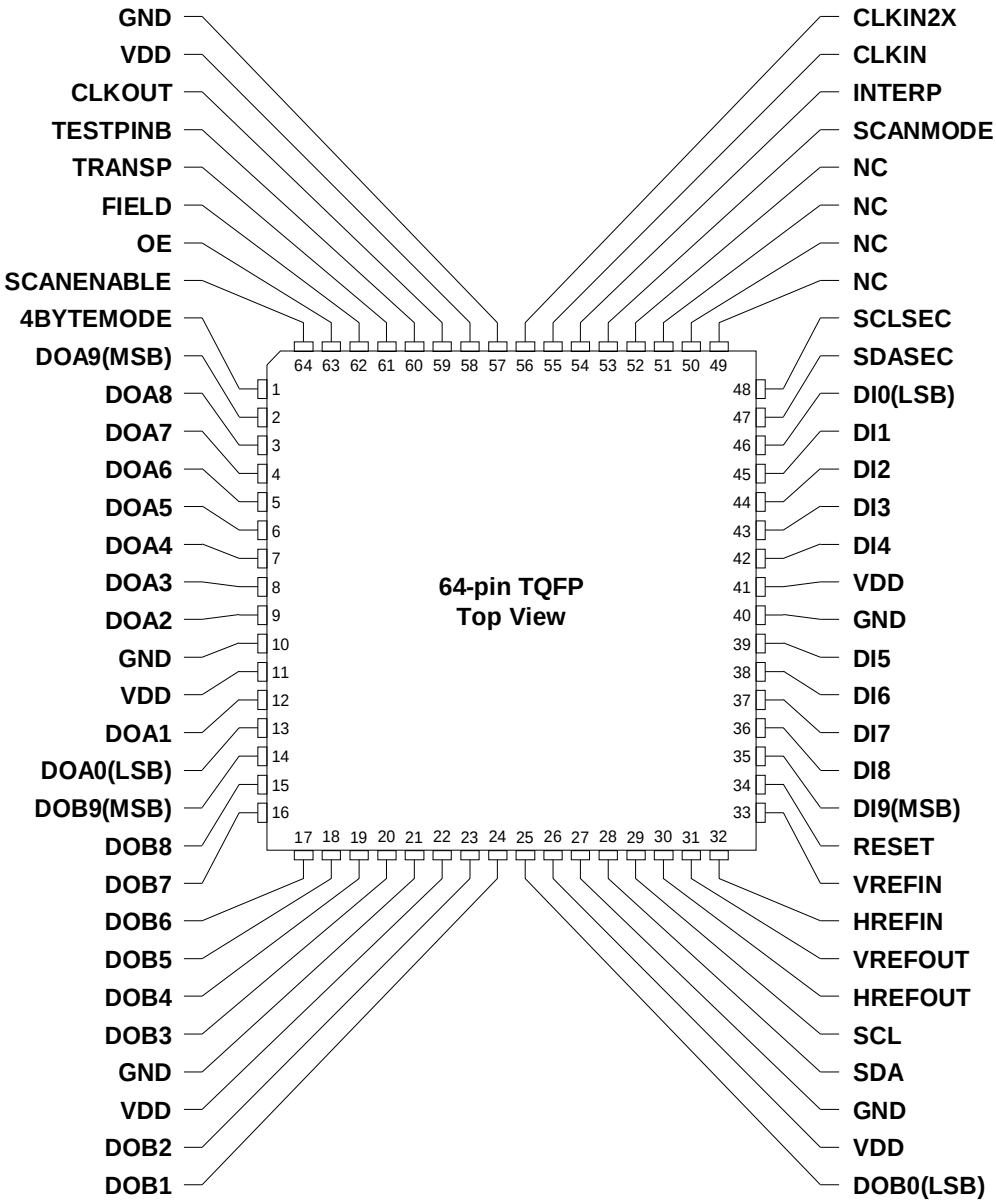
7	6	5	4	3	2	1	0
res	SA6	SA5	SA4	SA3	SA2	SA1	SA0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CS7615 station address, 7 MSBs (the LSB of the complete 8-bit station address is determined by the LSB which acts as a read/write direction bit).

Interpolation Test Register (24h)

7	6	5	4	3	2	1	0
Reserved							

PIN DESCRIPTIONS



Power Supply Connection

VDD - Power Supply, PINS 11, 22, 26, 41, 58.

Positive digital supplies. Nominally +5 volts.

GND - Digital Ground, PINS 10, 21, 27, 40, 57.

Digital ground supplies.

Input Data and Clocks

DI[0..9] - Digital Mosaic Inputs.

CMOS level mosaic coded CCD input data from CCD digitizer

Pin Name	Pin Function	Pin Number
DI0(LSB)	Digital Mosaic Input (LSB)	46
DI1	Digital Mosaic Input	45
DI2	Digital Mosaic Input	44
DI3	Digital Mosaic Input	43
DI4	Digital Mosaic Input	42
DI5	Digital Mosaic Input	39
DI6	Digital Mosaic Input	38
DI7	Digital Mosaic Input	37
DI8	Digital Mosaic Input	36
DI9(MSB)	Digital Mosaic Input (MSB)	35

Table 14. Digital Mosaic Inputs

CLKIN - Mosaic Input Data Clock, PIN 55.

Main system input clock, used to strobe incoming digital CCD mosaic data. The CLKIN frequency is the mosaic input data rate.

CLKIN2X - Mosaic Input Data Interpolation Clock, PIN 56.

Mosaic input data interpolation clock. Twice the CLKIN input in normal mode (non-interpolated output data ... see INTERP description). Twice the 5/4 output rate clock when internal 5 to 4 horizontal data rate scaler is in operation.

HREFIN - Horizontal Input Timing Reference, PIN 32.

Active low horizontal input timing reference. Used to synchronize the output timing signals with the incoming mosaic data and timing. When used with CCD digitizers like the CS7615 which imbed the necessary timing signals in the data stream, the HREFIN signal is not needed.

VREFIN - Vertical Input Timing Reference, PIN 33.

Active low vertical input timing reference. Used to synchronize the output timing signals with the incoming mosaic data and timing. When used with CCD digitizers like the CS7615 which embed the necessary timing signals in the data stream, the VREFIN signal is not needed.

I^2C Serial Control

SDA - Primary I^2C Data Bus, PIN 28.

Primary I^2C data bus. Used with SCL to read and write the internal register set.

SCL - Primary I^2C Clock, PIN 29.

Primary I^2C Clock. Used with SDA to read and write the internal register set.

SDASEC - Secondary I^2C Data Bus, PIN 47.

Secondary I^2C data bus with limited bus mastering capabilities. Used with SCLSEC to read and write I^2C devices located on the secondary bus. Various devices can be isolated by the CS7665 from the primary I^2C bus. The CS7665 will start reading I^2C EPROM devices at addresses A0h after RESET. It will download the EPROM contents into the specified registers inside the secondary bus devices as well as any CS7665 registers specified in the EPROM entries. Devices are typically connected to either the primary or the secondary I^2C bus. However, the two busses may be connected together when system design requires the use of EPROM initialization while at the same allowing direct access to all the camera devices from the external I^2C controller.

SCLSEC - Secondary I^2C Clock, PIN 48.

Secondary I^2C clock with limited bus mastering capabilities. Used with SDASEC to read and write I^2C devices located on the secondary bus. Various devices can be isolated by the CS7665 from the primary I^2C bus. The CS7665 will start reading I^2C EPROM devices at addresses A0h after RESET, and download the EPROM contents into the specified secondary bus registers, as well as any CS7665 registers specified in the EPROM entries. Devices are typically connected to either the primary or the secondary I^2C bus. However, the two busses may be connected together when system design requires the use of EPROM initialization while at the same allowing direct access to all the camera devices from the external I^2C controller.

4BYTEMODE - Four-byte Mode I^2C Operation Enable, PIN 1.

Places CS7665 in the Four-byte mode for I^2C transactions on the primary I^2C bus. Active high.

Digital Video Outputs and Clocking

$DO_{A[0..9]}$ - "A" Channel Digital Output Bits.

CMOS level 10-bit digital video output channel "A." Either YCrCb interleaved digital video output data, or Y component digital video data is available at this port according to the state of bit 5 in register 06h. $DO_{A0(LSB)}$ is the least significant bit of channel "A;" $DO_{A9(MSB)}$ is the most significant bit of channel "A."

$DO_{B[0..9]}$ "B" Channel Digital Output Bits.

CMOS level 10-bit digital video output channel "B." Either logic "0" in interleaved digital video output data mode, or CrCb component digital video data is available at this port according to the state of bit 5 in register 06h. $DO_{B0(LSB)}$ is the least significant bit of channel "B;" $DO_{B9(MSB)}$ is the most significant bit of channel "B."

Pin Name	Pin Function	Pin Number
$DO_{A0(LSB)}$	Channel "A" LSB	13
DO_{A1}	Channel "A" Data Output	12
DO_{A2}	Channel "A" Data Output	9
DO_{A3}	Channel "A" Data Output	8
DO_{A4}	Channel "A" Data Output	7
DO_{A5}	Channel "A" Data Output	6
DO_{A6}	Channel "A" Data Output	5
DO_{A7}	Channel "A" Data Output	4
DO_{A8}	Channel "A" Data Output	3
$DO_{A9(MSB)}$	Channel "A" MSB	2
$DO_{B0(LSB)}$	Channel "B" LSB	25
DO_{B1}	Channel "B" Data Output	24
DO_{B2}	Channel "B" Data Output	23
DO_{B3}	Channel "B" Data Output	20
DO_{B4}	Channel "B" Data Output	19
DO_{B5}	Channel "B" Data Output	18
DO_{B6}	Channel "B" Data Output	17
DO_{B7}	Channel "B" Data Output	16
DO_{B8}	Channel "B" Data Output	15
$DO_{B9(MSB)}$	Channel "B" MSB	14

Table 15. Digital Output Organization

CLKOUT - Digital Output Data Clock, PIN 59.

Digital output clock for both channel "A" and "B." Output data transitions on the falling edge of CLKOUT and can be latched on the rising edge. The CLKOUT rate is twice the input mosaic pixel rate in the interleaved output mode with Y and CrCb output data both available on Channel "A." If the internal 4:5 horizontal scaler is enabled, the CLKOUT rate will be 5/4 times the 2x mosaic input data rate in interleaved mode. The CLKOUT rate is equal to the input mosaic pixel rate in the non-interleaved output mode with Y output data available on Channel "A" and CrCb data available on channel "B." If the internal 4:5 horizontal scaler is enabled, the CLKOUT rate will be 5/4 times the 1x mosaic input data rate in non-interleaved mode.

Output Mode	Mosaic Data Rate	CLKIN	CLKIN2	Channel "A"	Channel "B"	CLKOUT	Horizontal Pixels
Interleaved, scaler disabled	9.818MHz	9.818MHz	19.63MHz	YCrCb	logic "0"	19.63MHz	512
Interleaved, scaler enabled	9.818MHz	9.818MHz	24.54MHz	YCrCb	logic "0"	24.54MHz	640
Parallel, scaler disabled	9.818MHz	9.818MHz	19.63MHz	Y	CrCb	9.818MHz	512
Parallel, scaler enabled	9.818MHz	9.818MHz	24.54MHz	Y	CrCb	12.27MHz	640

Table 16. Example 512x492 Imager Output Options

INTERP - Digital Video Horizontal Data Rate Scaler Enable, PIN 54.

CMOS input enabling the internal 4:5 horizontal data rate scaler. Requires the CLKIN2 to be supplied with a 5/2 rate clock relative to the CLKIN clock input which is the incoming CCD mosaic data. This pin control is active logic high.

HREFOUT - Horizontal Reference Output, PIN 30.

CMOS output providing HREF.

VREFOUT - Vertical Reference Output, PIN 31.

CMOS output providing a VREF, or alternatively VSYNC vertical blanking signal.

FIELD - Odd/Even Field Indicator, PIN 62.

CMOS input providing an odd or even field indication for interlaced field imagers. The FIELD indicator changes according to the embedded EAV/SAV timing data, or the input timing signals from the analog processor. Typically the field indicator changes on the fourth line of every field when using the CS7615. Odd fields are indicated with logic low, and even fields are indicated with logic high.

OE - Output Enable, PIN 63.

CMOS input used to place all output pins in a High-Z mode. This control works in conjunction with the OE bit in the 06h internal I^2C register.

OE Bit	OE Pin	Digital Outputs
0	0	Enabled
0	1	High-Z
1	0	High-Z
1	1	Enabled

Table 17. Control of High-Z mode of output pins

Miscellaneous

RESET - Master External Reset Control, PIN 34.

CMOS input which initiates a complete power-on reset, where all registers are reset to their defaults, and the secondary I^2C bus attempts to load any EPROM configuration information. This pin operates in conjunction with the 0-bit of the 00h internal I^2C register. RESET is an active logic low input.

SCANMODE - Test Pin, PIN 53.

Test pin, connect to GND.

TESTPINB - Test Pin, PIN 60.

Test pin, connect to VDD.

TRANSP - Test Pin, PIN 61.

Test pin, connect to VDD.

SCANENABLE - Test Pin, PIN 64.

Test pin, connect to GND.

NC - No Connect, PINS 49, 50, 51, 52.

No internal connection. Recommend that these pins not be connected.

DEFINITIONS

Color Space - A color space is a mathematical representation of a set of colors. Three fundamental color models are RGB (used in color computer graphics and color television), YIQ, YUV, or YCrCb (used in broadcast and television systems), and CMYK (used in color printing).

RGB Color Space - The red, green, and blue (RGB) is widely used throughout computer graphics and imaging. Red, green, and blue are three primary additive colors where the individual components are added together to form the desired color.

YUV Color Space - The YUV color space is the basic color space used by the PAL (Phase Alternation Line), NTSC (National Television System Committee), and SECAM (Sequential Couleur Avec Memoire or Sequential Color with Memory) composite color video standards. The format conveys intensity in the Y component and color information in the U and V components. In an 8-bit system, where RGB range from code 0 to code 255, Y has a range of code 0 to code 255. The U component ranges over code 0 +/-112 codes, and the V component ranges over code 0+/-157.

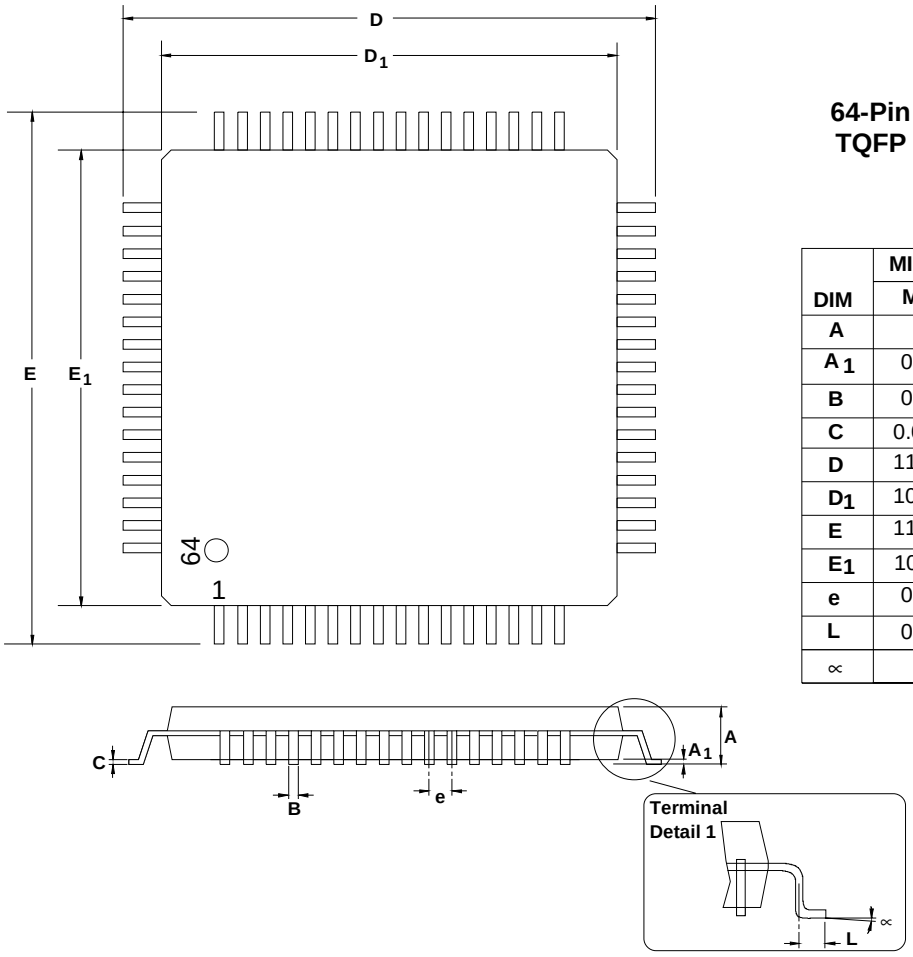
YCrCb Color Space - The YCrCb color space was developed as part of Recommendation ITU-601 during the development of a world-wide digital component video standard. YCrCb are scaled and offset versions of YUV color space. Y is defined to have a nominal range of code 16 to code 235; Cr and Cb are defined to have a range of code 16 to code 240, with code equal to the zero level.

MYCG Colors - Standard “color” CCD imagers employ integrated filter dots over the individual pixels. Typically, four color filters are used, Magenta, Yellow, Cyan, and Green.

Chroma Block - A group of four adjacent CCD pixel with integrated MYCG filter dots. These four pixels are generally formed with two pixels on one horizontal scan line, and two physically just below on the next scan line. There can also be some slight horizontal shift of the pixels to smooth the image. The chroma block is generally processed using a “color separator” into YUV, YCrCb, or RGB color space before any image processing.

PACKAGE DIMENSIONS

64-Pin TQFP



64-Pin TQFP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.66	-	0.068
A_1	0.00	-	0.00	-
B	0.14	0.26	0.006	0.010
C	0.077	0.177	0.003	0.007
D	11.70	12.30	0.461	0.484
D_1	10.00	10.00	0.394	0.394
E	11.70	12.30	0.461	0.484
E_1	10.00	10.00	0.394	0.394
e	0.40	0.60	0.016	0.024
L	0.35	0.70	0.014	0.028
∝	0°	12°	0°	12°

• Notes •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