AT 9020

AT(ISA) Bus Master Interface Chip for Intel 82596 Ethernet Controller

NOVEMBER 1991

T-52-33-55

Features

- Complete AT(ISA) Bus Master Interface for Intel 82596 Ethernet Controller
- Up to 10 Megabyte per second data transfer rate across the ATbus
- BIOS PROM and Node ID PROM support
- Direct connect to System Bus of all Host Interface Control Signals
- Low power CMOS in 128 Pin Plastic QFP Package

General Description

The AT 9020 is designed to provide the most compact, inexpensive and highest performance AT(ISA) bus interface for Bus Master adapter boards that use the Intel 82596 Ethernet Controller.

Use of the AT 9020 and other PLX -90X0 series of bus master chips minimizes hardware and software development costs and time because similar adapter hardware and driver designs can be used for AT, Micro Channel and EISA applications.

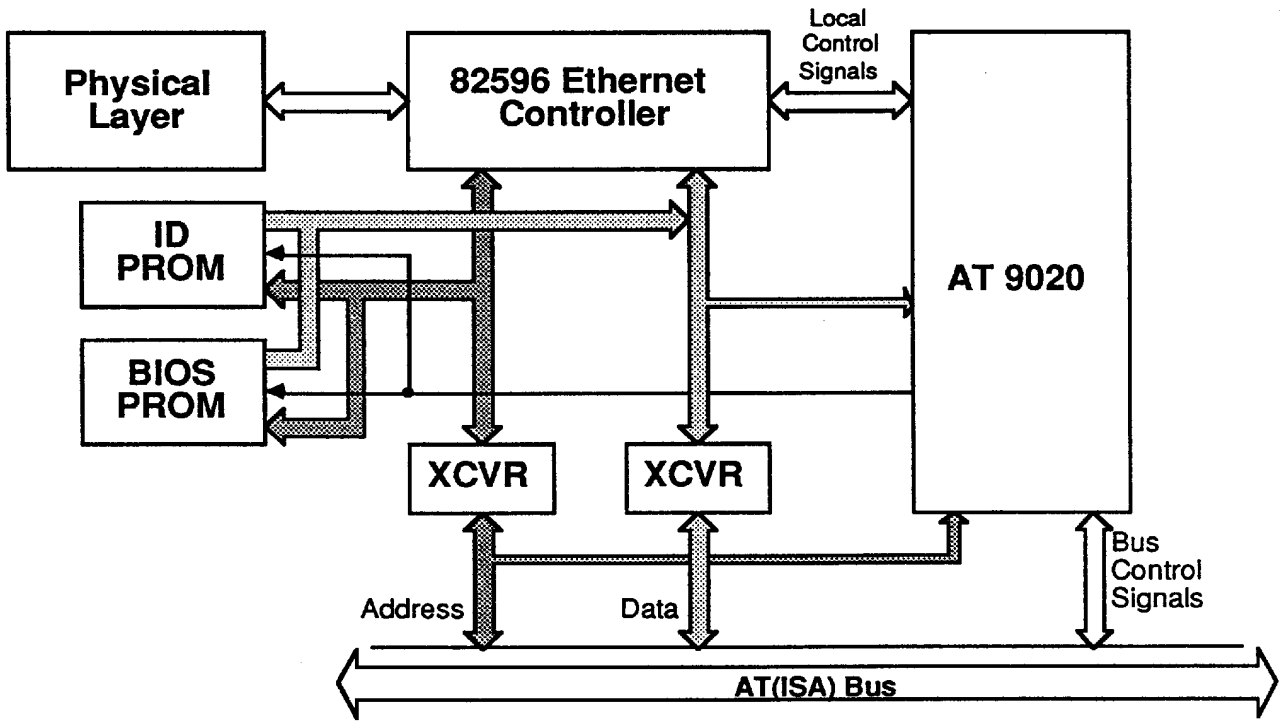

FIGURE 1. Typical Adapter Block Diagram

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SECTION 1 - INTRODUCTION

AT 9020 GENERAL DESCRIPTION

The AT 9020 is designed to provide the most compact, inexpensive and highest performance AT bus interface for Bus Master adapters that use the Intel 82596 Ethernet Controller Chip. Adapters which use the AT 9020 and the 82596 can achieve up to a 10 Megabyte/sec data transfer rate across the ATbus. This is several times the transfer rate of a typical sixteen bit slave LAN board, and can be accomplished while being competitive in cost. LAN performance is also enhanced by the more efficient protocol processing capabilities of the 82596. Furthermore, a bus master frees the host processor from managing bus data transfer operations, which improves overall system performance in multitasking operating environments

Use of the AT 9020 minimizes hardware and software development cost and time because one basic adapter hardware and driver design, with slight modifications, can be used in both AT, Micro Channel and EISA designs.

AT 9020 FUNCTIONS

The AT 9020 is a 128 pin plastic QFP CMOS bus master interface chip. AT 9020 major functions include:

1. **Master Control Signal Protocol Converter.** The chip converts all the handshakes of the 82596 to ATbus master handshakes.
2. **Slave controller.** The AT 9020 includes an AT slave interface for control of adapter board slave functions.

3. **Address Decoder.** The AT 9020 decodes host address bits A16-A13, A9-A0 and contains an enable pin for an external A23-A17 address decoder. The AT 9020 decodes these addresses to generate BIOS PROM, Node ID PROM and other chip selects.
4. **Interrupt generator.** The AT 9020 can generate one of four host interrupts from one local interrupt, programmable through POS.
5. **External Buffer Controller.** The AT 9020 generates all buffer enable, clocking and direction signals for external address and data transceivers or latching transceivers.
6. **Clock.** The AT 9020 runs from a crystal or TTL oscillator and can generate a clock up to 40 MHz for external and internal use.
7. **User programmable configuration bits.** The AT 9020 provides up to four external bits which can be configured through the configuration registers.
8. **Bus drivers.** AT control signals generated by the AT 9020 drive the bus directly, without requiring external drivers. Address and data signals do require buffers or transceivers.
9. **HOLD Release Idle timer.** The AT 9020 will retain control of the bus for approximately 800 ns after HOLD deassertion if the 82596 reasserts HOLD for a pre-fetch operation.
10. **Programmable Data Transfer Rate.** Through configuration registers, the AT 9020 may be programmed to supervise data transfers ranging from 5 to 10 Megabytes/sec by controling the width of the -MEMR or -MEMW pulses.

Data Transfer Modes

The AT 9020 supports the 82596 in both bus master mode and slave cycles for initialization.

Configuration Registers

The AT 9020 supports four registers which are configured from on board switches during power-on, which is controlled by the AT 9020. The four registers include the interrupt request level, Master bus cycle length configuration, I/O address decode bits, PROM address decode bits and DMA Channel indicator. The AT 9020 also provides four external user bits for application specific configuration information. In addition, the AT 9020 contains a transfer status register which flags and controls software reset, error and interrupt conditions.

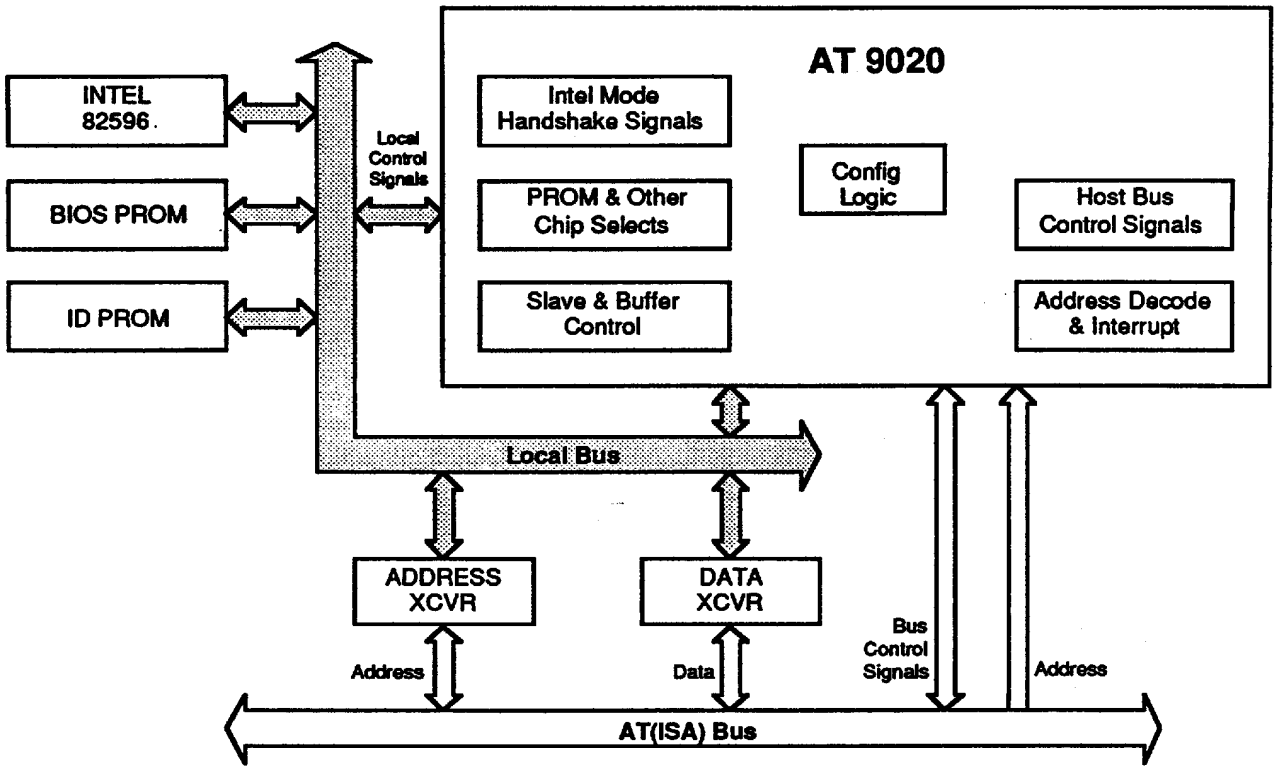

FIGURE 2. AT 9020 Functional Block Diagram

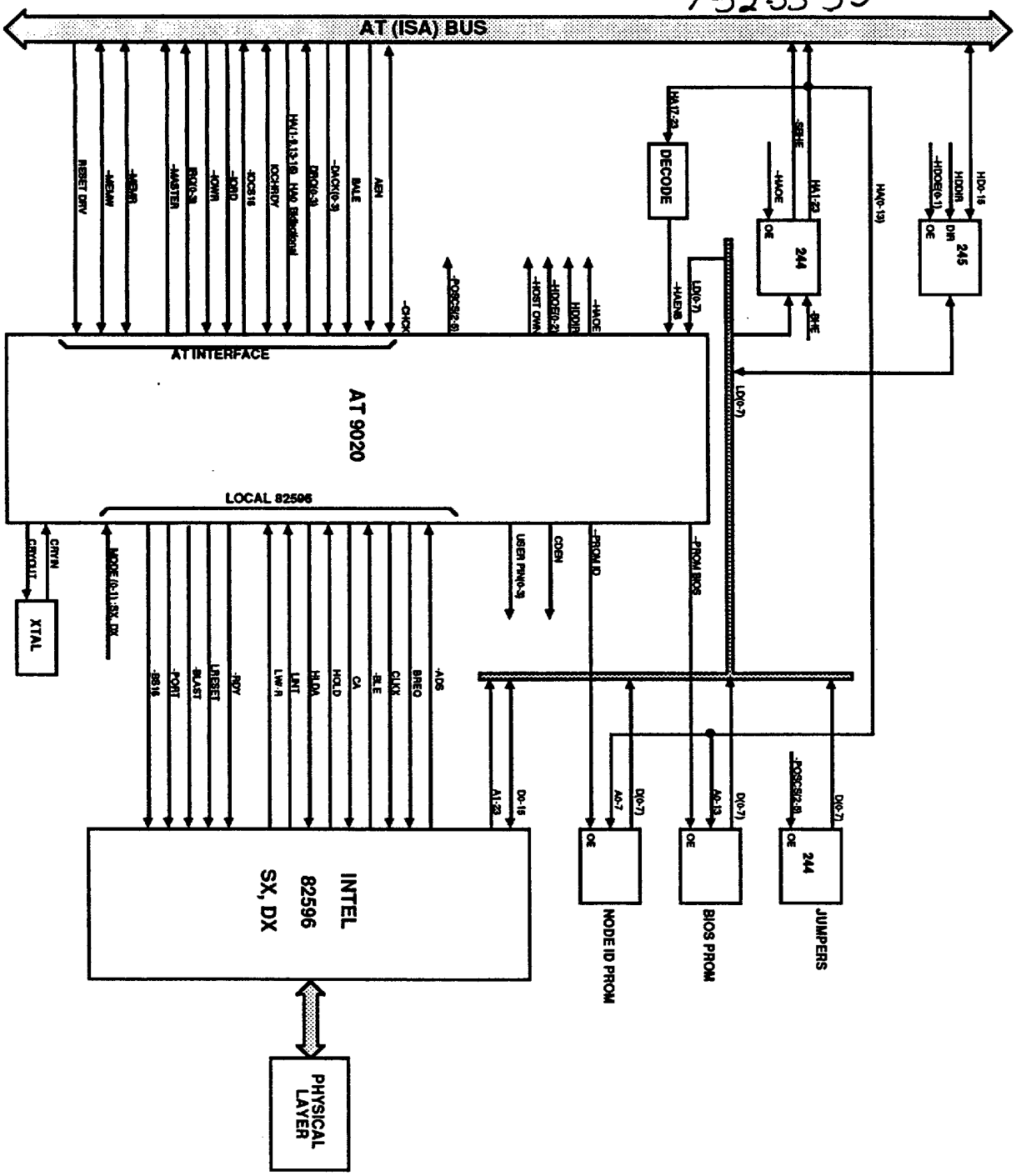

Figure 3.
Low Cost, ATbus Bus Master
Adapter Board

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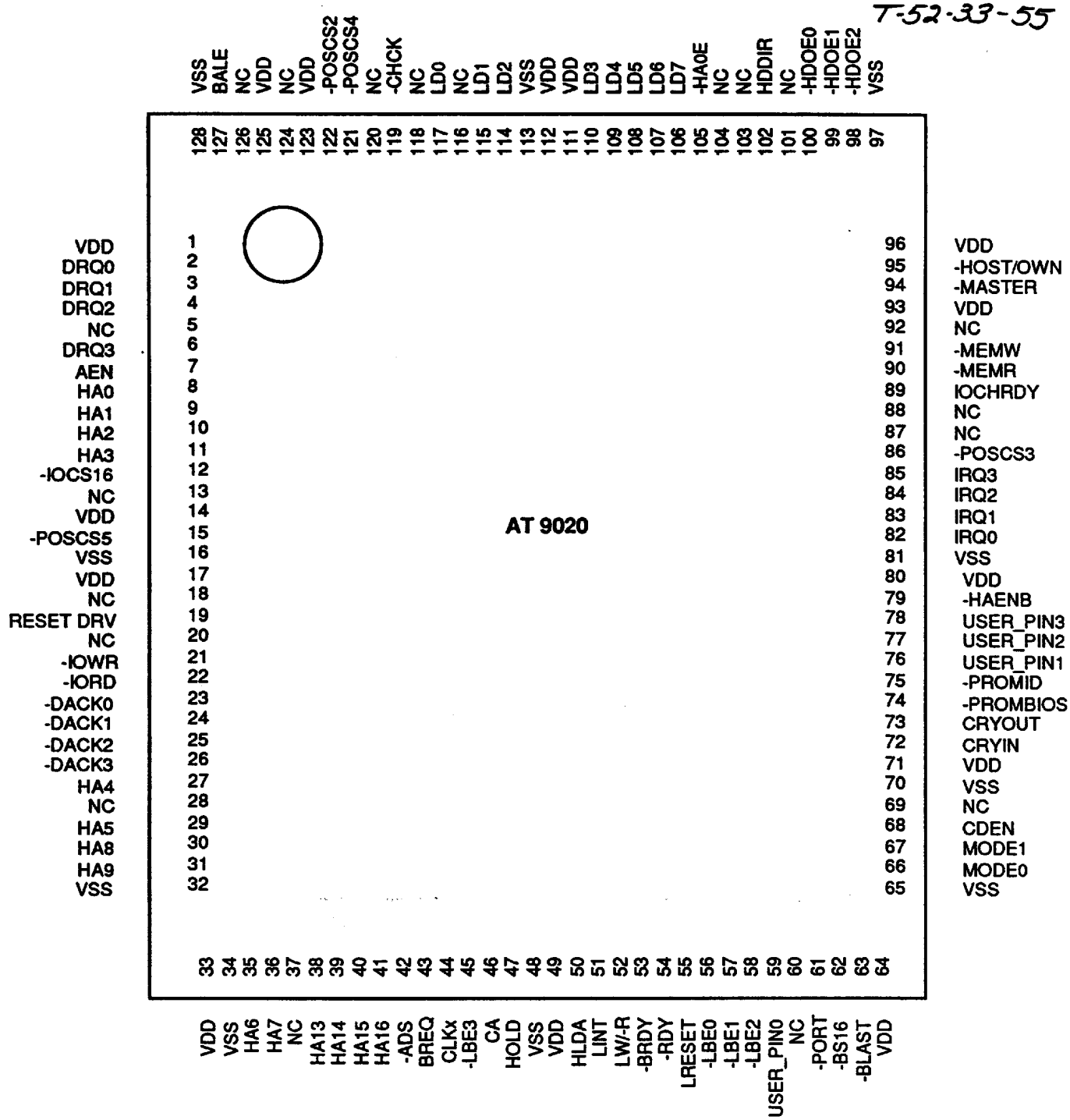

Figure 4.

SECTION 2 - REGISTER DESCRIPTION

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The AT 9020 contains four internal registers called Configuration 0-3, equivalent to POS 102-105 in Micro Channel. These registers are loaded at power-up. They provide essential configuration information to the AT 9020. The AT 9020 also contains a transfer status register (Register 15). The four configuration registers may be accessed through a normal I/O decode as well as the power-on setup routine. Register 15, the transfer status register, is accessed through an I/O decode only.

Table 2.1 summarizes the registers. The following abbreviations are used:

EI - This register is provided external to the AT 9020. At power-up, a copy of it is transferred internal to the AT 9020. A -POSCS pin gates the contents of the external register to the D(0-7) bus and into the AT 9020 on the trailing edge of -POSCS.

I - This register is internal to the AT 9020.

Table 2.1 Register Summary

Register Number	Description
0	EI - Config 0
1	EI- Config 1
2	EI - Config 2
3	EI - Config 3
15	I - Register 15

Address Decode Table

A9-A5	A4	A3-A0	
BASE (See Config. 1)	0	0010	- Config. 0 Resigter
BASE (See Config. 1)	0	0011	- Config. 1 Register
BASE (See Config. 1)	0	0100	- Config. 2 Register
BASE (See Config. 1)	0	0101	- Config. 3 Register
BASE (See Config. 1)	0	1000-1110	- Node ID PROM
BASE (See Config. 1)	0	1111	- Register 15
BASE (See Config. 1)	1	0000,1000,0010,1010	82596-PORT Select
BASE (See Config. 1)	1	0100,1100	- 82596 CA Select
BASE (See Config. 1)	All Others		- Reserved

Register 0 - Configuration 0

The Configuration 0 Register contains interrupt level, interrupt enable, card enable, bus hold time and master data size information.

WRITE / READ

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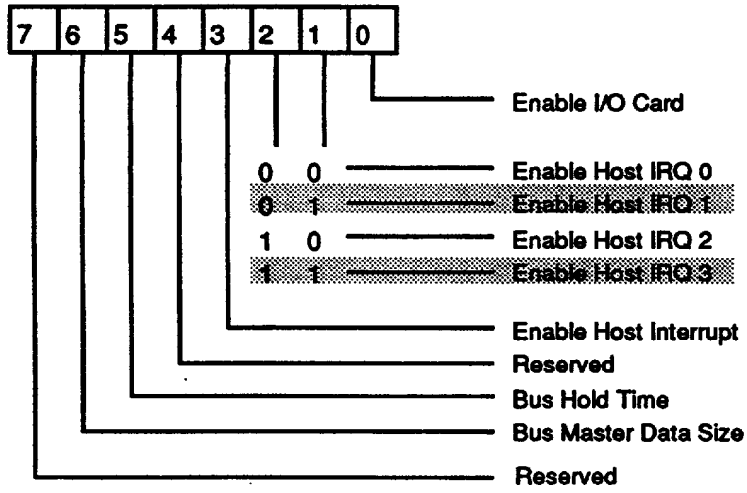
REGISTER 0 **FUNCTION**



Bit 0 - This bit should be set to 1 to enable the card. When this bit is set to 0, the AT 9020 does not respond to any host bus access except set-up.

Bits 1-2 - These bits select which AT interrupt signal to assert when the 82596 asserts its interrupt request line.

Bit 3 - When set to 1, this bit enables the IRQ(0-3) signals

Bit 4 - Reserved

Bit 5 - When set to 0, the AT 9020 will hold the bus no longer than 6 microseconds after -ACK. When this bit is set to 1, the AT 9020 holds the bus no longer than 12 microseconds after it detects -ACK.

Bit 6 - This bit specifies the data width for bus master transfers. This bit should be set to 0 for 16 bit masters and 1 for 32 bit masters.

Bit 7 - This bit should be set to 0.

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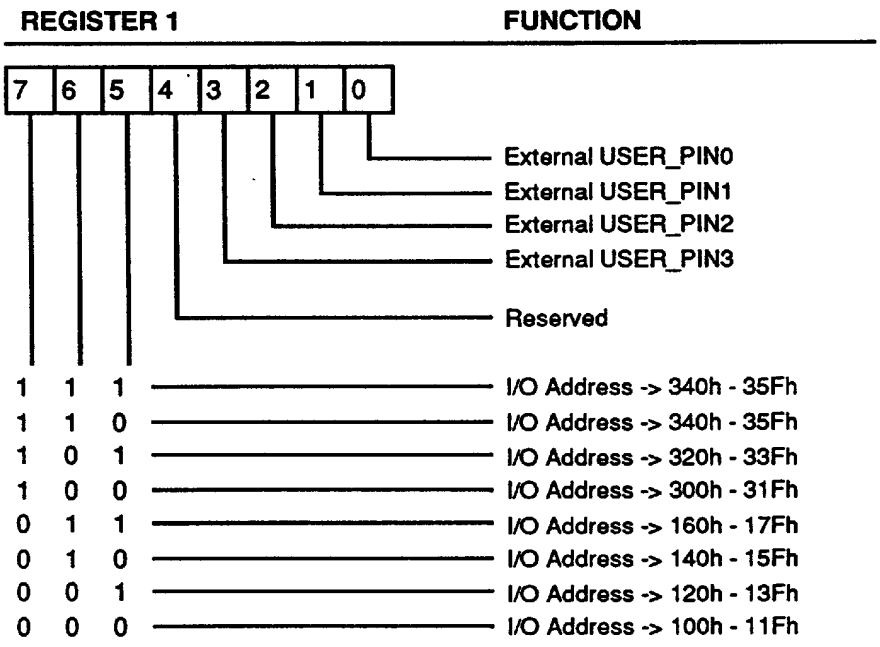
Register 1 - Configuration 1

The Configuration 1 Register contains the I/O address decode range for the AT 9020's chip selects and the chip's four configuration registers. Configuration 1 is also used to control external logic through bits 0-3. The register is loaded at power-up when the -POSCS(3) pin is asserted.

For decoding, bits 5-7 of Configuration 1 are compared against host address bits A9-5 to select the I/O address of the board as shown in the "Register 1" description below. The individual chip selects and the configuration registers reside in 32 bytes of AT I/O space as shown at the beginning of this section.

WRITE / READ



Bits 0-3 - These bits connect directly to the USER_PINs and allow control of external logic.

Bit 4 - Reserved

Bits 5-7 - The bits are compared against host address bits A5-A9 to select the I/O address of the board.

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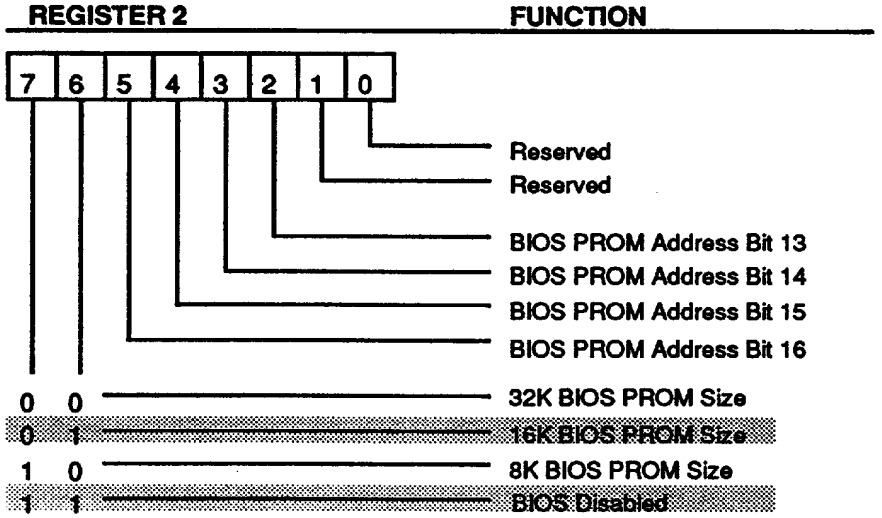
Register 2 - Configuration 2

The BIOS PROM starting address and size information is placed in this register at power-up when the -POSCS(4) pin is asserted. The BIOS PROM normally resides in the 0C0000h to 0DFFFFh address range. For BIOS PROM selection, address bits 23 - 13 are specified below:

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13
0	0	0	0	1	1	0	bit5	bit4	bit3	bit2

The I/O board designer must externally decode address bits A23 - A17 and connect the result of this decode to the -HAENB pin of the AT 9020. It should be noted that the BIOS PROM starting address must be on a memory boundary equal to the size of the BIOS PROM.

WRITE / READ



Bits 0-1 - Reserved

Bits 2-5 - These bits are compared against host address bits 13 - 16 for determining a BIOS PROM access.

Bits 6-7 - These bits specify the BIOS PROM size and BIOS Disable as indicated above.

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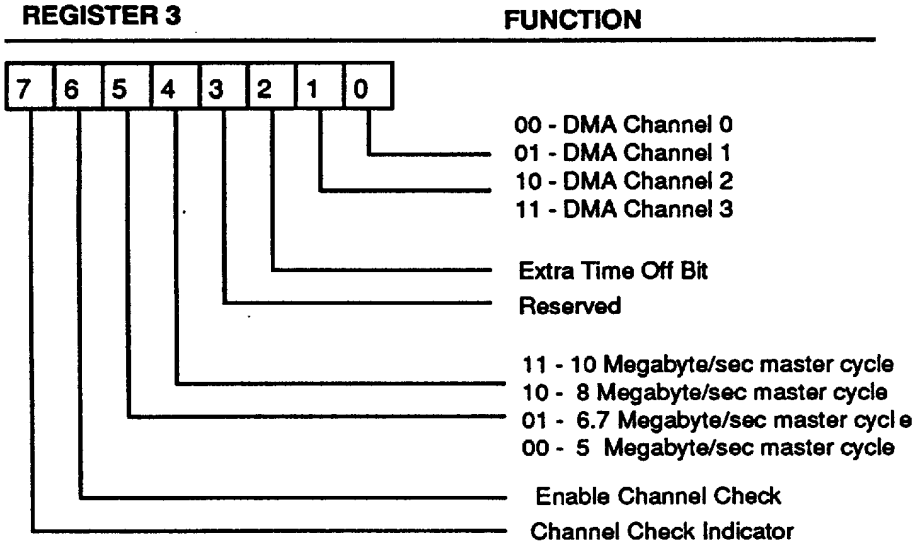
Register 3 - Configuration 3

This register provides the DMA Channel, data transfer rate and Channel Check configuration information to the AT 9020. This register is loaded at power-up when the -POSCS(5) pin is asserted.

WRITE / READ



Bits 0-1 - These bits select the DMA Channel to use for bus master operation.

Bit 2 - When set to 0, the AT 9020 will extend the -MEMW cycle by 50 ns

Bit 3 - Reserved

Bits 4-5 - These bits specify the length of the master data transfer cycle

Bit 6 - When this bit is set to 0, the -CHCK output of the AT 9020 is enabled.

Bit 7 - When the AT 9020 asserts -CHCK, it sets this bit to 0. A hardware reset will reset this bit to 1. It can also be set to 1 by an I/O write cycle.

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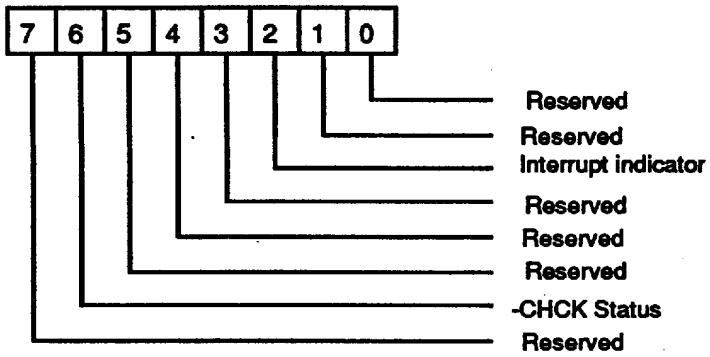
Register 15 - Configuration 15

This transfer status register controls and flags interrupt, reset and error conditions.

WRITE / READ

REGISTER 15	FUNCTION



Bit 0 - Reserved

Bit 1 - Reserved

Bit 2 - When the AT 9020 asserts an interrupt, it sets this bit to (1). **To reset this bit to 0, the software must write a 1 to this location, which clears it and sets it to 0.**

Bits 3-5 - Reserved

Bit 6 - If , while it is a bus master, the AT 9020 detects the assertion of -CHCK by another system component it sets this bit to 1. **To reset this bit to 0, the software must write a 1 to this location, which clears it and sets it to 0.**

Bit 7 - Reserved

SECTION 3- PIN DISCRIPTION

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The following abbreviations are used:

I/O - Input and Output Pin
I - Input Pin Only
O - Output Pin Only
TS - Three-State Pin
OC - Open Collector Pin
TP - Totem Pole Pin

Table 3.1 AT Bus Pin Summary

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (ma)
AEN	1	I	-	-
BALE	1	I	-	-
-CHCK	1	I/O	OC	24
-DACK(0-3)	4	I	-	-
DRQ(0-3)	4	O	TS	4
IOCHRDY	1	I/O	TS	24
-IOCS16	1	O	OC	24
-IORD	1	I	-	-
-IOWR	1	I	-	-
IRQ(0-3)	4	I/O	TS	24
-MASTER	1	O	OC	24
-MEMR	1	I/O	TS	24
-MEMW	1	I/O	TS	24
RESETDRV	1	I	-	-
TOTAL PINS	**23**			

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Table 3.2 Local Bus Pin Summary

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (ma)
-ADS	1	I	-	-
-BLAST	1	I	-	-
-BRDY	1	O	TP	4
BREQ	1	O	-	-
-BS16	1	O	TP	4
CA	1	O	TP	4
CDEN	1	O	TP	4
CLK2	1	O	TP	4
CRYIN	1	I	-	-
CRYOUT	1	O	-	-
HOLD	1	I	-	-
HLDA	1	O	TP	4
-LBE(0-3)	4	I	-	-
LINT	1	I	-	-
LRESET	1	O	TP	4
LW/-R	1	I	-	-
MODE(0-1)	2	I	-	-
-PORT	1	O	TP	4
-PROMBIOS	1	O	TP	4
-PROMID	1	O	TP	6
-RDY	1	O	TP	4
USER_PIN(0-3)	4	O	TP	6
TOTAL PINS	**29**			

Table 3.3 Buffer Control, Data and Address Pin Summary

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (ma)
HA0	1	I/O	TS	24
HA(13-16),(1-9)	13	I	-	-
-HAENB	1	I	-	-
-HAOE	1	O	TP	4
HDDIR	1	O	TP	4
-HDOE(0-2)	3	O	TP	4
-HOST_OWN	1	O	TP	4
LD(0-7)	8	I/O	TP	4
-POSCS(2-5)	4	O	TP	4
TOTAL PINS	**33**			

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Table 3.4 Power, Ground and No Connect Pin Summary

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (ma)
NC	19	-	-	-
VDD	14	-	-	-
VSS	10	-	-	-
TOTAL PINS	43			

Table 3.5 AT Bus Specific Pin Descriptions

Symbol	Signal Name	I/O	Pin Number	Function
AEN	Address Enable	I	7	This active high input signal indicates a DMA cycle is in progress. The AT 9020 uses the low level of this signal to qualify all AT bus access to the internal registers.
BALE	Address Latch Enable	I	127	This active high input signal is used to latch the contents of the address bus. The address latch is opened when BALE is high and the address is latched on the high to low transition on this signal.
-CHCK	Channel Check	I/O	119	This three-state pin indicates a check condition occurred on the host bus. This pin is asserted by the AT 9020 when a bus error occurs and Config 3, bit 6 is asserted.
-DACK(3) -DACK(2) -DACK(1) -DACK(0)	DMA Acknowledge	I	16 25 24 23	When the AT 9020 asserts one of the DRQ lines the corresponding, active low, DMA acknowledge is returned from the DMA subsystem. This signal indicates the AT 9020 has priority to use the AT bus. For AT bus operation the AT 9020 asserts the -MASTER signal and waits 1 BCLK clock cycle before asserting the AT bus control signals.
DRQ(3) DRQ(2) DRQ(1) DRQ(0)	DMA Request	O	6 4 3 2	These three-state outputs are used to request ownership of the AT bus. These signals are high true. The AT 9020 asserts one of these lines then waits for the corresponding -DACK to be returned from the system board. DRQ(0-3) selection is programmable in Configuration 3, bits 0-3.
IOCHRDY	I/O Channel Ready Input	I/O	89	This active high signal lengthens a bus cycle from its standard time when a device or memory cannot respond quickly enough. When IOCHRDY is low the AT 9020 inserts wait states until the device or memory brings it high. The AT 9020 may also assert this signal during slave accesses.

-IOCS16	I/O Chip Select 16	O	12	When this active low output signal is asserted by the AT 9020 it notifies the AT master of a 16 bit transfer. This pin is programmable in Config 0.
-IORD	I/O Read	I	22	This active low input signal indicates the system is transferring data to an I/O register.
-IOWR	I/O Write	I	21	This active low input signal indicates the system is writing data to an I/O register.
IRQ(3) IRQ(2) IRQ(1) IRQ(0)	Interrupt Request	I/O	85 84 83 82	These active high three-state signals are used to inform the system of the completion of a task. INT(0-3) are programmable in Configuration 0.
-MASTER	Master	O	94	This active low output signal indicates that the AT 9020 is controlling the AT bus. It is asserted when the DRQ signal is active and the corresponding -DACK signal is received.
-MEMR	Memory Read	I/O	90	This active low three-state signal indicates a read memory cycle.
-MEMW	Memory Write	I/O	91	This active low three-state signal indicates a memory write cycle.
RESET DRV	Bus Reset	I	19	This active high input signal provides a hard reset to the AT 9020 chip. Internal logic is initialized by this signal and any transfer operations are aborted.

Table 3.6 Local Bus Pin Description

Symbol	Signal Name	I/O	Pin Number	Function
-ADS	Address Strobe	I	42	This active low input signal indicates the Intel 82596 has begun a valid bus master cycle and that the 82596 pins A31-A2, -BE(0-3) and W/-R are being driven valid.
-BLAST	Last Burst Cycle	I	63	This active low input signal indicates that the next -BRDY will be treated as a normal -RDY. This input is only used for the 82596CA version. For the SX and DX versions this input should be tied high.

-BRDY	Burst Ready	O	53	This active low output signal performs the same function as -RDY during burst cycles. This output is not used for the Intel 82596 SX and DX versions. The AT 9020 asserts this active low signal to inform the Intel 82596 that the current bus master access cycle may be completed. When this signal is high, the 82596 inserts wait cycles in the current bus access.
BREQ	Bus Request	O	43	Bus Request to 82596. This signal is used to trigger the bus throttle timers.
-BS16	Bus Size	O	62	This active low output signal tells the Intel 82596CA or DX to operate in 16 bit host bus mode. This pin is a function of bit 6, in Config 0. It is not used with the 82596 SX.
CA	Channel Attention	O	46	This active high output is used to force the 82596 to begin executing memory resident commands. This signal wakes up the Intel 82596 and forces it to start executing command sequences from system memory. The I/O address of the signal is programmable in Configuration 1.
CDEN	Card Enable	O	68	This totem pole output is asserted when the I/O board has been enabled through configuration registers.
CLK2	Clock 2	O	44	This output signal provides the fundamental timing for the 82596. It is at the frequency or half the frequency of the crystal oscillator. The frequency depends on the setting of the MODE (0-1) pins. It provides all timing information. The AT 9020 synchronizes this signal with the Intel 82596 using the RESET pin. This ensures both the AT 9020 and the Intel 82596 are operating from the same CLKX edge.
CRYIN	Crystal Input	I	72	This input pin provides the timing for all synchronous operations in the AT 9020. It connects to either a TTL clock signal or directly to a crystal.
CRYOUT	Crystal Output	O	73	This output signal connects directly to a crystal oscillator. It is a no connect pin when the the CRYIN pin connects to a TTL clock signal.
HLDA	Bus Hold Acknowledge	O	50	This active high totem pole output signal indicates the AT 9020 has successfully gained access to the host bus. When the Intel 82596 receives this signal it begins bus master operation.
HOLD	Bus Hold Request	I	47	This active high input indicates the Intel 82596 needs to gain access to the host bus.

-LBE(0-3)	Byte Enable	I	56,57, 58,45	When operating in 16 bit mode, these pins are redefined to carry the -BLE signal into -LBE0. Also, -LBE (1,2,3) should be tied high, and -BHE from the controller must be driven through a buffer (244) to drive -SBHE onto the AT bus.
LINT	82596 Local Interrupt	I	51	This active high input is asserted when the 82596 has an interrupt pending. The AT 9020 asserts one of four host interrupts when this signal is active. The host interrupt line that is asserted is programmable in Configuration 0, bits 1 and 2. LINT is latched.
LRESET	Reset	O	55	This active high output signal provides a hard reset to the Intel 82596. It is also used to phase synchronize the clock for the AT 9020 and Intel 82596.
LW/-R	Write or Read	I	52	This input pin specifies whether the current bus master access is a read or write operation. When this pin is high, a write cycle is requested and when low a read cycle.
MODE(1) MODE(0)	Mode	I	67 66	These pins are used to select the various models of 82596 chips as outlined below: MODE1 MODE 0 596 Chip 0 0 Reserved 0 1 CA - 1x clk 1 0 DX - 2x clk 1 1 SX - 2x clk
-PORT	Port	O	61	This active low output signal causes the Intel 82596 to latch data from the system data bus into a 32 bit internal register. When operating in 16 bit mode, this signal must be activated twice for all CPU port access commands. This signal and the CA signal comprise the slave interface to the Intel 82596. The I/O address of the -PORT signal is programmable in Configuration 1.
-PROMBIOS	BIOS PROM Output Enable	O	74	This active low output pin connects to the output enable pin (-OE) of the BIOS Boot PROM. The AT 9020 gates the data from the PROM onto the system data bus. The system memory address of the BIOS PROM is programmable in Configuration 2.
-PROMID	ID PROM Output Enable	O	75	This active low output pin connects to the output enable pin (-0E) of the Node ID PROM. The AT 9020 gates the data from the Node ID PROM onto the system data bus. The system I/O address of the ID PROM is programmable in Configuration 1.
-RDY	Ready	O	54	The AT 9020 asserts this active low signal to inform the Intel 82596 that the current bus master access cycle may be completed. When this signal is high, the 82596 inserts wait cycles in the current bus access.

USER_PIN(3) USER_PIN(2) USER_PIN(1) USER_PIN(0)	User Defined Pin	O	59,78,77, 76	These totem pole output pins are controlled from Config 1 for each host interface. They control logic on the I/O board.

Table 3.7 Buffer Control, Data and Address Pin Description

Symbol	Signal Name	I/O	Pin Number	Function
HA0 HA(1-9) HA(13-16)	Host Address	I/O I I	8, 9, 10, 11, 27, 29, 30, 31, 35, 36, 38, 39, 40, 41,	These active high input signals are the host address lines used for POS, I/O and BIOS PROM space decode. HA(0-9) select the I/O address space and HA(13-16) are used with the -HAENB pin to select the BIOS PROM address space. Address ranges are programmed in Configuration 1 and 2.
-HAENB	Host Address Enable	I	79	This signal provides for an external decode of Host Address bits (17-23). This pin is used for BIOS PROM decode only.
-HAOE	Host Address Output Enable	O	105	This active low totem pole output signal connects to the -OE pin of the LS244s which gate the address bus between the adapter board and the Micro Channel, or AT bus.
HDDIR	Host Data Direction	O	102	This totem pole output signal connects to the DIR pin of the 245s which gate the data bus between the adapter board and the AT bus. When this pin is low the host data bus is gated to the adapter board. When this pin is high the data bus from the adapter board is gated to the host data bus.
-HDOE(2) -HDOE(1) -HDOE(0)	Host Data Output	O	98 99 100	These active low totem pole output signals connect to the -OE pin of the 245s which gate data between the adapter board and the host bus. These pins are connected as indicated below: Host byte -HDOE pin 0 -HDOE(0) 1 -HDOE(1) 2 -HDOE(2) 3 -HDOE(2)
-HOST/OWN	Host Own	O	95	When this active low totem pole signal is asserted, the AT 9020 is the owner of the host bus.
LD(0-7)	Host Data	I/O	117, 115, 114, 110, 109, 108, 107, 106,	These three-state data signals program Configuration registers in the AT 9020.The host processor may also read back the POS registers thought the 32 byte I/O port (see Configuration 1).
-POSCS(2-5)	POS Chip Select	O	122, 86, 121, 15	These active low totem pole outputs signals are used to load the registers in the AT 9020 after the RESET DRV has been asserted.

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Table 3.8 Power, Ground and No Connect Pin Description

VDD	Power	I	1, 14, 17, 33, 49, 64, 71, 80, 93, 96, 111, 112 , 123, 125	Five Volt Power Supply Pins
VSS	Ground	I	16, 32, 34, 48, 65, 70, 81, 97, 113, 128	Ground Pins
NC	No Connect	-	5, 13, 18, 20, 28, 37, 60, 69, 87, 88, 92, 101, 103, 104, 116, 118, 120, 124, 126	No Connect

Section 4 - Bus Cycles

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This section describes AT slave and master cycles. Timing relationships are described in more detail in Section 5. For detailed information on the 82596, see the Intel literature. Contact PLX Technology at 1-800- 759-3753 for assistance or other information.

Slave Cycles

Configuration Register Access

The AT 9020 initiates a setup routine when it detects the assertion of RESET. The AT 9020 will drive -POSCS(2-5) in the appropriate sequence to enable the gates which are connected to the four DIP switches that contain the configuration information. This configuration is loaded internally into the four configuration registers.

The four configuration registers plus the transfer status register (Register 15) may also be accessed through an I/O read or write operation at the I/O address described at the beginning of Section 2.

82596 Register Access

The 82596 registers are accessed through an AT slave I/O cycle. The AT 9020 decodes the system address as determined in the configuration registers (Section 2), and drives CA or -PORT to the 82596. The AT 9020 also drives the data direction signal (HDDIR) to the data buffers to indicate whether the cycle is read or write. The AT 9020 also drives the data buffer enable signals, -HDOE(0,1).

Node ID and BIOS PROM Access

The Ethernet Node ID PROM and BIOS PROM are accessed through an AT I/O slave cycle and Memory slave cycle respectively. The AT 9020 decodes the system address (as determined by section 2) and drives the -PROMID and -PROMBIOS chip selects. HDDIR and -HDOE(0,1) are enabled for the BIOS PROM access. The AT 9020 automatically inserts wait states by deasserting IOCHRDY.

Master Cycles

Bus Request

The 82596 initiates an AT Bus Request by asserting HOLD to the AT 9020. When the AT 9020 detects HOLD, it drives DRQn (channel programmable in configuration registers) and waits to receive -DACKn from the ATbus. When the AT 9020 receives -DACKn, it will assert -MASTER. Approximately 250ns after asserting -MASTER, the AT 9020 asserts HLDA to the 82596.

BURST and Single Data Transfer Cycle

The data transfer cycle starts when the AT 9020 asserts HLDA, which is an indication to the 82596 that it may begin transferring data. After detecting HLDA, the 82596 asserts -ADS to the AT 9020 and LW/-R depending on whether the cycle is Read or Write. On the next clock cycle, the AT 9020 will assert -MEMR (on the rising edge) or -MEMW (on the falling edge) depending on whether the cycle is read or write. The width of -MEMR and -MEMW is programmable in the configuration registers to determine the data transfer rate. The AT 9020 also enables the address and data buffers in the proper sequence and drives the status lines to the AT bus.

When valid data has been transferred to the ATbus, the AT 9020 asserts -RDY, which indicates to the 82596 that it may reassert -ADS and start another cycle.

Data transfers will continue in this way until either the 82596 deasserts HOLD or the adapter exceeds the maximum bus hold time limit programmed in the configuration registers. In either case the AT 9020 will deassert HLDA.

Provided that the adapter has not exceed the bus hold time limit programmed in the configuration registers, the AT 9020 will actually retain control of the bus for .8 microseconds after the deassertion of HOLD. If the 82596 does not reassert HOLD within this period, the AT 9020 will release the ATbus. This is to allow the 82596 to retain control of the bus for prefetch operations when the 82596 will immediately reassert HOLD.

The AT 9020 in conjunction with the 82596 can be programmed to sustain Read and Write BURST data transfer cycles of as low as 200 ns (10 Megabytes/second), provided the slave does not slow down the transfers with IOCHRDY.

Section 5 - Timing

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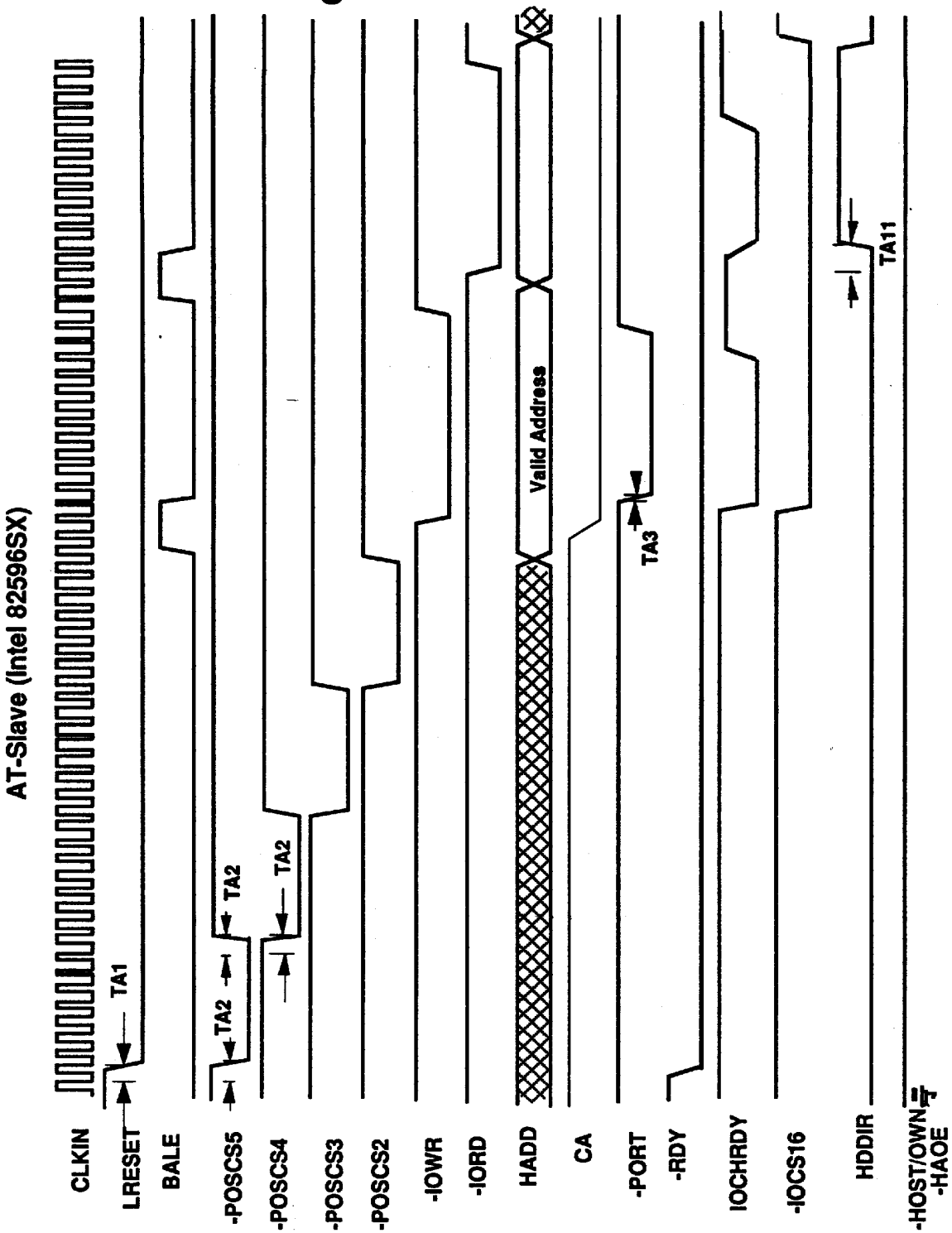

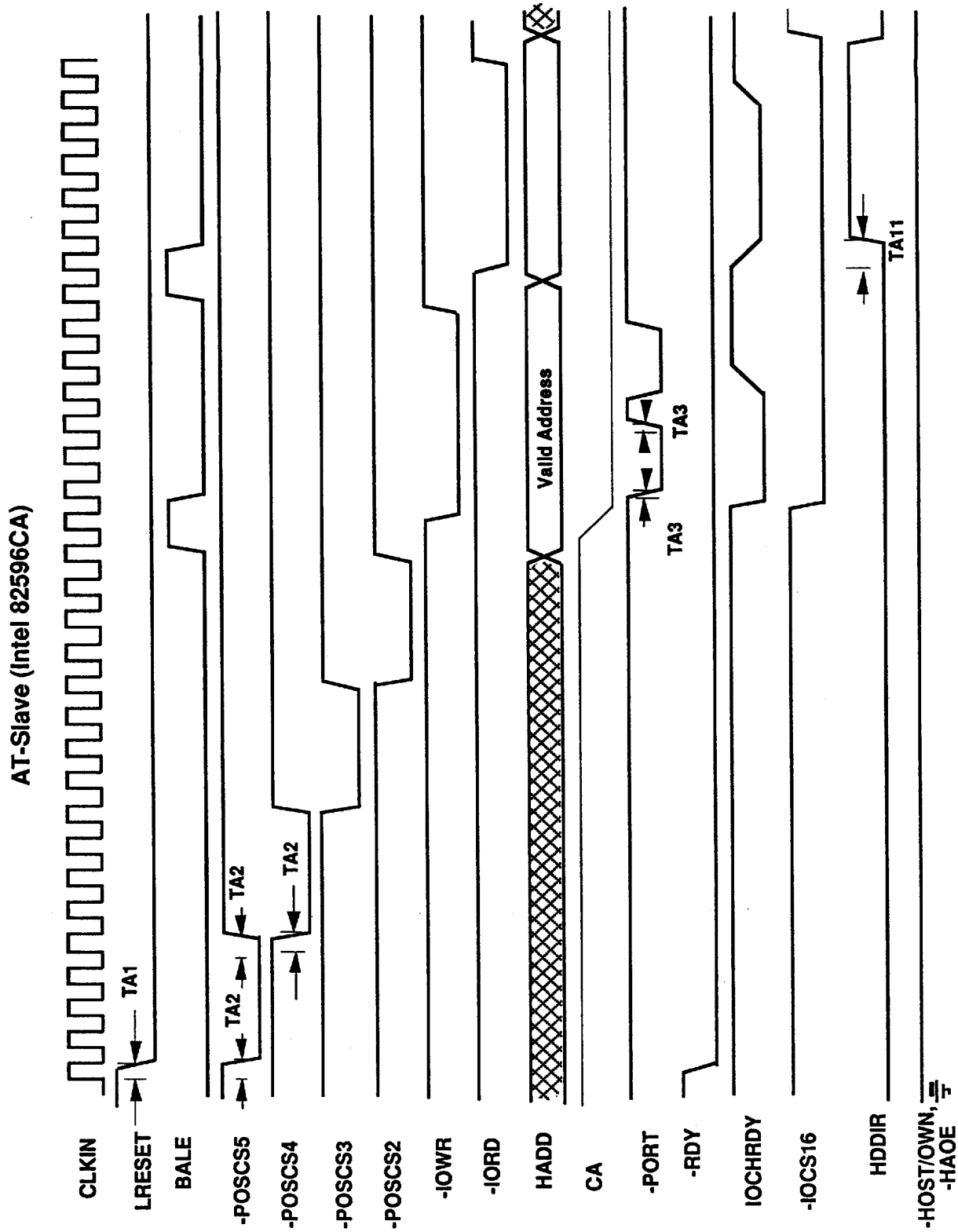

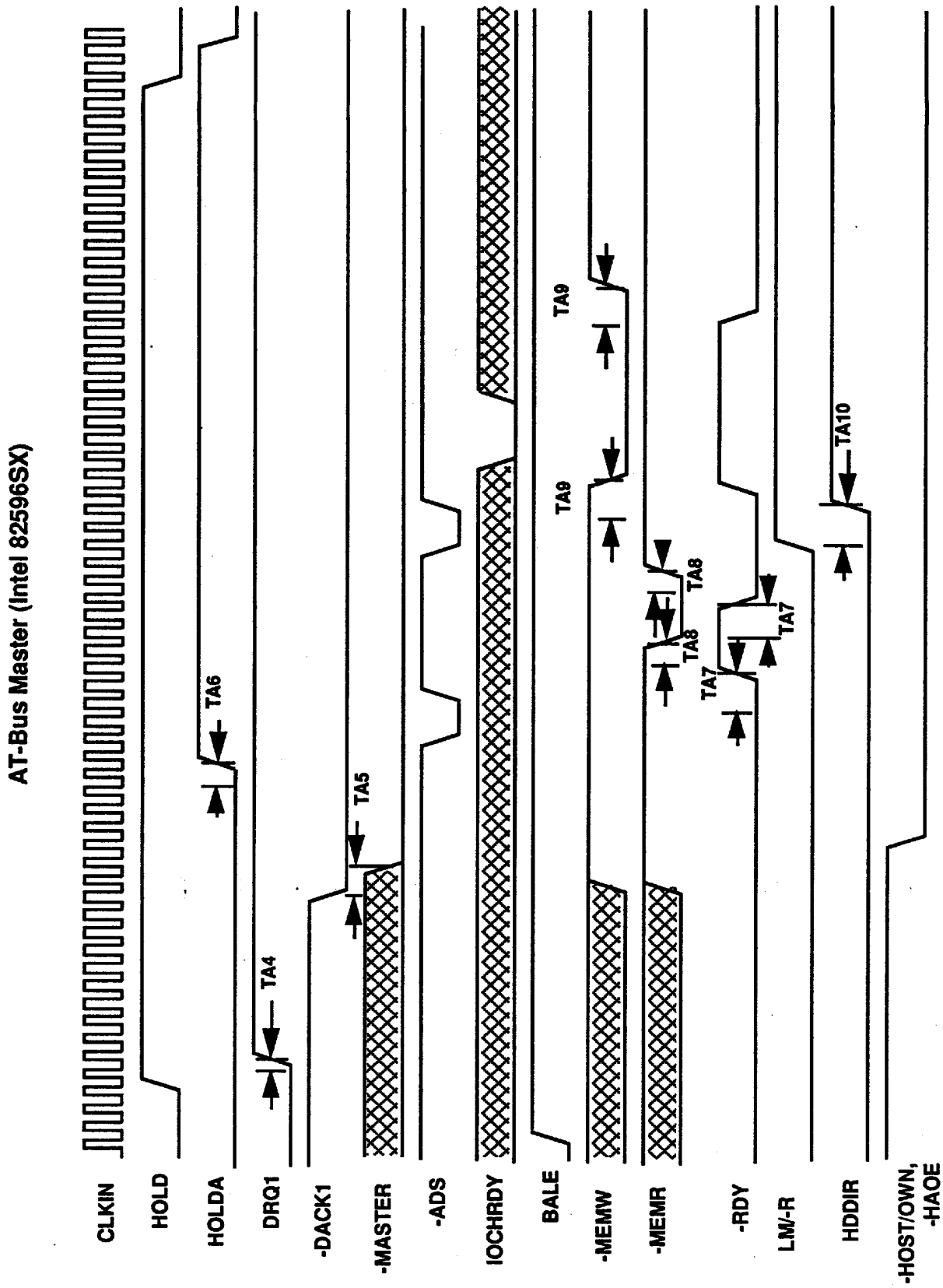

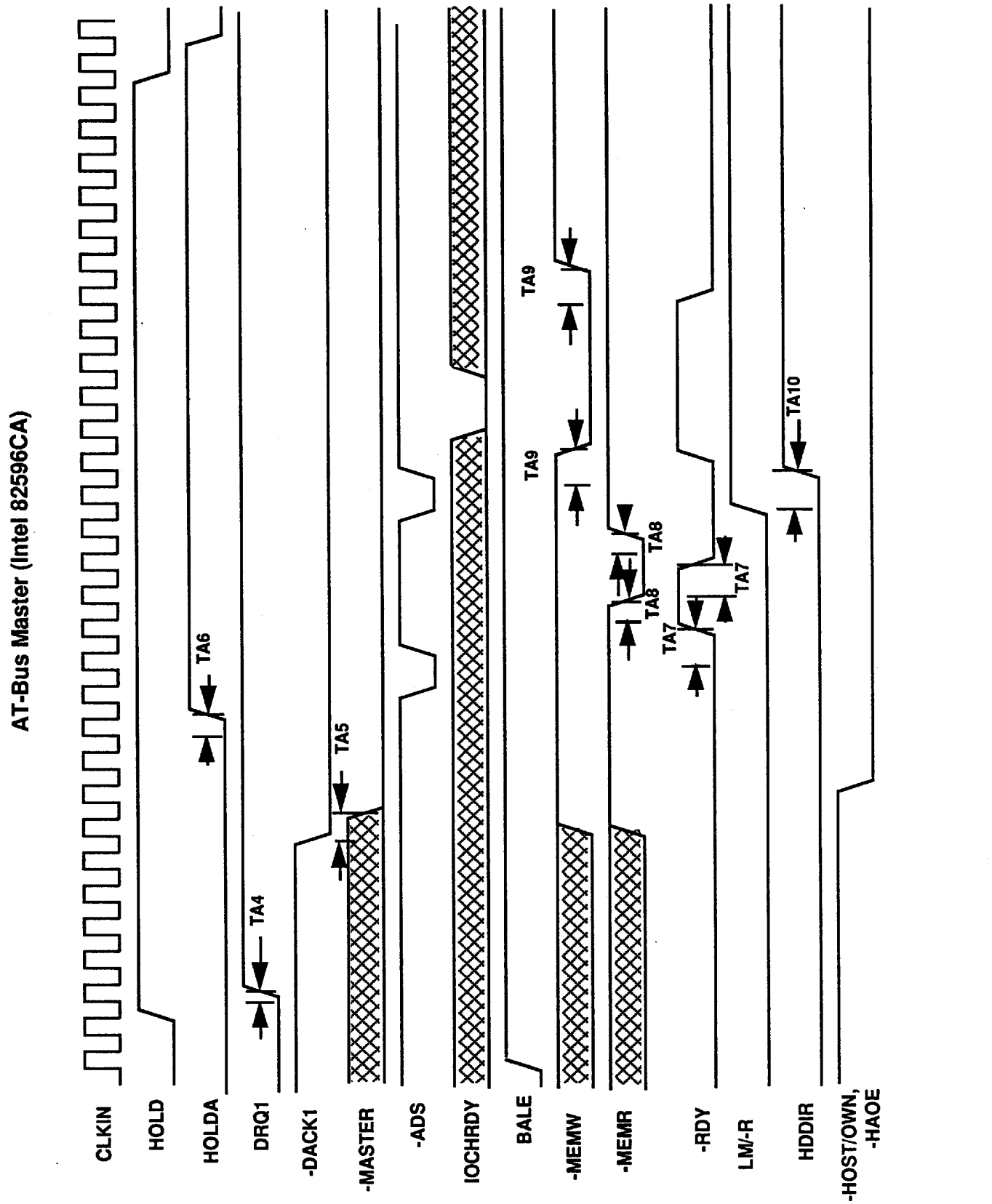

AC Timing Min/Max Specifications

AT 9020 timing

Time	Description	Min	Max	Unit
TA1	Clock high to LRESET low delay		40	ns
TA2	Clock high to --POSCS valid delay		35	ns
TA3	Clock high to -PORT valid delay		35	ns
TA4	Clock high to DRQ high delay		40	ns
TA5	Clock high to -MASTER low delay		40	ns
TA6	Clock high to HLDA high delay		35	ns
TA7	Clock high to -RDY valid delay		35	ns
TA8	Clock high to -MEMR valid delay		40	ns
TA9	Clock low to -MEMW valid delay		40	ns
TA10	LM/-R high to HDDIR high delay		30	ns
TA11	-IOWR low to HDDIR high delay		30	ns

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Section 6 - Electrical Specifications & Max Ratings

Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground	-0.5V to +7.0V
Input Voltage (VIN)	VSS - 0.5V VDD + 0.5V
Output Voltage (VOUT)	VSS - 0.5V VDD + 0.5V

Operating Ranges

Ambient Temperature	Supply Voltage (VDD)	Input Voltage (VIN)
0C to +70°C	5V +/- 5%	Min = VSS Max = VDD

Capacitance (sample tested only)

Parameter	Test Conditions	Pin Type	Typical Value	Units
CIN	VIN =2.0V f = 1 MHz	Input	5	pF
COUT	VOUT = 2.0V f = 1 MHz	Output	10	pF

Electrical Characteristics Tested Over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
VOH	Output High Voltage	VDD = Min, VIN=VIH or VIL	IOH = -4.0mA	2.4		V
VOL	Output Low Voltage		IOL per Tables 3.1-3.4		0.4	V
VIH	Input High Level			2.0		V
VIL	Input Low Level				0.8	V
ILI	Input Leakage Current	VSS <= VIN <=VDD VDD = Max		-10	+10	uA
IOZ	Tri-state Output Leakage Current	VDD= Max VSS <= VIN <=VDD		-10	+10	uA
ICC	Power Supply Current	VDD= Max		20	80	mA

Section 7 - Package Mechanical Dimensions

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