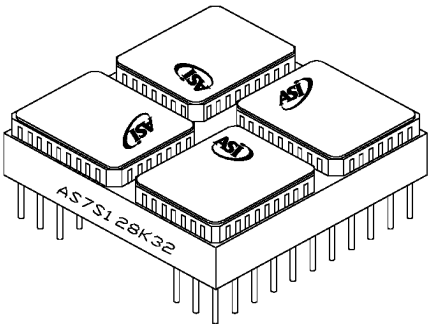
SRAM MODULE

FEATURES

- SMD 5962-93187 Pin Compatible
- Access times of 20, 25, 35 ns
- Built in decoupling caps for low noise operation
- Organized as 128K x32;
- Operation with single 5 volt supply
- Low power CMOS
- TTL Compatible Inputs and Outputs
- Packaging
  - 66 pin PGA type 1.09 inch square
  - 68 lead J leaded LCC (contact factory)
  - 68 lead quad flatpack (contact factory)

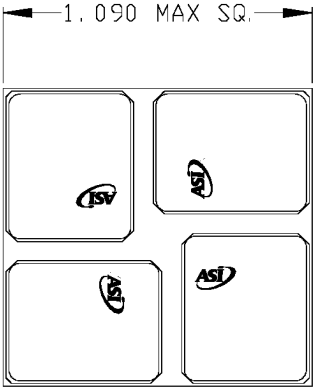


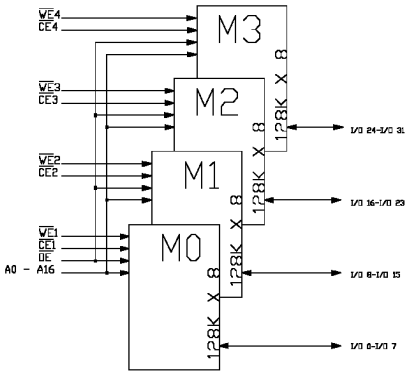
GENERAL DESCRIPTION

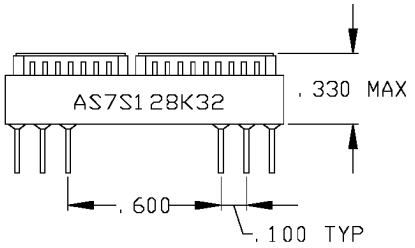
The Austin Semiconductor, Inc. AS7S128K32 is a 4 Megabit CMOS SRAM Module organized as 128Kx32 and is user configurable to 256K x 16 and 512K x 8. The AS7S128K32 achieves high speed access, low power consumption and high reliability by employing advanced CMOS memory technology.

These advanced features make ASI modules ideally suited for military applications.

The AS7S128K32 module is constructed using a 1.09 inch square ceramic pin grid array substrate. This compact layout reduces space requirements for board assembly to a minimum.







PIN CONFIGURATION

I/O8	1	$\overline{WE}$	12	I/O15	23			I/O24	34	VCC	45	I/O31	56
I/O9	2	$\overline{CE2}$	13	I/O14	24			I/O25	35	$\overline{CE4}$	46	I/O30	57
I/O10	3	GND	14	I/O13	25			I/O26	36	$\overline{WE4}$	47	I/O29	58
A13	4	I/O11	15	I/O12	26			A6	37	I/O27	48	I/O28	59
A14	5	A10	16	$\overline{OE}$	27			A7	38	A3	49	AO	60
NC	8	VCC	19	I/O7	30			A9	41	$\overline{WE3}$	52	I/O23	63
I/O0	9	$\overline{CE1}$	20	I/O6	31			I/O16	42	$\overline{CE3}$	53	I/O22	64
I/O1	10	NC	21	I/O5	32			I/O17	43	GND	54	I/O21	65
I/O2	11	I/O3	22	I/O4	33			I/O18	44	I/O19	55	I/O20	66

ABSOLUTE MAXIMUM RATINGS*

Voltage of Vcc Supply Relative to Vss.....-1V to +7V
Storage Temperature.....-55°C to +150°C
Short Circuit Output Current(per I/O).....20mA
Voltage on Any Pin Relative to Vss.....-.5V to Vcc+.5V
Junction Temperature**.....+175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation on the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See the Application Information section at the end of this datasheet for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C ≤ TA≤ 125°C; V_{CC} = 5V ± 10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+.5	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Outputs Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

			MAX					
DESCRIPTION	CONDITIONS	SYMBOL	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^{t}RC (MIN) Output Open	I_{CC}	620	560	520	500	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IL} ≤ V_{SS} +0.2V V_{IH} ≥ V_{CC} -0.2V; f = 0 Hz	I_{SBC2}	40	40	40	40	mA	
	"L" Version Only	I_{SBC2}	10	10	10	10	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz	C_I	40	pF	4
Output Capacitance	V_{CC} = 5V	C_O	30	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(-55°C ≤ T_C ≤ 125°C; V_{CC} = 5V ± 10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	t_{RC}	20		25		35		45		ns	
Address access time	t_{AA}	20		25		35		45	ns		
Chip Enable access time	t_{ACE}	20		25		35		45	ns		
Output hold from address change	t_{OH}	2		2		2		2		ns	
Chip Enable to output in Low-Z	t_{LZCE}	2		2		2		2		ns	7
Chip disable to output in High-Z	t_{HZCE}		9		10		14		15	ns	6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		ns	4
Chip disable to power-down time	t_{PD}		20		25		35		45	ns	4
WRITE Cycle											
WRITE cycle time	t_{WC}	20		25		35		45		ns	
Chip Enable to end of write	t_{CW}	15		18		20		25		ns	
Address valid to end of write	t_{AW}	15		18		20		25		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Address hold from end of write	t_{AH}	2		2		2		2		ns	
WRITE pulse width	t_{WP}	5		17		20		25		ns	
Data setup time	t_{DS}	10		12		15		20		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	2		2		2		2		ns	7
Write Enable to output in High-Z	t_{HZWE}		10		11		14		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	VSS to 3V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

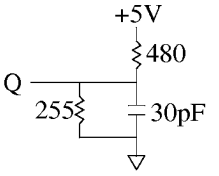


Fig. 1 OUTPUT LOAD EQUIVALENT

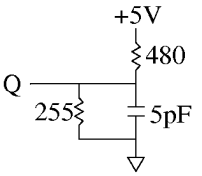


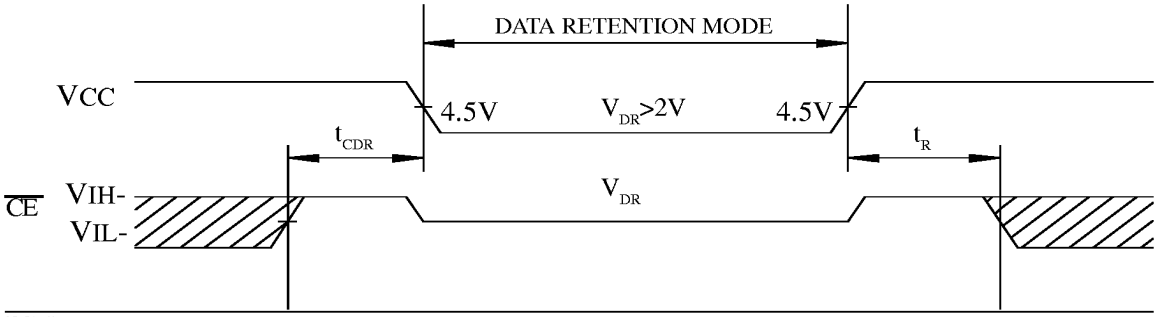
Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

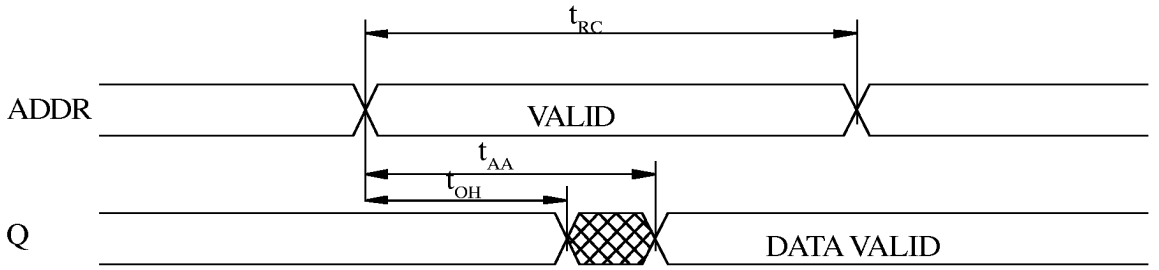
1. All voltages referenced to V_{ss} (GND).
2. -2v for pulse width <20ns.
3. ICC is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and f= $\frac{1}{t_{RC(MIN)}}$ HZ.
4. This parameter is guaranteed but not tested.
5. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
6. t_{HZCE}, t_{HZOE} and t_{HZWE} are specified with C_L= 5pF as in Fig. 2. Transition is measured +/- 500 mV typical from steady state coltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, t_{HZCE}, is less than t_{LZCE}, and t_{HZWE} is less than t_{HZWE}.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enable are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. t_{RC}= READ cycle time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. I_{CC} is for 32 bit mode.

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
VCC for Retention Data			VDR	2	—	V	
Data Retention Current	$\overline{CE}$ ≥ (VCC - 0.2V) VIN ≥ (VCC - 0.2V) or ≤ 0.2V	VCC = 2V	ICCDR		4	mA	
		VCC = 3V			8	mA	
Chip Deselect to Data Retention Time			t_{CDR}	0	—	ns	4
Operation Recovery Time			t_R	t_{RC}		ns	4, 11

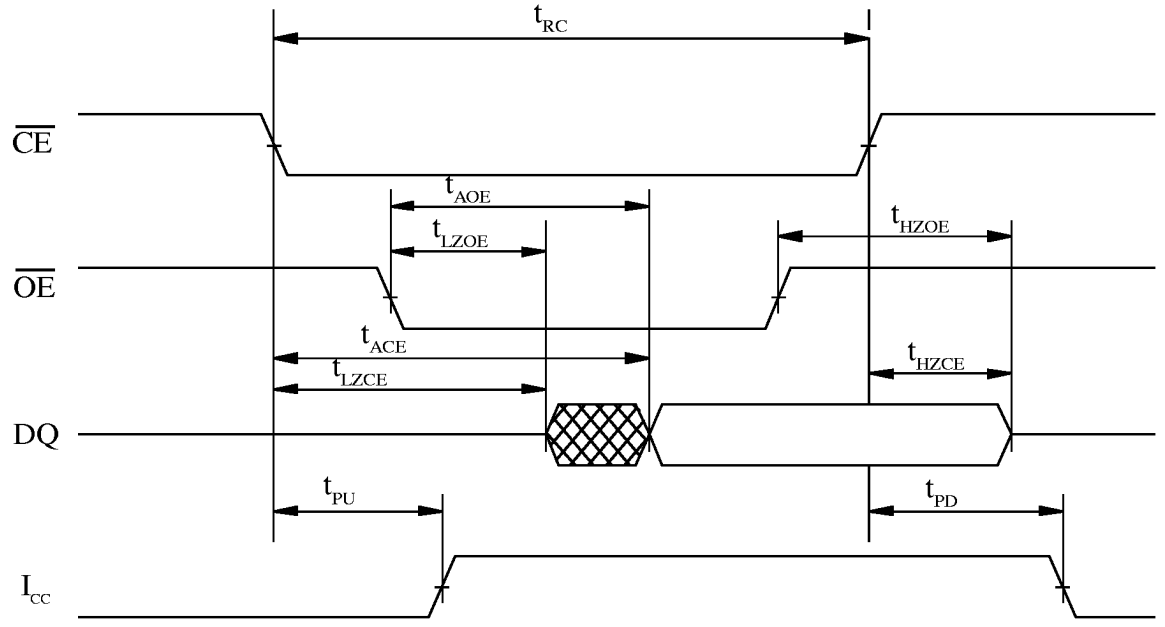
LOW V_{CC} DATA RETENTION WAVEFORM



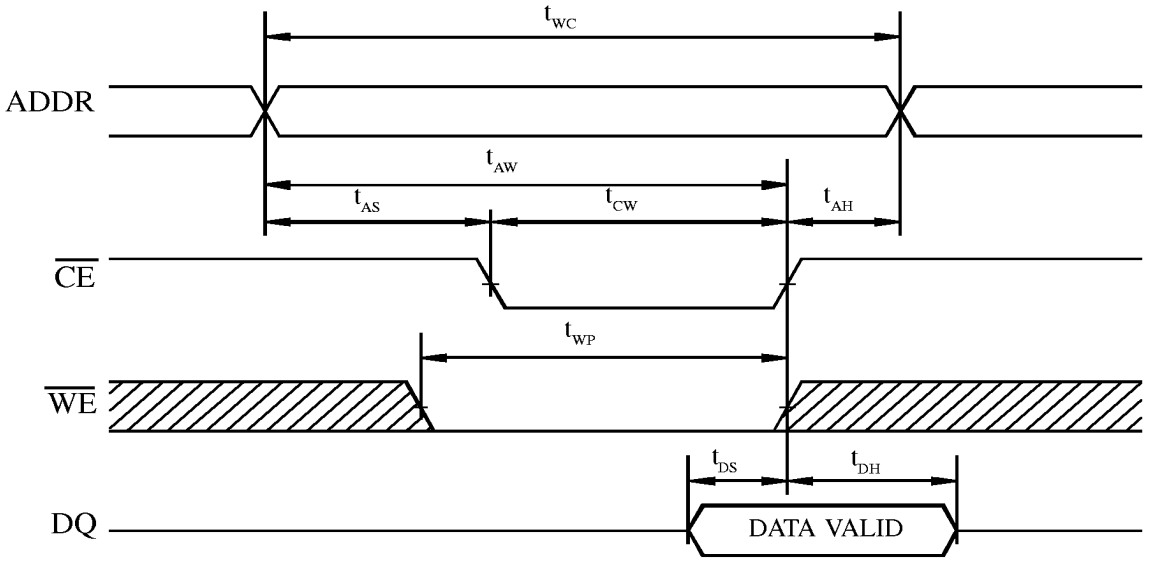
READ CYCLE NO. 1



READ CYCLE NO. 2



WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2
(Write Enable Controlled)