

SANYO

No.2515

2SA1591/2SC4133

PNP/NPN Epitaxial Planar Silicon Transistors

Switching Applications
(with Bias Resistance)**Applications**

- Switching circuit, inverter circuit, interface circuit, driver circuit

Features

- On-chip bias resistance ($R_1=4.7k\Omega$, $R_2=47k\Omega$)
- Small-sized package (SPA)

(): 2SA1591

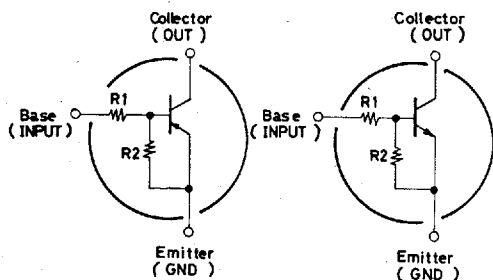
Absolute Maximum Ratings at $T_a=25^\circ\text{C}$

			unit
Collector to Base Voltage	V_{CB0}	(-)50	V
Collector to Emitter Voltage	V_{CE0}	(-)50	V
Emitter to Base Voltage	V_{EB0}	(-)6	V
Collector Current	I_C	(-)100	mA
Collector Current (Pulse)	I_{CP}	(-)200	mA
Collector Dissipation	P_C	300	mW
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics at $T_a=25^\circ\text{C}$

			min	typ	max	unit
Collector Cutoff Current	I_{CB0}	$V_{CB}=(-)40\text{V}, I_E=0$			(-)0.1	μA
Collector Cutoff Current	I_{CE0}	$V_{CE}=(-)40\text{V}, I_B=0$			(-)0.5	μA
Emitter Cutoff Current	I_{EB0}	$V_{EB}=(-)5\text{V}, I_C=0$	(-)74	(-)97	(-)138	μA
DC Current Gain	h_{FE}	$V_{CE}=(-)5\text{V}, I_C=(-)5\text{mA}$	70			
Gain-Bandwidth Product	f_T	$V_{CE}=(-)10\text{V}, I_C=(-)5\text{mA}$		250 (200)		MHz
Output Capacitance	C_{ob}	$V_{CB}=(-)10\text{V}, f=1\text{MHz}$		3.7 (5.5)		pF
C-E Saturation Voltage	$V_{CE(sat)}$	$I_C=(-)10\text{mA}, I_B=(-)0.5\text{mA}$		(-)0.1	(-)0.3	V
C-B Breakdown Voltage	$V_{(BR)CB0}$	$I_C=(-)10\mu\text{A}, I_E=0$	(-)50			V
C-E Breakdown Voltage	$V_{(BR)CE0}$	$I_C=(-)100\mu\text{A}, R_{BE}=\infty$	(-)50			V

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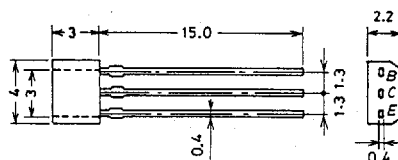
Electrical Connection

2SA1591(PNP)

2SC4133(NPN)

Case Outline 2033

(unit:mm)



B: Base
C: Collector
E: Emitter

SANYO: SPA

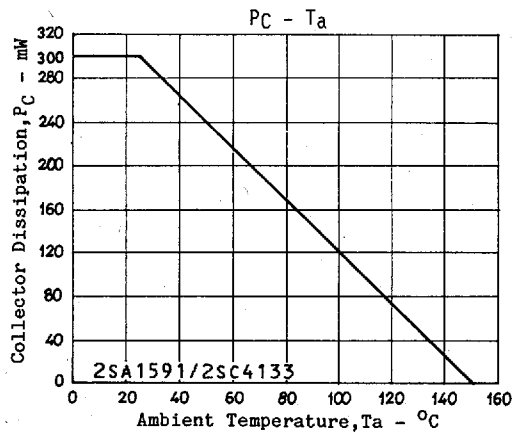
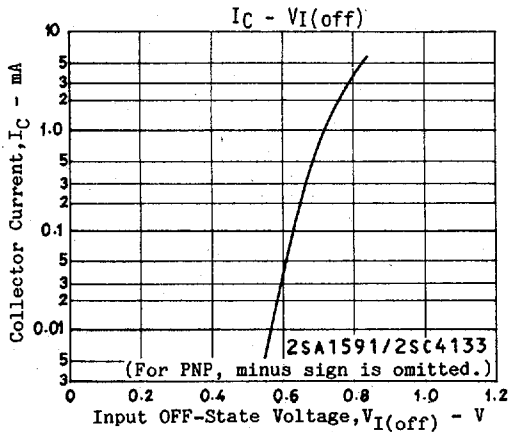
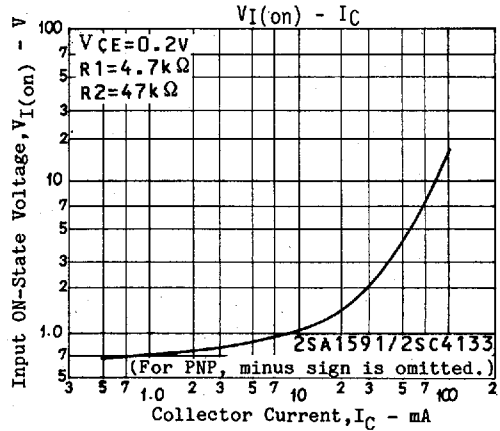
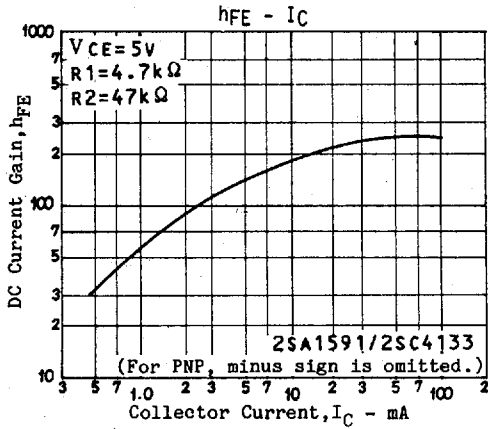
Specifications and information herein are subject to change without notice.

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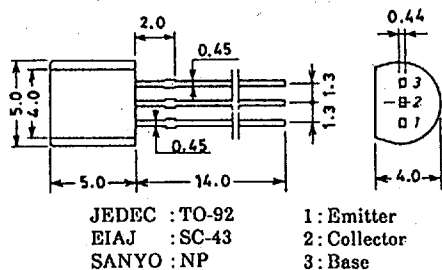
			min	typ	max	unit
Input OFF-State Voltage	$V_{I(off)}$	$V_{CE}=(-)5V, I_C=(-)100\mu A$	(-)0.5	(-)0.6	(-)0.8	V
Input ON-State Voltage	$V_{I(on)}$	$V_{CE}=(-)0.2V, I_C=(-)5mA$	(-)0.7	(-)0.85	(-)1.3	V
Input Resistance	R_1		3.3	4.7	6.1	k Ω
Resistance Ratio	R_1/R_2		0.09	0.1	0.11	



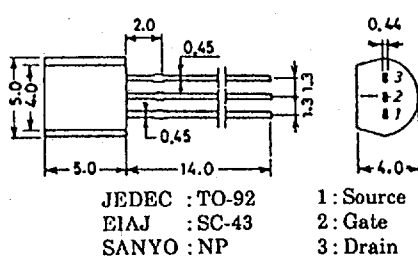
CASE OUTLINES OF LEAD FORMED SMALL SIGNAL TRANSISTORS

- All of Sanyo lead formed small signal transistor case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.

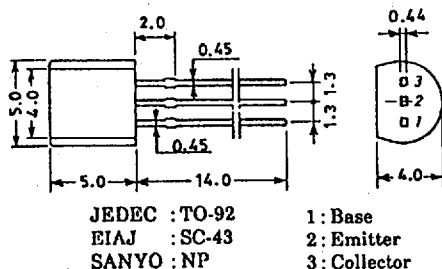
Case Outline 2003A/2003B (unit : mm)



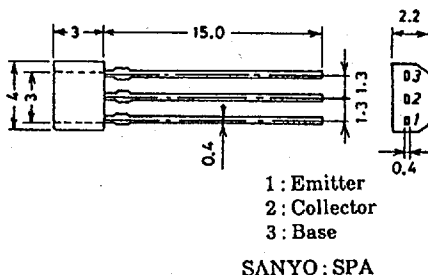
Case Outline 2019A/2019B (unit : mm)



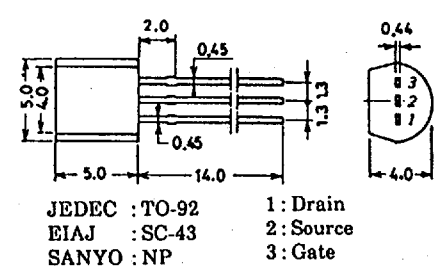
Case Outline 2004A (unit : mm)



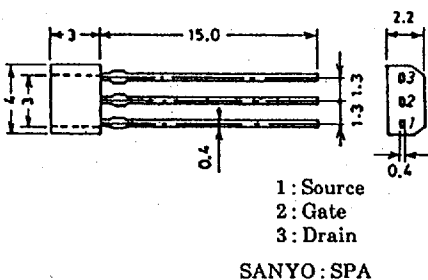
Case Outline 2033 (unit : mm)



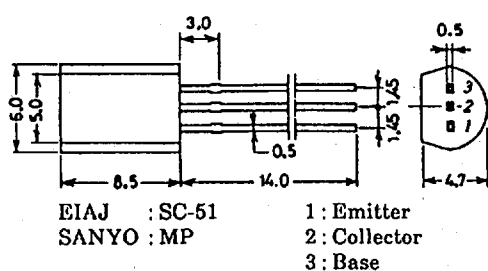
Case Outline 2005A (unit : mm)



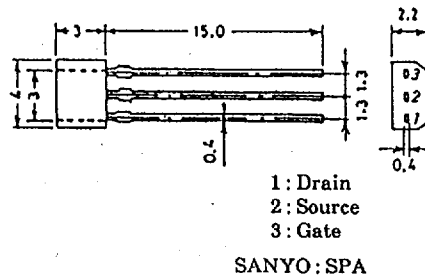
Case Outline 2034/2034A (unit : mm)



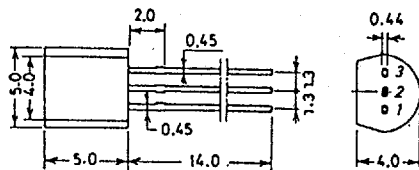
Case Outline 2006A (unit : mm)



Case Outline 2040 (unit : mm)



Case Outline 2061 (unit : mm)



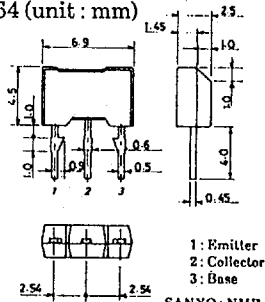
JEDEC : TO-92

EIAJ : SC-43

SANYO : NP

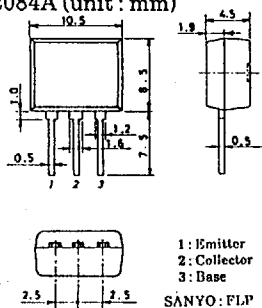
- 1: Emitter
- 2: Base
- 3: Collector

Case Outline 2064 (unit : mm)



- 1: Emitter
 - 2: Collector
 - 3: Base
- SANYO : NMP

Case Outline 2084A (unit : mm)



- 1: Emitter
 - 2: Collector
 - 3: Base
- SANYO : FLP