silicon systems®
A TDK Group Company

# SSI 32H6820
# Servo/Spindle Predriver

**Advance Information**

November 1993

## DESCRIPTION

The SSI 32H6820 is a CMOS monolithic integrated circuit housed in a 64-pin TQFP, operates from a single +5V supply and provides control signals for external FET drivers operating on 5 to 12 volt supplies. In addition to supporting disk drives with embedded servo sectors, it contains all timing and control functions necessary to start, drive, and brake a 3-phase, 4-, 8-, 12-, 16-pole brushless DC spindle motor without sensors. The circuit is controlled via the Silicon Systems standard 3-wire serial port.

## FEATURES

Servo Head Positioning Control

- **Servo control for embedded servo head positioning systems**
- **H-bridge MOSFET pre-driver for linear and rotary voice coil motor**
- **Class B linear mode and constant voltage retract mode**
- **Active head retract on power failure**

Spindle Motor Speed Control

- **3-phase 4-, 8-, 12-, 16-pole bipolar/unipolar operation without need for sensors**
- **Programmable precision speed regulation 2µs speed resolution**
- **"At speed" indication**
- **Motor peak current limiting function**
- **Pulse amplitude modulation (PAM) for bridge MOSFET drivers**
- **Dynamic braking function on power failure**

General Functions

- **Voltage fault detection for two supply voltages**
- **Low power CMOS design, two low power idle states**
- **Three wire serial control interface**
- **8 bit Digital-to-analog converter for voice coil control**
- **Available in 64-lead TQFP package**

## FUNCTIONAL DESCRIPTION

As shown in Figure 1, the SSI 32H6820 can be divided into four major sections: servo head positioning control, spindle motor speed control, digital control, and miscellaneous functions.

### SERVO HEAD POSITIONING CONTROL

The SSI 32H6820 is intended for a servo head positioner for disk drives with embedded servo sectors. The head positioning control section contains the following sections: servo position error amplifier, H-bridge MOSFET pre-driver, actuator current sense, and voltage fault detection and servo head retract.

### SERVO POSITION ERROR AMPLIFIER

The servo driver has two modes of operation, linear and retract. The retract mode is activated by a power supply failure or when the control signal RETRACT is low. Otherwise the driver operates in linear mode. During linear operation, the microcontroller acquires servo burst amplitudes and analyzes them to establish a position error signal. The microcontroller develops a digital error signal which is sent to the 8-bit D/A converter (with output ERRDAC and reference ERRREF) and is applied to an amplifier whose three connections, ERRM, ERRP and ERR, are available externally. External R-C components may be used to establish the gain and bandwidth of this amplifier. Additional analog input via SWIN may be provided to this amplifier by setting the SWON bit in the SERVO CONTROL register.

### H-BRIDGE MOSFET PRE-DRIVER

The error signal ERR generated from the position error amplifier drives two precision differential amplifiers, each with a gain of 15. The differential amplifier outputs, AOUTA, AOUTB, AOUTC and AOUTD drive an external MOSFET bridge powered by VBRIDGE. Feedback from the MOSFET drain terminals via sense inputs SE1 and SE3 allow the differential amplifier gains to be established precisely. The voice coil actuator and a current sense resistor are connected in series between SE1 and SE3. Included in the output control circuitry is a crossover protection function which ensures class B operation by permitting only one MOSFET in each leg of the bridge to be in conduction. The crossover circuit can be adjusted for different MOSFET threshold voltages with a resistor connected to VX. The crossover

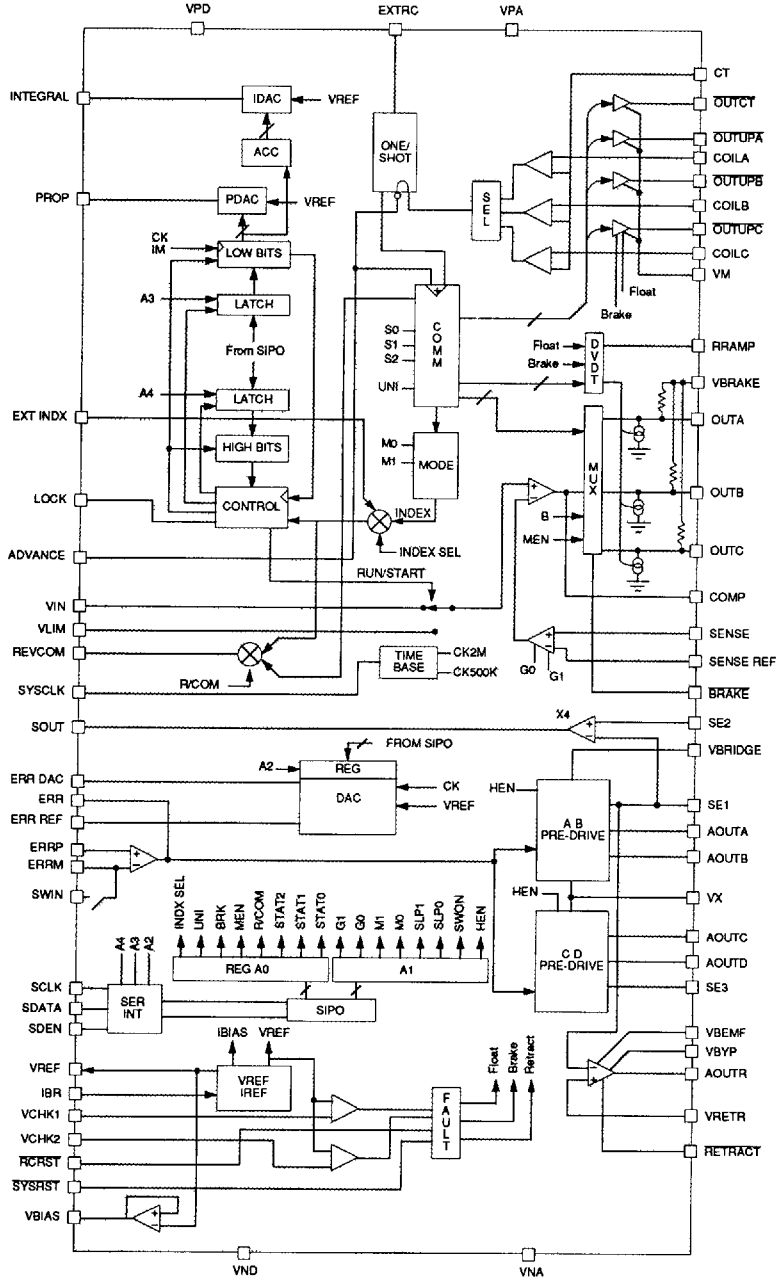



**Figure 1: SSI 32H6820 Block Diagram**

## FUNCTIONAL DESCRIPTION (continued)

### H-BRIDGE MOSFET PRE-DRIVER (continued)

circuitry can be commanded by the µP to shut down the MOSFET drivers and thus remove current to the external bridge.

### MOTOR CURRENT SENSE

Motor current is sensed by a resistor placed in series with the actuator. The voltage drop across the resistor is level-shifted and amplified by a differential amplifier with a gain of 4. The resulting signal, SOUT, is proportional to actuator current. This signal is externally fed back to the position error amplifier so that the error signal ERR represents the difference between the desired and actual actuator currents.

### VOLTAGE FAULT DETECTION AND SERVO HEAD RETRACT

During retract, a constant voltage is applied across the actuator in order to cause a constant velocity head retraction. This is accomplished by applying the voltage stored on VBYP to AOUTD and by driving AOUTR with an amplifier that monitors SE1. The amplifier is powered by VBEMF. During retract, VRETR is biased by an internal voltage reference and determines the retract voltage. At other times, power is saved by disconnecting VRETR from the voltage reference and letting it be pulled to VBEMF by a high value resistor. External components (a diode, for instance) can be connected between VRETR and ground to modify the retract voltage.

An open-drain output, $\overline{\text{SYSRST}}$, which is active low while the servo driver is in retract mode, is provided for spindle motor braking. An external R-C delay may be used to defer braking until the head is retracted. The minimum duration of $\overline{\text{SYSRST}}$ being active low is determined by the external capacitor which is connected to pin $\overline{\text{RCRST}}$.

### SPINDLE MOTOR SPEED CONTROL

In conjunction with several external components, the spindle motor speed control provides the starting, accelerating, and precise rotational speed regulation functions. The circuit will control 4-, 8-, 12-, or 16-pole brushless DC motors without the need for Hall sensors. It will operate in either bipolar or unipolar drive mode. Control, configuration, and status monitoring are handled by a companion ASIC or µP. The complete speed control loop is contained in the circuit and the µP is only required during start and to monitor status.

### SPINDLE MOTOR START-UP

Motor starting is accomplished with the µP utilizing various features contained in the motor speed control circuitry. The µP can write to the commutation counter and set it to a predetermined value with STAT0, STAT1, STAT2 bits. The counter can then be incremented with the ADVANCE pin which also excludes internal commutations when held HIGH. Bit REVCOM informs the µP on motor activity. The µP can enable the drivers with MEN and UNI bits as required.

Under µP control, initial open-loop commutation sequence is provided to the commutation logic which thereby advances and accelerates the spindle motor. The start-up process settles the motor initially by selecting the bits STAT0, STAT1, STAT2 in Register 0 to energize a proper motor winding. Motor current is enabled by setting the MEN bit in Register 0. The commutation state is advanced by raising the ADVANCE pin. The period between ADVANCE pulses will be based upon the motor and load characteristics and decreased gradually during the acceleration of the motor. The µP may look at the REVCOM pin information indicating whether the motor has achieved a sufficient speed. Once the motor has achieved a sufficient speed, ADVANCE is held low and the motor will accelerate to target speed.

Motor rotor position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back-emf at the coil in conjunction with the state of the output drivers indicates rotor position. The back-emf is compared to a reference at CT and initiates "commutation events" when the appropriate comparison is made. Commutation is the sequential switching of the drive current to the motor windings. Since the back-emf comparison event occurs prior to the time when optimum commutation should occur, it is thus required to delay actual commutation by a predetermined time after the comparison. The commutation delay is provided by a non-retriggerable one-shot circuit wherein the time delay is a function of external R-C timing components connected at EXTRC. Because commutation of the motor windings typically results in large transient voltages which could falsely indicate "commutation events," the one-shot circuit also provides a "noise filter" function which holds off retriggering further and blanks the back-emf comparison events for a period of time (approximately one half the commutation delay) after commutation (Figure 3). The commutation states are defined in Table 4.

## FUNCTIONAL DESCRIPTION (continued)

### SPINDLE MOTOR SPEED REGULATION

Motor speed regulation is accomplished with mixed analog and digital techniques, converting a motor speed error derived from a reference clock and a period counter into a voltage. The voltage translates into a motor current across the current sense resistor regulating the motor speed. The speed regulation loop consists of a period counter, proportional and integral channels, two 6-bit D/A converters and a linear transconductance amplifier.

In operation, the motor speed error is determined by measuring the period of each revolution with a 500 kHz clock signal. Period resolution is therefore 2 µs with the desired period being given by:

period = (load count + 6) • 2.0 µsec

Both register 3 and register 4 must be written, in order, via the serial data interface to accomplish writing a new period value.

The period counter is loaded with the desired count initially, and period measurement results in residual counts (ideally zero) in the period counter as it counts down during the index-to-index time interval. The residual count is fed to the proportional D/A converter (5-bit plus sign) whose output is provided at PROP. No period error will output half of VBIAS at PROP, too short a period will output a value less than half of VBIAS, and too long a period will output a value greater than half of VBIAS depending on the amount of error. When the residual count is within ±15 counts of zero, the motor is indicated as "in lock." The lower eight bits of the period counter are fed to an accumulator which adds the present period residue to the previous accumulation thus accomplishing an integrating effect to force the speed error to zero over time. The upper six bits of the accumulator are fed to the integral DAC whose output is INTEGRAL. Gross period errors will cause PROP and INTEGRAL to saturate at the appropriate extreme to achieve the maximum corrective control voltage.

The outputs at PROP and INTEGRAL are connected to VIN with an external resistor network. The outputs of the proportional DAC and Integral DAC give coefficients given by:

$$K_P = (RPS^2)/(2.35v/64)/4\pi e^{-6})$$

$$K_I = (RPS^{-1})/(2.35v/64)/(16\pi e^{-6})$$

(RPS is the desired motor speed in revolutions per second.)

The resistor values should be selected to modify the coefficients given above to values required for proper loop response based upon motor requirements. The input VIN is the non-inverting input of the linear transconductance amplifier which uses the lower driver transistor that is presently active per the commutation state. An external resistor is used to sense the current flowing through the drive transistor drain (and hence the motor coil current). The voltage across the sense resistor, the difference between SENSE and SENSEREF, is amplified by a programmable gain stage and fed to the inverting input of the transconductance amplifier. The gain of the programmable amplifier is determined by G0 and G1 bits.

### MOTOR PEAK CURRENT LIMITING

When the period error exceeds 256 counts too slow, the voltage at VLIM is selected as the control voltage in lieu of VIN. VLIM is to be used to set the motor peak current during start-up and acceleration. The motor current is limited to a value such that the voltage across the sense resistor (SENSE - SENSEREF) times the gain of the sense amplifier (5, 10, 15, 20) is equal to VLIM.

### MOTOR BRAKING

Fault conditions on power supplies and internal voltage reference generator will trigger an internal retract condition. The internal retract condition will cause all pre-driver outputs to the states which will turn the driver transistors off, allowing the motor to coast. $\overline{\text{BRAKE}}$ typically has a capacitor to ground attached and is connected to pin $\overline{\text{SYSRST}}$ via a resistor. $\overline{\text{SYSRST}}$ goes low in the retract condition, and thus $\overline{\text{BRAKE}}$ will go low after the R-C delay. When $\overline{\text{BRAKE}}$ goes low, all external N-FETs are activated to achieve dynamic braking of the motor. The circuitry for these operations is powered by voltage on VBRAKE stored on an external capacitor.

Dynamic braking can also be activated under external serial port control by setting BRK to HIGH in REG 0. During dynamic braking, the control loop is opened.

### EXTERNAL INDEX APPLICATION

Normal operation is performed with an internal index signal derived from the commutation counter (scaled via the M0 and M1 bits based upon the number of motor poles). For both an internal "index" or External Index, the period between index signals is measured as described above and used to control the PROP and INTEGRAL outputs.

## DATA CONVERSION AND SERIAL INTERFACE

An 8-bit D/A converter which runs synchronously with the internal 500 kHz clock is provided. The converter is 2's complement format (7 Fhex is positive full scale, 80 hex is negative full scale and Reset condition is 00 hex, midscale). Conversion is started by writing to the D/A register address, Register 2. The output of the D/A converter is ERRDAC and is referenced to ERREF. The output is held constant between data loads. The circuit is configured and controlled via the Serial data inputs in accordance with the standard Silicon Systems Serial interface Specifications.

Per the timing diagram (Figure 2), data are clocked into the serial port on the rising edge of SCLK. It is required that 16 data clocks be used for all transfers for proper operation. The data are loaded from the serial interface to the destination registers (controlled parameter) when SDEN is lowered signalling the end of serial data transfer.

## MISCELLANEOUS FUNCTIONS

The miscellaneous functions include generating the reference voltages VREF and VBIAS, and the voltage fault detection circuits which activate power fault retract and braking operation. A voltage fault detector which can monitor two voltage supplies is included to prevent the actuator from responding to a false error signal during a power failure. Retract mode is started when a power supply failure is sensed by the VCHK1 or VCHK2 comparators or when $\overline{\text{RETRACT}}$ is pulled low externally.

The internal bias currents for analog functions are set by an external resistor connected between IBR and ground. A 23.7 kΩ ±1% resistor should be used for proper operations.

**TABLE 1: Serial Data Format**

| | |
|---|---|
| Data bit 1 | R/$\overline{\text{W}}$ control - must be a 0, this circuit is write-only |
| Data bit 2 | Circuit ID bit - must be 1 |
| Data bit 3 | Circuit ID bit - must be 1 |
| Data bit 4 | Circuit ID bit - must be 1 |
| Data bit 5 | Register address bit 0 |
| Data bit 6 | Register address bit 1 |
| Data bit 7 | Register address bit 2 |
| Data bit 8 | Register address bit 3 - not used, 1 or 0 allowed |
| Data bit 9 | Register data bit 0 |
| Data bit 10 | Register data bit 1 |
| Data bit 11 | Register data bit 2 |
| Data bit 12 | Register data bit 3 |
| Data bit 13 | Register data bit 4 |
| Data bit 14 | Register data bit 5 |
| Data bit 15 | Register data bit 6 |
| Data bit 16 | Register data bit 7 |

**TABLE 2: Operating Modes**

| MODE | VFAULT condition | $\overline{\text{RETRACT}}$ PIN | $\overline{\text{BRAKE}}$ PIN | SLEEP BIT | HEN BIT | MEN BIT | BRK BIT | POS driver | SPINDLE driver |
|---|---|---|---|---|---|---|---|---|---|
| SLEEP (1) | X | X | X | 1 | X | X | X | float | float |
| VFAULT retract (2) | 1 | X | 1 | 0 | X | X | X | retract | float |
| VFAULT brake (3) | 1 | X | 0 | 0 | X | X | X | retract | brake |
| RETRACT | 0 | 0 | 1/0 | 0 | X | X | X | retract | float/brake |
| BRAKE | 0 | 1/0 | 0 | 0 | X | X | X | float/retract | brake |
| BRAKE Register | 0 | 1 | 1 | 0 | 1/0 | X | 1 | on/float | brake |
| IDLE | 0 | 1 | 1 | 0 | 0 | 0 | 0 | float | float |
| SPIN only | 0 | 1 | 1 | 0 | 0 | 1 | 0 | float | on |
| SERVO coast | 0 | 1 | 1 | 0 | 1 | 0 | 0 | on | float |
| RUN | 0 | 1 | 1 | 0 | 1 | 1 | 0 | on | on |

(1) All analog circuits off
(2) Initiated by low power supply voltage
(3) Vfault followed by RC delay from $\overline{\text{SYSRST}}$ to $\overline{\text{BRAKE}}$

## REGISTER DESCRIPTIONS

The SSI 32H6820 contains five 8-bit internal registers which provide control and option select. Writing to an address other than 0 to 4 will have no effect.

**TABLE 3: Internal Registers**

**ADDRESS 0**

| BIT | NAME | FUNCTION |
|---|---|---|
| 0 | STAT0 | LSB of commutation state counter preset value - Refer to Table 4. |
| 1 | STAT1 | Commutation state counter preset value. |
| 2 | STAT2 | MSB of commutation state counter preset value. |
| 3 | R/COM | Selects REVCLK (once per revolution) when set low or COMMU when set high as output on pin REVCOM. |
| 4 | MEN | Motor enable. Active high enables spindle motor drive. Reset to low on power on. |
| 5 | BRK | BRAKE function when set high. Spindle lower drivers full on with no current limiting. |
| 6 | UNI | Selects UNIPOLAR mode, upper spindle drivers off, $\overline{CT}$ driver on (low). |
| 7 | INDX_SEL | Selects external index when set high. |

**ADDRESS 1**

| | | |
|---|---|---|
| 0 | HEN | Enable head driver outputs. Reset to low on power on. |
| 1 | SWON | Close switch between ERR and SWIN. Set open on power on reset. |
| 2 | SLP0 | Sleep mode control bit. When set high, head positioner and motor analog circuits are inactive with drivers off. Miscellaneous circuitry is still active. |
| 3 | SLP1 | Full SLEEP mode select. Overrides SLP0 bit. All analog circuits de-biased and internal clocks are off. Only the serial data port is operable. |
| 4 | M0 | Spindle motor pole configuration mode. See below. |
| 5 | M1 | Spindle motor pole configuration.<br>M0 = 0, M1 = 0 for 4 poles<br>M0 = 1, M1 = 0 for 8 poles<br>M0 = 0, M1 = 1 for 12 poles<br>M0 = 1, M1 = 1 for 16 poles |
| 6 | G0 | Spindle motor current sense amplifier gain control. |
| 7 | G1 | Spindle motor current sense amplifier gain control.<br>G0 = 0, G1 = 0 for gain of 5<br>G0 = 1, G1 = 0 for gain of 10<br>G0 = 0, G1 = 1 for gain of 15<br>G0 = 1, G1 = 1 for gain of 20 |

## REGISTER DESCRIPTIONS (continued)

**ADDRESS 2**

| BIT | NAME | FUNCTION |
|---|---|---|
| 0 | DAC0 | DAC LSB |
| 1 | DAC1 | DAC data bit 1 |
| 2 | DAC2 | DAC data bit 2 |
| 3 | DAC3 | DAC data bit 3 |
| 4 | DAC4 | DAC data bit 4 |
| 5 | DAC5 | DAC data bit 5 |
| 6 | DAC6 | DAC data bit 6 |
| 7 | DAC7 | DAC MSB |

**ADDRESS 3**

| | | |
|---|---|---|
| 0 | CNT0 | Period counter LSB |
| 1 | CNT1 | Period counter bit 1 |
| 2 | CNT2 | Period counter bit 2 |
| 3 | CNT3 | Period counter bit 3 |
| 4 | CNT4 | Period counter bit 4 |
| 5 | CNT5 | Period counter bit 5 |
| 6 | CNT6 | Period counter bit 6 |
| 7 | CNT7 | Period counter bit 7 |

**ADDRESS 4**

| | | |
|---|---|---|
| 0 | CNT8 | Period counter bit 8 |
| 1 | CNT9 | Period counter bit 9 |
| 2 | CNT10 | Period counter bit 10 |
| 3 | CNT11 | Period counter bit 11 |
| 4 | CNT12 | Period counter bit 12 |
| 5 | CNT13 | Period counter bit 13 |
| 6 | CNT14 | Period counter bit 14 |
| 7 | CNT15 | Period counter MSB - Always load 0 in this bit |

**TABLE 4** (See Table 2)

| STATE | STAT 2 | STAT 1 | STAT 0 | OUTA | OUTB | OUTC | $\overline{\text{OUTUPA}}$ | $\overline{\text{OUTUPB}}$ | $\overline{\text{OUTUPC}}$ | REVCOM (COMMU SELECTED) |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | OFF | ON | OFF | ON | OFF | OFF | 1 |
| 1 | 0 | 0 | 1 | OFF | OFF | ON | ON | OFF | OFF | 0 |
| 2 | 0 | 1 | 0 | OFF | OFF | ON | OFF | ON | OFF | 1 |
| 3 | 0 | 1 | 1 | ON | OFF | OFF | OFF | ON | OFF | 0 |
| 4 | 1 | 0 | 0 | ON | OFF | OFF | OFF | OFF | ON | 1 |
| 5 | 1 | 0 | 1 | OFF | ON | OFF | OFF | OFF | ON | 0 |
| | 1 | 1 | 0 | No load for | | | | | | |
| | 1 | 1 | 1 | 110 or 111 | | | | | | |

## PIN DESCRIPTION

### POWER SUPPLIES

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VPA | P | Analog +5V supply. |
| VPD | P | Digital +5V supply. VPA and VPD must be within 0.3V of each other at all times. |
| VNA | P | Analog ground. |
| VND | P | Digital ground. |

### HEAD POSITIONER MOSFET DRIVER AND VOLTAGE FAULT DETECTION

| | | |
|---|---|---|
| ERRM | I | Error Amplifier Inverting Input - Inverting input to the position error amplifier of the MOSFET pre-driver. |
| ERRP | I | Error Amplifier Non-inverting Input - Non-inverting input of the error amplifier. Typically connected to ERRREF pin directly. |
| SWIN | I | This input is shorted to ERRM when the bit SWON is set HIGH. SWIN floats otherwise. |
| ERR | O | Acceleration Error - Position error amplifier output. This signal is amplified by the MOSFET drivers and applied to the actuator through an external MOSFET H-bridge as follows: |
| | | SE3-SE1 = 30 (ERR-VREF) |
| ERRDAC | O | DAC output pin, referenced to ERREF. |
| ERREF | O | Reference voltage for DAC output. Connected to non-inverting input of error amplifier. |
| AOUT(A,C) | O | PFET Driver - Drive signals for P-channel MOSFETs connected between VBRIDGE and the voice coil actuator. Crossover protection circuitry ensures that the external P- and N-channel FETs driven by AOUT(A,C) and AOUT(B,D) are never enabled simultaneously. |
| AOUT(B,D) | O | NFET Driver - Drive signals for N-channel MOSFETs connected between the current sense resistor and the voice coil actuator. |

## PIN DESCRIPTION (continued)

### HEAD POSITIONER MOSFET DRIVER AND VOLTAGE FAULT DETECTION (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VBRIDGE | I | Bridge Voltage Supply - Pin for connection to the voltage supply provided to external power transistors. |
| VRETR | I | Retract Voltage - In head retract mode this voltage is applied across the actuator to force the heads to move at a constant speed. |
| AOUTR | O | Head Retract Amplifier Output - Voltage output to drive an external head retract circuit. |
| SE1, SE3 | I | Motor Voltage Sense Input - These inputs provide feedback to the internal MOSFET drive amplifier. |
| SE2 | I | Motor Current Sense Input - Non-inverting input to the current sense differential amplifier. It should be connected to an external current sense resistor. The inverting input of the differential amplifier is SE1. |
| SOUT | O | Motor Current Sense Output - This output provides a voltage proportional to the voltage drop across the external current sense resistor as follows: |
| | | SOUT-ERREF = 4 (SE2-SE1) |
| VX | O | Crossover Protection Voltage - The current source output at VX is converted to a voltage with an external resistor. The value of the resistor should be adjusted so that VX is less than the specified minimum threshold voltage of the MOSFET bridge. |
| VBYP | I | Bypass Voltage Supply - The VBRIDGE voltage is stored on this node for use during retract. |
| VCHK1, VCHK2 | I | Fault Voltage Comparator Inputs - Voltage inputs for the low voltage comparators. These two inputs should be connected to separate external resistor dividers. Each resistor divider divides its corresponding supply voltage to a proper value which is comparable with the internal voltage reference at 2.35 volts. |
| VREF | O | Internal Voltage Reference - A voltage reference at 2.35 volts is generated internally for the DC reference level throughout the device. Due to limited drive capability provided with on-chip voltage reference, this pin shall be used only for connecting an external bypass capacitor of 10 μF. |
| IBR | O | Bias Current Reference - Pin for connection to an external resistor (from VNA) to establish a reference current for bias currents used in analog circuits. |
| $\overline{\text{RETRACT}}$ | I | Retract Input - When set low, the head positioner is put into retract mode. |
| SYSRST | O | Active low, open drain output signal which indicates that a voltage fault has occurred or $\overline{\text{RCRST}}$ pin has been pulled low externally. |
| RCRST | I | An external R/C network at this pin will stretch short (internally detected) voltage fault pulses and set a minimum $\overline{\text{SYSRST}}$ pulse width. When this pin is pulled low externally, $\overline{\text{SYSRST}}$ will go low and the device will enter the retract mode. |

**SPINDLE MOTOR SPEED CONTROL**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| EXTINDX | I | External Index Input - This TTL compatible input, when selected via the INDEXSEL bit, is used to provide a once-per-revolution indication of angular position and speed to the device. The falling edge of EXTINDX is the reference. |
| SYSCLK | I | System Clock Input - A 4 MHz, TTL compatible input is provided to derive internal timing signals. |
| ADVANCE | I | Input signal used to increment the commutation state counter. When held high, the commutation counter is prevented from incrementing due to back-emf signals from the motor. |
| EXTRC | I | Pin for connection to a resistor (from VPD) and a capacitor (from VND) to provide the commutation delay. The commutation delay is 0.56 R-C. After the commutation delay, the timing block provides a noise rejection interval to reject transients on the motor coils due to commutations. This noise rejection is an additional 0.29 R-C. The total time (commutation delay and noise rejection internal) must be less than a commutation cycle time. |
| BRAKE | I | Spindle Braking Enable - This input, when active low, dynamically brakes the spindle motor. A resistor (from $\overline{\text{SYSRST}}$) and a capacitor (from VND) are connected to this pin to provide a delay between the initiation of fault-induced head retraction and motor braking. R-C are selected such that 1.2 R-C is equal to the maximum time required for head retraction. |
| VBIAS | O | Buffered Bias Voltage - VBIAS is buffered VREF to be used for VLIM and motor speed setting bias. (In some applications, it is necessary to create an "offset" to the speed control loop to obtain proper speed regulation.) |
| PROP | O | Proportional Channel D/A Output - The proportional channel output is the least significant 5 bits plus sign of the period measuring counter. The LSB signifies a 2 µs period variation. |
| INTEGRAL | O | Integral Channel D/A Output - The integral channel output is the most significant 6 bits of an 8-bit accumulator. The accumulator adds the least 8 bits of the period measurement counter to the previous value obtained from prior period measurements and accumulations. |
| VIN | I | Speed Control Voltage Input - The combination of external driver transistors and internal pre-driver circuits forms a transconductance amplifier which will define the motor current in relation to VIN. In conjunction with the SENSE input and the gain setting for the sense amplifier, the transconductance gain is given by:<br>gm=IMOTOR/VIN=1/(RSENSE•Gain)<br>where IMOTOR is the current flowing through the spindle motor coils, RSENSE the current sense resistor and Gain is the gain of the current sense amplifier as set by the gain control bits G0 and G1. |
| VLIM | I | Current Limit Setting Voltage - The spindle motor current will be limited to a value determined by RSENSE, VLIM and Gain such that Imax=VLIM/(RSENSE•Gain). VLIM is used whenever the spindle speed is measured to be 256 counts too slow. |

## PIN DESCRIPTION (continued)

### SPINDLE MOTOR SPEED CONTROL (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| SENSE | I | Current Sense Amplifier Non-inverting Input - The external driver transistor sources are connected to a current sense resistor RSENSE to monitor motor current. The device will control the voltage across the sense resistor to match either VIN (during normal operation) and VLIM (during acceleration) such that: (VSENSE - VSENSEREF) • Gain = VLIM or VIN |
| SENSEREF | I | Current Sense Amplifier Reference Input - Pin for a Kelvin connection to the ground side of the sense resistor. |
| OUT(A,B,C) | O | Pre-driver Outputs - These pre-driver outputs drive the gates of external power NFETs. |
| $\overline{\text{OUTUP}}$(A,B,C) | O | Upper Pull-up Outputs - These pre-driver outputs drive the gates of external power PFETs. They are configured as open-drain outputs with internal 10 kΩ pull-up resistors to VM. |
| $\overline{\text{OUTCT}}$ | O | Center Tap Pre-driver - This output drives an external PFET driver which connects the motor center tap to VM for unipolar drive applications. $\overline{\text{OUTCT}}$ has the same characteristics as $\overline{\text{OUTUP}}$ (A,B,C) and is enabled via the UNI bit. |
| VM | I | Spindle motor upper driver power supply pin. |
| VBRAKE | I | This pin provides the power for spindle motor braking upon power loss. An external diode from VM is used to charge an energy storage capacitor (10 μF, typical) which provides gate drive voltage for the external NFETs. |
| RRAMP | I | An external resistor (to VPD) sets the lower driver turn-off characteristics for noise reduction, 100 KΩ typical. |
| VBEMF | I | Back-emf Voltage - A power diode voltage drop from the system power supply is defined as VBEMF. For "power-fail" retract and braking, VBEMF is connected to VM and the external PFET sources. During power failure, the diodes in the PFETs rectify the motor voltage for head retract power. |
| COIL(A,B,C) | I | Back-emf Inputs - Inputs to be connected to their respective motor coils and the center tap for sensing generated back-emf voltages. The device uses the back-emf voltages to determine the rotor position and effect commutation. |
| CT | I | Center tap of motor used as reference for back-emf comparison. |
| REVCOM | O | Output selected by R/COM bit in REG 0 to be either REVCLK (once per revolution) or COMMU, the LSB of the commutation state counter. |
| LOCK | O | Output true indicates rotational period of motor is within ± 30 μs of desired value. |
| COMP | I | Compensation capacitor for the spindle transconductance loop. Typical value 0.01 μF to 0.1 μF. |

### SERIAL DATA INTERFACE

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| SDEN | I | Serial Data Enable, active high. SDEN is raised prior to serial data input and lowered after 16 SCLK pulses. |
| SCLK | I | Serial Data clock, falling edge clocks serial data into circuit. |
| SDATA | I | Serial Data input consisting of 8-bit mode and address word followed by 8-bit data word (MSB last). The first bit clocked in is the mode bit which for this circuit is Write mode only, (write a zero). |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect reliability.

| PARAMETER | | RATING |
|---|---|---|
| Voltage applied to VPA, VPD | VDD | 0.1 to 14.0 |
| Voltage applied to VBRIDGE | VBRIDGE | 0.1 to 14.0 |
| Voltage applied to VBYP | VBYP | 0.1 to 14.0 |
| Voltage applied to VBEMF | VBEMF | 0.1 to 18 |
| Voltage applied to VM | VM | 0.1 to 14.0 |
| Voltage applied to VBRAKE | VBRAKE | 0.1 to 14.0 |
| VBEMF current if VBEMF>18V | IBEMF | 5.0 |
| Signal pins | VMAX | -0.3 to VDD + 0.3 |
| Storage temperature | Tstg | -65 to 150 |
| Lead temperature | Tlead | 300 |

### OPERATING ENVIRONMENT LIMITATIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply where the device is operating outside these limits.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply voltage applied at VPA,VPD | VDD | | 4.5 | - | 5.5 | V |
| Bridge voltage applied at VBRIDGE, VM | VBRIDGE VM | | 4.5 | - | 13.2 | V |
| Ambient temperature | Ta | | 0.0 | - | 70.0 | °C |
| System clock | Fc | | 3.92 | 4 | 4.08 | MHz |
| Capacitive load | CL | | | | 100 | pF |
| digital outputs | | | | | | |
| Analog input impedance | Rin | | 100 | - | - | kΩ |

## ELECTRICAL SPECIFICATIONS (continued)

### OPERATING ENVIRONMENT LIMITATIONS (continued)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Cin | | - | - | 20 | pF |
| Load on analog outputs | Rout | | 10 | - | - | kΩ |
| | Cout | | - | - | 40 | pF |
| Bias resistor | RBIAS | 23.7 kΩ | | ±1 | | % |

### DC CHARACTERISTICS

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. Positive current is defined as entering the device. Minimum and maximum are based upon the magnitude of the number.

| | | | | | | |
|---|---|---|---|---|---|---|
| Supply current | IDD | VDD = 5.5V | - | - | 30 | mA |
| | | SLP0 | - | - | 15 | mA |
| | | SLP1 | | | 50 | µA |
| Supply current on VBRAKE | IBRK | VBRAKE = 12V<br>VDD = 0V | - | - | 25 | µA |
| Supply current on VBYP | IBYP | VBYP = 12V | - | - | 25 | µA |
| Output logic 1 | Voh | Ioh = -0.4 mA<br>VDD = 4.5V | 2.4 | - | - | V |
| Output logic 0 | Vol | Iol=1.6 mA<br>VDD=4.5V | - | - | 0.4 | V |
| Input logic 1 | Vih | VDD=4.5V | 2.0 | - | - | V |
| Input logic 0 | Vil | VDD=4.5V | - | - | 0.8 | V |
| Input logic 1 current | Iih | Vih=5.5V<br>VDD=5.5V | - | - | 10 | µA |
| Input logic 0 current | Iil | Vil=0.0<br>VDD=5.5V | - | - | -10 | µA |
| Input capacitance | Cin | | - | - | 10 | pF |

## FUNCTIONAL CHARACTERISTICS

### Head Positioner MOSFET Driver

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VRETR voltage | VBEMF = 3V | 0.3 | - | 0.9 | V |
| | VBEMF = 12V | 0.4 | - | 1.2 | V |
| Retract offset | VBEMF = 3V<br>VRETRACT = 0.5V | -70 | | 50 | mV |
| | VBEMF = 6V<br>VBYP = 4V to 13V | -70 | | 70 | mV |
| | VBEMF = 12V<br>IAOUTR < 1mA | -150 | - | 150 | mV |
| Voh at AOUTR | Ioh = -1 mA<br>VBEMF = 4V<br>VBYP = 4V | 1.5 | - | - | V |
| | VBEMF = 3V<br>VBYP = 4V | 1.3 | - | - | V |
| Leakage current at AOUTR | $\overline{\text{RETRACT}}$ = LOW<br>AOUTR = 0V to 14V | - | - | 1 | µA |
| Voh at AOUTA, AOUTC | Ioh = -1 mA | VBRIDGE -1.5 | | | V |
| | Ioh = -1 µA | VBRIDGE -0.1 | | - | V |
| Vol at AOUTA, AOUTC | Iol = 10 µA | - | | 1 | V |
| Voh at AOUTB | Ioh = -10 µA | VBRIDGE -0.5 | | - | V |
| Voh at AOUTD | Ioh = -10 µA | VBYP -0.5 | | - | V |
| Vol at AOUTB, AOUTD | Iol = 1 mA | - | - | 1 | V |
| | Iol = 10 µA | | - | 0.2 | V |
| Input offset at SOUT | | - | - | ±3 | mV |
| SOUT/(SE1-SE2) | | 3.9 | - | 4.1 | V/V |
| SE1/ERR, SE3/ERR | | 14.0 | | 15.4 | V/V |
| ERRAMP input offset | | - | - | ±10 | mV |
| ERRAMP gain | | | 1000 | - | V/V |
| Output crossover time PFET VTH = -2V<br>CL = 600 pF at AOUTA,C NFET VTH = 2V<br>CL = 150 pF at AOUTB,D RX = 50 kΩ | | - | - | 45 | µs |
| Input impedance at SE1, SE2, SE3 | | 20 | - | - | kΩ |
| Output resistance at SOUT | | - | - | 350 | Ω |
| Analog switch on-resistance at SWIN | | - | - | 600 | Ω |
| Output resistance at ERR | | - | - | 100 | Ω |
| Output current from VX | | | TBD | | µA |

## ELECTRICAL SPECIFICATIONS (continued)

### FUNCTIONAL CHARACTERISTICS (continued)

**Voltage Reference and Voltage Fault Circuit**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VPA voltage for $\overline{SYSRST}$ & $\overline{RCRST}$ in operation | | 2.0 | | - | V |
| On resistance at $\overline{RCRST}$ VPA > 3.5V VBRAKE > 4V | | - | - | 800 | Ω |
| VPA > 3.5V VBRAKE > 10V | | - | - | 550 | Ω |
| $\overline{RCRST}$ input threshold VBRAKE = 4V | | 0.8 | - | 2.0 | V |
| IBR voltage w.r.t. VREF | | -80 | - | 20 | mV |
| Output voltage at VREF \|IL\| < 10 µA | | 2.28 | 2.35 | 2.42 | V |
| VCHK1, VCHK2 comparator offset | | 2.25 | - | 2.45 | V |

**Spindle Motor Speed Control**

| | | | | | |
|---|---|---|---|---|---|
| SYSCLK duty cycle | | 40 | - | 60 | % |
| EXTINDX pulse width | | 200 | - | - | ns |
| Advance pulse width | | 3 | - | - | µs |
| Timing resistor at EXTRC | | 0.01 | - | 10 | MΩ |
| Timing capacitor at EXTRC | | 100 | - | - | pF |
| Delay time variation relative to T0* | | - | - | ±5 | % |
| Vil at $\overline{BRAKE}$ | VBRAKE = 5V | 0 | - | 0.8 | V |
| Vih at $\overline{BRAKE}$ | VBRAKE = 5V | 2.0 | - | - | V |
| Output voltage swing at PROP & INTEGRAL | Iout < 0.1 mA | 0 | - | VBIAS ±5% | V |
| DAC step size at PROP, INTEGRAL | | 33 | - | 40 | mV |
| Output impedance at PROP, INTEGRAL | 0.5V < Vout < 2.0V Iout = 0.1 mA | - | - | 300 | Ω |
| VBIAS output w.r.t. VREF | | -50 | - | 25 | mV |
| Input voltage at VIN & VLIM | | 0 | - | 2.35 | V |
| Input leakage current at VIN & VLIM | | - | - | ±1 | µA |

* NOTE: T0 is the commutation delay and is given by the relationship T0 = 0.56RC. Suggested value for C would be 470 to 1000 pF. An external R and C must be provided such that T0 is greater than 10 µs (R = 22 kΩ, C = 470 pF).

**Spindle Motor Speed Control** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Output resistance at $\overline{\text{OUTUP}}$ (A,B,C) & $\overline{\text{OUTCT}}$ | Output HIGH pulled to VM | 5 | - | 20 | kΩ |
| Vol at OUTUP (A,B,C) & OUTCT | Iout = 3mA VM = 13.2V | | - | 1.0 | V |
| Voh, OUT (A,B,C) | Vpd = 5V, Vm ≥ 6V Iout = -50 µA | 4.5 | - | | V |
| Vol at OUT (A,B,C) | Iout = 1 mA | | - | 1.0 | V |
| Input voltage at SENSE | Av = 5 | 0.0 | | 0.5 | V |
| Input voltage at SENSEREF | | 0.0 | - | 0.05 | V |
| Input leakage current at SENSE | 0.0V < Vin < 1.0V | - | - | ±10 | µA |
| Input leakage current at SENSEREF | 0.0V < Vin < 0.05V | -200 | - | 10 | µA |
| Input capacitance at SENSE & SENSEREF | | - | - | 20 | pF |
| Gain variation | Av = 5,10,15,20 | - | - | ±10 | % |
| Input impedance at COIL(A,B,C) | -0.3V < Vin < 15V | 100 | - | - | kΩ |
| Input capacitance at COIL(A,B,C) | | - | - | 10 | pF |
| Input impedance at CT | | 30 | - | - | kΩ |
| Input capacitance at CT | | - | - | 10 | pF |
| LOCK indication range | | -30 | - | +30 | µs |
| Speed resolution | | | 2 | | µs |

The motor speed control loop can be described as: H(s)=Kp+Ki/s

The transconductance gain from VIN or VLIM to the steady-state current flowing through the motor is given by G = 1/(RSENSE • AV)

**Error D/A Converter**

| | | | | | |
|---|---|---|---|---|---|
| ERRDAC full-scale voltage swing w.r.t ERREF | | - | ±(VREF/2) | - | V |
| Resolution | | - | 8 | - | Bits |
| Conversion time* | | - | 4.0 | | µs |
| LSB voltage | | - | VREF/256 | | mV |
| Output voltage at ERREF | | 1.568 | 1.616 | 1.664 | V |
| ERRDAC offset w.r.t. ERREF | | - | - | ±5 | mV |
| Differential linearity error | | - | - | ±0.75 | LSB |
| Relative accuracy** | | - | - | ±1.0 | LSB |
| Power supply sensitivity | | - | - | ±0.5 | LSB |

## ELECTRICAL SPECIFICATIONS(continued)

**Error D/A Converter** (continued)

*A maximum of 4 µs of latency between a conversion request and the actual start of conversion must be added to this conversion time of 4 µs to calculate the total delay time from a conversion request to the completion of conversion.

**Relative accuracy is the deviation of the analog value at any code (relative to the full analog range of the D/A transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range has been calibrated.

**Serial Data Interface**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| SDEN enable to SCLK delay | Tsens | | 35 | | | ns |
| SDEN hold past SCLK | Tsensh | | 40 | | | ns |
| SDATA setup | Tds | | 15 | | | ns |
| SDATA hold time | Tdh | | 15 | | | ns |
| SDATA address word to data word | Tad | | 40 | | | ns |
| SCLK cycle time | Tc | | 100 | | | ns |
| SCLK width low | Twcl | | 40 | | | ns |
| SCLK width high | Twch | | 40 | | | ns |

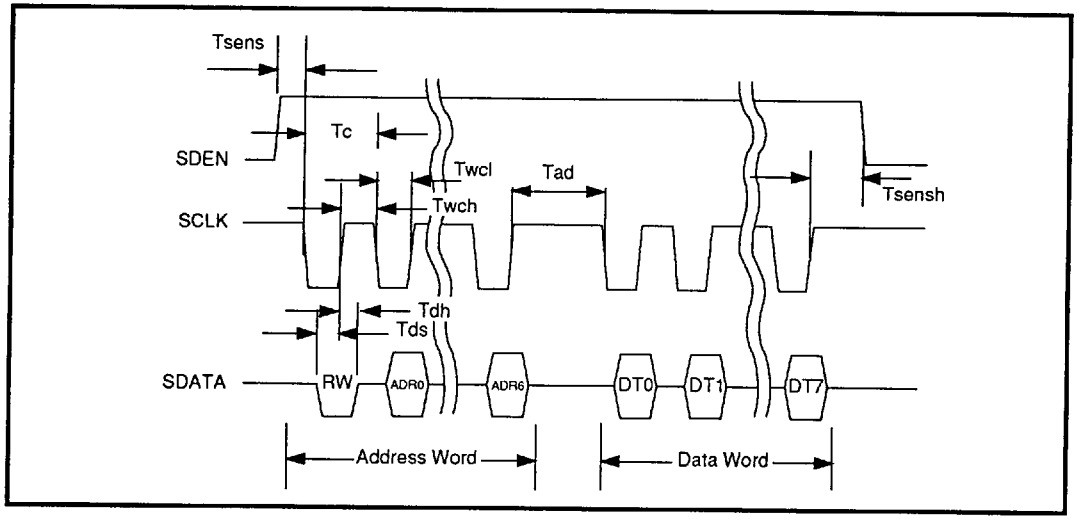



**FIGURE 2: Timing Diagram**

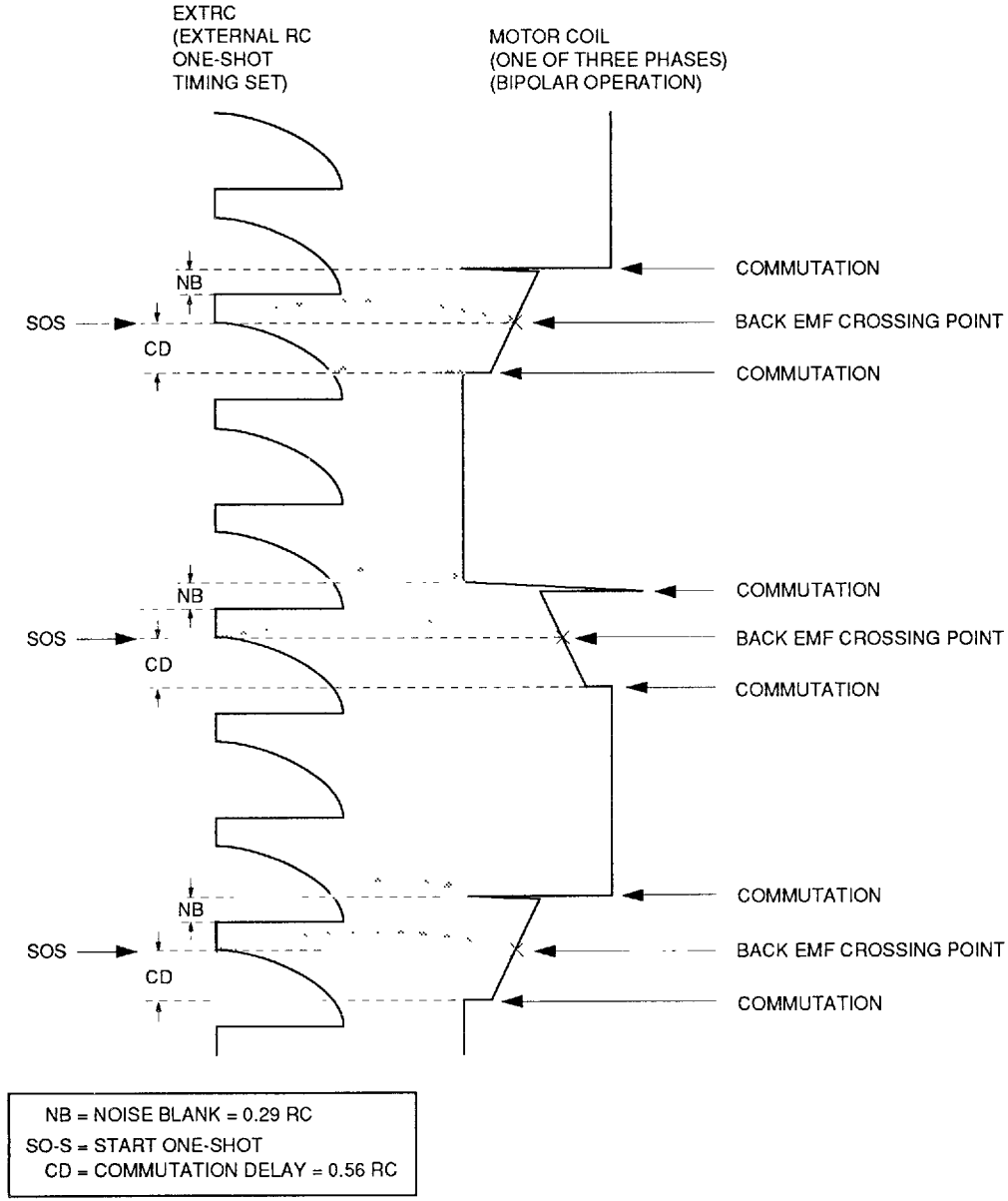
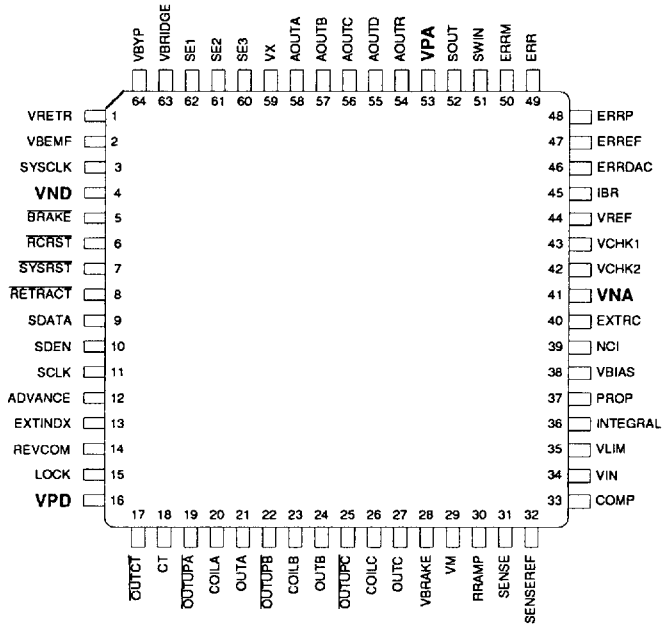



**FIGURE 3: One-Shot Commutation Delay Timing Diagram**

# SSI 32H6820
# Servo/Spindle
# Predriver

## PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION. Use handling procedures necessary for a static sensitive component.




**64-Lead TQFP**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914