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A TDK Group Company

SSI 32C9020
SCSI Combo Controller
48 Mbit/s; single bit NRZ interface

Advance Information

January 1994

DESCRIPTION

The SSI 32C9020 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build an SCSI disk drive. The circuitry of the SSI 32C9020 includes a complete SCSI target interface, an advanced buffer manager, a high performance disk formatter and an 88-bit Reed-Solomon ECC with fast "on-the-fly" hardware correction. The SSI 32C9020 provides maximum performance while minimizing micro controller intervention.

The SSI 32C9020 is capable of concurrent transfers of up to 48 megabits per second on the disk interface and 10 megabytes per second across the SCSI bus. In addition, on-the-fly error corrections and micro controller accesses to the buffer memory will not degrade the throughput during transfers.

The SSI 32C9020 is one of a family of Silicon Systems' single chip disk controllers which support a wide range

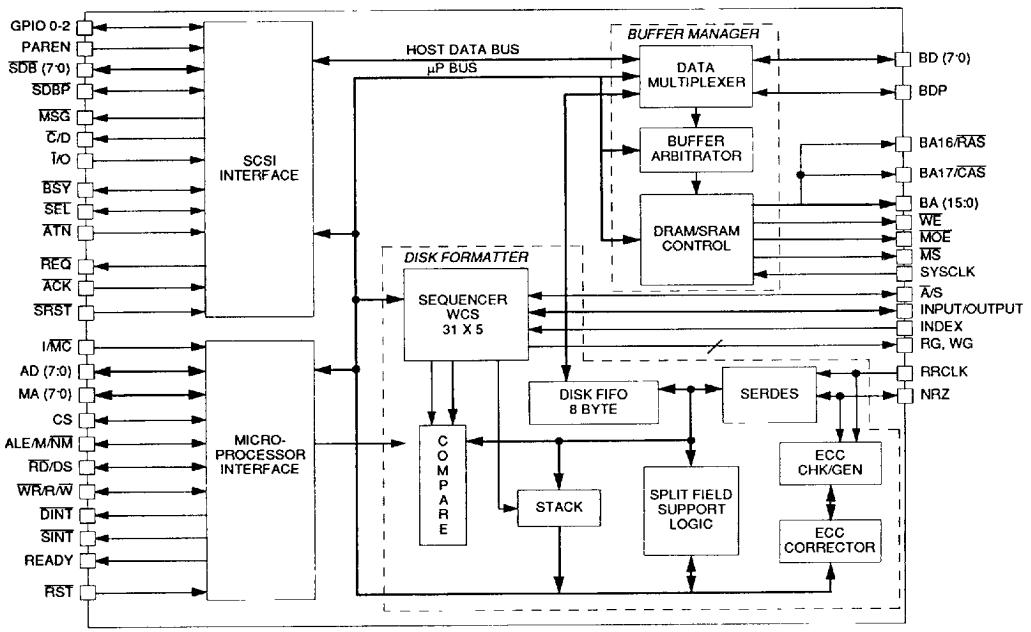
(continued)

FEATURES

- **SCSI Bus Interface**
  - **Full SCSI-2 Compatibility**
  - **Direct bus interface logic with on-chip 48 mA drivers**
  - **Synchronous transfer rates up to 10 megabytes per second**
  - **Asynchronous transfer rates up to 5 megabytes per second**
  - **Parity generation and checking**
  - **Auto Command Mode (ACM) SCSI state machine performs high level SCSI sequences without microprocessor intervention**
  - **Four level ACM command FIFO supports automatic execution of multiple ACM commands**

(continued)

BLOCK DIAGRAM



DESCRIPTION (continued)

of device interfaces. The SSI 32C9022 provides the same basic capabilities as the SSI 32C9020 but has a dual NRZ disk interface. Other family members support AT and PCMCIA interfaces. All members are based on a common architecture allowing major portions of firmware to be reused. The Silicon Systems' chip family is illustrated in the hierarchy chart shown in Figure 1.

The high level of integration within the SSI 32C9020 represents a major reduction in parts count. When the SSI 32C9020 SCSI Controller is combined with the SSI 32R2010 Read/Write device, the SSI 32P3000 Pulse Detector, the SSI 32D5391 Data Synchronizer with 1,7 ENDEC, the 32H4631 Servo and Motor Speed Controller, an appropriate micro controller and memory, a complete, cost efficient, high performance intelligent drive solution is created.

FEATURES (continued)

- Hardware support for automatic handling of SCSI-2 command queuing
- Automatic SCSI CDB size determination
- Automatic SCSI Disconnect and Reconnect
- Sixteen byte data FIFO between SCSI channel and Buffer Manager
- Buffer Manager
  - Direct support of DRAM or SRAM
  - SRAM throughput to 20 megabytes per second
  - SRAM size up to 256k bytes
  - DRAM throughput to 17.78 megabytes per second
  - DRAM size up to 1 megabyte
  - Programmable memory timing
  - Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1 megabyte
  - Dedicated host, disk and microprocessor address pointers
  - Internal buffer protection circuit provides buffer integrity
- Disk Formatter
  - NRZ Data Rates to 48 megabits/s
  - Automatic multi-sector transfer
  - Header or microprocessor based split data field support
  - Advanced sequencer organized in 31 x 5 bytes
  - 88-bit Reed Solomon ECC with "on-the-fly" fast hardware correction circuitry

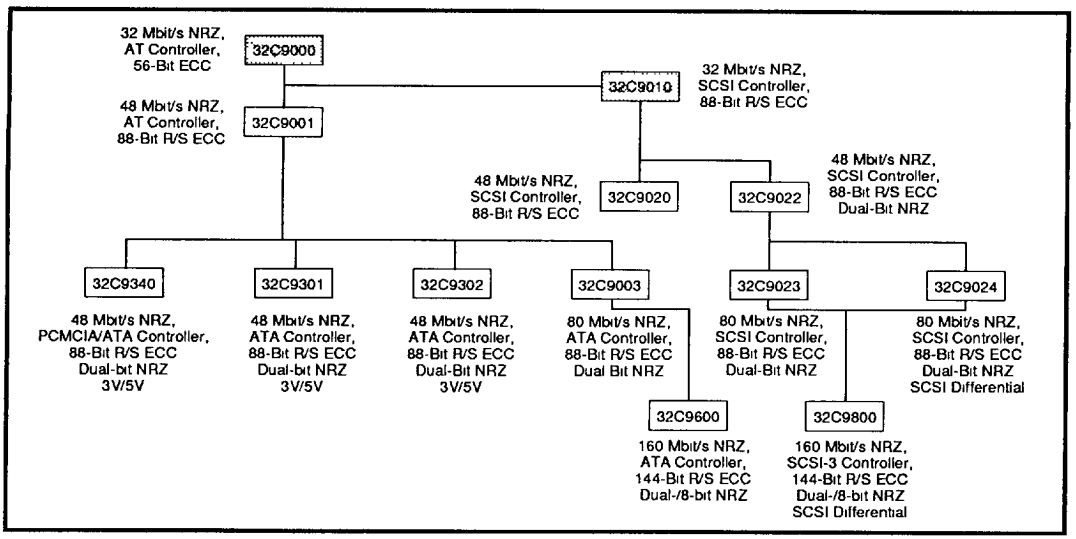


FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy

  - Capable of correcting up to four 10-bit symbols in error
  - Guaranteed to correct one 31-bit burst or two 11-bit bursts
  - Hardware on-the-fly correction of either an 11- or 31-bit single burst error within a half sector time
  - Detects up to one 51-bit burst or three 11-bit bursts
- Microprocessor Interface
  - Supports both multiplexed or non-multiplexed microprocessors
  - Separate or combined host and disk interrupts
  - Programmable wait state insertion
- Other Features
  - Internal power down mode
  - Available in 100-pin QFP

FUNCTIONAL DESCRIPTION

The SSI 32C9020 contains the following four major functional blocks:

Microprocessor Interface

SCSI Interface

Disk Formatter

Buffer Manager

The Microprocessor Interface allows the local microprocessor access to all of the SSI 32C9020 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers can control all activities of the SSI 32C9020. The microprocessor can elect to perform SCSI and/or disk operations directly, or it can enable the advanced features of the SSI 32C9020 which can perform all typical operations automatically.

The SCSI Interface block handles all SCSI activities. The SCSI interface includes 48 mA drivers allowing for direct connection of the SSI 32C9020 to the SCSI bus. The SCSI interface logic includes Auto Command Mode (ACM) logic, an advanced state machine capable of handling a variety of complex SCSI sequences without microprocessor intervention. The microprocessor can queue up to four ACM commands into the ACM Command FIFO to create even more sophisticated command sequences. The SCSI block interfaces directly with the Buffer Manager via an internal speed matching FIFO. This FIFO, plus the bandwidth capabilities of the Buffer Manager guarantee sustained full speed transfers across the SCSI bus. The high level of automation of the ACM minimizes SCSI bus overhead. The net result is maximized performance with minimum SCSI bus band width utilization.

The Disk Formatter performs the serialization and deserialization of data. It provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the Disk Formatter is an advanced programmable sequencer which is flexible enough to interface to a wide variety of read/write channels. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The flexible disk interface can be configured through a wide range of capabilities. This allows the SSI 32C9020 to interface with nearly any read/write channel and allows the user of the SSI 32C9020 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9020 controller and the SSI 32D5391 Data Synchronizer with 1,7 ENDEC, you are guaranteed a problem free interface.

Within the Disk Formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 32-bit ECC for headers and an 88-bit Reed Solomon code for data. If the checker detects an error in an 88-bit Reed Solomon data field, the syndrome information is transferred into the corrector. The corrector performs the necessary operations to determine if the error was correctable and interfaces directly with the buffer controller to perform the correction automatically. The corrector performs its correction within one half of a sector time. This guarantees that the corrector will always be available to correct the next sector if necessary.

As its name implies, the Buffer Manager manages the data buffer of the controller. The Buffer Manager can support either SRAM or DRAM. When configured to operate with DRAM, the Buffer Manager automatically performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. The Buffer Manager interfaces with the buffer memory, the SCSI Interface block, the data path of the Disk Formatter block, the ECC corrector and the microprocessor. If more than one of these devices

requires access to the buffer memory, the Buffer Manager arbitrates the requests automatically. The Buffer Manager of the SSI 32C9020 can sustain SCSI operations at the rate of 10 megabytes per second, Disk Formatter operations at 48 megabits per second (6 megabytes per second) and still have sufficient band width left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

PIN DESCRIPTION

The following convention is used in the pin description:

(I) denotes an input

(O) denotes an output

(Z) denotes a tri-state output

(OD) denotes an open drain output

GENERAL

NAME	TYPE	DESCRIPTION
VDD		POWER SUPPLY PIN, VCC
GND		GROUND

HOST INTERFACE

$\overline{SDBP}$	I/O	SCSI DATA BUS PARITY. Odd parity bit for the SCSI data bus.
$\overline{SDB(7:0)}$	I/O	SCSI DATA BUS BITS 7-0.
$\overline{ATN}$	I	ATTENTION. This active low signal is used by the initiator to request a message out phase.
$\overline{BSY}$	I/O	BUSY. This active low signal is used to indicate when the bus is active.
$\overline{ACK}$	I	ACKNOWLEDGE. This active low signal is used in the handshake protocol to indicate the completion of a data byte transfer.
$\overline{SRST}$	I	SCSI RESET. This active low signal is used to reset the SCSI controller.
$\overline{MSG}$	O	MESSAGE. This active low signal is used to indicate a message phase.
$\overline{SEL}$	I/O	SELECT. This active low signal is used to indicate either a selection or reselection phase.
$\overline{C}$/D	O	COMMAND/DATA. This signal is used to indicate either a command or data phase.
$\overline{REQ}$	I	REQUEST. This active low signal is used in the handshake protocol to initiate a data byte transfer.
$\overline{I}$/O	I	INPUT/OUTPUT. This signal is used to indicate the direction of data transfer.
PAREN	I	SCSI PARITY ENABLE. This active high signal is used to enable parity checking of the SCSI data bus. Parity checking is disabled when this pin is held low.

DISK INTERFACE

NAME	TYPE	DESCRIPTION
GPIO(2:0)	I/O	INPUT/OUTPUT. These pins are used to indicate the SCSI ID of the target device. The pins can be programmed as outputs for test purposes only.
INDEX	I	INDEX. Input for index pulse received from the drive.
INPUT/	I/O	DISK SEQUENCER INPUT/OUTPUT. A general purpose control (output) and status (input) pin configured by the Output Enable Bit of Register 71H, bit 7. At power-on, this pin is an input. As an input, it can be used to synchronize the disk sequencer to an external event. As an output, it is controlled by bit 2 of the Control Field of the disk sequencer.
$\overline{\text{AMD}}$/SECTOR	I/O	ADDRESS MARK DETECT/SECTOR. This pin is used in the hard sector mode as the sector input. A pulse on this pin indicates a sector mark is found. In the soft sector mode a low-level input indicates an address mark was detected. The device powers up in soft sector default mode.
RG	O	READ GATE. During disk data read, this pin is asserted. Active high.
WG	O	WRITE GATE. During disk data write, this pin is asserted. Active high.
RRCLK	I	READ/REFERENCE CLOCK. This pin is used to clock data on the NRZ pin into and out of the device.
NRZ0	I/O	NON RETURN TO ZERO. This signal is the read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted.

MICROPROCESSOR INTERFACE

$\overline{\text{RST}}$	I	RESET. An asserted low input generates a component reset that holds the internal registers at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals are set to the high-Z state during the assertion of this signal.
ALE/M/$\overline{\text{NM}}$	I	ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high or left floating after reset, the microprocessor interface is configured as non-multiplexed. When driven low, then the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs.
CS	I	CHIP SELECT. Active high signal, when asserted, the internal registers of the SSI 32C9020 can be accessed.
$\overline{\text{WR}}$/R/$\overline{\text{W}}$	I	WRITE STROBE/READ/WRITE. In the Intel bus mode, when an active low signal is present with CS signal high, the data is written to the internal registers. In the Motorola bus mode, this signal acts as the R/$\overline{\text{W}}$ signal.
$\overline{\text{RD}}$/DS	I	READ STROBE/DATA STROBE. In the Intel bus mode, when an active low signal is present with CS signal high, internal register data is read. In the Motorola mode, this signal acts as the DS signal. DS when active high is data strobe.

MICROPROCESSOR INTERFACE (continued)

NAME	TYPE	DESCRIPTION
$\overline{DINT}$	O, OD,Z	DISK INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the disk side. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state. Register 4F bit 3 enables the pull-up.
$\overline{SINT}$	O, OD,Z	SCSI INTERRUPT. This signal is generated by the SCSI controller and is an interrupt line to the microprocessor. It is programmable for either a push-pull or open drain output circuit. This signal powers up in the high-Z state. The interrupt is sourced from the SCSI Interrupt Register. Register 4F bit 3 enables the pull-up. This signal is also programmable to be either an active high or low interrupt.
AD(7:0)	I/O	ADDRESS/DATA BUS. When configured in the Intel mode, these lines are multiplexed, bidirectional microprocessor register address and data lines. When configured in the Motorola mode, these lines are bidirectional data lines.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS: These signals are nonmultiplexed address input or latched address output lines.
READY	O	READY: When this signal is deasserted low, the microprocessor shall insert wait states to allow time for the chip to respond.
I/$\overline{MC}$	I	INTEL/MOTOROLA: This signal selects the microprocessor interface to be used. When this signal is asserted high, it selects the Intel bus control interface. When this signal is deasserted low, it selects the Motorola bus control interface. This signal has an internal pull-up to allow the default selection of the Intel bus control interface.

BUFFER MANAGER INTERFACE

BA(15:0)	O	BUFFER MEMORY ADDRESS LINES 0:15. Active high, for direct connection to a Static or Dynamic RAM address lines 0:15.
BA16/$\overline{RAS}$	O	BUFFER MEMORY ADDRESS 16: In SRAM mode, for direct connection to a Static RAM address line 16. ROW ADDRESS STROBE: In DRAM mode, for direct connection to a Dynamic RAM Row Address Strobe signal.
BA17/$\overline{CAS}$	O	BUFFER MEMORY ADDRESS 17: In SRAM mode, for direct connection to a Static RAM address line 17. ROW ADDRESS STROBE: In DRAM mode, active low, for direct connection to a Dynamic RAM Column Address Strobe signal.
BD(7:0)	I/O	BUFFER MEMORY DATA BUS. 7 through 0. Active high, buffer data bus that connects directly to the buffer RAM data lines.

BUFFER MANAGER INTERFACE

NAME	TYPE	DESCRIPTION
BDP	I/O	BUFFER MEMORY DATA PARITY. This signal provides odd parity for the buffer memory data bus during transfers to/from the buffer memory to the buffer RAM.
$\overline{MOE}$	O	MEMORY OUTPUT ENABLE. This signal is asserted low only for buffer memory read operations.
$\overline{WE}$	O	WRITE ENABLE. Active low, write enable for the buffer RAM.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address bits, write enable $\overline{WE}$, and memory output enable $\overline{MOE}$.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

PARAMETER	RATING
Power Supply Voltage, VCC	7V
Ambient Temperature	0 to 70°C
Storage Temperature	-65 to 150°C
Power Dissipation	750 mW
Input, Output pins	-0.5 to VCC + 0.5V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Power Supply Voltage		4.5		5.5	V
ICC Supply Current	Ta = 25°C Outputs Unloaded			50	mA
ICCS Supply Current				250	µA
VIL Input Low Voltage		-0.5		0.8	V
V0IH Input High Voltage		2		VCC + 0.5	V
VOL Output Low Voltage	All pins except SCSI interface, IOL = 2 mA			0.4	
VOL Output Low Voltage	SCSI interface pins, IOL = 48 mA			0.5	V
VOH Output High Voltage	IOH = -400 µA			2.4	V
IL Input Leakage Current	0 < VIN < VCC	-10		10	µA
CIN Input Capacitance				10	pF
COUT Output Capacitance				10	pF

ELECTRICAL SPECIFICATIONS (continued)

Microprocessor Interface Timing Parameters

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Ta	Ale width		20			ns
Tma	Address valid to MA0:7 valid				30	ns
Tr	$\overline{RD}$ Width		80			ns
As	Address valid to ALE ↓		5			ns
Ah	ALE ↓ to address invalid		10			ns
Cs	CS Valid to $\overline{RD}$ ↓ or DS ↑		20			ns
Ch	$\overline{RD}$ ↑ or DS ↓ to CS ↓		0			ns
Tda	$\overline{RD}$ ↓ or DS ↑ to read data valid				60	ns
Tds	DS width		80			ns
Tdh	$\overline{RD}$ ↑ or DS ↓ to read data invalid		0		25	ns
Tsrw	R/$\overline{W}$ valid to DS ↑		20			ns
Thrw	DS ↓ to R/$\overline{W}$ invalid		20			ns
Tdrdy	$\overline{RD}$ ↓ to READY ↓ (Intel) or DS ↑ to READY ↓ (Motorola)				30	ns
Wds	Write data valid to $\overline{WR}$ ↑ or DS ↓ to write data invalid		40			ns
Wdh	$\overline{WR}$ ↑ or DS ↓ to write data invalid		10			ns
Note:	↑ indicates rising edge	↓ indicates falling edge				

Non-Multiplexed Bus Interface Timings

Tmas	MA(7:0) valid to DS ↓		5			ns
Tmah	DS ↑ to MA(7:0) invalid		5			ns
Cs	CS valid to DS ↓		20			ns
Ch	DS ↑ to CS ↓		0			ns
Tda	DS ↑ to read data valid				60	ns
Tds	DS width		80			ns
Tdh	DS ↑ to read data invalid		0		25	ns
Tsrw	R/$\overline{W}$ valid to DS ↓		20			ns
Thrw	DS ↑ to R/$\overline{W}$ invalid		20			ns
Tdrdy	DS ↑ to READY ↓ (Motorola)				30	ns
WDS	Write data valid to $\overline{WR}$ ↑ or DS ↓		40			ns
Wdh	$\overline{WR}$ ↑ or DS ↓ to write data invalid		10			ns

Note 1: ↑ indicates rising edge ↓ indicates falling edge
Note 2: Loading capacitor = 30 pF

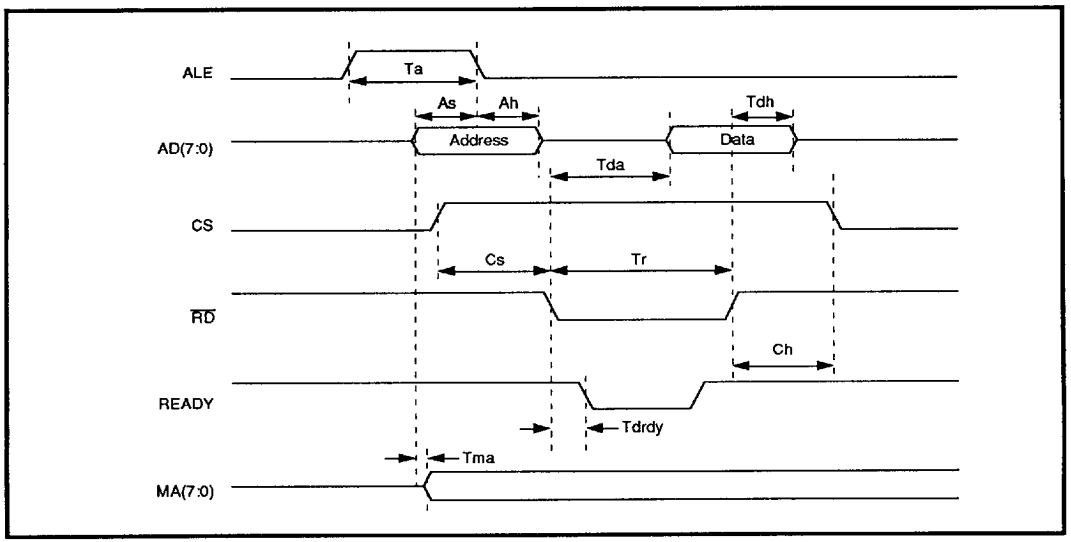


FIGURE 2: Intel Register Multiplexed Read Timing

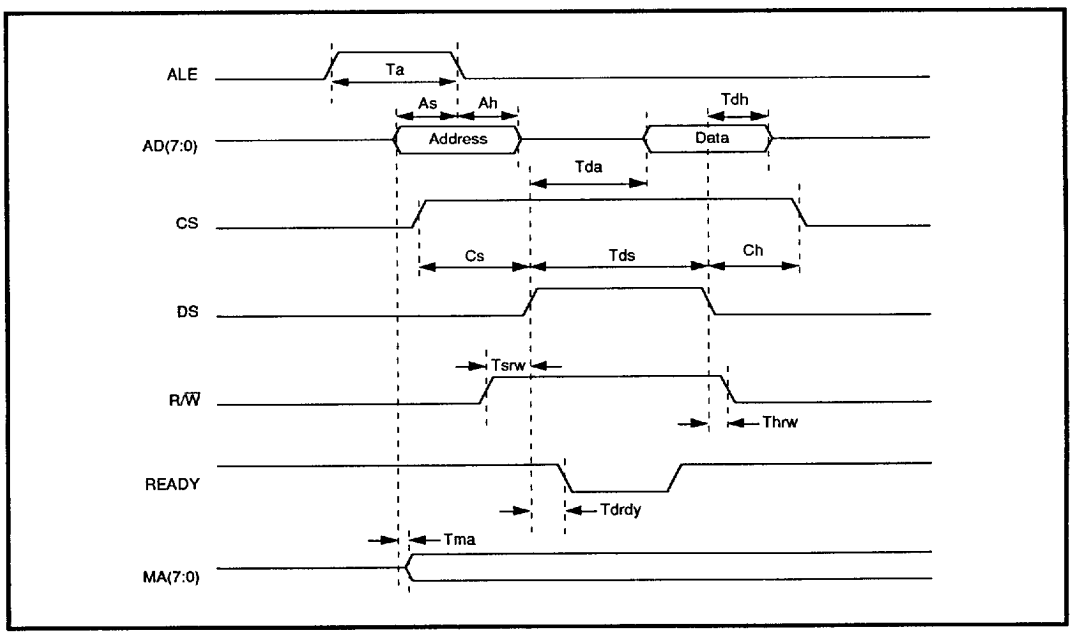


FIGURE 3: Motorola Register Multiplexed Read Timing

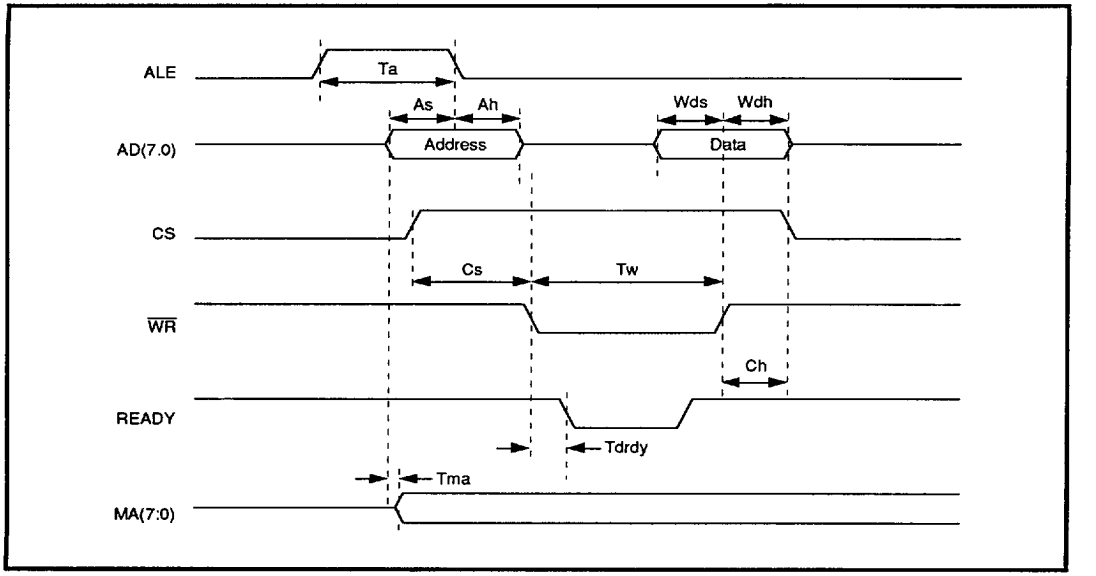


FIGURE 4: Intel Register Multiplexed Write Timing

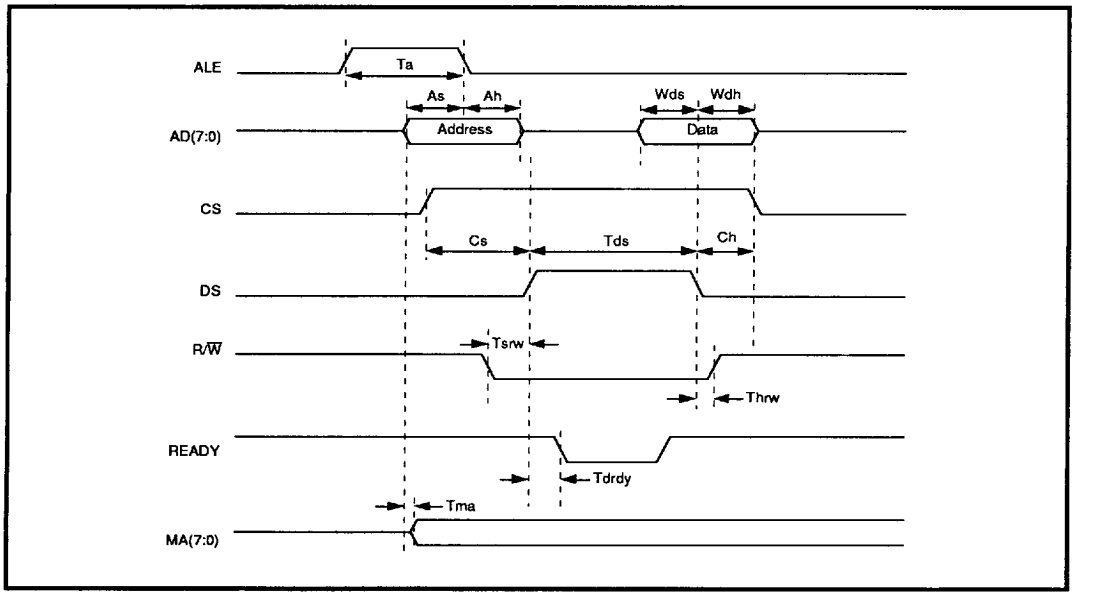


FIGURE 5: Motorola Register Multiplexed Write Timing

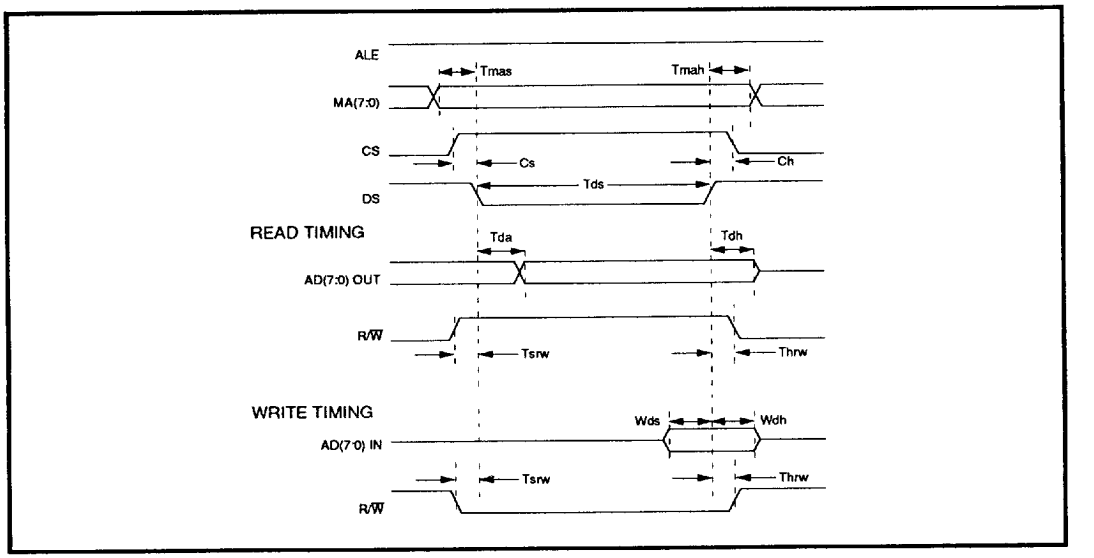


FIGURE 6: Non-Multiplexed Bus Timing Diagrams

ELECTRICAL SPECIFICATIONS (continued)

Disk Interface Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
T	RRCLK		20.8			ns
T/2	RRCLK high/low time		8.5			ns
Tr, Tf	RRCLK rise and fall time		0		2	ns
Ds	NRZ in valid to RRCLK ↑		3			ns
Dh	RRCLK ↑ to NRZ in invalid		3			ns
As	$\overline{AME}$ valid to RRCLK ↑		3			ns
Dv	RRCLK ↑ to NRZ out		3		15	ns
Note:	↑ indicates rising edge					
Loading capacitor = 10 pF						

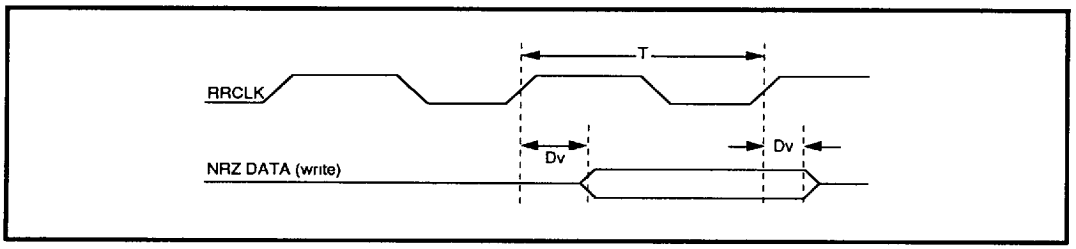


FIGURE 7: Disk Write Timing

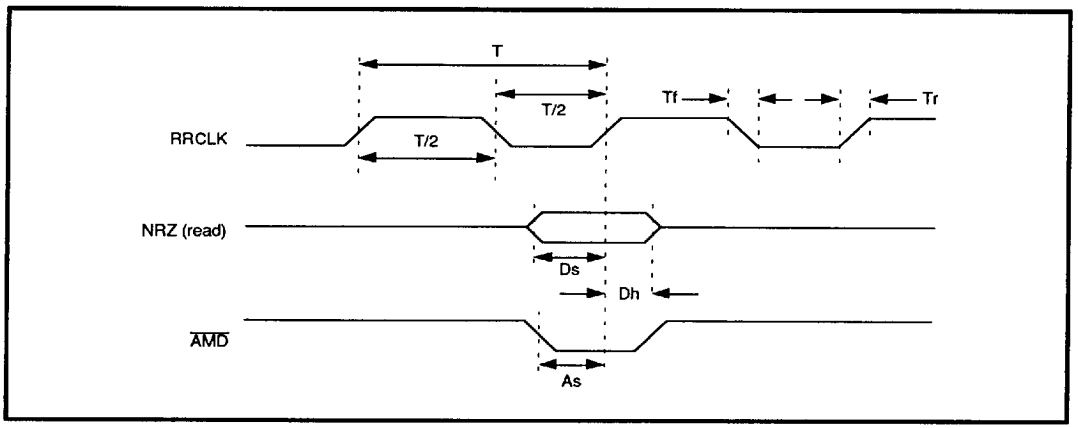


FIGURE 8: Disk Read Timing

BUFFER MEMORY READ/WRITE TIMING PARAMETERS (Figures 9 through 14)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
T	SYSCLK period		25			ns
T/2	SYSCLK high/low time		10			ns
Tav	SYSCLK ↑ to address valid	Note 1			18	ns
Tmsv	SYSCLK ↑ to $\overline{MS}$↓	Notes 1, 6			18	ns
Tmsh	SYSCLK ↑ to $\overline{MS}$↑	Note 1			18	ns
Tmv	SYSCLK ↑ to $\overline{MOE}$↓	Note 1			18	ns
Tmh	SYSCLK ↑ to $\overline{MOE}$↑	Note 1			18	ns
Twv	SYSCLK ↑ to $\overline{WE}$↓	Note 1			18	ns
Twh	SYSCLK ↑ to $\overline{WE}$↑	Note 1			18	ns
Tdov	SYSCLK ↑ to data out valid	Note 1			18	ns
Tdoh	SYSCLK ↑ to data out invalid	Note 1			18	ns
Tdis	Data in valid to $\overline{MOE}$ ↑ (SRAM) Data in valid to $\overline{CAS}$ ↑ (DRAM)		5			ns
Tdih	$\overline{MOE}$ ↑ to data in valid (SRAM) $\overline{CAS}$ ↑ to data in valid (DRAM)		0			ns
Trv	SYSCLK ↑ to $\overline{RAS}$↓	Note 1			18	ns
Trh	SYSCLK ↑ to $\overline{RAS}$↑	Note 1			18	ns
Trav	SYSCLK ↑ to row address valid	Note 1			18	ns
Trah	SYSCLK ↑ to row address invalid	Note 1			18	ns
Tcv	SYSCLK ↑ to $\overline{CAS}$↓	Note 1			18	ns
Tch	SYSCLK ↑ to $\overline{CAS}$↑	Note 1			18	ns
Tcav	SYSCLK ↑ to column address valid	Note 1			18	ns
Tcah	SYSCLK ↑ to column address invalid		0			ns

ELECTRICAL SPECIFICATIONS (continued)

BUFFER MEMORY READ/WRITE TIMING PARAMETERS (Figures 9 through 14) (continued)

PARAMETER		CONDITIONS	MIN	UNIT
Trwl	$\overline{RAS}\downarrow$ to $\overline{RAS}\uparrow$	Notes 2, 3	((RWL + 3) • T)	ns
Trwh	$\overline{RAS}\uparrow$ to $\overline{RAS}\downarrow$	Notes 2, 4	((RWH + 1) • T)	ns
Tcwl	$\overline{CAS}\downarrow$ to $\overline{CAS}\uparrow$	Note 2	((CWL + 1) • T)	ns
Tcwl	$\overline{CAS}\uparrow$ to $\overline{CAS}\downarrow$	Notes 2, 5	((CWL + 1) • T)	ns

Note: Loading capacitance = 30 pF

Note 1: The measured delay for any of the signal indicated by this note will not vary from the measured delay of any other signal indicated by this note by more than ±1 ns.

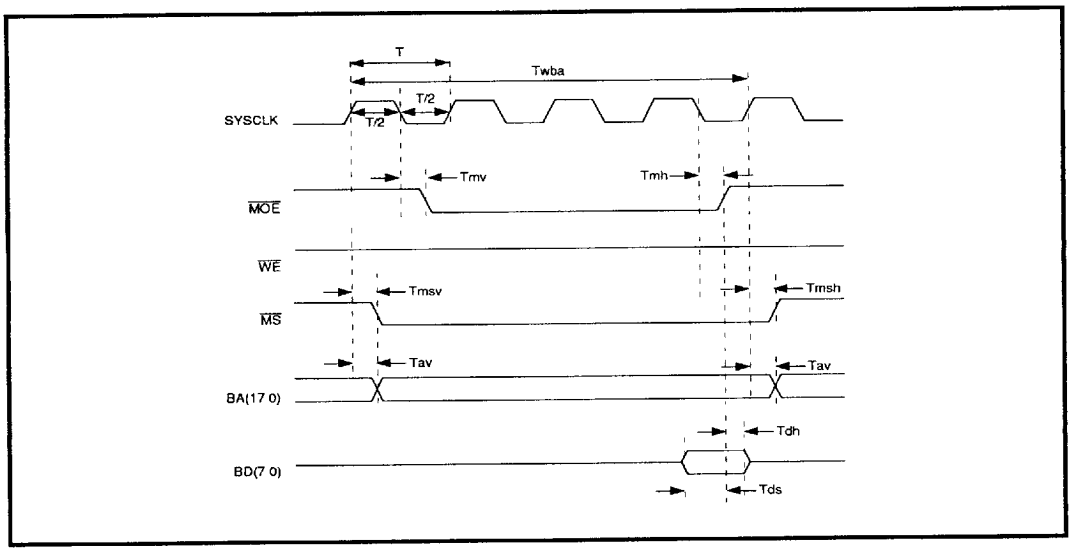
Note 2: RWL, RWH, CWL and CWH are fields in the Buffer Manager Timing Control Register (54H). Each is a two bit field which can contain a value of 0, 1, 2, or 3. These values determine the minimum number of SYSCLK periods (T) for the associated signal width.

Note 3: The minimum width value of Trwl will be generated for refresh cycles and for any buffer memory access cycle except when multiple page mode accesses are performed. When multiple page mode accesses are performed, the width of the $\overline{RAS}$ low pulse is extended until the end of the last $\overline{CAS}$ low cycle.

Note 4: The minumum value of Trwh will be generated whenever the Buffer Manager determines that a buffer request is pending at the ocmpletion of the current memory cycle and a page mode access can not be used either because page mode operation is not enabled or the needed location is not within the current page.

Note 5: The minumum value of Tcwh will be generated only between consecutive page mode accesses.

Note 6: $\overline{MS}$ will rise only if the Buffer Manager determines that no additional requests for buffer access are pending. If the Buffer Manager determines that another access is to be Made, $\overline{MS}$ is kept low between the accesses for improved speed.



Note: Twba is a functional parameter that gives the duration of one RAM data buffer access cycle in SYSCLK periods. The value is programmed in bits 1-0 of register 54H. These examples show Twba = 4T.

FIGURE 9: SRAM Read Timing

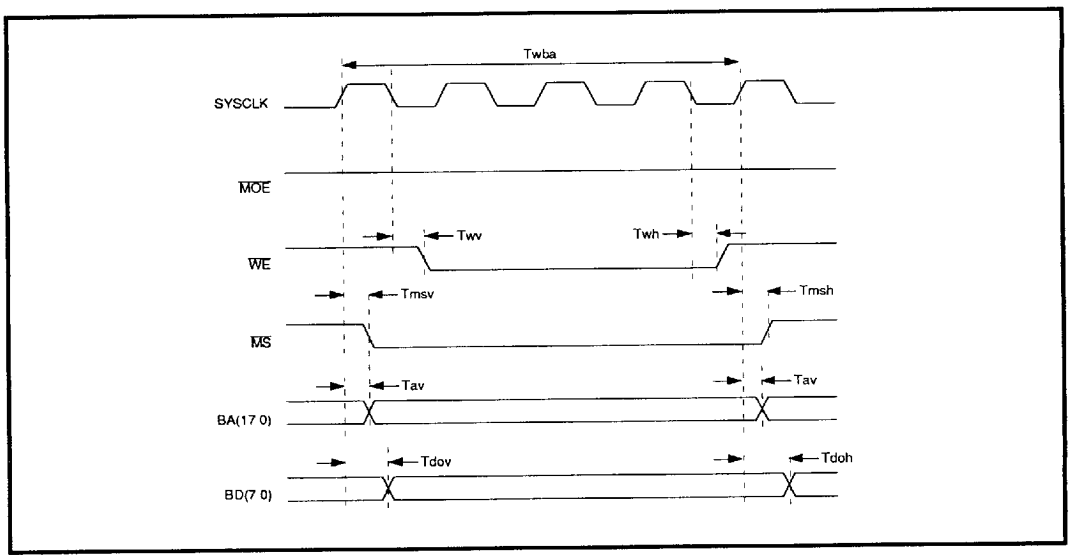


FIGURE 10: SRAM Write Timing

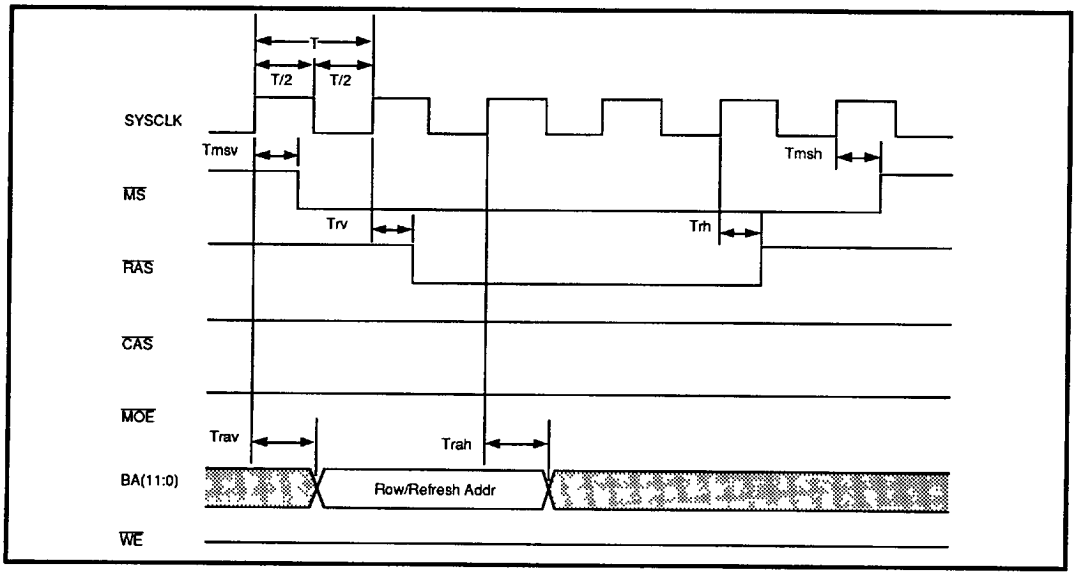


FIGURE 11: DRAM Timing, Refresh Cycle (Shown with WRL = 0)

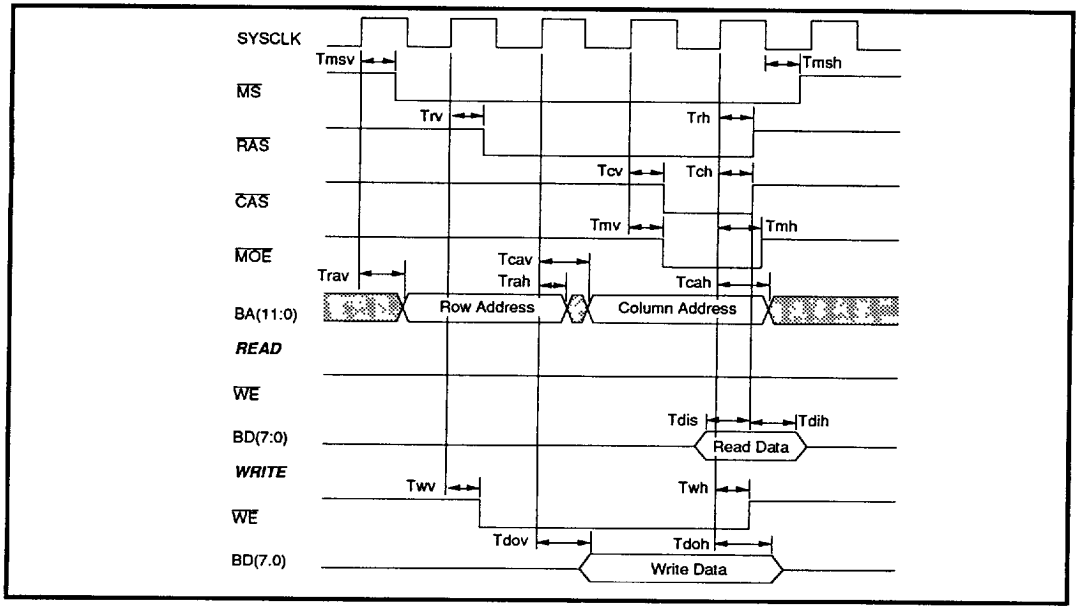


FIGURE 12: DRAM Timing, Standard Cycle (Shown with RWL = 0 and CWL = 0)

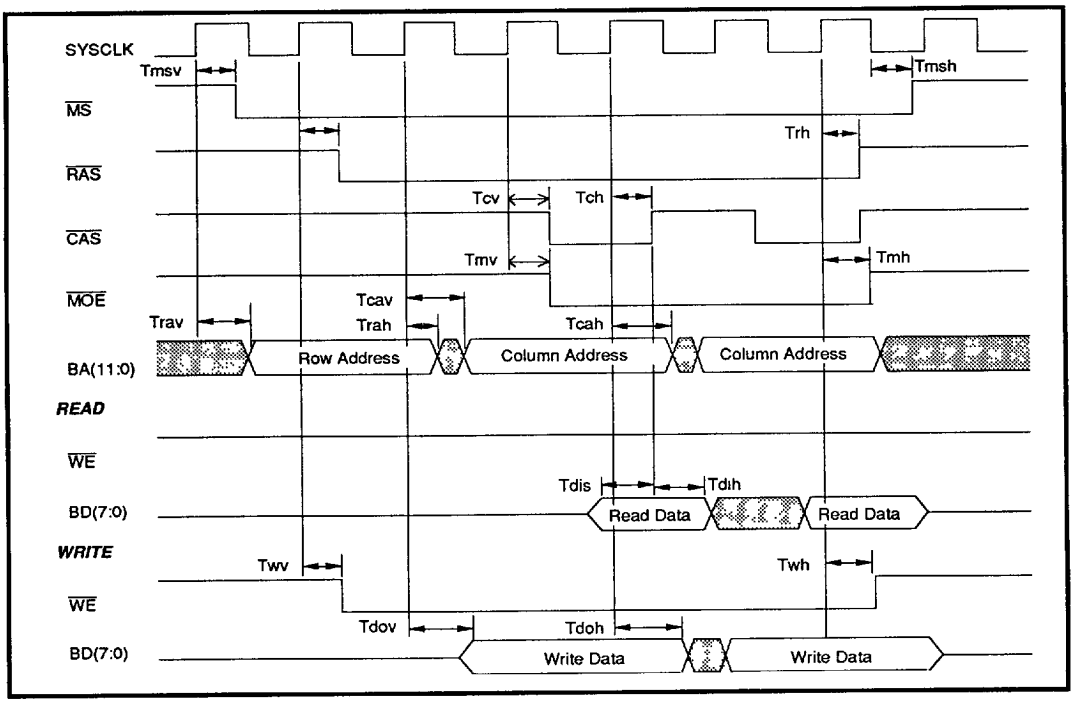


FIGURE 13: DRAM Timing, Fast Page Cycles (Shown with RWL = 0, RWH = 0, CWL = 0 and CWH = 0)

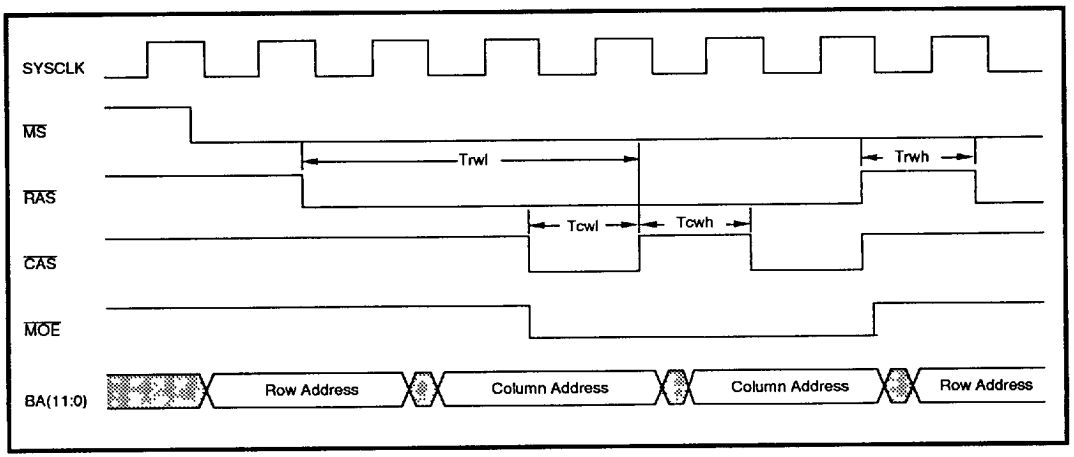


FIGURE 14: DRAM Timing (Showing the Relationship of RWL, RWH, CWL and CWH to overall timing)

ELECTRICAL SPECIFICATIONS (continued)

PARAMETER		MIN (Fast)	MAX (Fast)	MIN (Slow)	MAX (Slow)	UNIT
Trh	$\overline{REQ}$ Assertion Time	37	48			ns
Trl	$\overline{REQ}$ Deassertion Time	63	52			ns
Tids	Setup time SCSI Data to $\overline{REQ}\downarrow$ (write to SCSI bus)	43				ns
Tidh	Hold time $\overline{REQ}\downarrow$ to SCSI Data invalid (write to bus)	43				ns
Tal	Minimum $\overline{ACK}$ Assertion Width Required	10				ns
Tods	Data Hold from $\overline{ACK}\downarrow$ (Read from the SCSI bus)	5				ns
Todh	Data Hold from $\overline{ACK}\downarrow$ (Read from the SCSI bus)	12				ns
Note: All timing parameters are measured with 200 pF load, two SCSI terminator loads, $\overline{ACK}$ filter turned off.						

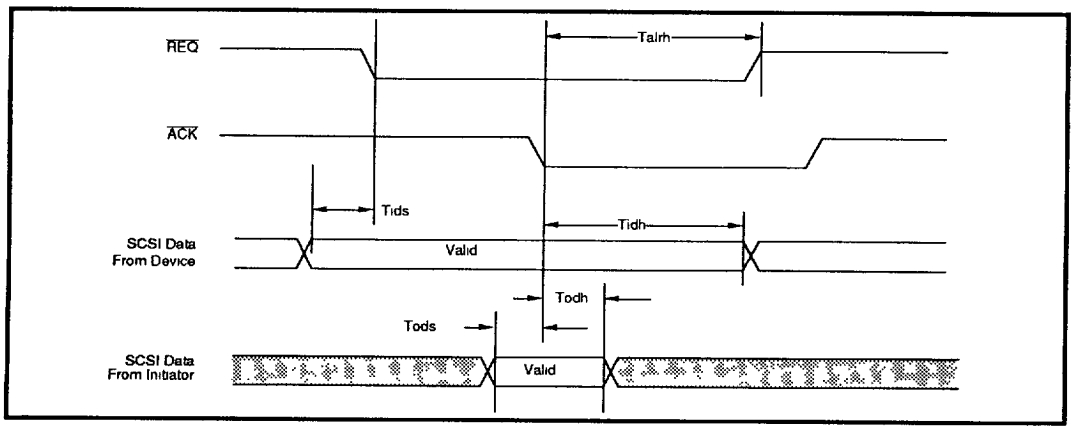


FIGURE 15: SCSI Synchronous Timing

ELECTRICAL SPECIFICATIONS (continued)

PARAMETER		MIN	MAX	UNIT
Tods	Data Setup to $\overline{ACK}\downarrow$ (SCSI Output phase)	5		ns
Todh	Data Hold form $\overline{ACK}\downarrow$ (SCSI Output phase)	12		ns
Talrh	$\overline{ACK}\downarrow$ to $\overline{REQ}\uparrow$		49	ns
Tids	Data Setup to $\overline{REQ}\downarrow$ (SCSI Input phase)	80		ns
Tidh	Data Hold from $\overline{ACK}\downarrow$ (SCSI Input phase)	29		ns
Note: All timing parameters are measured with 200 pF load, two SCSI terminator loads, $\overline{ACK}$ filter turned off.				

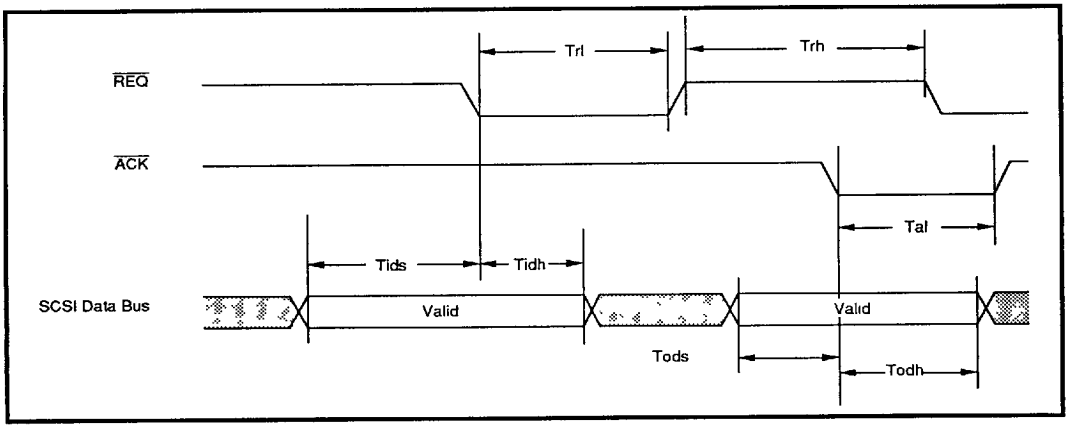


FIGURE 16: SCSI Asynchronous Timing

Synchronous Data In/Out Phase

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Txtrp*	Synchronous Transfer Period	(see note)				ns
Tsrl	SYSFREQ high to $\overline{REQ}$ low				50	
Tsrh	SYSFREQ high to $\overline{REQ}$ high				60	ns
Tdov	SYSFREQ high to data out valid				40	ns
Tdsu	Data setup to $\overline{ACK}$ low		55			ns
Tdh	Data hold from $\overline{ACK}$ low		40			ns

Note: Txtrp is the Synchronous Transfer Period as defined by the Synchronous Control Register (Reg: 43H). SYSFREQ is a function of the BUFCLK and is determined by the prescale value as defined by the Clock Control Register (Reg: 49H).

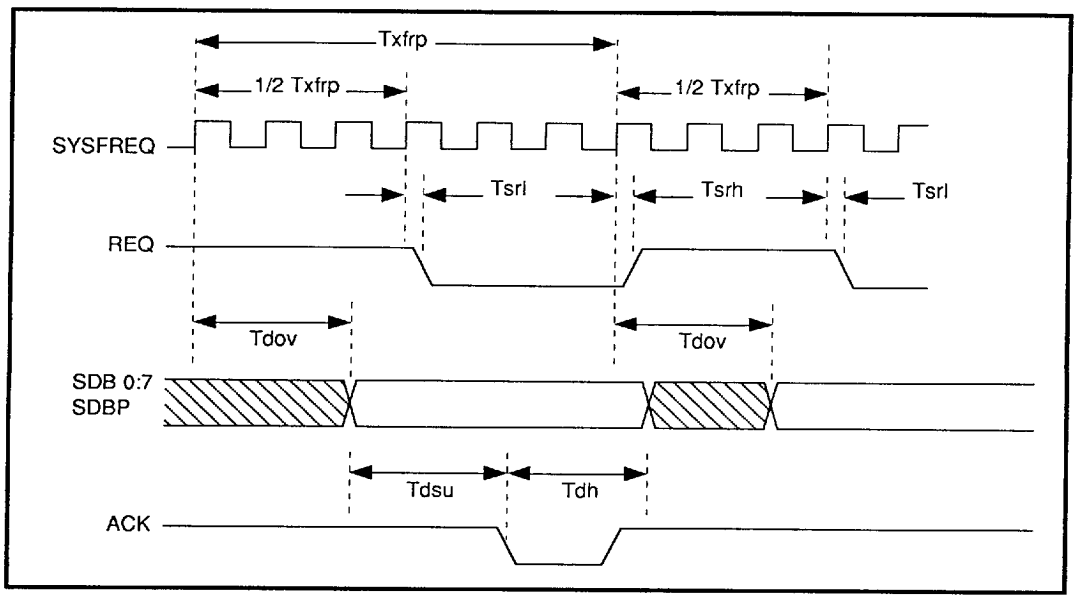


FIGURE 17: Even Number of SYSFREQ Cycles/SCSI Transfer Period

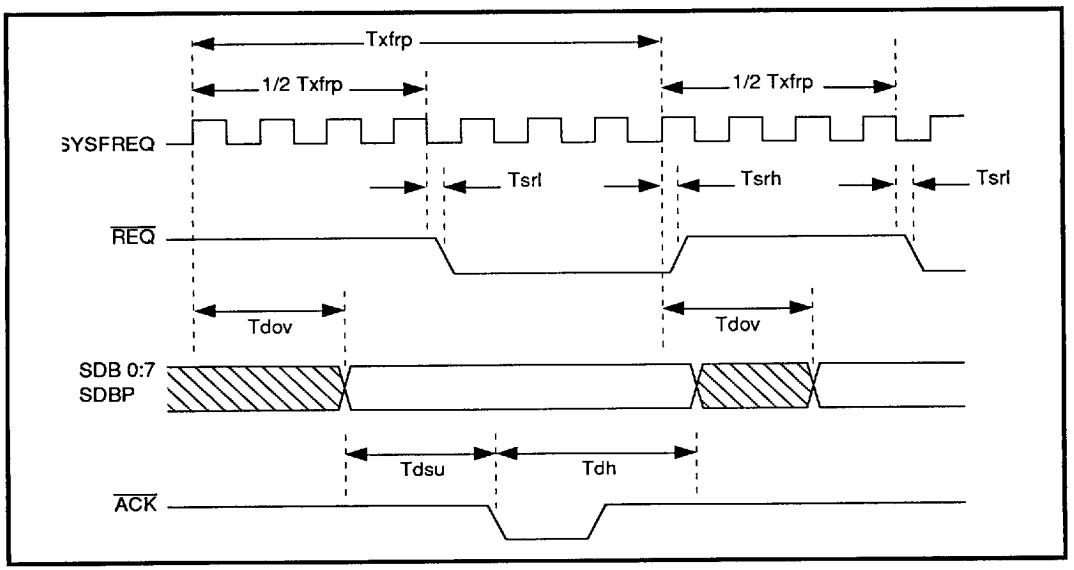


FIGURE 18: Odd Number of SYSFREQ Cycles/SCSI Transfer Period

Wait for Selection

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tbsd	Bus Settle Delay (400 ns) to the assertion of $\overline{BSY}$		3T + 90		4T + 90	ns
Note: T is the SCSI Clock Period (SCP) as defined in Register 49H (CLKCTL).						

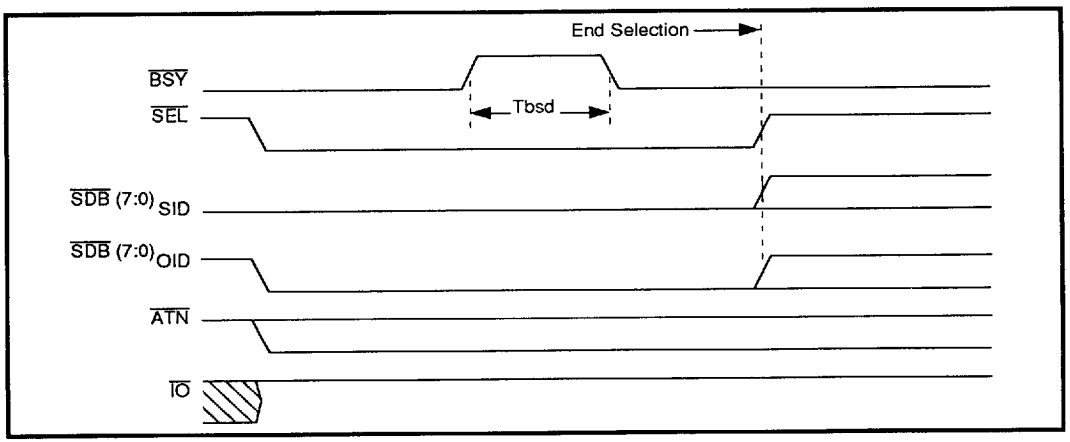


FIGURE 19: Wait for Selection

Arbitration

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tbfsd	Bus Settle Delay (400 ns) + Bus Free Delay (800 ns) to the assertion of BSY and $\overline{SDB}_{OID}$		6T + 110		7T + 110	ns
Tad	Arbitration Delay (2.4 µsec) to the assertion of $\overline{SEL}$ (win) or deassertion of $\overline{BSY}$ and $\overline{SDB}_{OID}$ (lost)		-		13T + 100	ns
Tbcsd	Bus Clear Delay (800 ns)+ Bus Settle Delay (400 ns) to end of Arbitration Phase		-		6T + 100	ns

Note: T is the SCSI Clock Period (SCP) as defined in Register 61H (CLKCTL).

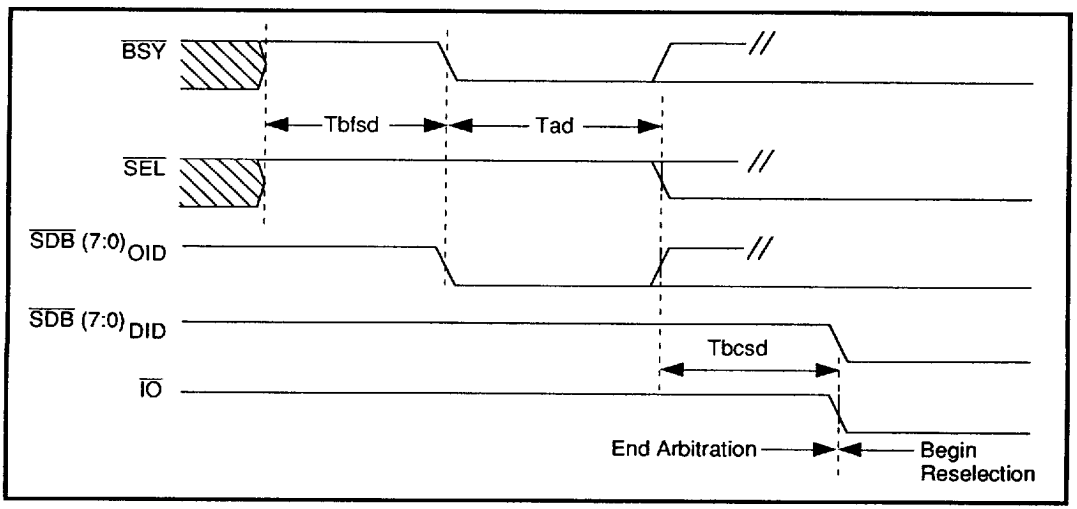


FIGURE 20: Arbitration

Reselection

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tbcsd	Bus Clear Delay (800 ns) + Bus Settle Delay (400 ns) to end of Arbitration Phase		-		6T + 100	ns
Tdskd1	Two Deskew Delays (90 ns) to the deassertion of $\overline{BSY}$		-		160	ns
Tbsd	Bus Settle Delay (400 ns) to the assertion of $\overline{BSY}$		-		2T + 40	ns
Tdskd2	Two Deskew Delays (90 ns) to the deassertion of SEL, $\overline{SDB}_{OID}$, and $\overline{SDB}_{DID}$		1T +70		2T + 70	ns
Note: T is the SCSI Clock Period (SCP) as defined in Register 61H (CLKCTL).						

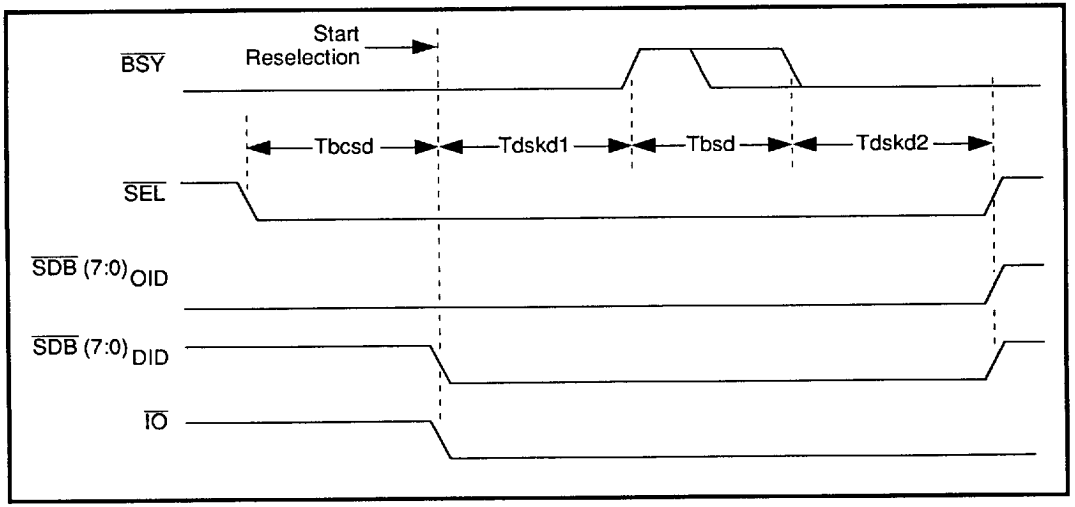
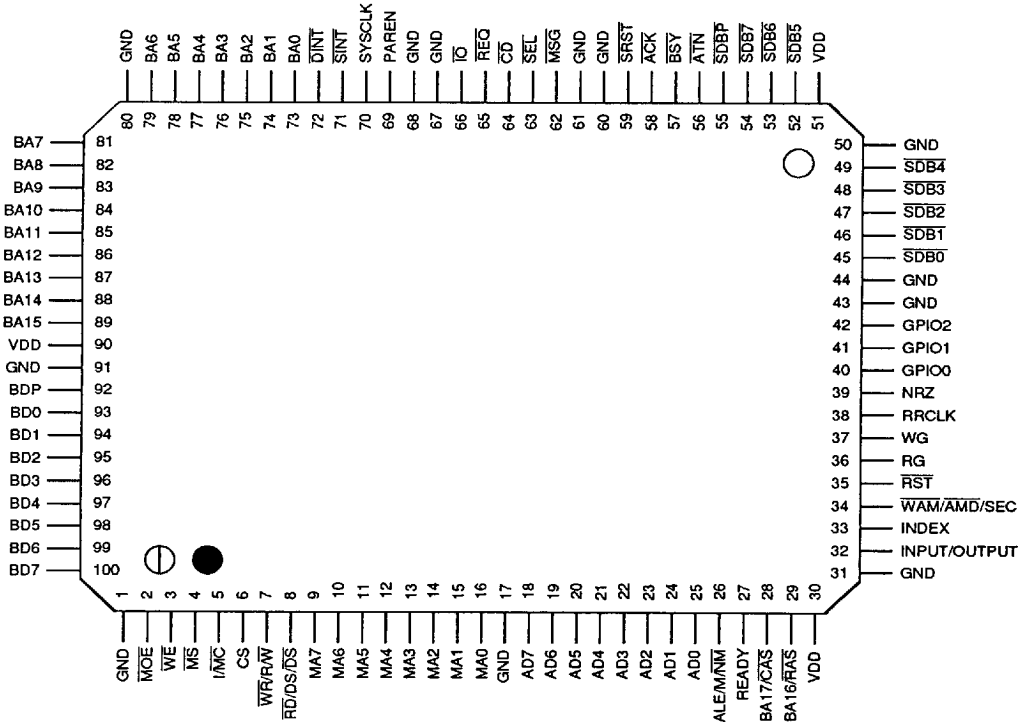


FIGURE 21: Reselection

SSI 32C9020
SCSI Combo Controller
48 Mbit/s; single bit NRZ interface

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



100-pin QFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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