Product Brief

Bipolar Integrated Technology Inc.

B2032

32-Output Clock Generator

with 1ns Edge Placement

Introduction:

The B2032 is a high-speed integrated clock generation solution which is targeted to solve many of today's clock generation problems. Since the B2032 is reprogrammable with just a change to an external PROM, the systems can be margined and critical timing relationships may be found by simply reprogramming the device.

The B2032 has an internal PLL which will lock a feedback clock input to the reference clock input. The feedback clock can be any clock output or externally generated signal having the same period as the reference clock. Each clock generator can produce a clock with a programmable period in the range of 10ns to 1ns in 1ns increments and can place the clock's rising or falling edge at any 1ns boundary within the cycle. Since the B2032 uses a single ultra high-speed PLL to time all of the clock generators, it is possible for the B2032 to have a very low skew between any two similar outputs.

On power-up the B2032 reads the contents of a serial ROM and programs each of its 32 internal clock generators. Once programmed the B2032 will start all of the clock generators and will run until the PLL gains a locked condition. It will then assert the LOCK output which can be used to control the board's reset logic.

The B2032 also supports JTAG boundary scan and a PLL bypass feature for board test functions. Package is a 108-pin PGA.

Features:

- Generates 32 clock outputs from 1MHz to 100MHz.
- The B2032 has 32 programmable clock generators. A lower cost chip, the B2033 has 8 programmable clock generators. Both have 32 clock outputs.
- Each clock can have a programmable frequency between 1MHz and 100MHz.
- Any clock rising or falling edge can be placed on any 1ns boundary.
- Low output-to-output skew of less than 500ps.
- Up to 4 hold terms can inhibit any selected clocks for single stepping.
- Single high impedance reference clock input enables this device to be used in bus clock distribution systems where loading is an issue.
- PLL lock output indicated PLL status.
- JTAG compatible boundary scan and a PLL bypass mode enable board test and open loop testing.
- Programs with a single external serial PROM.
- TTL I/Os with 20mA drive.

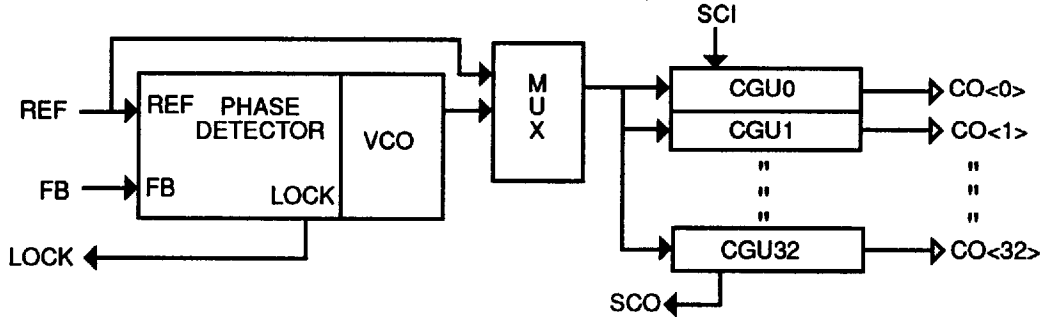

Figure 1 - B2032 32-Output Clock Generator

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32-Output Clock Generator
with 1ns Edge Placement

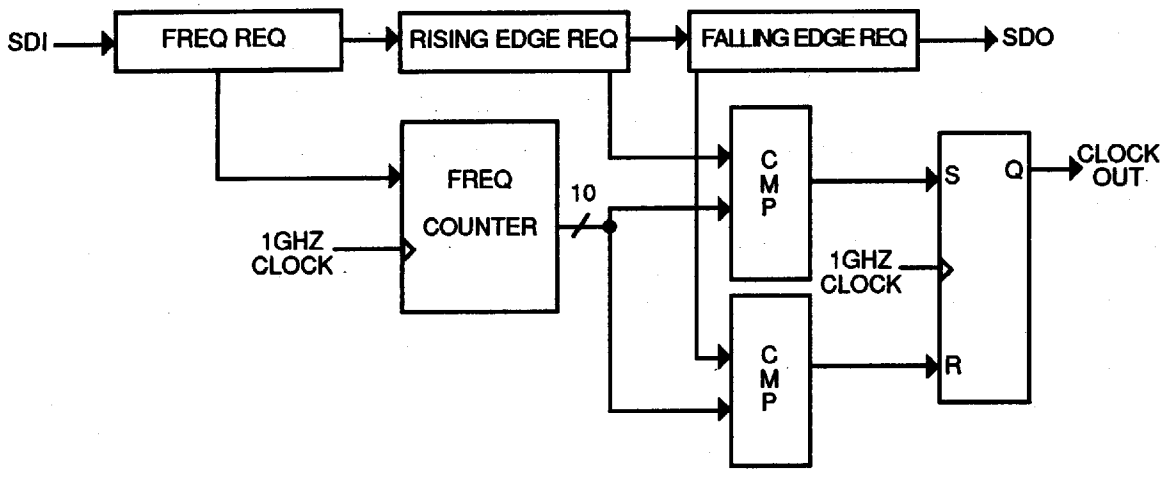

Figure 2 - CGU (Detail)

Pin Descriptions

REF (I) Reference clock input to PLL in the range of 1MHz to 100MHz.

FB (I) Feedback clock to PLL in the range of 1MHz to 100MHz.

PDI (I) Program Data input from external serial ROM.

PRST (O) Program ROM reset.

CO<31..0> (O) Clock outputs.

HOLD<3..0> (I) Clock hold inputs can be used at any clock generator.

BYPASS (I) Use REG instead of the VCO internally. This mode is useful for ATE.

LOCK (O) PLL lock output.

SDI (I) JTAG scan data in.

SDI (O) JTAG scan data out.

TMS (I) JTAG Test Mode Select.

TCK (I) JTAG Test Clock.

TRST (I) JTAG Test Reset.

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