Triple Half-bridge DMOS Output Driver with Serial Input and PWM Control ATA6831/ATA6832

1. Introduction

ATA6831 and ATA6832 are fully protected universal driver interfaces designed in SMARTIS1 technology. They are used to control up to 3 different loads by a microcontroller in automotive and industrial applications. The ATA6831 is housed in a QFN18 4 × 4 mm package.

Each of the 3 high-side and 3 low-side drivers is capable of driving currents of up to 1A. The drivers are internally connected to form 3 half-bridges and can be controlled separately from a standard serial peripheral data interface. Therefore, all kinds of loads such as bulbs, resistors, capacitors, and inductors can be combined. The IC design particularly supports the application of H-bridges to drive DC motors. The PWM feature allows a smooth operation of DC motors and BLDC motor control. Protection against short-circuit conditions, overtemperature, and undervoltage is implemented. Various diagnosis functions and a very low quiescent current in standby mode open a wide range of applications. Automotive qualification referring to conducted interferences, EMC, and 2 kV ESD protection gives added value and enhanced quality for demanding up-market applications.

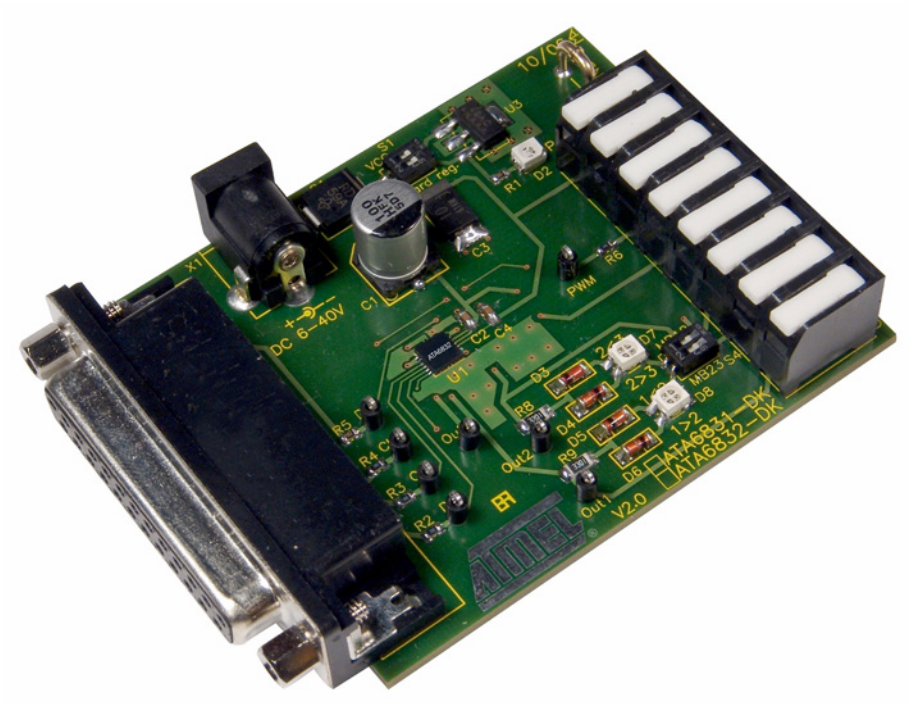
ATA6831 is designed to operate on junction temperatures up to 150°C. ATA6832 is designed for high temperature applications on junction temperatures up to 200°C If not explicit mentioned, all comments in this document for ATA6831 are valid for ATA6832 as well.

ATA6831/ ATA6832 Driver ICs

Application Note

9120A–AUTO–01/08

Figure 1-1. Triple Half-bridge DMOS Output Driver with Serial Input Control ATA6831



2. Design Kit

The design kit includes the following components:

- Application board ATA6831-DK
- Design software
- Link cable to PC 25-lead 1:1
- Application note
- Datasheet ATA6831 and ATA6832

3. Description

The core of the ATA6831-DK design kit is a PC-controlled application board. Using the ATA6831 design kit, users can easily adapt their loads via row connector pins (refer to ATA6831). The design software interface controls the design kit. The PWM input clamp allows to modulate the pace signal.

4. Features

- Screwless row connector pins for external loads switched by low-side or high-side drivers
- Easy and direct adaptation of loads with the ATA6831 design kit
- Direct switching of loads to V_S or GND
- Fully driver function for V_{Batt} up to 40V
- Forward/reverse rotation of DC motors by full-bridge application
- Paralleling of outputs for powerful applications
- PC linked via standard “SUB-D” connectors (plug X2 in ATA6831-DK)
- Input for 5V VCC power supply on board or externally using row connector 2
- Input pin PWM on row connector 2
- Indication of rotation direction of DC motors by LEDs, best function at V_{Batt} = 12V
- PC-controlled functions via software user interface
- All pins are easily accessible via test points

Figure 4-1. ATA6831-DK Application Board Schematic

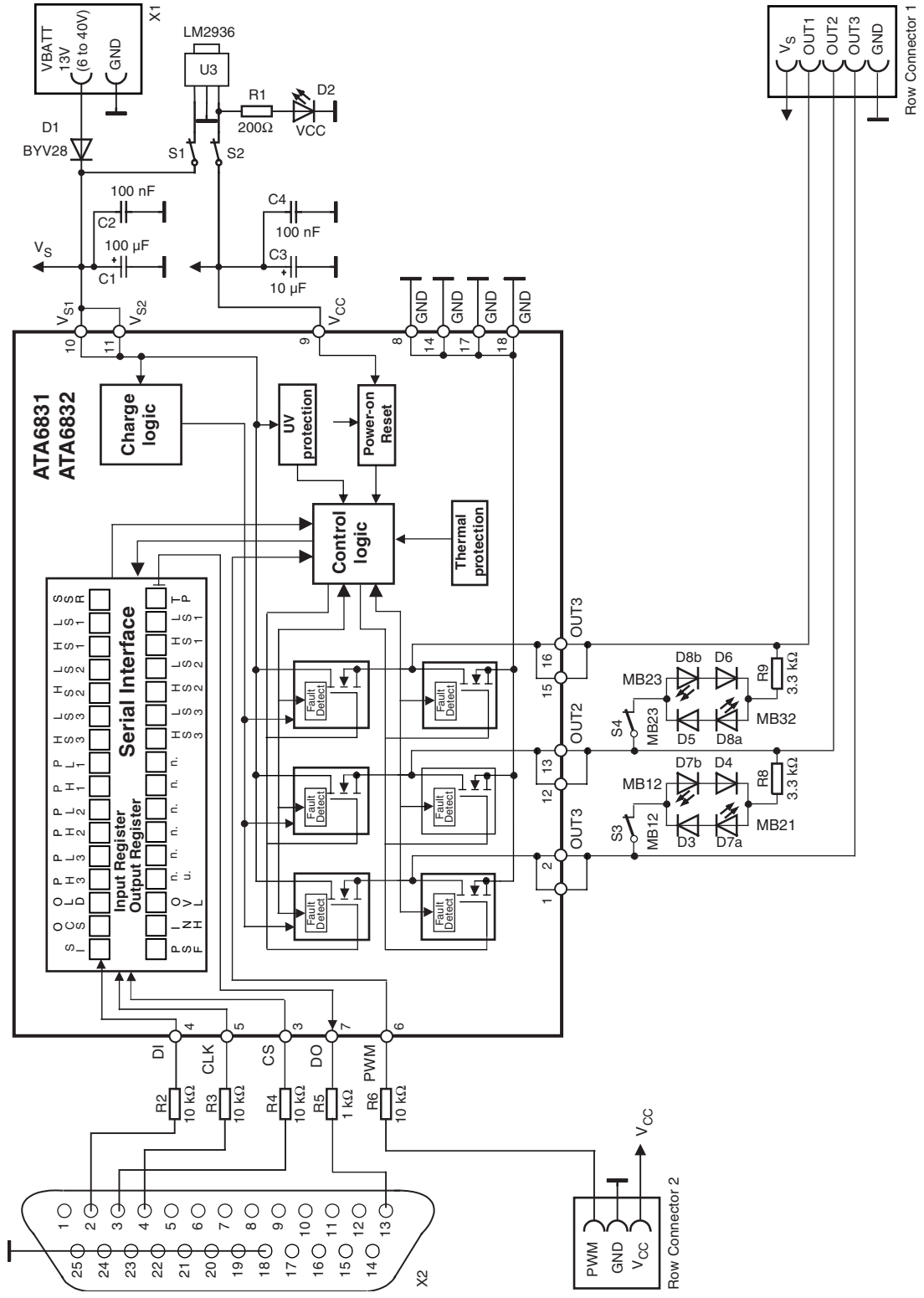


Figure 4-2. ATA6831-DK Design Kit, Application Board Component Placement; Top Side, Top View

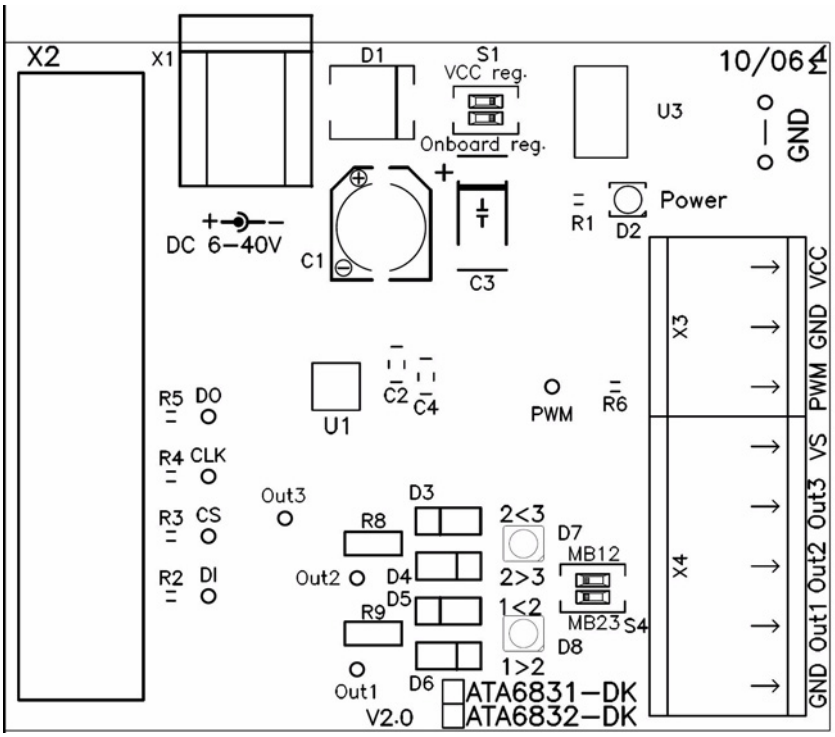


Figure 4-3. ATA6831-DK Design Kit, Application Board Top Side, Top View

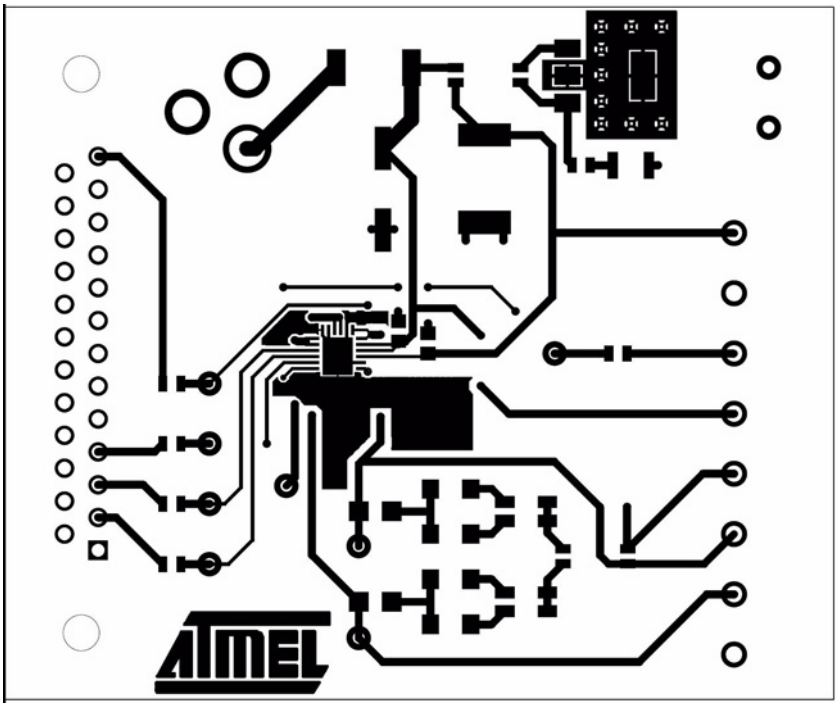
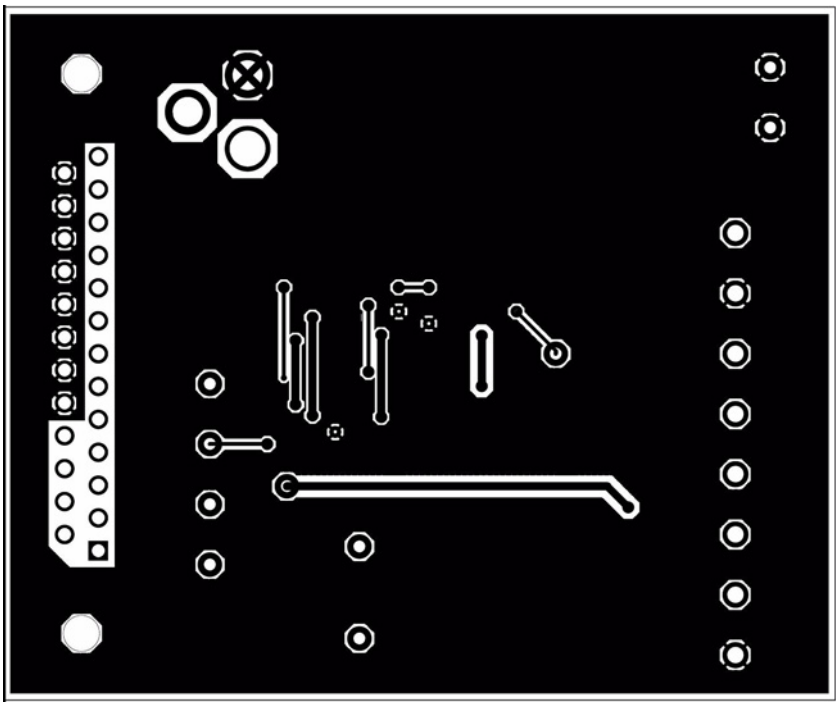


Figure 4-4. ATA6831-DK Design Kit, Application Board; Bottom Side, Top View (As if PCB were Transparent)

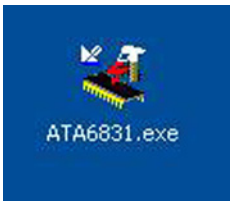


5. Design Software

5.1 Installation

The ATA6831 design kit includes the software ATA6831. The user can also download the latest revision of the software from the Atmel® web site, http://www.atmel.com/. Start the installation process by running the .exe file from the CD-ROM or from the downloaded file. The ATA6831.exe file is saved to a user-defined directory (for example, D:\Programs\ATA6831), and the system files are saved to the system directories. Use the parallel cable supplied with the kit to connect the PC's parallel port to the basic application board. Double-click the ATA6831 icon to start the software user interface (Figure 5-1).

Figure 5-1. Software Icon



5.2 Description

The ATA6831 design kit and the software user interface demonstrate the principal functions of the ATA6831 and enable designers to create a design according to their own requirements. The software user interface includes all functions of the ATA6831 and provides convenient control of the ATA6831 via the application board. Use the adjust register (representing the microcontroller) on the left side of the software user interface to pre-adjust the required input data (Figure 5-2 on page 8). Selecting PHx or PLx will switch the output stage to PWM mode; in this case an external PWM signal with 5V COMS logic level and maximum frequency up to 25 kHz has to be applied to the board. Any output set to PWM mode is tagged with a dedicated PWM symbol in the software user interface. Click the Send Data button to shift the pre-adjusted data (16 bits) into the input register of the serial peripheral interface. The output drivers are activated in accordance with the 16-bit input information. For more detailed information about the serial peripheral interface, please refer to the datasheet for ATA6831.

Click the Send Data Loop button to initiate an uninterrupted data transfer. In this case, each output is directly adjusted by switching the accessory bit. Click the Reset button to reset all bits to the starting condition. Click the End button to switch the software off.

By default, 3 input register bits are selected, setting the bits to "1" and choosing the following modes:

- SI = Software inhibit is set, for normal operation
- OCS = Overcurrent shutdown is set, activating overcurrent shutdown
- OLD = Open-load detection is set, turning open-load detection off

Before the first data word is sent, the IC is in standby (inhibit) mode. As soon as the first data word is sent, the IC reports the previous condition.

If available, up to three parallel interface ports (LPT1 to LPT3) can be selected to establish a connection. The software detects the connected port.

5.3 Ordering Information

Please contact your Atmel Sales Office or Distributor.

Figure 5-2. Software User Interface

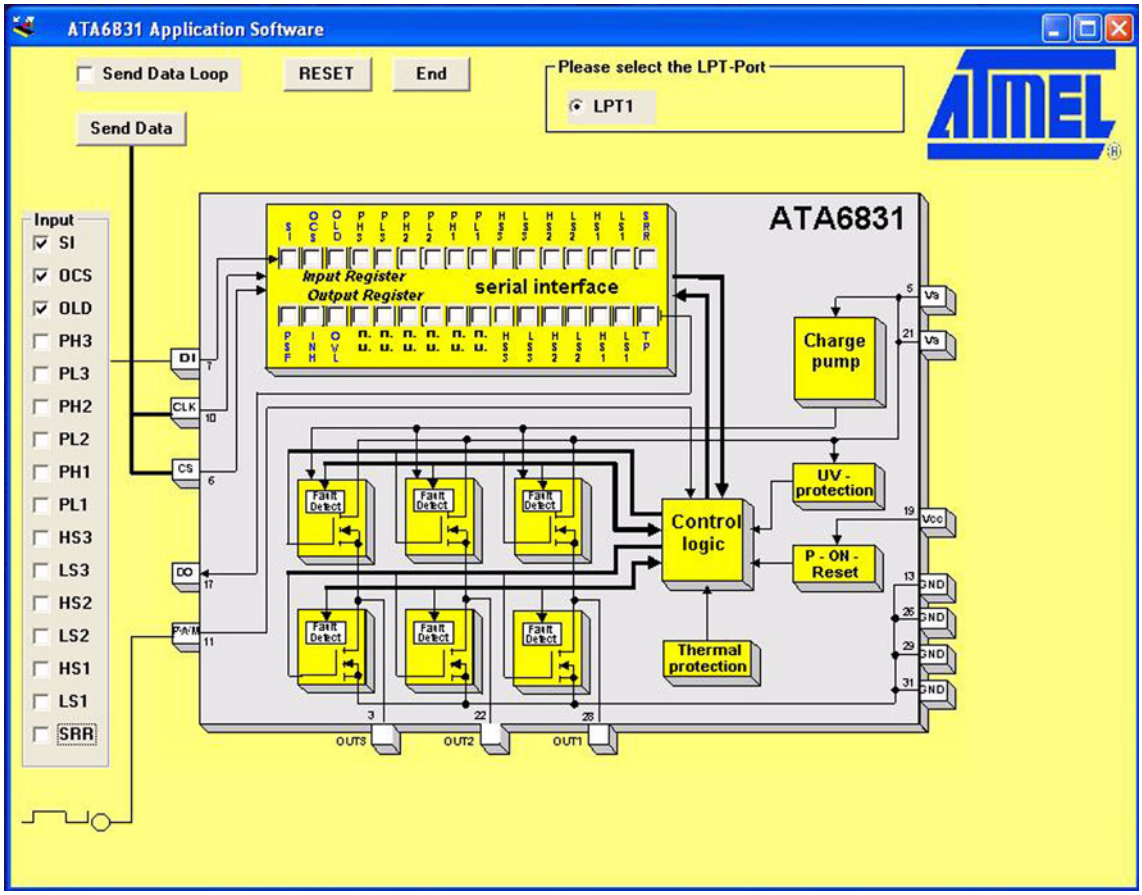


Table 5-1. Functions of the Serial Interface Register Bits

Bit	Input Register	Function
0	SRR	Status register reset (high = reset; the bits PSF, OPL, and SCD in the output data register are set to low)
1	LS1	Controls output LS1 (high = switch output LS1 on)
2	HS1	Controls output HS1 (high = switch output HS1 on)
3	LS2	See LS1
4	HS2	See HS1
5	LS3	See LS1
6	HS3	See HS1
7	PL1	Output LS1 additonally controlled by PWM input pin
8	PH1	Output HS1 additonally controlled by PWM input pin
9	PL2	See PL1
10	PH2	See PH1
11	PL3	See PL2
12	PH3	See PH2
13	OLD	Open load detection (low = open load currents are active)
14	OCS	Overcurrent shutdown (high = overcurrent shutdown is active)
15	SI	Software inhibit; low = standby, high = normal operation (data transfer is not affected by the standby function because the digital part is still powered)

6. Applications

6.1 Demonstration Application

A typical demonstration application consists of a dual full bridge arrangement with microcontroller and watchdog to control two DC motors. Such dual H-bridge arrangement with common mid-rail allows independent control of the motors for both rotation directions. Enter the appropriate dataword according to Table 6-1 on page 11 to set the required function. Instead of HSx and LSx, the corresponding bits PHx and PLx can be used to control the motor speed by an external PWM signal.

When operating in a safety-critical environment, the use of a separate watchdog IC is recommended (for example U5021M).

If OLD is activated, the open-load detection is active for all outputs stages that are currently switched off. A pull-up current for each high-side switch and a pull-down current for each low-side switch is turned on (open-load detection current IHS1-3, ILS1-3). If VVS-VHS1-3 or VLS1-3 is lower than the open load detection threshold, an open-load is detected: in the output register the corresponding bit of the appropriate output is set to high.

If no outputs were activated, all low-side drivers of half bridges are detected as open loads. This behavior is caused by the low-side open-load-detection current being larger than its high-side counterpart. This configuration ensures that with half-bridge or H-bridge applications the open-load detection also works in a well-defined way. If, for example, an open load at motor M1 should be detected, HS1 or HS2 has to be switched “on”, while the diametrical low-side output register LS2 and LS1 respectively has to be evaluated.

If INH is activated by software inhibit bit SI, all activated loads are switched off, but the input and output registers remain set.

Short-circuit detection can easily be demonstrated by intentional false activation of the half-bridge components, for example, HS1 and LS1. This causes the OVL bit in the output register to be set. Depending on the OCS bit, the affected outputs are switched off either by reaching overtemperature or by reaching overcurrent. The corresponding status bits in the output register are set to low. The OVL bit can be reset, and the disabled outputs can be re-enabled by activating the SRR bit. Please note that such activation of SRR only initiates a reset pulse, not a permanent reset state.

The overtemperature prewarning is visible at the TP bit. When the CS pin is set to low, the prewarning information is visible in real time at the DO pin because TP is the first bit of output register. Consequently, the TP bit is not buffered.

In case of overtemperature shutdown only overheated output switches off. The other outputs are not touched. The dedicated output cannot be switched on again until activating the SRR bit.

As all high-side drivers are internally connected to their low-side counterparts in order to form a half-bridge, switching from HS active to LS active or vice versa with a single programming sequence could potentially imply some shoot-through current peak across both drivers during the switching operation. The intelligent internal timing of ATA6831 guarantees that such cross-over currents are avoided.

Undervoltage detection can be demonstrated with a variable power supply. As soon as the supply voltage VVS falls below threshold, all activated loads are switched off, and the PSF bit in the output register is set. If the voltage returns to the normal level, the outputs switch on again to their previous setting. The PSF bit latches the undervoltage occurrence and needs to be reset by SRR activation in the input register.

If the IC is not used in the typical H-bridge arrangement, parallel operation of outputs is possible for more powerful applications. Two output stages at a time can be paralleled to achieve currents up to 2A.

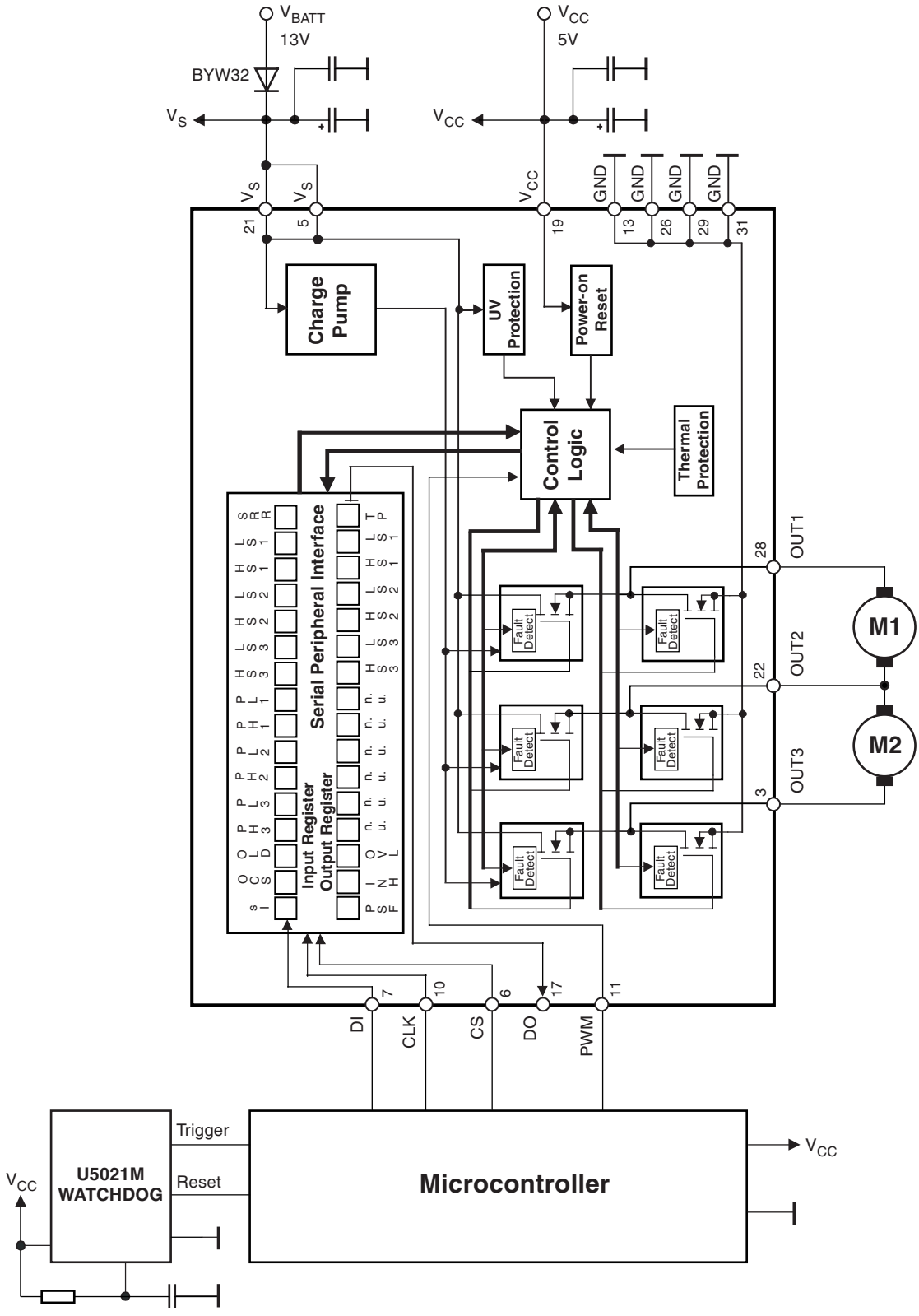
In any case, the IC's maximum power dissipation has to be considered. Excellent thermal contact to an on-board cooling area is obligatory for powerful applications.

Table 6-1. Configuration Table of Datawords Required to Set Certain Functions of the Application Circuit (See Figure 6-1 on page 12)

	Bit 13 (OCS)	Bit 6 (HS3)	Bit 5 (LS3)	Bit 4 (HS2)	Bit 3 (LS2)	Bit 2 (HS1)	Bit 1 (LS1)	Bit 0 (SRR)
M1 Forward	x			H			H	
M1 Reverse	x				H	H		
M2 Forward	x	H			H			
M2 Reverse	x		H	H				

Note: x = do not care for this demonstration; if set to high: overcurrent shutdown is active

Figure 6-1. Application with Microcontroller and Watchdog



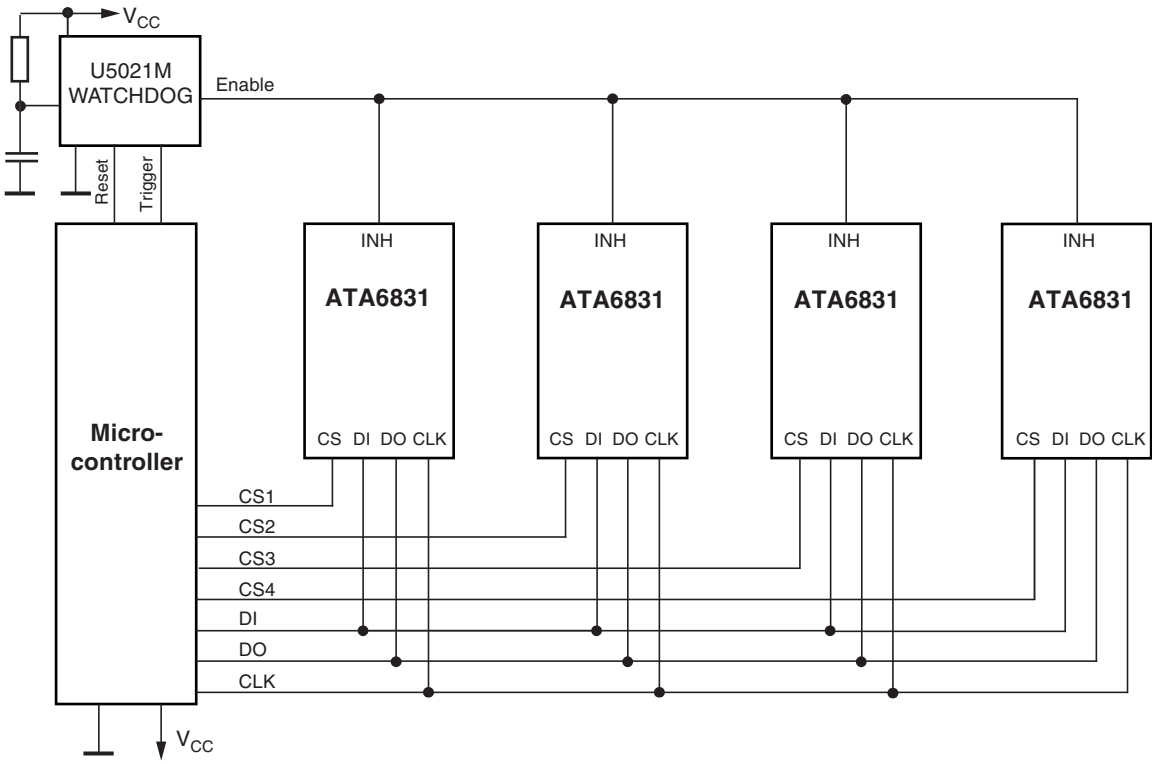
6.2 Parallel Operation of Several ATA6831s

In applications with a high number of loads, parallel operation of the ATA6831 via the microcontroller is possible.

Chip select pins CS1 to CS4 each provides an independent means of controlling the ATA6831's serial peripheral interface. (For a functional description of the serial peripheral interface, please refer to the datasheet.)

For simultaneous operation of the serial peripheral interfaces (i.e., CS1 through CS4 active at the same time), each of the data outputs (DO) needs to communicate with a dedicated microcontroller input pin.

Figure 6-2. Parallel Operation with Microcontroller and Watchdog



6.3 Daisy Chaining of Several ATA6831s

Daisy chaining is a second option available to connect several ATA6831s to the microcontroller for applications with a high number of loads. A daisy chain arrangement requires only one CS line. The data signal is handed over step-by-step from one ATA6831 to the next as long as CS signal stays low. The use of only one CS link, however, results in slower reaction times, as several programming cycles are needed to load the desired setting into each ATA6831.

The DI pin of the first IC acts as input for all ICs, and the DO of the last IC represents the output for the whole chain. The dataword intended for the last IC has to be put in first, followed by the word for the IC before and so on. In contrast to other ICs of the Atmel driver family, only a total of *n* shifts are needed for *n* ICs as any DI information is transferred immediately to the output register.

Table 6-2 clarifies the daisy chain method. The n = 3 datawords A, B, and C shall be shifted into the driver ICs 1, 2 and 3. The initial content of the registers are termed as X to Z. The required status of the input registers DI is reached after n = 3 shift operations.

Figure 6-3. Daisy Chain Operation with Microcontroller and Watchdog

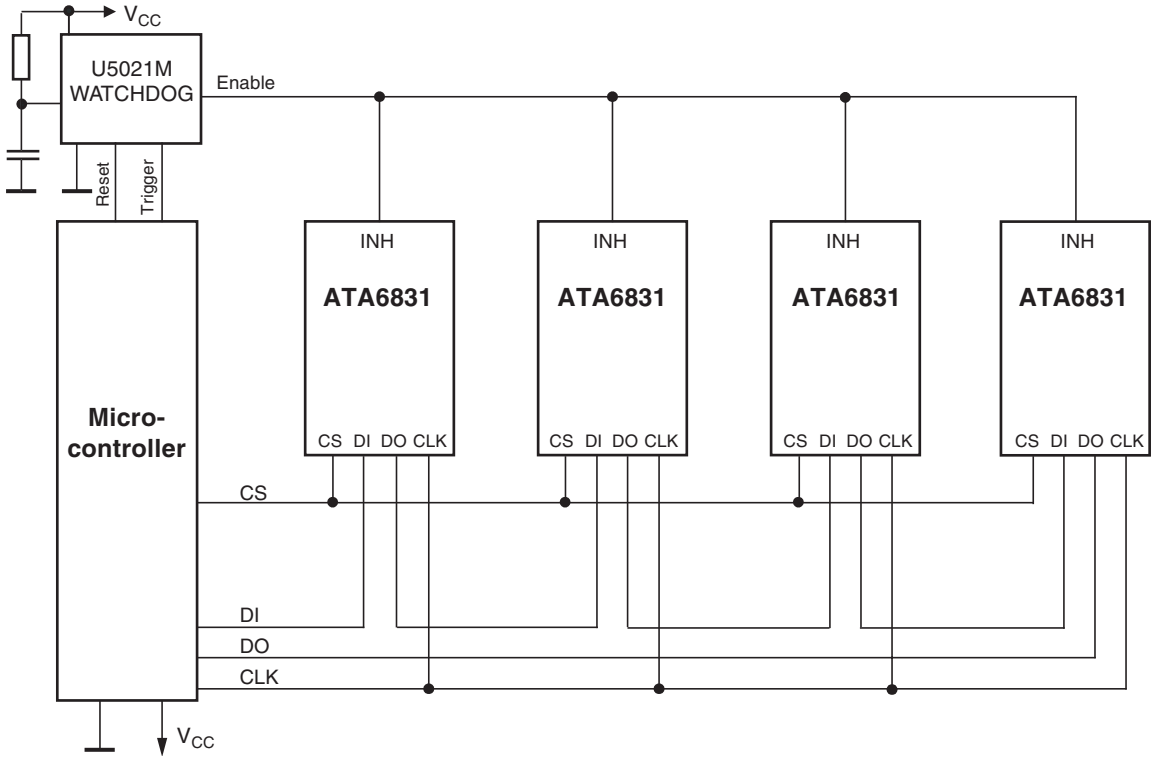


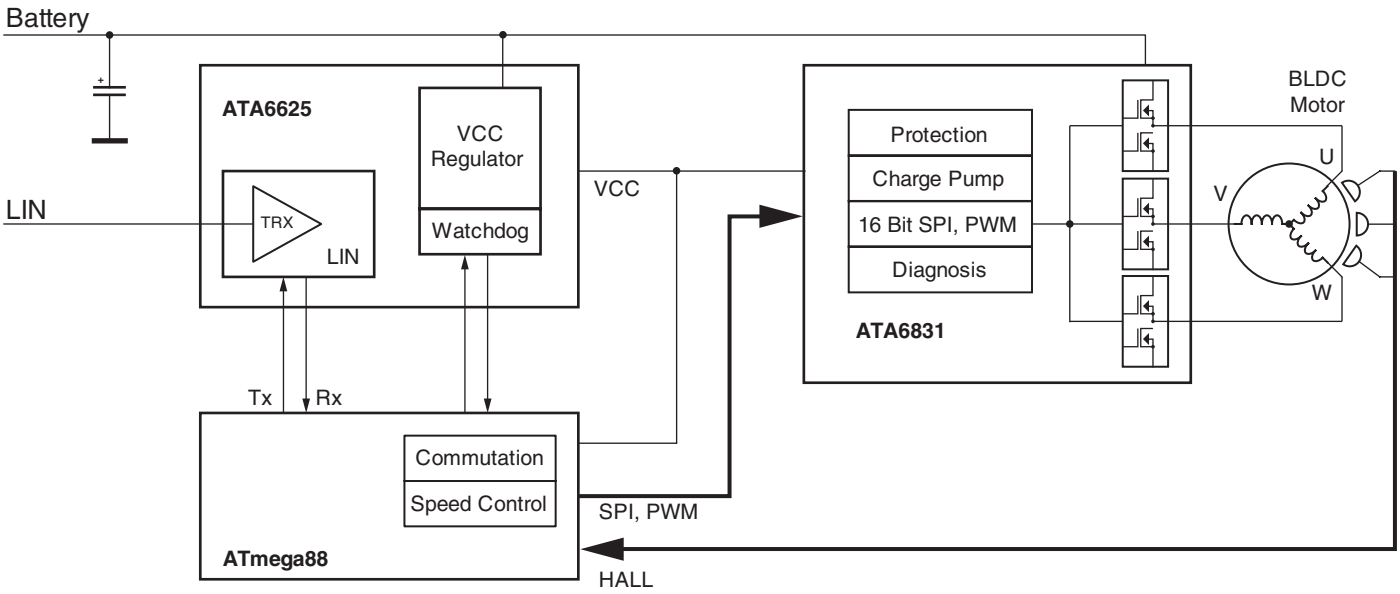
Table 6-2. Principal Method of Shifting Datawords Through Daisy-chained ICs

I/O Cycle	0			1			2		
IC number	1	2	3	1	2	3	1	2	3
DI	A			B	A		C	B	A
DO	Z	Y	X	A	Z	Y	B	A	Z

6.4 Driving a BLDC Motor with ATA6831

The PWM capability of the ATA6831 allows to run BLDC motors, see Figure 6-4. For detailed information see Application note
http://www.atmel.com/dyn/resources/prod_documents/doc4987.pdf

Figure 6-4. BLDC Motor Control Application



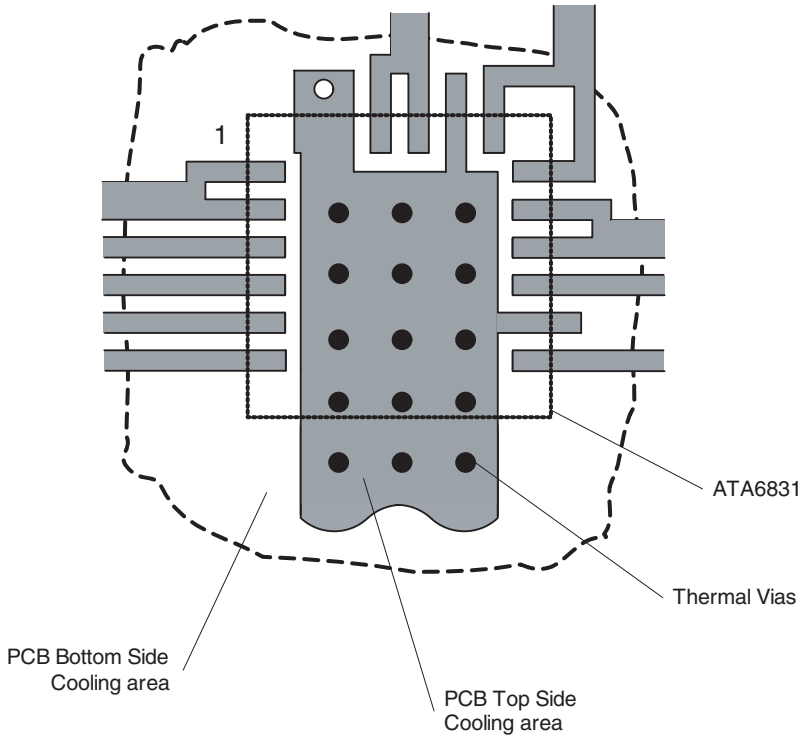
7. Thermal Considerations

7.1 Cooling Area Design

The IC should be connected to an on-board cooling area. All thermal pins (4 GND pins) as well as the exposed die pad are directly adapted to the cooling area. Figure 7-1 shows the cooling arrangement of the ATA6831's QFN 4 × 4 mm housing.

The effect of the cooling area on the PCB can be further improved if the bottom side of the PCB is ground-plated and thermal vias are placed along the cooling area. Some care should be taken of the copper area's planarity, in particular, any solder bumps arising at the thermal vias should be avoided.

Figure 7-1. Recommended Cooling Area Extension and PCB Pin Layout



8. Overload Considerations

8.1 Driver Output Shorted to V_S

During normal operation ATA6831 is protected against short circuits by an overcurrent limitation. However, some attention has to be paid to certain abnormal operating conditions that might occur in practice. In particular, consider the case of an output shorted to V_{out} while the IC is not connected to supply voltage V_S. Under these conditions, an unwanted backward current flows from the shorted output via the voltage supply pin to the capacitor C1. Figure 8-1 illustrates this situation.

The backward current I_b flows from OUTx via the HSx output stage to the VS pin until the capacitor C1 is charged to V_{out} (minus drop across the diode). Its value is strongly influenced by the capacitance of C1, but the quality of C1 (ESR) and any parasitic resistance can also have an impact. The recommended range of C1 is 22 µF to 100 µF. As stated in the ATA6831 datasheet, the maximum reverse current is 17A for a duration of 150 µs. The graph illustrated in Figure 8-2 shows the typical voltage and reverse current gradients for a capacitor value of 100 µF.

Figure 8-1. Current Flow in Case of OUTx Shorted to V_{out}

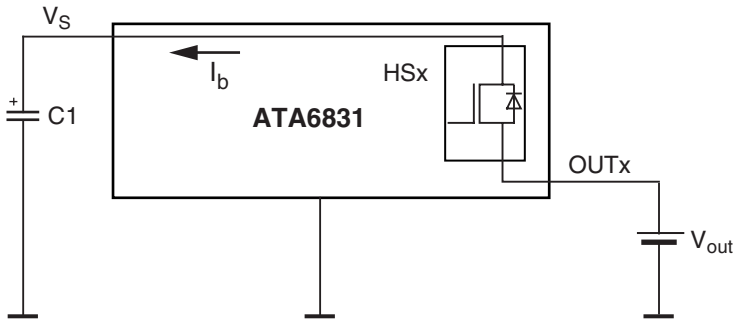
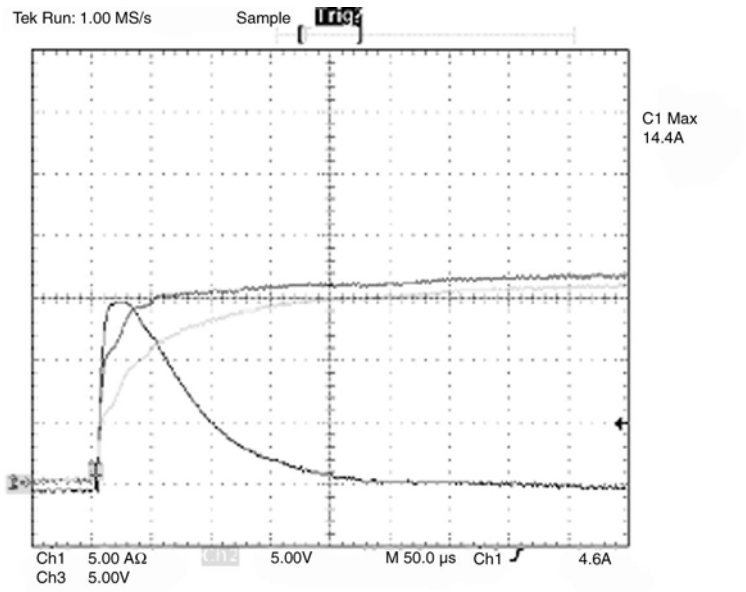


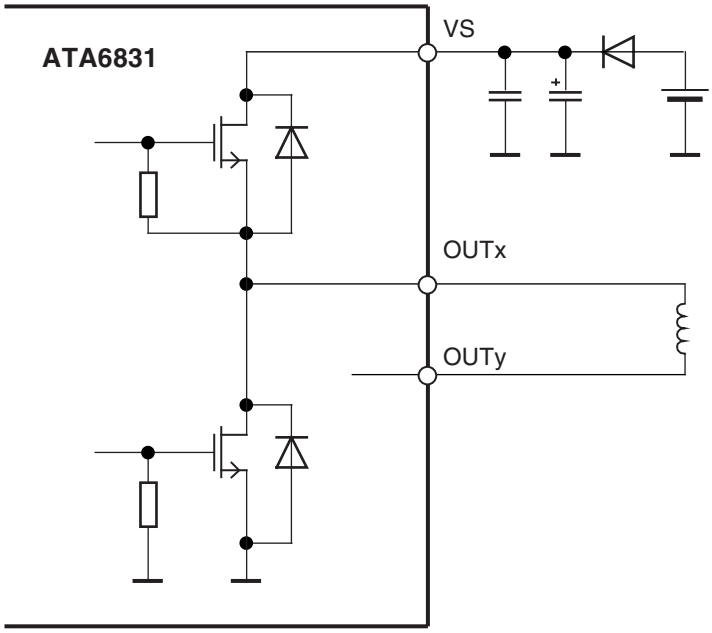
Figure 8-2. Current and Voltage Gradients for V_{out} = 16V, C1 = 100 µF; Channel 1 = I_b, Channel 2 = V_{VS}, Channel 3 = V_{out}



8.2 Inductive Shutdown

A driver IC faces a challenge when an inductive load is connected to its outputs as the energy stored in the inductance leads to a voltage peak when the load is switched off. An inductive load connected to the low-side driver outputs causes a voltage peak with positive polarity, while for the high-side outputs such peak is negative. In order to prevent any damage to the IC's output stages, some protective measures have to be implemented. Figure 8-3 illustrates the principle protection circuit of the outputs.

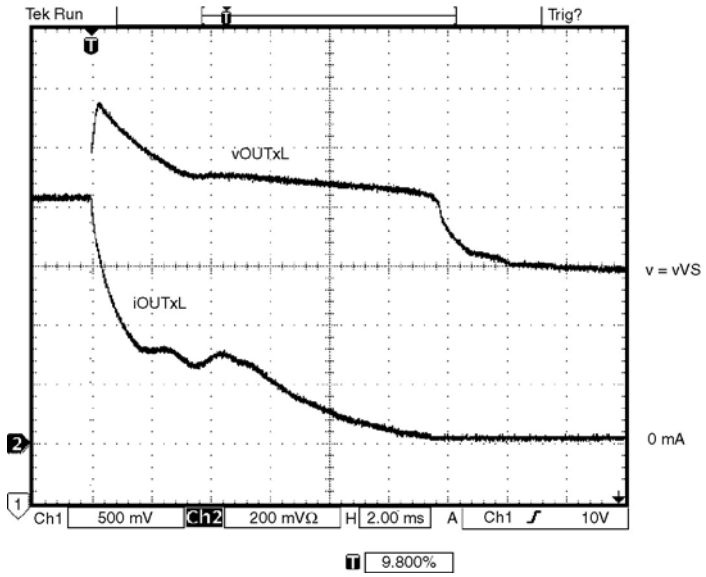
Figure 8-3. Principle Clamping Structure at a Driver Stage



The clamping structures at the output stages limit the voltage peak and provide a path for the current after switching off. The maximum inductive shutdown energy for ATA6831 is specified as 15 mJ. This value applies for both low-side and high-side outputs. The energy, WL, stored in the inductor L during the switched-on state can be calculated using the following formula:

$$W_L = \frac{L \times I_L^2}{2}$$

Figure 8-4. Inductive Pulse at Low-side Output; Channel 1: Gradient of V_{out} [10V Offset], Channel 2: Gradient of I_{out} [200 mA/Div.], Pulse Energy: W_L = 10 mJ.



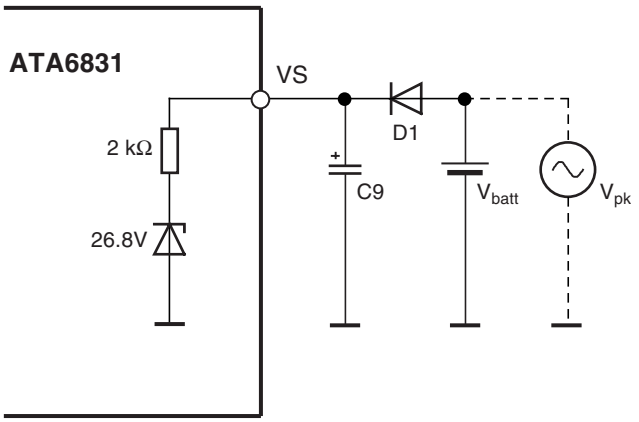
8.3 Discharger Circuit

Many applications use an inverse-polarity protection diode, such as D1 in Figure 8-5, in the power supply feed to prevent any damage if V_S is applied with the wrong polarity. Despite the popularity of this method, it involves a risk of damage.

During inhibit mode, the IC consumes only an extremely low current IVS, such as 5 µA at maximum. Any peaks on the supply voltage (V_{pk} in Figure 8-5) gradually charge the blocking capacitor (C9 in Figure 8-5). D1 prevents the capacitor from discharging via the power supply. Because of the extremely small quiescent current, discharging via the IC can also be neglected.

This means that during long periods in inhibit mode, the IC's supply voltage could increase continuously until the maximum supply voltage limit of 40V is exceeded, damaging the IC. ATA6831, therefore, features a discharger circuit that prevents such unwanted effects. If V_S exceeds a threshold value of approximately 27V, the blocking capacitor is discharged via an integrated resistor until V_S falls again below the threshold.

Figure 8-5. Functional Principle of the Discharger Circuit



Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054
Saint-Quentin-en-Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
auto_control@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature