High-Performance
128K×9
CMOS SRAM

AS7C1029
AS7C1029L

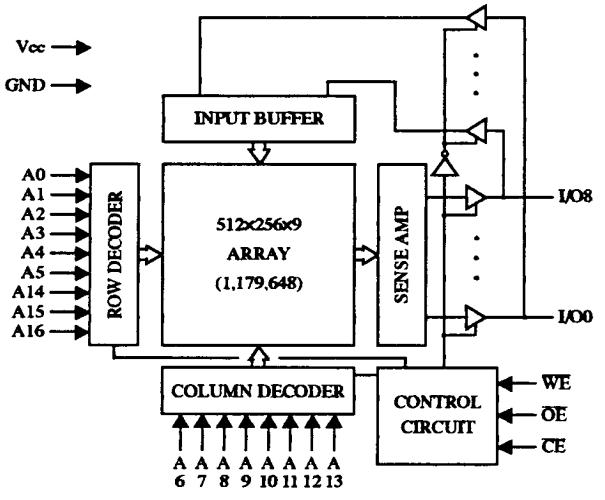
PRELIMINARY

128K×9 CMOS SRAM (Common I/O)

FEATURES

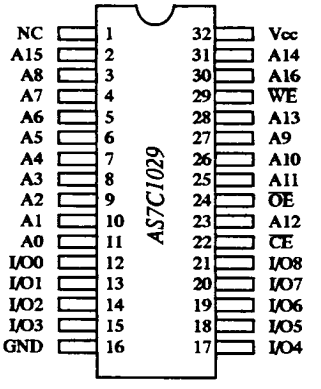
- Organization: 131,072 words × 9 bits
- High speed
  - 15/20/25/35 ns address access time
  - 4/5/6/8 ns output enable access time
- Low power consumption
  - Active: 660 mW max (15 ns cycle)
  - Standby: 27.5 mW max, CMOS I/O
    2.75 mW max, CMOS I/O, L version
  - Very low DC component in active power
- 2.0V data retention (L version)
- Equal access and cycle times
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
- Popular 32-pin packages
  - 300 and 400 mil PDIP
  - 300 and 400 mil SOJ
- ESD protection > 2000 volts
- Latch-up current > 200 mA

LOGIC BLOCK DIAGRAM



PIN ARRANGEMENT

DIP, SOJ



SELECTION GUIDE

		7C1029-15	7C1029-20	7C1029-25	7C1029-35	Unit
Maximum address access time		15	20	25	35	ns
Maximum output enable access time		4	5	6	8	ns
Maximum operating current		120	110	100	90	mA
Maximum standby current		5.0	5.0	5.0	5.0	mA
	L	0.5	0.5	0.5	0.5	mA

FUNCTIONAL DESCRIPTION

The AS7C1029 is a high performance CMOS 1,179,648-bit Static Random-Access Memory (SRAM) organized as 131,072 words of 9 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 15/20/25/35 ns with output enable access times (t_{OE}) of 4/5/6/8 ns are ideal for high performance applications. A chip enable ($\overline{CE}$) input permits easy memory expansion with multiple-bank memory organizations.

When $\overline{CE}$ is HIGH the device enters standby mode. The standard AS7C1029 is guaranteed not to exceed 27.5 mW power consumption in standby mode; the L version is guaranteed not to exceed 2.75 mW, and typically requires only 800 µW. The L version also offers 2.0V data retention, with maximum power consumption in this mode of 400 µW.

A write cycle is accomplished by asserting chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) LOW. Data on the input pins I/O0-I/O8 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW, with write enable ($\overline{WE}$) HIGH. The chip drives I/O pins with the data word referenced by the input address. When chip enable or output enable is HIGH, or write enable is LOW, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5V supply. The AS7C1029 is packaged in high volume industry standard packages.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Voltage on Any Pin Relative to GND	V_t	-0.5	+7.0	V
Power Dissipation	P_D	—	1.0	W
Storage Temperature (Plastic)	T_{stg}	-55	+150	°C
Temperature Under Bias	T_{bias}	-10	+85	°C
DC Output Current	I_{out}	—	20	mA

NOTE: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High-Z	Standby (I_{SB}, I_{SB1})
L	H	H	High-Z	Output Disable
L	H	L	D_{out}	Read
L	L	X	D_{in}	Write

RECOMMENDED OPERATING CONDITIONS (T_a = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	-0.5*	—	0.8	V

* V_{IL} min = -3.0V for pulse width less than 10 ns.

DC OPERATING CHARACTERISTICS [1] (V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

Parameter	Sym	Test Conditions		-15		-20		-25		-35		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC} = Max, V_{in} = GND to V_{CC}		—	1	—	1	—	1	—	1	µA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CE}$ = V_{IH}, V_{CC} = Max, V_{out} = GND to V_{CC}		—	1	—	1	—	1	—	1	µA
Operating Power Supply Current	I_{CC}	$\overline{CE}$ = V_{IL}, $f = f_{max}$, I_{out} = 0 mA		—	120	—	110	—	120	—	110	mA
			L	—	115	—	105	—	115	—	105	mA
Standby Power Supply Current	I_{SB}	$\overline{CE}$ = V_{IH}, $f = f_{max}$		—	15	—	15	—	15	—	15	mA
			L	—	10	—	10	—	10	—	10	mA
	I_{SB1}	$\overline{CE}$ > V_{CC}–0.2V, f = 0, V_{in} ≤ 0.2V *or* V_{in} ≥ V_{CC}–0.2V		—	5.0	—	5.0	—	5.0	—	5.0	mA
			L	—	0.5	—	0.5	—	0.5	—	0.5	mA
Output Voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min		—	0.4	—	0.4	—	0.4	—	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min		2.4	—	2.4	—	2.4	—	2.4	—	V

CAPACITANCE [2] (f = 1 MHz, T_a = Room Temperature, V_{CC} = 5V)

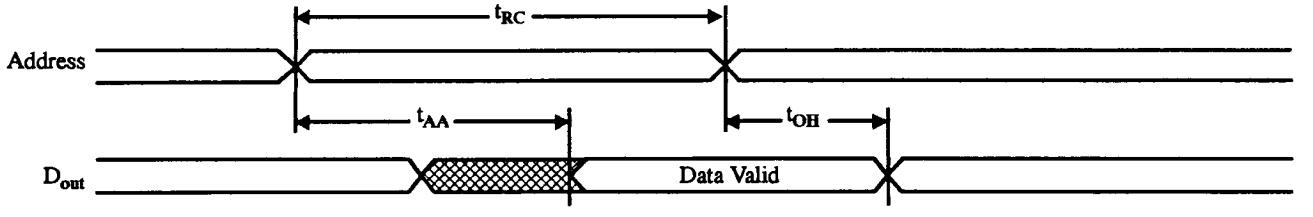
Parameter	Symbol	Signals	Test Conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$	V_{in} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{in} = V_{out} = 0V	7	pF

READ CYCLE[3, 9]

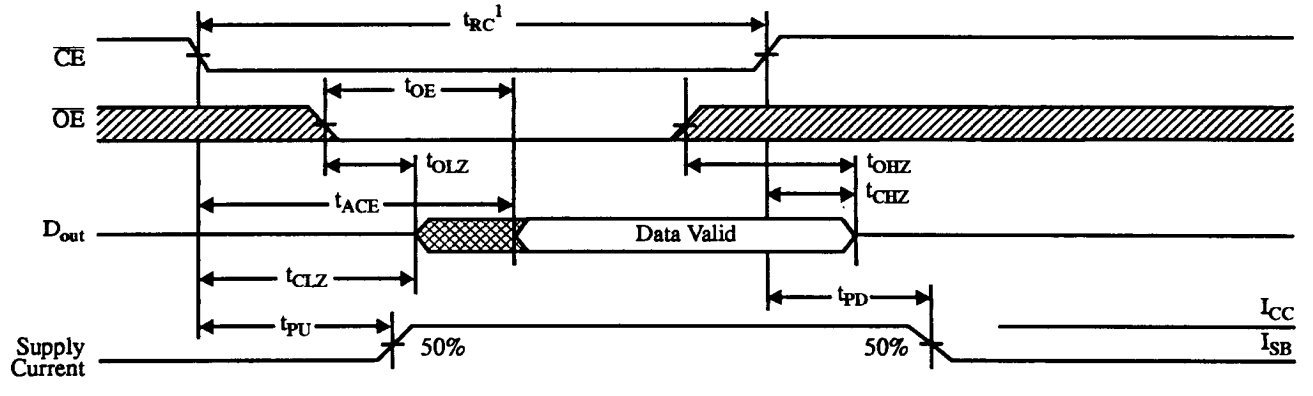
(V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

Parameter	Sym	-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{RC}	15	—	20	—	25	—	35	—	ns	
Address Access Time	t_{AA}	—	15	—	20	—	25	—	35	ns	3
Chip Enable ($\overline{CE}$) Access Time	t_{ACE}	—	15	—	20	—	25	—	35	ns	3
Output Enable ($\overline{OE}$) Access Time	t_{OE}	—	4	—	5	—	6	—	8	ns	
Output Hold from Address Change	t_{OH}	3	—	3	—	3	—	3	—	ns	5
Chip Enable to Output in Low Z	t_{CLZ}	3	—	3	—	3	—	3	—	ns	4, 5
Chip Disable to Output in High Z	t_{CHZ}	—	4	—	5	—	6	—	8	ns	4, 5
Output Enable to Output in Low Z	t_{OLZ}	0	—	0	—	0	—	0	—	ns	4, 5
Output Disable to Output in High Z	t_{OHZ}	—	4	—	5	—	6	—	8	ns	4, 5
Chip Enable to Power Up Time	t_{PU}	0	—	0	—	0	—	0	—	ns	4, 5
Chip Disable to Power Down Time	t_{PD}	—	15	—	20	—	25	—	35	ns	4, 5

TIMING WAVEFORM OF READ CYCLE 1[3, 6, 7, 9] (Address controlled)



TIMING WAVEFORM OF READ CYCLE 2[3, 6, 8, 9] ($\overline{CE}$ controlled)



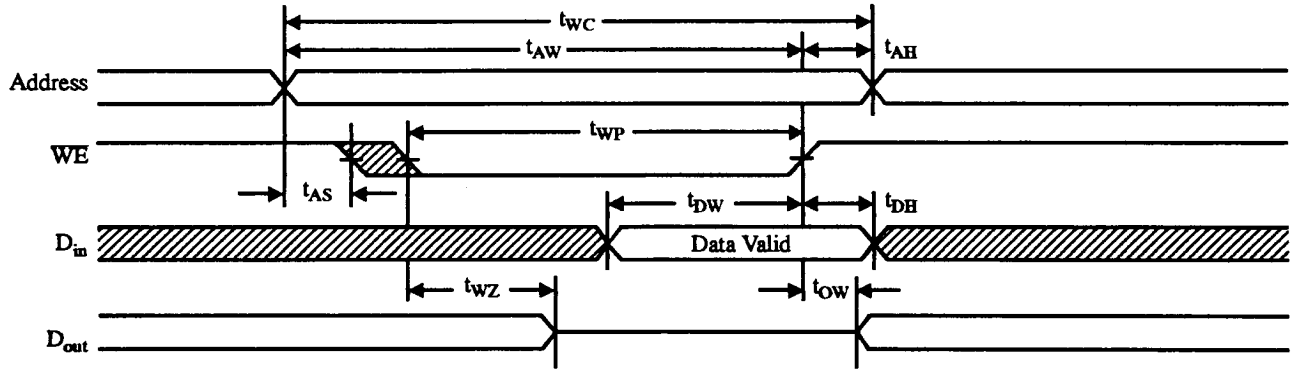
WRITE CYCLE [11]

(V_{CC} = 5V±10%, GND = 0V, T_a = 0 to +70°C)

Parameter	Sym	-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{WC}	15	—	20	—	20	—	30	—	ns	
Chip Enable to Write End	t_{CW}	10	—	12	—	15	—	20	—	ns	
Address Set-up to Write End	t_{AW}	10	—	12	—	15	—	20	—	ns	
Address Set-up Time	t_{AS}	0	—	0	—	0	—	0	—	ns	
Write Pulse Width	t_{WP}	9	—	12	—	15	—	17	—	ns	
Address Hold From End of Write	t_{AH}	0	—	0	—	0	—	0	—	ns	
Data Valid to Write End	t_{DW}	9	—	12	—	15	—	15	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	0	—	0	—	ns	4, 5
Write Enable to Output in High Z	t_{WZ}	—	5	—	5	—	5	—	5	ns	4, 5
Output Active from Write End	t_{OW}	3	—	3	—	3	—	3	—	ns	4, 5

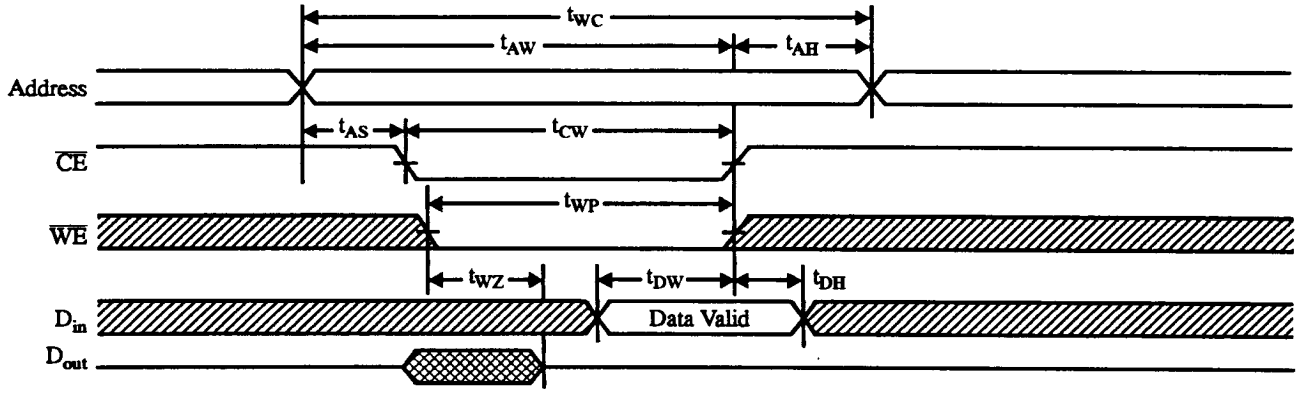
TIMING WAVEFORM OF WRITE CYCLE 1 [10, 11]

($\overline{WE}$ controlled)



TIMING WAVEFORM OF WRITE CYCLE 2 [10, 11]

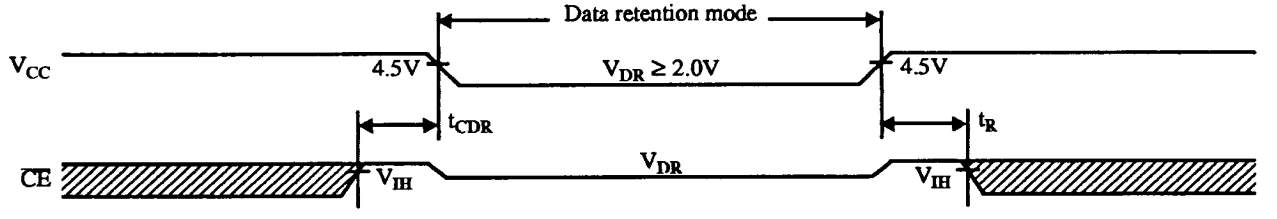
($\overline{CE}$ controlled)



DATA RETENTION CHARACTERISTICS (L version only)

Parameter	Symbol	Test Conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	V_{CC} = 2.0V $\overline{CE} \geq V_{CC}-0.2V$ $V_{in} \geq V_{CC}-0.2V$ *or* $V_{in} \leq 0.2V$	2.0	—	V
Data retention current	I_{CCDR}		—	200	µA
Chip deselect to data retention time	t_{CDR}		0	—	ns
Operation recovery time	t_R		t_{RC}	—	ns
Input leakage current	$\lvert I_{LI} \rvert$		—	1	µA

DATA RETENTION WAVEFORM (L version only)



AC TEST CONDITIONS

- Output load: see Figure B, except for t_{CLZ} and t_{CHZ} see Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

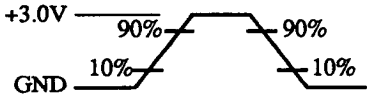


Figure A. Input Waveform

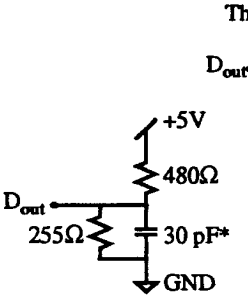


Figure B. Output Load

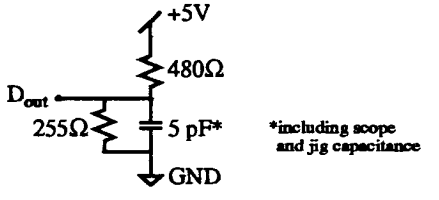


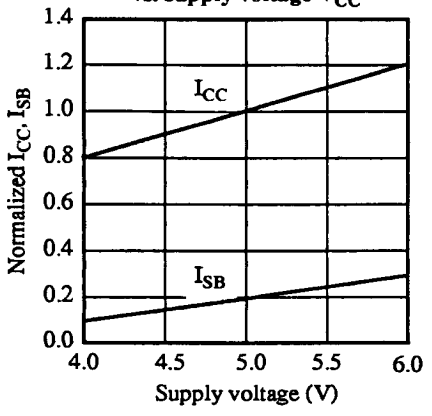
Figure C. Output Load for t_{CLZ}, t_{CHZ}

NOTES

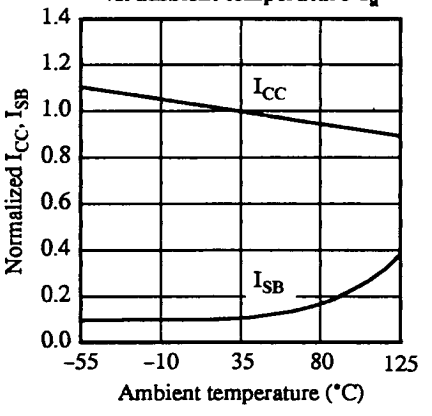
1. During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
2. This parameter is sampled and not 100% tested.
3. For test conditions, see AC Test Loads and Waveforms, Figures A, B, C.
4. t_{CLZ} and t_{CHZ} are specified with CL = 5pF as in Figure C. Transition is measured 500mV from steady-state voltage.
5. This parameter is guaranteed but not tested.
6. $\overline{WE}$ is high for read cycle
7. $\overline{CE}$ and $\overline{OE}$ are low for read cycle.
8. Address valid prior to or coincident with $\overline{CE}$ transition low.
9. All read cycle timings are referenced from the last valid address to the first transitioning address.
10. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.
11. All write cycle timings are referenced from the last valid address to the first transitioning address.

TYPICAL DC and AC CHARACTERISTICS

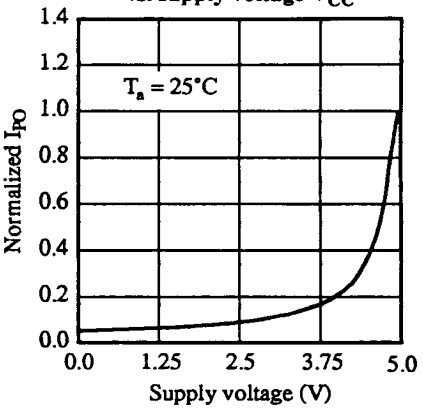
Normalized supply current I_{CC}, I_{SB} vs. supply voltage V_{CC}



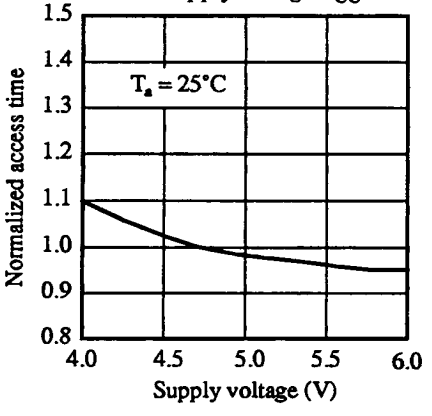
Normalized supply current I_{CC}, I_{SB} vs. ambient temperature T_a



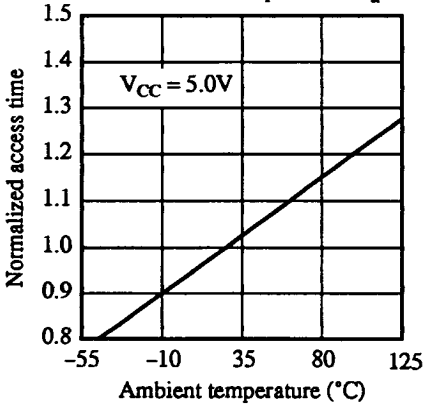
Normalized power-on current I_{PO} vs. supply voltage V_{CC}



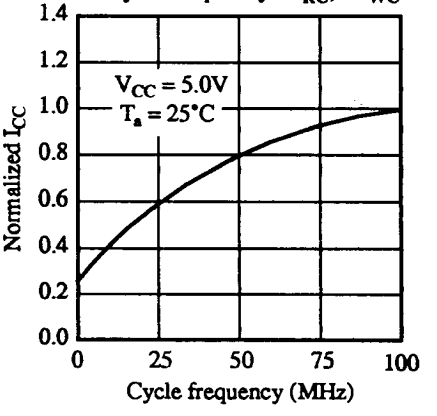
Normalized access time t_{AA} vs. supply voltage V_{CC}



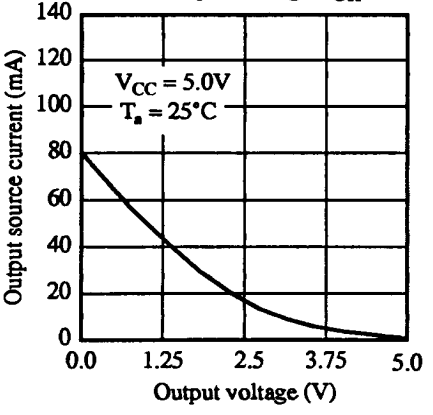
Normalized access time t_{AA} vs. ambient temperature T_a



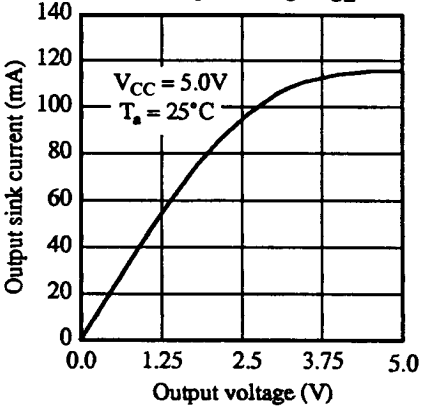
Normalized supply current I_{CC} vs. cycle frequency $1/t_{RC}$, $1/t_{WC}$



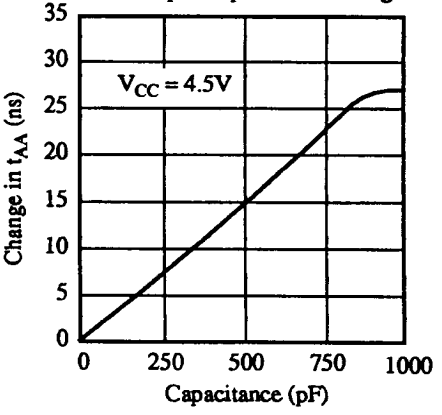
Output source current I_{OH} vs. output voltage V_{OH}



Output sink current I_{OL} vs. output voltage V_{OL}



Typical access time change Δt_{AA} vs. output capacitive loading



ORDERING CODES

Package	Address Access Time			
	15 ns	20 ns	25 ns	35 ns
Plastic DIP, 300 mil	AS7C1029-15TPC AS7C1029L-15TPC	AS7C1029-20TPC AS7C1029L-20TPC	AS7C1029-25TPC AS7C1029L-25TPC	AS7C1029-35TPC AS7C1029L-35TPC
Plastic DIP, 400 mil	AS7C1029-15PC AS7C1029L-15PC	AS7C1029-20PC AS7C1029L-20PC	AS7C1029-25PC AS7C1029L-25PC	AS7C1029-35PC AS7C1029L-35PC
Plastic SOJ, 300 mil	AS7C1029-15TJC AS7C1029L-15TJC	AS7C1029-20TJC AS7C1029L-20TJC	AS7C1029-25TJC AS7C1029L-25TJC	AS7C1029-35TJC AS7C1029L-35TJC
Plastic SOJ, 400 mil	AS7C1029-15JC AS7C1029L-15JC	AS7C1029-20JC AS7C1029L-20JC	AS7C1029-25JC AS7C1029L-25JC	AS7C1029-35JC AS7C1029L-35JC

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