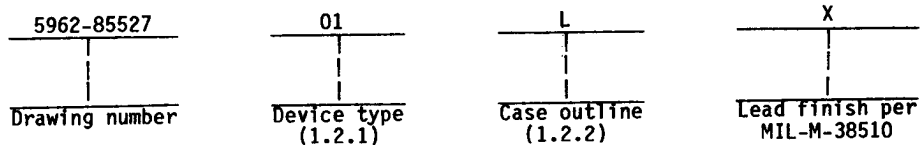


1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Clock-to-output delay
01	27S45	2048 x 8 bit registered PROM with programmable INITIALIZE (Asynchronous)	30 ns
02	27S45A	2048 x 8 bit registered PROM with programmable INITIALIZE (Asynchronous)	25 ns
03	27S47	2048 x 8 bit registered PROM with programmable INITIALIZE (Synchronous)	30 ns
04	27S47A	2048 x 8 bit registered PROM with programmable INITIALIZE (Synchronous)	25 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
K	F-6 (24-lead, 3/8" x 5/8"), flat package
L	D-9 (24-lead, 1/4" x 1 1/4"), dual-in-line package
X	C-12 (32-terminal, .450" x .550"), rectangular chip carrier package
3	C-4 (28-terminal, .450" x .450"), square chip carrier package

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1.3 Absolute maximum ratings.

Supply voltage range - - - - -	-0.5 V dc to +7.0 V dc
DC input voltage - - - - -	-0.5 V dc to +5.5 V dc
DC voltage applied to outputs - - - - -	-0.5 V dc to +5.5 V dc
DC input current - - - - -	-30 mA to +5.0 mA
Storage temperature range - - - - -	-65°C to +150°C
Maximum power dissipation (P _D) ^{1/} - - - - -	1.02 W
Lead temperature (soldering, 10 seconds) - - - - -	+300°C
Thermal resistance, junction-to-case (θ _{JC}): ^{2/}	
Case K - - - - -	53°C/W) see MIL-M-38510, appendix C
Case L - - - - -	40°C/W
Case X - - - - -	75°C/W ^{3/}
Case 3 - - - - -	80°C/W ^{3/}
Junction temperature (T _J) - - - - -	+175°C
DC voltage applied to outputs during programming - - - - -	21 V dc
DC current into outputs during programming (max duration of 1.0 s) - - - - -	250 mA dc

1.4 Recommended operating conditions.

Supply voltage (V _{CC}) - - - - -	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V _{IH}) - - - - -	2.0 V dc
Maximum low level input voltage (V _{IL}) - - - - -	0.8 V dc
Case operating temperature range (T _C) - - - - -	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

- ^{1/} Must withstand the added P_D due to short circuit test (e.g., I_{OS}).
- ^{2/} Heat sinking is recommended to reduce the junction temperature.
- ^{3/} When a thermal resistance value for this case is included in MIL-M-38510, appendix C, that value shall supersede the value indicated herein.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Logic diagram. The logic diagram shall be as specified on figure 2.

3.2.3 Truth table.

3.2.3.1 Unprogrammed devices. Testing to the applicable truth table, or alternate testing as specified in 4.3.1c, shall be used for unprogrammed devices for contracts involving no altered item drawing. When testing is required in accordance with 4.3 herein, the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.3.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.4 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.9 Processing options. Since the PROM is an unprogrammed memory capable of being programmed by either the manufacturer or the user to result in a wide variety of PROM configurations, two processing options are provided for selection, using an altered item drawing.

3.9.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1, tables II and III. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.9.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing shall be satisfied by the manufacturer prior to delivery.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C < T _C < +125°C 4.5 V < V _{CC} < 5.5 V (unless otherwise specified)	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Output high voltage	V _{OH}	V _{CC} = 4.5 V, V _{IN} = V _{IH} or V _{IL} , I _{OH} = -2.0 mA	A11	1, 2, 3	2.4		V
Output low voltage	V _{OL}	V _{CC} = 4.5 V, I _{OL} = 16 mA V _{IN} = V _{IH} or V _{IL}	A11	1, 2, 3		0.50	V
Input high voltage	V _{IH}	2/ 3/	A11	1, 2, 3	2.0		V
Input low voltage	V _{IL}	2/ 3/	A11	1, 2, 3		0.8	V
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V, I _{IN} = -18 mA	A11	1, 2, 3		-1.2	V
Input low current	I _{IL}	V _{CC} = 5.5 V, V _{IN} = 0.45 V	A11	1, 2, 3		-.250	mA
Input high current	I _{IH}	V _{CC} = 5.5 V, V _{IN} = 5.5 V	A11	1, 2, 3		40	μA
Output short-circuit current	I _{OS}	V _{CC} = 5.5 V, V _{OUT} = 0 V 4/	A11	1, 2, 3	-20	-90	mA
Power supply current	I _{CC}	V _{CC} = 5.5 V, All inputs = GND	A11	1, 2, 3		185	mA
Output leakage current	I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	A11	1, 2, 3		40	μA
		V _E = 2.4 V, V _O = 0.4 V	A11	1, 2, 3		-40	μA
Functional tests		See 4.3.1d	A11	7, 8			
Input capacitance	C _{IN}	V _{IN} = 2.0 V, f = 1.0 MHz 5/	A11	4		8.0	pF
Output capacitance	C _{OUT}	V _{OUT} = 2.0 V, f = 1.0 MHz 5/	A11	4		15.0	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V (unless otherwise specified)	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Address to K high, setup time	TAVKH	6/ See figure 3	02, 04	9, 10, 11	45		ns
				01, 03	50		ns
Address to K high, hold time	TKHAX		A11	9, 10, 11	0		ns
Delay from K high to output valid, for initially active outputs (high or low)	TKHQV1		02, 04	9, 10, 11		25	ns
				01, 03	9, 10, 11		30
K pulse width (high or low)	TKHKL, TKLKH		A11	9, 10, 11	20		ns
\overline{GS} to K high setup time	TGSVKH		A11	9, 10, 11	15		ns
\overline{GS} to K high hold time	TKHGSX		A11	9, 10, 11	5.0		ns
Delay from \overline{I} low to output valid (high or low) 7/	TILQV		01	9, 10, 11		40	ns
				02	9, 10, 11		35
Asynchronous \overline{I} recovery to K (high) 7/	TIHKH		01	9, 10, 11	25		ns
				02	9, 10, 11	20	
Asynchronous \overline{I} pulse width (low) 7/	TILIH		01, 02	9, 10, 11	30		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

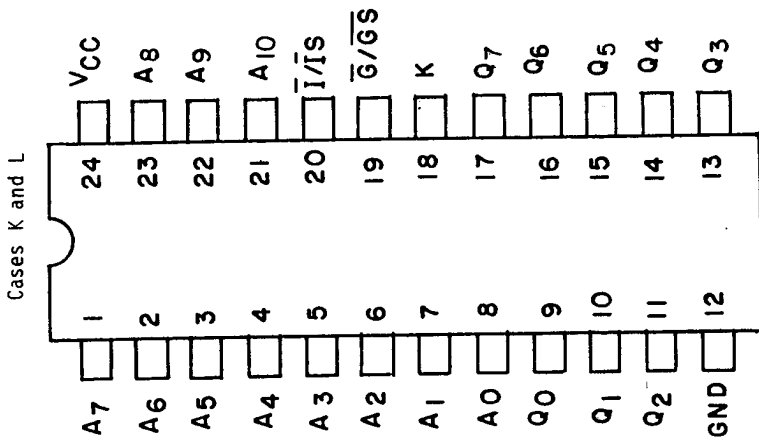
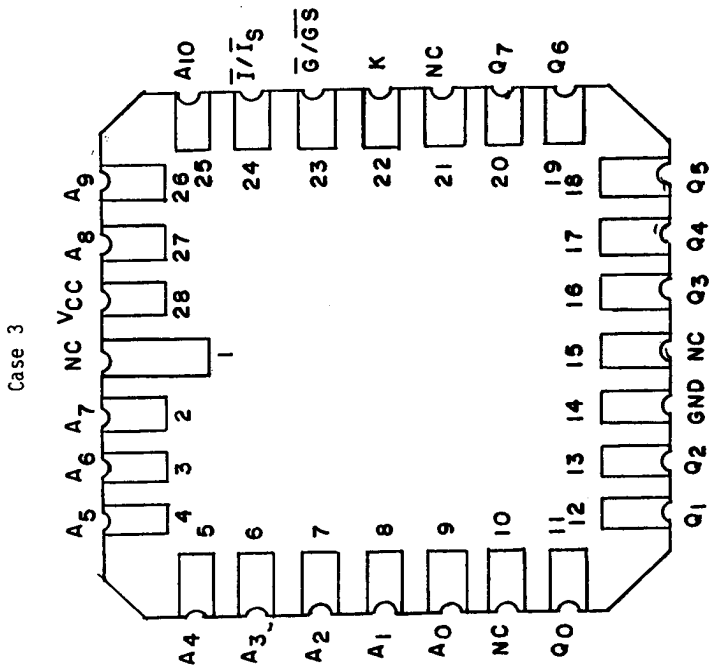
Test	Symbol	Conditions 1/ -55°C < T _C < +125°C 4.5 V < V _{CC} < 5.5 V (unless otherwise specified)	Device type	Group A subgroups	Limits		Unit
					Min	Max	
IS to K high setup time 8/	TISVKH 6/	See figure 3	03	9, 10, 11	35		ns
			04	9, 10, 11	30		ns
IS to K high hold time 8/	TKHISX		03, 04	9, 10, 11	0		ns
Delay from K high to output valid for initially high-Z outputs	TKHQV2		01, 03	9, 10, 11		35	ns
			02, 04	9, 10, 11		30	ns
Delay from G low to output valid (high or low)	TGLQV		01, 03	9, 10, 11		35	ns
			02, 04	9, 10, 11		30	ns
Delay from K high to output high-Z 9/	TKHQZ		01, 03	9, 10, 11		35	ns
			02, 04	9, 10, 11		30	ns
Delay from G high to output high-Z 9/	TGHQZ		01, 03	9, 10, 11		35	ns
			02, 04	9, 10, 11		30	ns

- 1/ All voltages given are referenced to the test system ground for ac and functional testing. Voltages given for dc testing are referenced to the microcircuit ground terminal.
- 2/ These are absolute voltages with respect to device ground pin and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.
- 3/ V_{IL} and V_{IH} threshold levels are guaranteed for 0.8 V and 2.0 V respectively during dc testing. For ac and functional testing V_{IL} and V_{IH} limits of -0.2 V and 4.0 V are implemented to allow for noise margins needed in a high speed, automated test equipment environment, when fast switching of multiple I/O's is encountered.
- 4/ Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.
- 5/ These parameters are not 100 percent tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.
- 6/ AC tests are performed with input 10 to 90 percent rise and fall times of 5 ns or less.
- 7/ Applies only when programmable initialize is in the asynchronous operation mode.
- 8/ Applies only when programmable initialize is in the synchronous operation mode.
- 9/ TKHQZ and TGHQZ are measured to the V_{OH}-0.5 V and V_{OL}+0.5 V output levels respectively. All other switching parameters are tested from and to the 1.5 V threshold levels.

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Device types 01 through 04



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FIGURE 1. Terminal connections (top view).

Case X

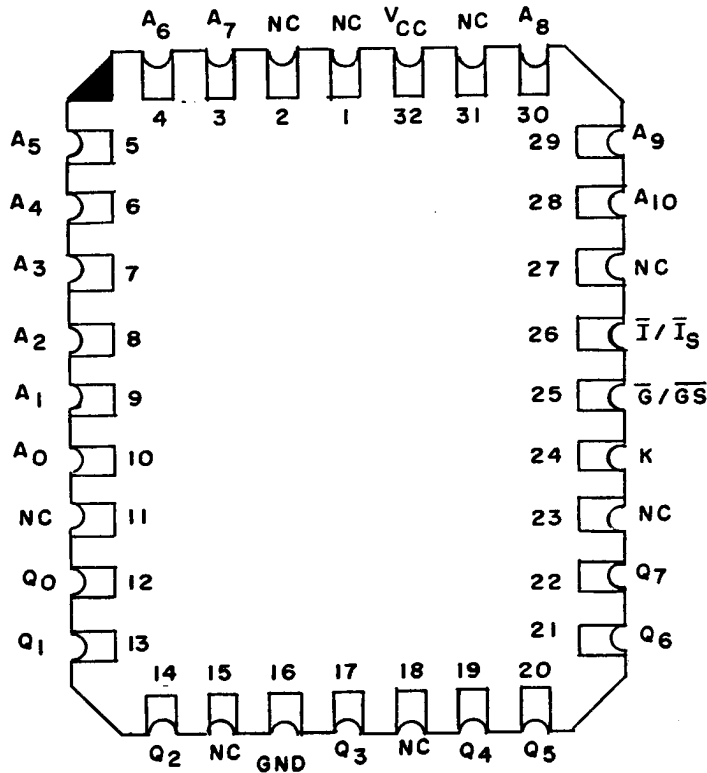


FIGURE 1. Terminal connections (top view) - Continued.

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Device types 01 and 02

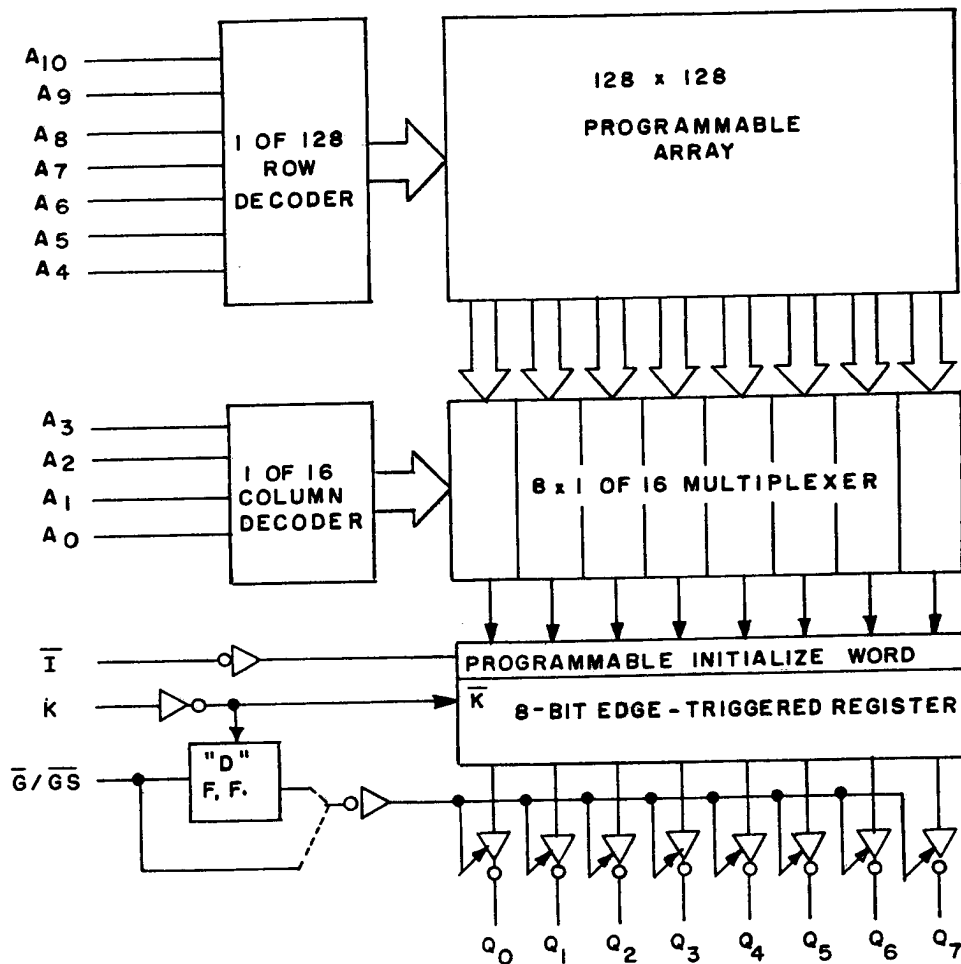


FIGURE 2. Logic diagram.

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Device types 03 and 04

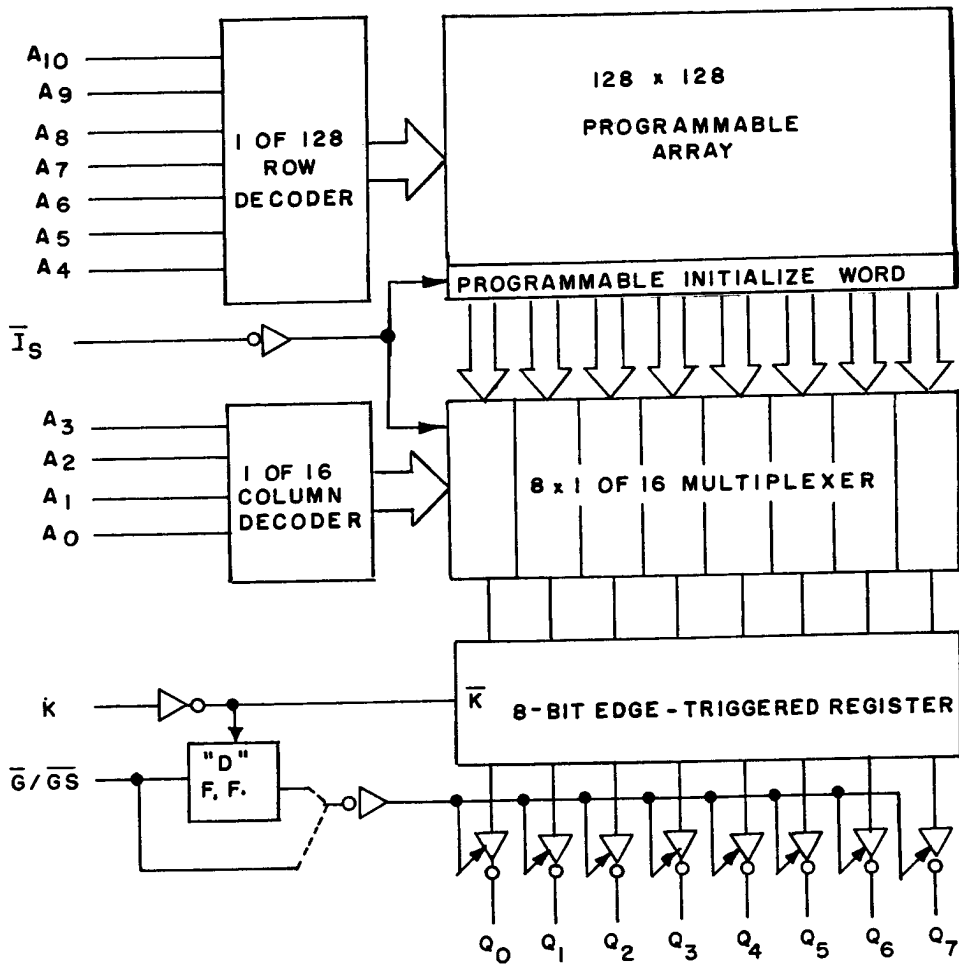
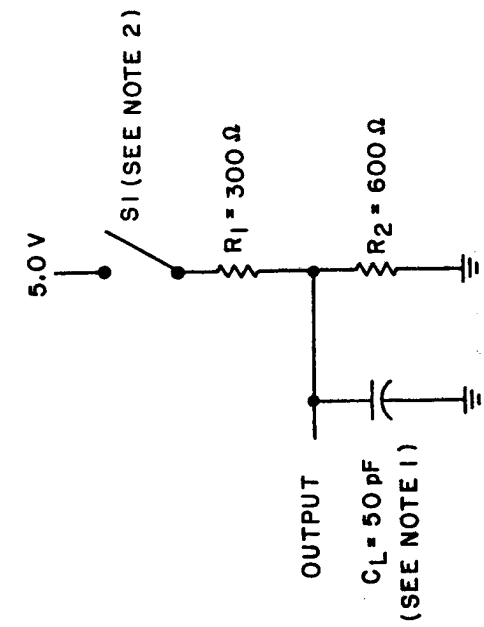


FIGURE 2. Logic diagram - Continued.

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OUTPUT LOAD FOR ALL AC TESTS
EXCEPT TGHQZ AND TKHQZ



OUTPUT LOAD FOR TGHQZ AND TKHQZ

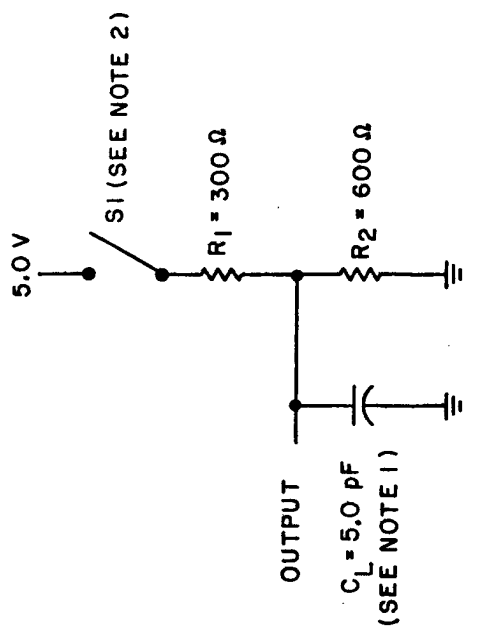
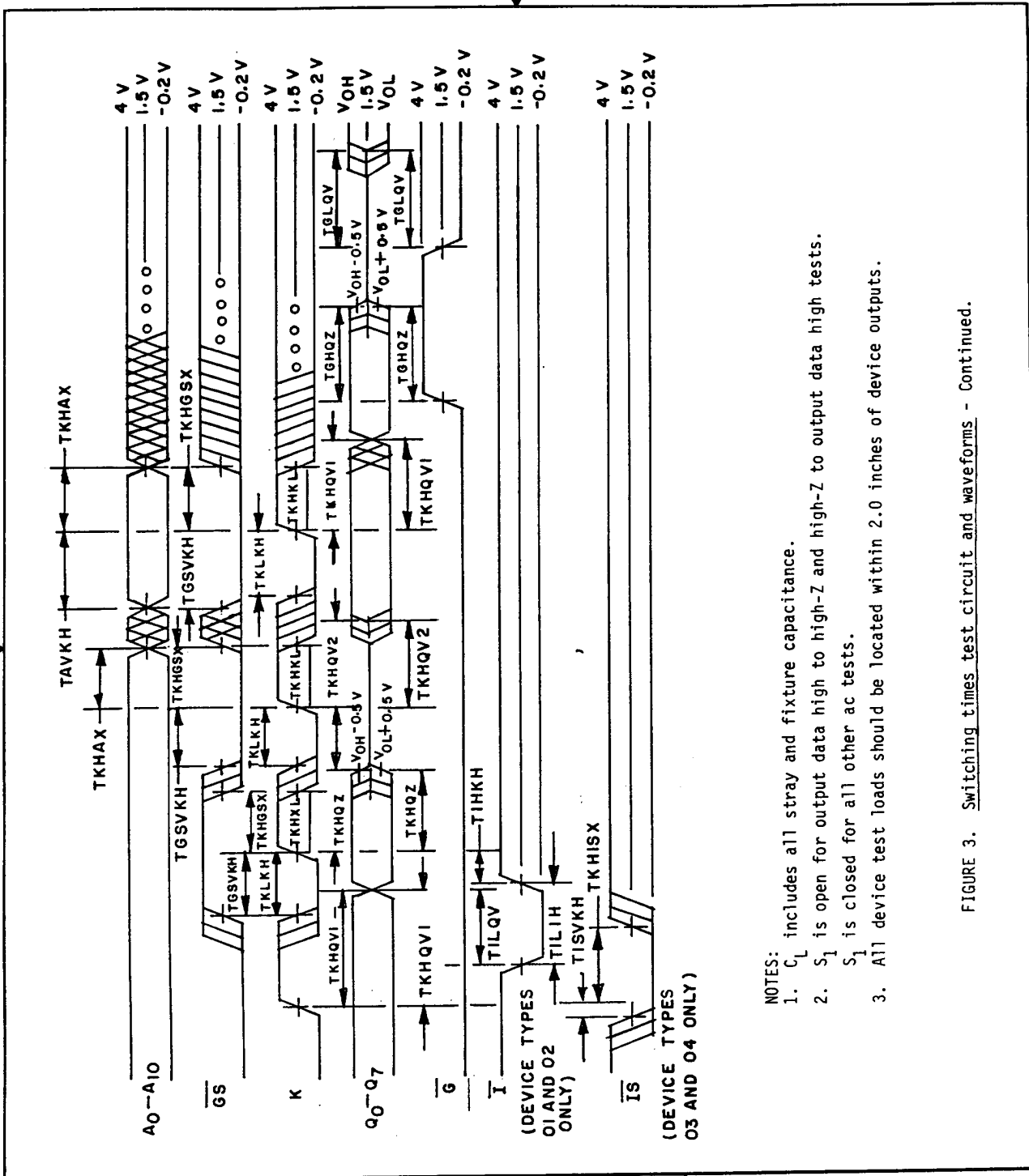


FIGURE 3. Switching times test circuit and waveforms.

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- NOTES:
1. C_L includes all stray and fixture capacitance.
 2. S_1 is open for output data high to high-Z and high-Z to output data high tests.
 S_1 is closed for all other ac tests.
 3. All device test loads should be located within 2.0 inches of device outputs.

FIGURE 3. Switching times test circuit and waveforms - Continued.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test (method 1015 of MIL-STD-883).
 - (1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.
- c. All devices processed by the manufacturer to an altered item drawing shall be programmed prior to burn-in.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:
 - (1) Additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices in group A sample testing, in accordance with MIL-STD-883, method 5005, group A, subgroups 9, 10, and 11.
 - (2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroup 9. Twelve devices shall be submitted to programming (see 3.2.3.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than four total device failures allowed. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroup 9. If more than two total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than four total device failures allowable.
- d. Subgroups 7 and 8 must verify input to output logic combinations.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.

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b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

- (1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).
- (2) $T_A = +125^\circ\text{C}$, minimum.
- (3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

c. The group C, subgroup 1 sample shall include devices tested in accordance with 4.3.1c.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10**, 11**
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8,
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.

** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

4.4 Array programming procedure for circuit A. The characteristics on table IIIA and the following procedures shall be used for programming the device.

- a. Connect the device in the electrical configuration for programming as shown on figure 4. The waveforms on figure 4 and the programming procedures of table IIIA shall apply to these procedures.
- b. Terminate all outputs, to V_{ONP} through a pull up resistor, R.
- c. Apply V_{CCP} to V_{CC} .
- d. Connect $\overline{G}/\overline{GS}$ to V_{ILP} .
- e. Raise $\overline{T}/\overline{IS}$ input to V_{IHP} .
- f. Address the PROM with the binary address of the selected word to be programmed.
- g. Apply V_{IHP} to the $\overline{G}/\overline{GS}$ input.
- h. After a delay of t_1 , apply a low to high transition to the clock (K).

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- i. After a delay of t_2 plus rise time of the programmed output, apply V_{OP} for a duration of $t_3 + (\text{rise time of the enable input}) + t_p$, to the output selected for programming.
- j. After a delay of $t_3 + \text{rise time of the enable input}$, apply V_{FE} for a duration of $t_p + \text{rise time of the programmed output} + t_4$, to the \bar{G}/GS input. \bar{G}/GS is then reduced to V_{ILP} .
- k. After a delay of t_5 , the opening of the fuse is verified. Each data verification must be preceded by a low-to-high transition of the clock (K). This will load the array data into the output data register. During verification, V_{CC} remains unchanged at V_{CCP} .
- l. The outputs should be programmed one at a time, since the internal decoding circuitry is capable of sinking only one unit of programming current at a time. Note that the PROM is supplied with fuses generating a low level logic output. Programming a fuse will cause the output to go to a high level logic in the verify mode.
- m. Repeat 4.4a through 4.4k for all other bits to be programmed.
- n. If any unit does not verify data as programmed, it shall be considered a programming reject.

4.4.1 Programming the initialized word.

- a. Repeat steps 4.4a through 4.4d.
- b. Connect T/T_S to V_{ILP} . This deselects the internal programming circuitry for all other addresses.
- c. The initialized word is then programmed, output by output, similar to any other address location, following 4.4g through 4.4n. Address A_0 must be low.

4.4.2 Programming the synchronous enable (\bar{E}_S)

- a. Repeat steps 4.4a through 4.4d.
- b. Connect T/T_S to V_{ILP} . This deselects the internal programming circuitry for all other addresses. Address A_0 must be in a logic high state.
- c. A standard programming pulse (in accordance with 4.4g through 4.4l) is then applied to output Q. Tie the remaining address inputs to high or low; do not leave any inputs open.
- d. Enable \bar{G}/GS fuse verification circuitry by taking the A_0 input to ~ 15 V. This zener level enables on-chip circuitry, which causes the \bar{G}/GS fuse to appear as data on all outputs. Therefore, all outputs will be in low logic states when the device is in the asynchronous mode, or high logic states when the device is in the synchronous mode.

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TABLE IIIA. Programming characteristics for circuit A.

Description	Parameter	Conditions $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$	Limits			Unit
			Min	Recom- mended	Max	
Fusing enable voltage	V_{FE}	At 10 to 40 mA	14.5	15	15.5	V
Program voltage	V_{OP}	At 15 to 200 mA	19.5	20	20.5	V
Input high level during programming and verify	V_{IHP}		2.4	5	5.5	V
Input low level during programming and verify	V_{ILP}		0.0	0.3	0.5	V
V_{CC} during programming	V_{CCP}	At $I_{CC} = 50$ to 200 mA	5	5.2	5.5	V
Rate of output voltage change	dV_{OP}/dt		20		250	V/ μs
Rate of fusing enable voltage change	dV_{FE}/dt		50		1000	V/ μs
Fusing time first attempt	t_p		40	50	100	μs
Fusing time subsequent attempts	t_p		4	5	1000	ms

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TABLE IIIA. Programming characteristics for circuit A - Continued.

Description	Parameter	Conditions $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$	Limits			Unit
			Min	Recom- mended	Max	
Delays between various level changes	t_1-t_6		100		2000	ns
Period during which output is sensed for V_{BLOWN} level	t_y			500		ns
Pull-up voltage on outputs not being programmed	V_{ONP}		$V_{\text{CCP}} - 0.3$	V_{CCP}	$V_{\text{CCP}} + 0.3$	V
Pull-up resistor on outputs not being programmed	R		0.2	2	5.1	$k\Omega$
Current into outputs not to be programmed	I_{ONP}				20	mA

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CIRCUIT A
Simplified programming circuit

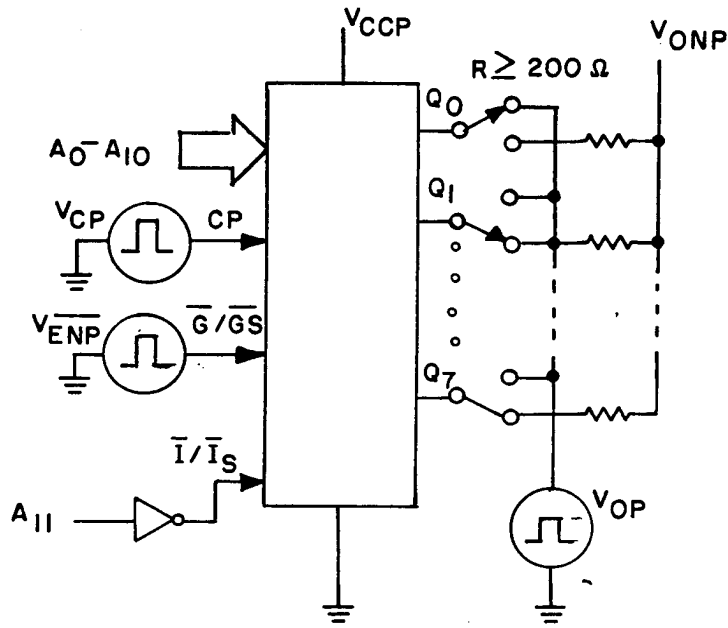
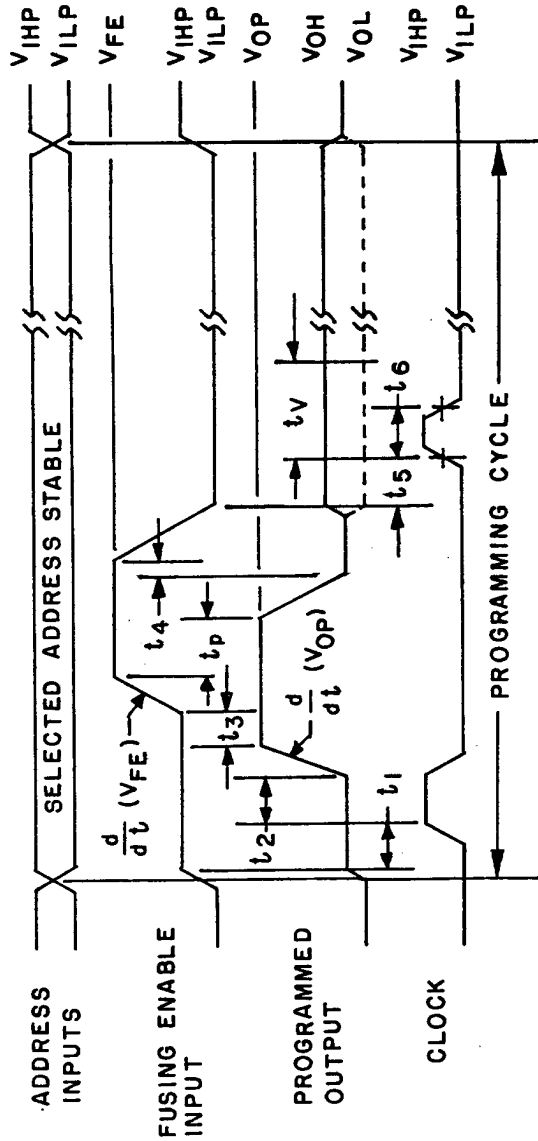


FIGURE 4. Programming circuit and waveforms.

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PROGRAMMING WAVEFORMS



- NOTES:
1. All delays between edges are specified from the completion of the first edge to the beginning of the second edge; i.e., not the midpoints.
 2. Delays t_1 through t_6 must be greater than 100 ns; maximum delays of 1 μ s are recommended to minimize heating during programming.
 3. During t_v the output being programmed is switched to the load R and read to determine if additional programming pulses are required.
 4. Outputs not being programmed are connected to V_{OP} through register R which provides output current limiting.

FIGURE 4. Programming circuit and waveforms - Continued.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1/</u>
5962-8552701LX	34335	AM27S45/BLA
5962-8552701KX	34335	AM27S45/BKA
5962-8552701XX	34335	AM27S45/BUA
5962-85527013X	34335	AM27S45/B3A
5962-8552702LX	34335	AM27S45A/BLA
5962-8552702KX	34335	AM27S45A/BKA
5962-8552702XX	34335	AM27S45A/BUA
5962-85527023X	34335	AM27S45A/B3A
5962-8552703LX	34335	AM27S47/BLA
5962-8552703KX	34335	AM27S47/BKA
5962-8552703XX	34335	AM27S47/BUA
5962-85527033X	34335	AM27S47/B3A
5962-8552704LX	34335	AM27S47A/BLA
5962-8552704KX	34335	AM27S47A/BKA
5962-8552704XX	34335	AM27S47A/BUA
5962-85527043X	34335	AM27S47A/B3A

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

<u>Vendor CAGE number</u>	<u>Vendor name and address</u>	<u>Programming procedure</u>	<u>Fusible link</u>
34335	Advanced Micro Devices, Incorporated 901 Thompson Place Sunnyvale, CA 94088	A	Platinum silicide fuse

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