NEC
NEC Electronics Inc.

μPD72185
Advanced Compression/ Expansion Engine

T-52-33-90

Description

The μPD72185 Advanced Compression/Expansion Engine (ACEE) is a dedicated high-speed processor that performs binary image data compression and expansion using CCITT Group 3 and Group 4 algorithms. The μPD72185 supports all the coding methods specified in the CCITT T.4 and T.6 recommendations.

The μPD72185 ACEE operates on 8- or 16-bit-wide data residing in memory. It can compress image data into reduced codes and also expand reduced codes into an image. Compressed codes can be transferred to or from a separate processor or parallel peripheral through an I/O port.

The μPD72185 has a high-performance, four-stage pipelined architecture. It has separate host CPU and image data buses for maximum data throughput. The on-chip DMA controller manages all data transfer on the image bus.

The μPD72185 is designed for high-performance image compression applications, such as facsimile machines, PC FAX boards, scanners, printers, image workstations, electronic document storage systems, and magnetic and optical disk based electronic filing systems.

Features

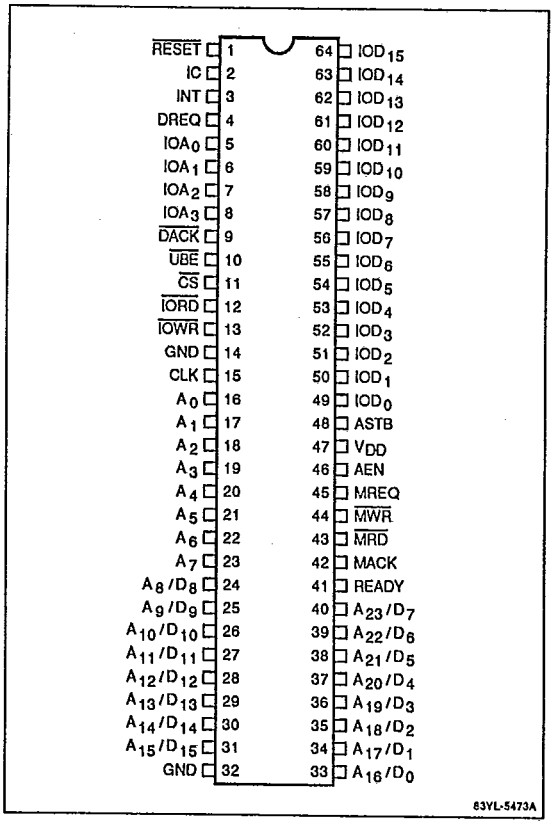
- High-speed processing
  - Compression/expansion of CCITT standard test chart (A4 size, 400 PPI x 400 LPI) in under 1 second
  - Internal four-stage pipelined CPU
- Handles a variety of encoding/decoding methods: CCITT standard MH, MR, and MMR
- 32K pixels maximum per line
- Supports 32-megabyte image memory
- Image data enlargement/reduction
  - Horizontally
    - x2 enlargement (on decoding)
    - x1/2 reduction (on encoding)
  - Vertically
    - x2 and x4 enlargement (on decoding)
    - x1/2 and x1/4 reduction (on encoding)
- Bit boundary processing
- Automatic error handling on decoding
- Multitasking capability
- Dual bus system
  - Image memory side (24-bit address bus, 8/16-bit data bus)
  - Host CPU side (8/16-bit data bus)
- High integration
  - On-chip DMA controller
  - On-chip refresh timing generation circuit
- CMOS process
  - Single +5-volt power supply
  - System clock: 8 MHz maximum

Ordering Information

Part No.	Package
μPD72185CW	64-pin plastic shrink DIP (750 mil)
μPD72185L	68-pin PLCC (plastic leaded chip carrier)

Pin Configurations

64-Pin Plastic Shrink DIP



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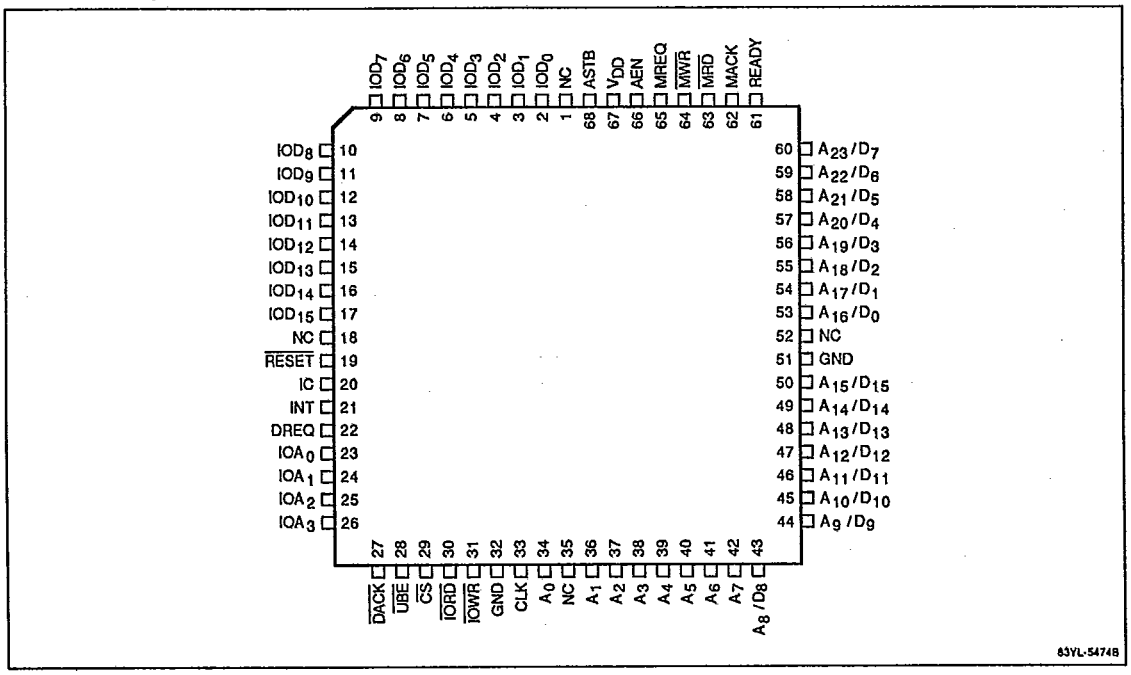
68-Pin PLCC (Plastic Leaded Chip Carrier)



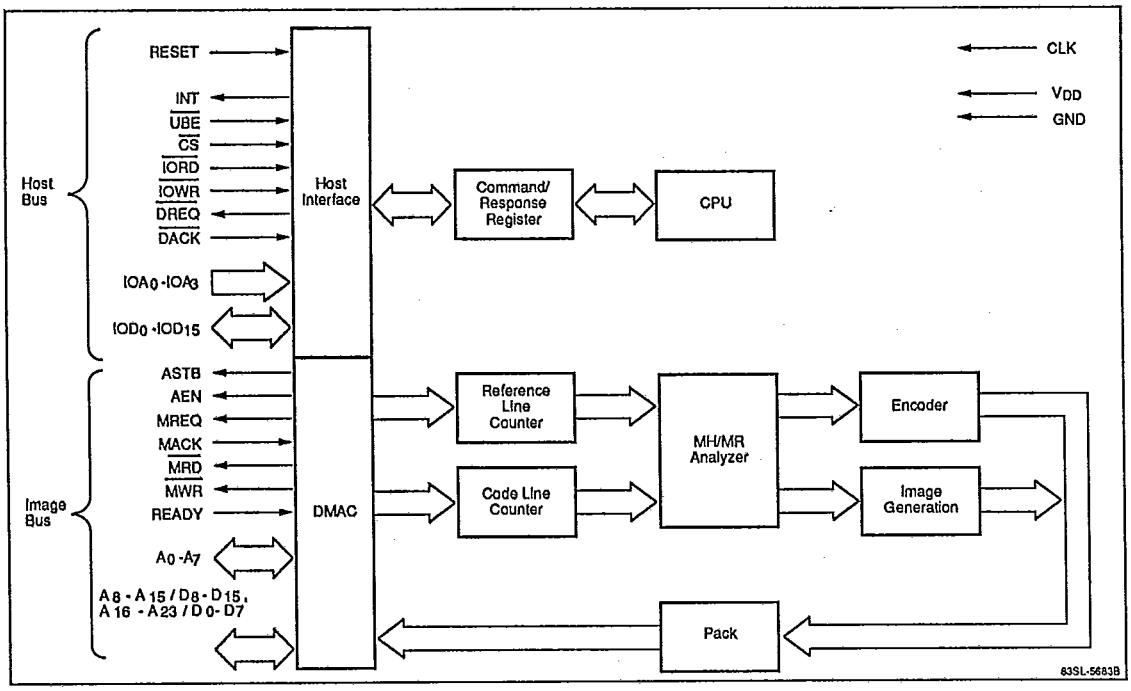
Pin Identification

Symbol	Function
Host Interface	
$\overline{CS}$ (Chip Select)	Active-low input signal enables I/O access to μPD72185 from host bus.
$\overline{DACK}$ (DMA Acknowledge)	Input signal from external DMA controller. Must be inactive (high) when host CPU performs I/O access to μPD72185.
DREQ (DMA Request)	Output signal to external DMA controller. Becomes active low when there is readable data or space that can be written to in the μPD72185.
INT (Interrupt Request)	Output signal to host CPU.
IOA_0-IOA_3 I/O Address)	4-bit address input selects register or register pair when host CPU performs I/O access to μPD72185.
IOD_0-IOD_{15} (I/O Data Bus)	16-bit, two-way data bus
$\overline{IORD}$ (I/O Read)	Low-level input signal when host CPU reads from μPD72185 by I/O access.
$\overline{IOWR}$ (I/O Write)	Low-level input signal when host CPU writes to μPD72185 by I/O access.
$\overline{UBE}$ (Upper Byte Enable)	When host CPU writes to μPD72185 by I/O access, byte or word transfer is specified by $\overline{UBE}$ input signal in combination with IOA_0 input.
Image Memory Interface	
A_0-A_7 (Address Bus)	Lower 8-bit address of image memory bus.
A_8-A_{15}/D_8-D_{15}, A_{16}-A_{23}/D_0-D_7 (Address/Data Bus)	Upper 16-bit address of image memory bus multiplexed with the 16-bit data bus.
AEN (Address Enable)	Output signal becomes active when μPD72185 is Bus Master on the image bus.
ASTB (Address Strobe)	High-level output signal used to latch address output from μPD72185.
MACK (Memory Acknowledge)	Active-high input signal grants μPD72185 use of image memory bus in response to MREQ signal.
$\overline{MRD}$ (Memory Read)	High-level output when μPD72185 is Bus Master on the image bus. Becomes low level when data is read from image memory. Set to high impedance when μPD72185 is Bus Slave.
MREQ (Memory Request)	High-level output signal requests use of image memory bus when μPD72185 is Bus Slave on the image bus. Becomes active for a DMA transfer between μPD72185 and image memory.

Pin Identification (cont)

Symbol	Function
$\overline{MWR}$ (Memory Write)	High-level output when μPD72185 is Bus Master on the image bus. Becomes low level when data is written to image memory. Set to high impedance when μPD72185 is Bus Slave.
READY (Ready)	Low-level input signal extends $\overline{MRD}$ and $\overline{MWR}$ cycle by adding wait states.. Signal must not be altered within setup/hold time period.
Other Pins	
CLK (Clock)	External clock input.
$\overline{RESET}$ (Reset)	System reset input. Must be held low for at least seven system clock cycles. After reset, μPD72185 becomes Bus Slave on the image bus.
IC (Internal Connection)	This pin must always be pulled up.
NC (No Connection)	No internal connections are made to this pin.
V_{DD}	Positive power supply pin.
GND (Ground)	Both ground pins must be connected.

μPD72185 Block Diagram



Absolute Maximum Ratings

T_A = +25°C

Power supply voltage, V_{DD}	−0.5 to +7.0 V
Input voltage, V_I	−0.5 to V_{DD} + 0.3 V
Output voltage, V_O	−0.5 to V_{DD} + 0.3 V
Operating temperature, T_{OPT}	−40 to +85°C
Storage temperature, T_{STG}	−40 to +125°C

DC Characteristics

T_A = −40 to +85°C; V_{DD} = +5 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input voltage, low-level	V_{ILC}	−0.5		+0.8	V	CLK pin
	V_{IL}	−0.5		+0.8	V	Other pins
Input voltage, high-level	V_{IHC}	+3.3		V_{DD} + 0.3	V	CLK, $\overline{RESET}$ pins
	V_{IH}	+2.2		V_{DD} + 0.3	V	Other pins
Output voltage, low-level	V_{OL}			+0.4	V	I_{OL} = 2.5 mA
Output voltage, high-level	V_{OH}	0.7 V_{DD}			V	I_{OH} = −400 μA
Input leakage current	I_{LI}			±10	μA	V_{IN} = 0 to V_{DD}
Output leakage current	I_{LO}			±10	μA	V_{OUT} = 0 to V_{DD}
Supply current	I_{DD}		50	100	mA	While operating

AC Characteristics

T_A = −40 to +85°C; V_{DD} = 5 V ±10%

Parameter	Figure	Symbol	Min	Max	Unit	Condition
Clock						
CLK cycle	2	t_{CYK}	125	1000	ns	
CLK low-level width	2	t_{KKL}	50		ns	
CLK high-level width	2	t_{KKH}	50		ns	
CLK rise time	2	t_{KR}		10	ns	1.5 → 3.0 V
CLK fall time	2	t_{KF}				3.0 → 1.5 V
Image Memory Interface						
MREQ ↑ delay time from CLK ↑	3	t_{DMQH}		100	ns	
MREQ ↓ delay time from CLK ↑	3	t_{DMQH}		100	ns	
MACK ↑ setup time to CLK ↑	3	t_{SMA}	35		ns	
MACK ↓ hold time from CLK ↑	3	t_{HMA}	20		ns	
AEN ↑ delay time from CLK ↑	3	t_{DAEH}		100	ns	
AEN ↓ delay time from CLK ↑	3	t_{DAEL}		100	ns	
ASTB ↑ delay time from CLK ↓	3	t_{DSTH}		70	ns	
ASTB high-level width	3	t_{STST}	t_{KKH} − 15		ns	
ASTB ↓ delay time from CLK ↑	3	t_{DSTL}		100	ns	
Address/data/$\overline{MRD}$/$\overline{MWR}$ delay time from CLK ↓	3	t_{DA}		100	ns	
Address/data/$\overline{MRD}$/$\overline{MWR}$ float time from CLK ↓	3	t_{FA}	25	70	ns	
Address setup time to ASTB ↓	3	t_{SAST}	t_{KKH} − 35		ns	
Address hold time from ASTB ↓	3	t_{HSTA}	t_{KKL} − 20		ns	
$\overline{MRD}$ ↓ delay time from Address float	3	t_{DAR}	0		ns	
$\overline{MRD}$ ↓ delay time from CLK ↓	3	t_{DRL}		70	ns	
$\overline{MRD}$ low-level width	3	t_{RRL2}	$2t_{CYK}$ − 50		ns	WAIT = 0
$\overline{MRD}$↑ delay time from CLK ↑	3	t_{DRH}		70	ns	
Input data setup time to $\overline{MRD}$ ↑	3	t_{SDR}	70		ns	
Input data hold time from MRD ↑	3	t_{HRD}	0		ns	
$\overline{MWR}$↓ delay time from CLK ↓	3	t_{DWL}		70	ns	
$\overline{MWR}$ low-level width	3	t_{WWL2}	$2t_{CYK}$ − 50		ns	WAIT = 0
$\overline{MWR}$↑ delay time from CLK ↑	3	t_{DWH}		70	ns	
READY setup time to CLK ↑	3	t_{SRY}	35		ns	
READY hold time from CLK ↑	3	t_{HRY}	20		ns	
Host Interface						
$\overline{DACK}$/$\overline{CS}$ recovery time	4, 5	t_{RDC}	200		ns	
$\overline{IORD}$ low-level width	4, 7	t_{RRL}	150		ns	
Address/$\overline{CS}$ ↓ setup time to $\overline{IORD}$ ↓	4	t_{SAR}	35		ns	
Address/$\overline{CS}$ ↓ hold time from $\overline{IORD}$ ↑	4	t_{HRA}	0		ns	
Output data delay time from $\overline{IORD}$ ↓	4	t_{DRD}		120	ns	
Output data float time from $\overline{IORD}$ ↑	4	t_{FRD}	10	70	ns	
$\overline{IOWR}$ low-level width	5	t_{WWL}	100		ns	
$\overline{CS}$ ↓ hold time from $\overline{IOWR}$ ↑	5	t_{WWCS}	0		ns	

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AC Characteristics (cont)

T_A = −40 to +85°C; V_{DD} = 5 V ±10%

Parameter	Figure	Symbol	Min	Max	Unit	Condition
Address/$\overline{UBE}$/$\overline{CS}$ ↓ setup time to $\overline{IOWR}$ ↓	5	t_{SAW}	0		ns	
Address/$\overline{UBE}$ hold time from $\overline{IOWR}$ ↑	5	t_{HWA}	0		ns	
Input data setup time to $\overline{IOWR}$ ↑	5	t_{SDW}	100		ns	
Input data hold time from $\overline{IOWR}$ ↑	5	t_{HWD}	0		ns	
$\overline{RESET}$ low-level width	6	t_{RSTL}	$7t_{CYK}$		ns	
V_{DD} setup time to $\overline{RESET}$ ↑	6	t_{SVDD}	1000		ns	
$\overline{IOWR}$/$\overline{IORD}$ wait time from $\overline{RESET}$ ↑	6	t_{SYWR}	$2t_{CYK}$		ns	
$\overline{IOWR}$/$\overline{IORD}$ recovery time	7	t_{RVWR}	200		ns	
DREQ ↓ delay time from $\overline{IORD}$ ↓	7	t_{DRDQ}		140	ns	
DREQ ↓ delay time from $\overline{IOWR}$ ↓	7	t_{DWDQ}		140	ns	

Figure 1. Voltage Thresholds for Timing Measurements

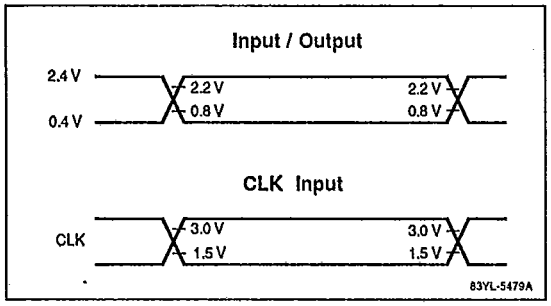


Figure 2. Clock Timing

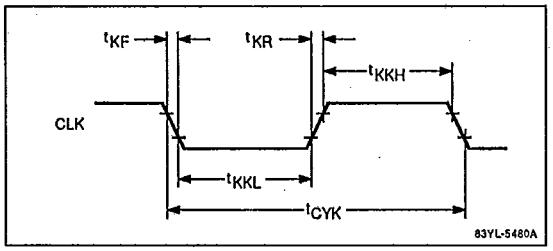
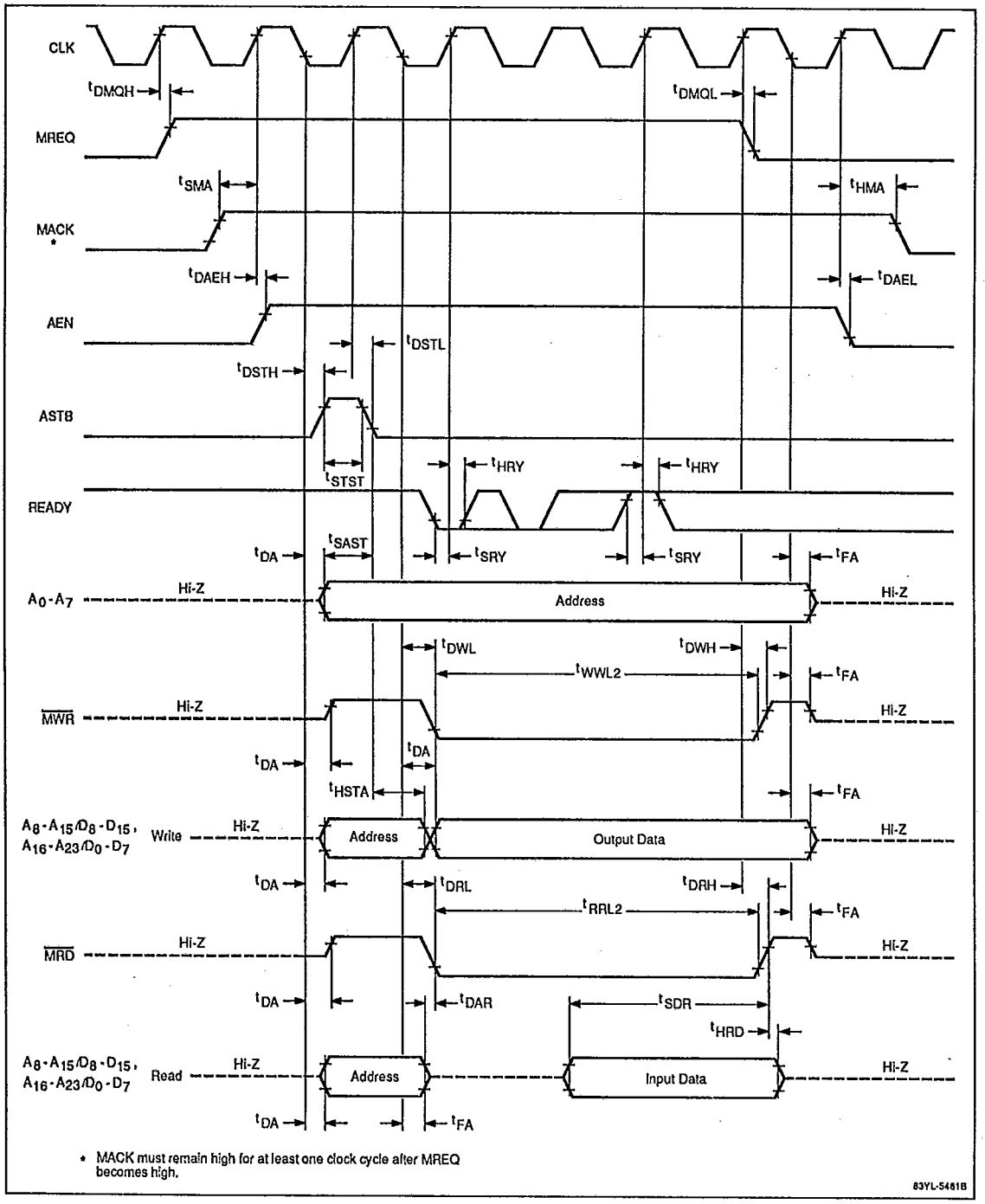


Figure 3. DMA Transfer Timing on Image Bus



* MACK must remain high for at least one clock cycle after MREQ becomes high.

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Figure 4. Timing for Read from μPD72185 on Host Bus

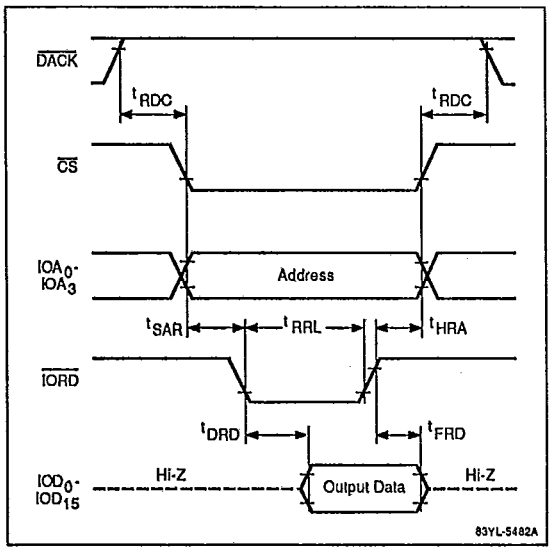


Figure 5. Timing for Write to μPD72185 on Host Bus

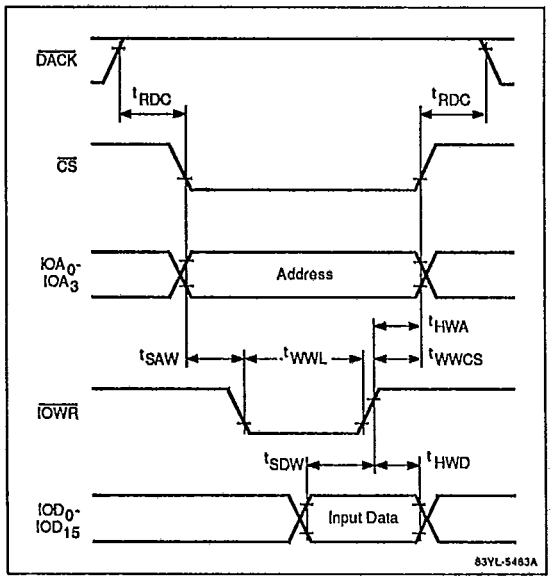


Figure 6. Reset Timing

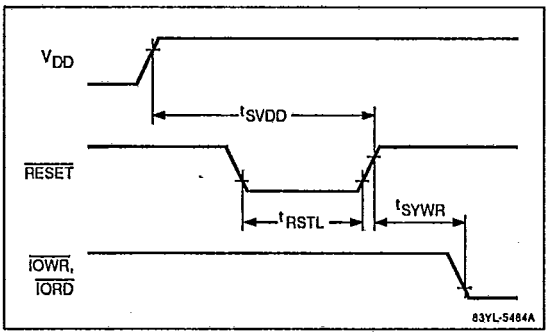
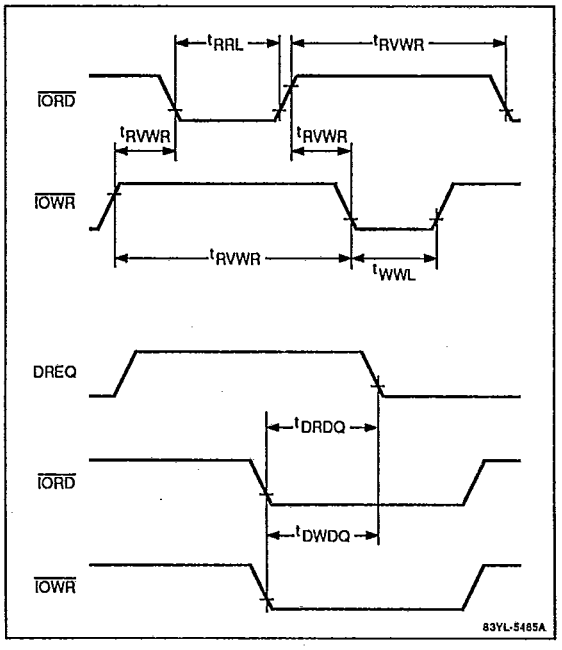


Figure 7. Read/Write Cycle Timing



OVERVIEW

The μPD72185 encodes and decodes binary image data in accordance with the standard system prescribed by the CCITT (International Telegraph and Telephone Consultative Committee). See table 1.

Table 1. CCITT Standard Systems

System	CCITT Recommendation
MW	T.4 (G3 Facsimile)
MR	T.4 (G3 Facsimile)
MMR	T.6 (G4 Facsimile)

The μPD72185 has two bus interfaces with which it connects to the system.One interface is with the host CPU and the other is with image memory. Data exchange with the host CPU is by ordinary I/O accesses; data exchange with image memory is by DMA transfers using the on-chip DMA controller.

In this document, the bus on the host CPU side is called the host bus, and the the bus on the image memory side is called the image memory bus.

In addition to encoding/decoding, the μPD72185 can perform data transfers between the image memory and the host CPU. Also, it can perform image enlargement and reduction on expansion and compression and logical operations (AND, OR, XOR,) while transferring data. Table 2 and figure 8 show the processing patterns.

Table 2. μPD72185 Processing Patterns

Type	Processing	Data Flow, Bus-to-Bus		
A	Encoding	Image memory	→	Image memory
B	Decoding	Image memory	→	Image memory
C	Encoding	Image memory	→	Host
D	Decoding	Host	→	Image memory
E	Data transfer	Image memory	→	Host
F	Data transfer	Host	→	Image memory
G	Data transfer	Image memory	→	Image memory

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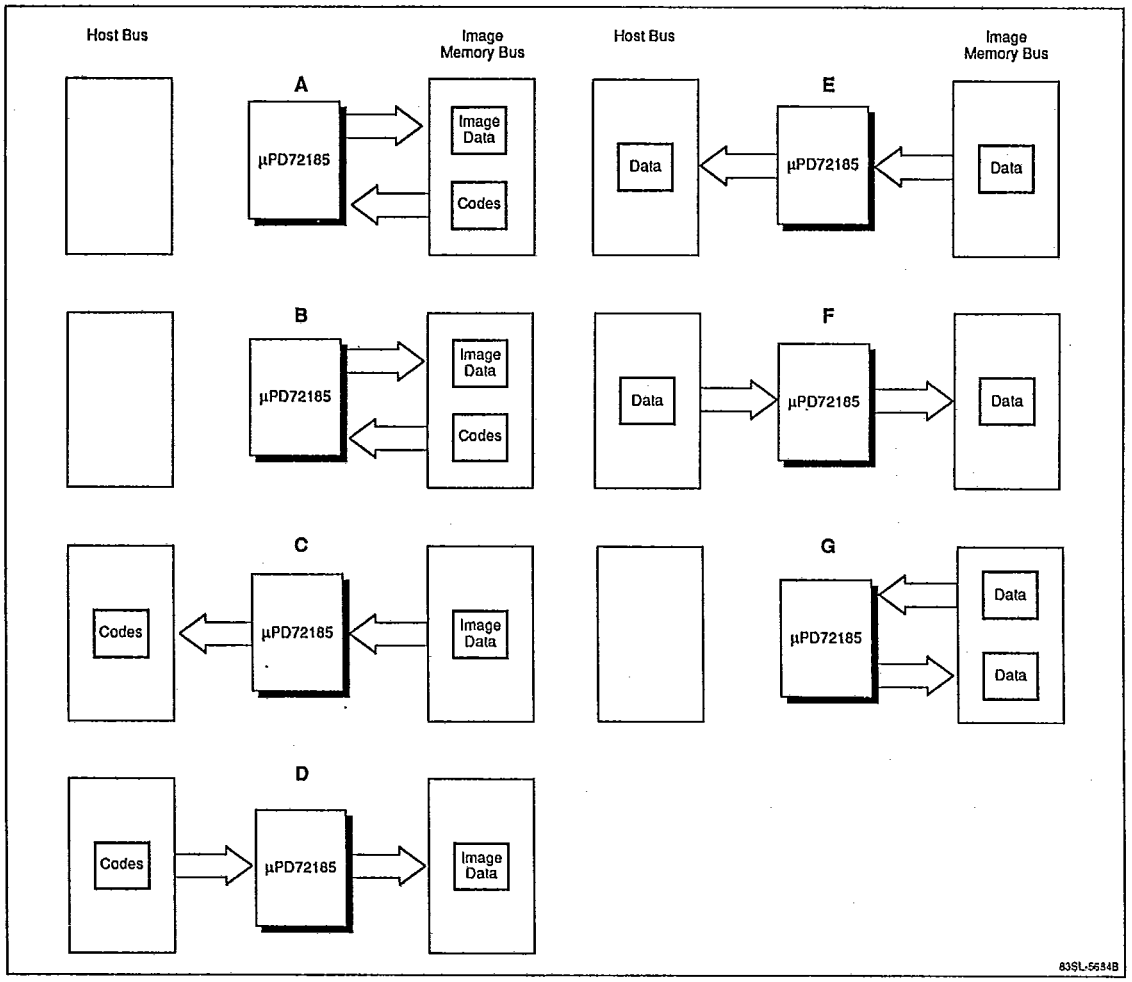
Figure 8. μPD72185 Processing Patterns



PROCESSING

Modes

The two processing modes of the μPD72185—block and line—are selected by commands from the host CPU. In block mode, which is more commonly used, one command controls processing of multiple lines. In line mode, one command is required for each line. Line mode allows encoding/decoding methods other those prescribed by the CCITT.

Line Processing

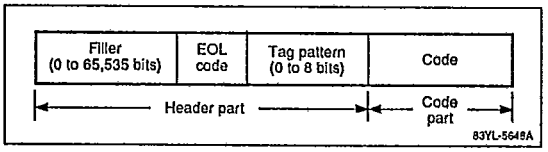
A compressed line consists of a header and code as shown in figure 9. In the header, commands from the host CPU specify the number of filler bits (0 to 65,535), the presence/absence of the EOL code, and the number of bits in the tag pattern (0 to 8).

The code that follows the header consists of encoded binary image data. The encoding method can be specified per line by commands from the host CPU.

At the time of encoding, a line is generated in this order: filler + EOL code + tag pattern + code. This filler is appended to the immediately preceding line.

Decoding is performed one line at a time in this order: code + filler + EOL code + tag pattern. If a page starts with an EOL code, the μPD72185 detects the EOL code and the following tag pattern and processes them before starting line-by-line decoding.

Figure 9. Line Composition (Line Mode)



EXTERNAL INTERFACE

The μPD72185 exchanges data with image memory by DMA transfers via the on-chip DMA controller. When the μPD72185 needs to access image memory, it requests use of the image memory bus by activating MREQ. Data is exchanged with a host CPU (including an external DMA controller) by normal I/O accesses. The host CPU reads and writes data through the μPD72185 I/O addresses.

MULTITASKING

Multitasking means using the μPD72185 to process multiple image areas in parallel by time division.

The μPD72185 processes an image area specified by the host CPU as a unit. On completion of processing, the μPD72185 sends back to the host CPU in the form of a response: memory manage ment information, processing information, counter information, etc.

As an example, consider a case in which image data encoded by one method is to be recoded by another method. When the recoded data extends over multiple image areas, the following two methods can be employed.

(1) All encoded data in the multiple image areas is decoded. This image data is then reencoded all at once.

(2) Encoded data in multiple image areas is decoded in small blocks. This image data is then recoded a block at a time, processing only a section of each image each time..

Depending on the system design, pipelining with method 2 may improve processing efficiency. This method can be implemented through the host CPU's management of responses sent back by the μPD72185.

ENLARGEMENT/REDUCTION

The μPD72185 can reduce an image when encoding and enlarge image data when decoding. Reduction is performed by a simple thinning-out operation, and enlargement by repeating the same data. Enlargement/reduction types are shown in table 3.

Table 3. Enlargement/Reduction Types

	Enlargement and (Reduction) Factors	
Type	Horizontal	Vertical
A	1 (1)	1 (1)
B	1 (1)	2 (1/2)
C	2 (1/2)	2 (1/2)
D	2 (1/2)	4 (1/4)

WHITE MASK

The μPD72185 can perform white mask processing on the right edge and left edge of image data. The amount of white masking is specified separately for each edge in word units (0 to 255 words)

The μPD72185 automatically white masks data on encoding image data. It is not able to perform decoding and white mask processing at the same time. Hence, white mask processing is performed once decoding is completed

BIT BOUNDARY

Some image areas consist of lines not terminated in either byte or word units but with an odd number of bits. The μPD72185 handles image areas of this kind with bit boundary processing.

Lines with an odd number of bits are processed by specifying void bits up to the byte or word boundary. See figure 10.

Figure 10. Bit Boundary Processing (Word Units)

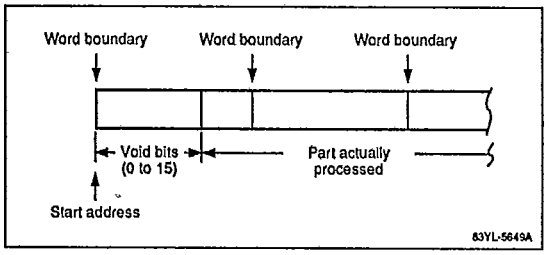


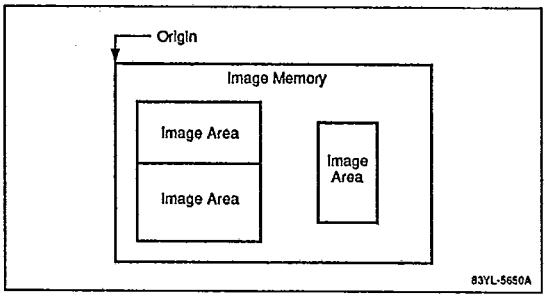
IMAGE MEMORY

Image Area

Image memory means the whole area of memory accessible by the μPD72185. An image area, on the other hand, is a rectangular area within image memory (figure 11), the size and location of which is specified by commands from the host CPU. The unit of processing is an image area.

The μPD72185 can append and also detect the code indicating the end of a page using commands from the host CPU. Page management, however, is performed by the host CPU.

Figure 11. Image Area Examples



Memory Organization

Under control of the host CPU, image memory can be either byte-organized (8-bit units) or word-organized (16-bit units). One μPD72185 address corresponds to one byte or one word in memory. In both cases the μPD72185 does its internal processing and writes to image memory in 16-bit units. Thus, when image memory is byte-organized, two accesses are required, one to an odd-numbered address and one to an even-numbered address.

The 24-line address bus allows access to a large amount of image memory. Table 4 shows image memory capacity for byte and word organization.

Table 4. Image Memory Capacity

Organization	Size	*Capacity
Byte	16M bytes	64 A4 sheets
Word	32M bytes	128 A4 sheets

*A4 sheet = 210 mm wide by 297 mm long
Horizontal: 8 dots/mm
Vertical: 4 dots/mm

Data Storage

Image memory can store code and other general data as well as binary image data. Binary image data is converted to white/black levels shown in table 5 and stored as follows.

(1) The first bits scanned are packed in sequence starting from the LSB of a byte/word.

(2) The first data byte/word scanned is packed in sequence in byte/word units starting from the lower address side.

Code transferred serially is stored as follows.

(1) The first bits transmitted are packed in sequence starting from the LSB of a byte/word.

(2) The first data byte/word transmitted is packed in sequence starting from the lower address side.

Table 5. Binary Image Data Levels

Level	Binary Notation
White	0
Black	1

ENCODING/DECODING SYSTEMS

Table 6 lists the encoding/decoding systems the μPD72185 can handle, including CCITT standard systems. Figure 12 shows coded data formats for MH, MR, and MMR systems.

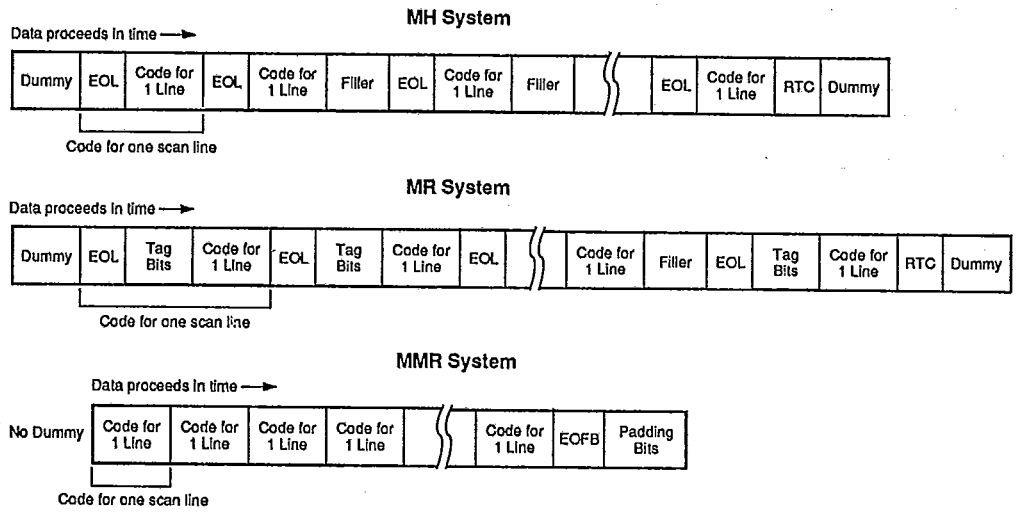
Table 6. Encoding/Decoding Systems

System	Summary
MH	One-dimensional encoding/decoding system, G3 facsimile, CCITT standard.
MR	Two-dimensional encoding/decoding system, G3 facsimile, CCITT standard.
MMR	Two-dimensional encoding/decoding system, G4 facsimile, CCITT standard.
Other	Systems other than CCITT standards that can be implemented by selecting line mode

Picture Elements

Image data that exceeds 2623 picture elements (pixels) per scan line is processed using the run-length code table expansion method stipulated in CCITT Recommendation T.6.

Figure 12. Code Data Formats in MH, MR, and MMR Systems



Item	MH System	MR System	MMR System
Start of each scan line	EOL	EOL	No EOL
Filler	Insertable	Insertable	None
RTC	Normally EOL x 6	(EOL + 1) x 6	EOL x 2
K-parameter	Undefined	Present	None
Tag bits	None	Normally 1 bit	None
EOL for head of page	None	None	None
≥ 2624 run length code	Make-up code x n + termination code		

Symbols

EOFB	End of facsimile block
EOL	End of line
RTC	Return to control
Dummy	Variable-length string of zeros

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K-Parameter

In the MR system, the K-parameter determines the coding technique and the transmission error recovery procedures. The value of the K-parameter can be specified as a number from 1 to 255 or as infinity (∞).

Whether the code for a particular line uses one-dimensional encoding or two-dimensional encoding is indicated by the value of the tag bit inserted after EOL. See table 7.

Table 7. Relation Between Encoding System and Tag Bit

Encoding System	Tag Bit Value	Method of Representation
One-dimensional	1	EOL + 1 (tag bit)
Two-dimensional	0	EOL + 0 (tag bit)

Filler Bits

When encoding, the μPD72185 can adjust the length of the coded data by adding filler bits. The two methods of adding filler bits are as follows.

(1) Specify minimum number of bits transmitted with the BLO command

(2) Specify number of added filler bits with the LNO command.

When decoding, the μPD72185 ignores the added filler bits.

Error Detection

When decoding, the μPD72185 can detect errors in the code and carry out appropriate processing. Table 8 lists the types of error detection.

Table 8. Types of Error Detection

Error Detection	Applicable Encoding Systems
Illegal code	MH, MR, MMR
Logically inconsistent code	MR, MMR
Decoded line longer than specified line length	MH, MR, MMR
Decoded line shorter than specified line length	
Abnormal page end	

Line Number Count

When decoding, the μPD72185 performs three kinds of line counting.

(1) The number of normally-decoded lines (normally-processed line count).

(2) The number of lines in error (error line count).

(3) The maximum number of consecutive lines in which errors occurred (consecutive error line count).

The start of error line counting and successive error line counting can be specified in either of two ways as shown below. The selection and setting of the initial value of each line count is done by command.

(1) Start count from occurrence of first error.

(2) Start count from normal decoding of one line.

HOST INTERFACE

Exchanges between the μPD72185 and the host CPU (or an external DMA controller) are performed by I/O accesses over the host interface. In general, writes from the host CPU to the μPD72185 are in the form of commands and reads from the μPD72185 are in the form of responses.

The host bus width is 16 data bits but can be accessed 8 bits at a time by manipulation of the logic level on pins IOA_0 and $\overline{UBE}$. See table 9.

Table 9. Host Bus Width

IOA_0	$\overline{UBE}$	Bus Width	Pins
0	0	16 bits	IOD_0-IOD_{15}
X	1	8 bits	IOD_0-IOD_7
1	0	8 bits	IOD_8-IOD_{15}

To get the μPD72185 to start processing, the following operations are necessary.

(1) Write the command into the command registers.

(2) Write 1 into the CRQ bit of the control register.

When the CRQ bit is set, the μPD72185 begins processing as directed by the command received. Once processing has begun, the host CPU cannot write 1 to the CRQ bit again for the next processing operation until it confirms that processing has been completed or interrupted.

Basic Timing

Figure 13 is a timing diagram applicable to reads from the μPD72185 and writes by the host CPU. Figure 14 shows the timing for an external DMA controller in the word mode and byte mode.

REGISTERS

Exchanges between the μPD72185 and the host CPU, including commands and responses, utilize the registers and the data FIFO area illustrated in figure 15. The register I/O addresses are 0H through DH; EH and FH are not allowed. Note that the I/O addresses are shared by corresponding registers in the read and write configurations of figure 15.

Figure 13. Read/Write Timing

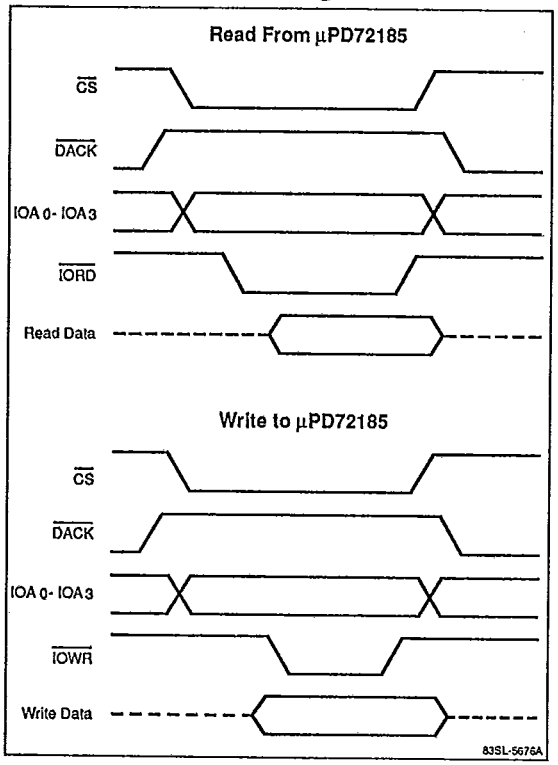

Figure 14. Read/Write Timing With External DMA Controller

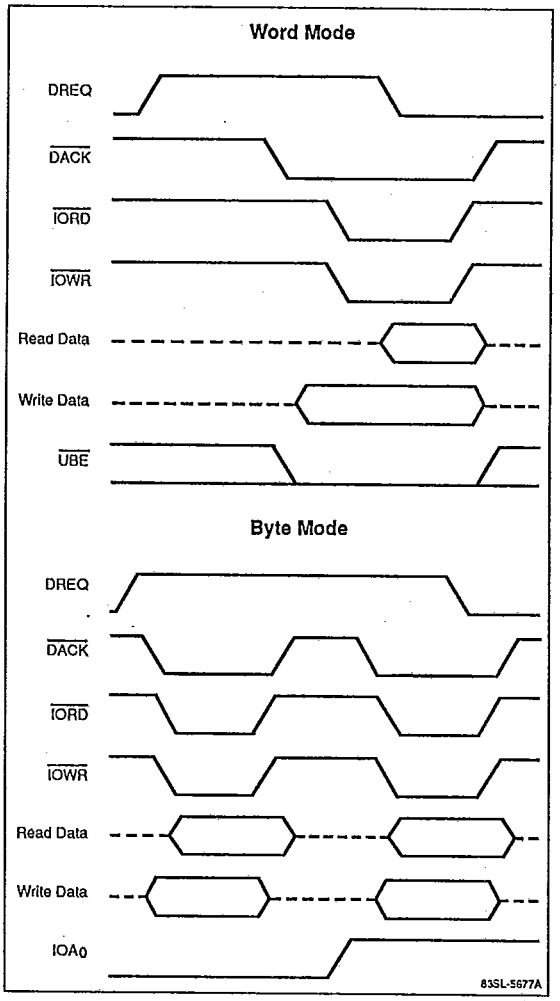

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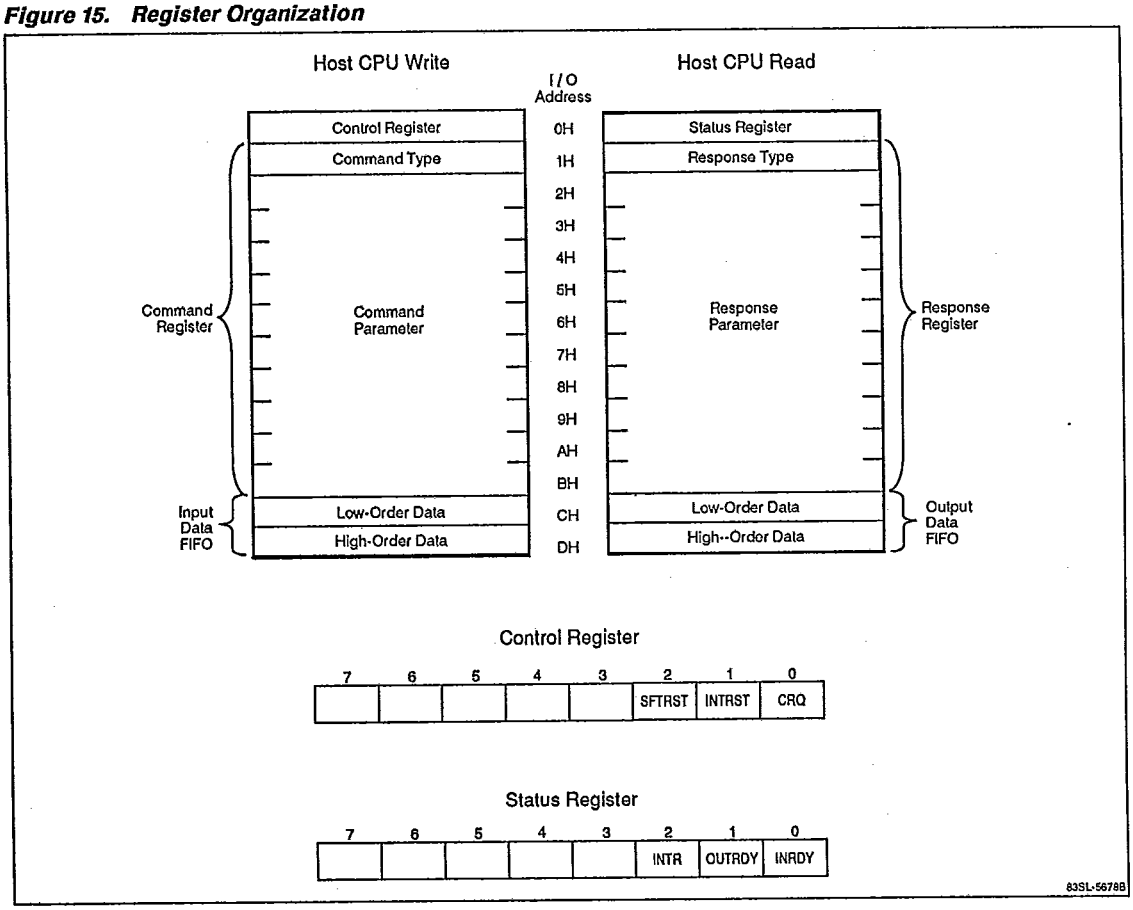
Figure 15. Register Organization



Control Register

The control register is used in writes from the host CPU. The functions of bits 0, 1, and 2 are explained below.

Command Request (CRQ). When 1 is written to the CRQ bit after the host CPU has written a command, the μPD72185 begins processing according to the command. The CRQ bit is automatically reset after completion of processing.

Interrupt Reset (INTRST). When the host CPU writes a 1 to the INTRST bit, the INT pin output and the INTR bit are reset. After being set, the INTRST bit will be reset automatically.

Software Reset (SFTRST). Software reset by setting SFTRST to 1 is functionally identical to hardware reset at the $\overline{\text{RESET}}$ pin.

Status Register

The status register is used in reads from the host CPU. The functions of bits 0, 1, and 2 are explained below.

Input Ready (INRDY). A 1 in the INRDY bit indicates the input data FIFO is ready to receive data from the host CPU.

Interrupt Request (INTR). The INTR bit shows the same logic level as the INT pin. The μPD72185 sets this bit to notify the host CPU that processing has been completed or interrupted.

Command Register

The command register is used in writes from the host CPU. It has two parts: command type and command parameter.

Response Register

The response register is used in reads from the host CPU. It has two parts: response type and response parameter.

Input/Output Data FIFO

The μPD72185 exchanges image data, code, etc., with the host CPU via the data FIFOs. The input data FIFO and the output data FIFO are each two bytes wide.

IMAGE MEMORY INTERFACE

The image memory interface is between the μPD72185 and the image memory, which stores image data and code. Accesses to image memory from the μPD72185 are performed by DMA operations using the on-chip DMA controller. Via the image memory interface, the μPD72185 directly controls image memory.

When the μPD72185 completes command processing, it reports completion or interruption to the host CPU by setting the output of the INT pin to high and at the same time setting the INTR bit in the status register. See figure 15.

The host CPU, meanwhile, confirms completion or interruption of processing either by sampling the INT signal level or by software polling the INTR bit.

DMA Transfer Timing

The basic bus cycle in a DMA transfer takes three system clock pulses: S1, S2, and S3. In this bus cycle, the μPD72185 reads or writes 1 byte or 1 word. See figure 16.

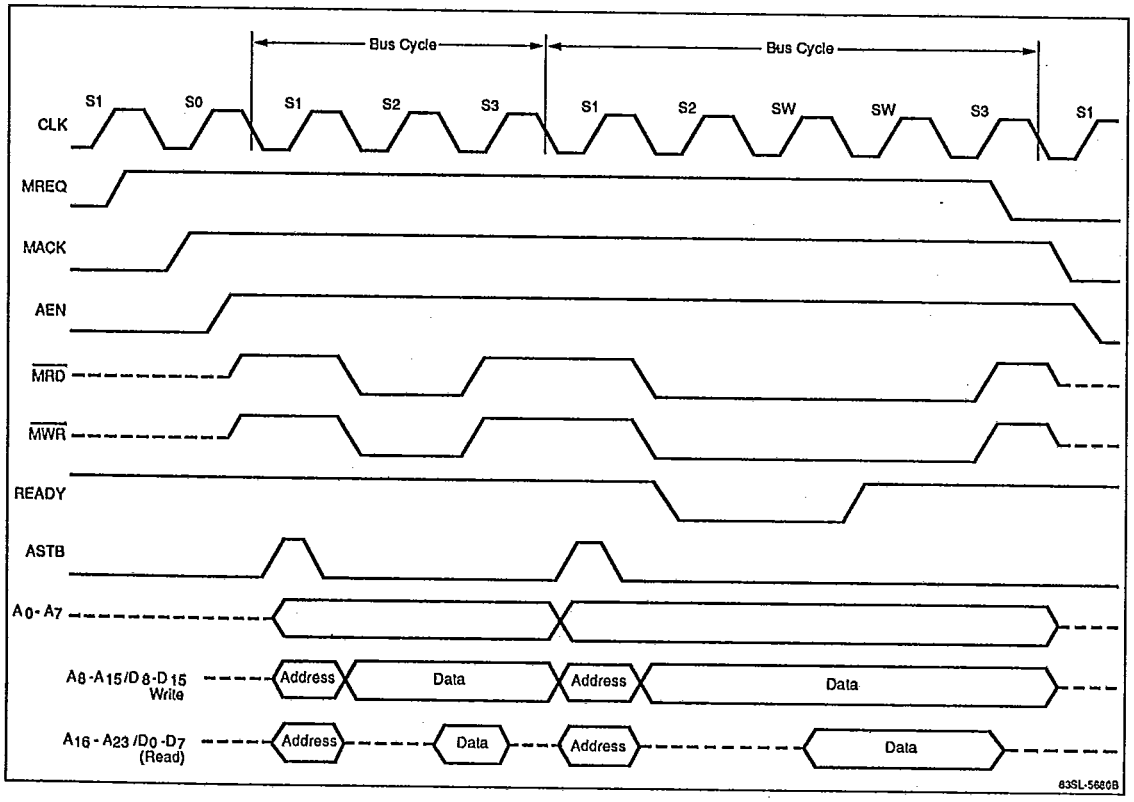
If the access time to an image memory element is long, and a read/write is not possible within the basic bus cycle, then the μPD72185 can insert wait states (SW) between S2 and S3, extending the read/write pulse width.

The two methods of inserting a wait state are:

(1) Using the READY pin.

(2) Programming wait states with a command

Figure 16. DMA Transfer Timing



Bus Cycle Modes

The μPD72185 has three modes in which it operates on the image memory bus as a Bus Master. A command selects the bus cycle mode.

Total Bus Monopolization Mode. The μPD72185 completely monopolizes the bus. The MREQ and MACK signals are not used.

Demand Mode. The μPD72185 holds on to the bus by keeping the MREQ signal high. The length of time held depends on the data being processed. The μPD72185 will always surrender the bus on completing the processing of a line.

Eight Bus Cycle Monopolization Mode. The μPD72185 monopolizes the bus for a maximum of eight bus cycles, after which it releases the bus by dropping MREQ to low. It waits at least three clock intervals before raising MREQ high again .

DMA Break

When the μPD72185 is monopolizing the image memory bus (MREQ = 1), MACK is normally kept high. If MACK falls to low while MREQ is high, the μPD72185 immediately discontinues the DMA transfer. However, because the MACK signal level is sampled at the rising edge of S3, there is a maximum delay of 1 bus cycle + 1/2 clock interval from the fall of MACK until the μPD72185 actually releases the bus.

In the total bus monopolization mode, DMA break does not operate.

Refresh

The μPD72185 is able to output refresh timing to image memory, thus facilitating the connection of pseudo-SRAM. However, the μPD72185 does not output the refresh address itself. Consequently, when DRAM is used in image memory, a refresh address generation circuit must be connected externally or a CAS-before-RAS cycle must be generated.

The refresh function is enabled with a command and performed with a read cycle to address 80000H. Pin A_{23}/D_7 used as the refresh timing output pin decreases the bus width to 23 bits..

COMMANDS

The μPD72185 has five types of commands: assignment, operation, statistical, CLB switch, and special. Table 11 describes the command types; table 12 describes the commands

Table 11. Command Types

Type	Function	Command
Assignment	Specifies system configuration, storage locations of data processed or to be processed, and processing mode.	MOD, SCDB, SIMB, SPRS, SYS
Operation	Gives directions to μPD72185 for start of encoding/decoding, data transfer (composition), and similar processing.	ABT, BLO, CNT, EOL, LNO, MSK, RTAG, RTC, TRO
Statistical	Requests information on processing executed by μPD72185.	RCLB. RPRS
CLB switch	Specifies use/non-use of compressed line buffer.*	CLB-ON, CLB-OFF
Special	Reads firmware version of the μPD72185.	RVER

* The compressed line buffer handles compressed storage of the code for one line according to the coding mode.

Table 12. List of Commands

Name	Function
ABT (Abort)	When a CFE interrupt* is generated, the μPD72185 resumes processing with the ABT command. However, this is done only for the line being processed when the interrupt was generated. When this line is completed, the μPD72185 interrupts processing again. If the ABT command is issued when an interrupt has not been generated, the μPD72185 cancels the continuous processing mode.
BLO (Block operation)	For block mode, specifies minimum number of bits transferred, word length of a line, number of void bits at left/right side, word length of white mask at left/ right side, etc. Normally, encoding/decoding by the μPD72185 is performed through this command.
CLB-ON/OFF (Compression line buffer on/off)	User specifies use of compression line buffer by CLB-ON or CLB-OFF command. Valid only in line mode.
CNT (Continue)	When the CNT command is issued, the μPD72185 processes the next consecutive image area equal in size to the area previously processed using the same processing mode and encoding/decoding system. By means of the CNT command, the μPD72185 can resume processing even when a CFE interrupt has been generated.
EOL (End of line)	During encoding, adds EOL code to coded data; during decoding, detects added EOL code. If the detected EOL code is judged to be part of the RTC code, the μPD72185 starts RTC search.
FILL (Fill	During encoding, adds fill bits to coded data.
LNO (Line operation)	For line mode, specifies number of fill bits to be added, word length of a line, number of void bits at left/right side, tag bit, etc.
MOD (Mode)	Assigns processing mode, encoding/ decoding format (transfer mode in case of a transfer), K-parameter, RTC, enlargement/ reduction, etc.
MSK (White mask)	For line-to-receive mask processing, specifies word length, word length of left/right side white mask, number of void bits on left/ right, etc. Also performs white mask processing on image buffer.
RCLB (Read compression line buffer)	When the RCLB command is received, the μPD72185 reads the contents of the compression line buffer. Provides user with pixel distribution data for a line.

Table 12. List of Commands (cont)

Name	Function
RPRS (Read process status)	Requests statistical information from μPD72185 on number of normally-processed lines, number of error lines, etc., resulting from processing.
RTAG (Read tag pattern)	During decoding, reads tag pattern attached to start of a line. In line mode, interpretation of the tag pattern by the host CPU allows an individual non-CCITT standard encoding/decoding system to be implemented.
RTC (Return to control)	During encoding, adds RTC code to coded data; during decoding, detects added RTC code.
RVER (Read version number)	Reads firmware versions built into μPD72185
SCDB (Set code buffer)	Specifies start address, size, and start bit position of image area (code buffer) that stores code. When the coded data is coming from the host CPU side, the start address should be set to 0.
SIMB (Set image buffer)	Specifies start address of reference line in image memory, and start address and size of image area (image buffer) that stores image data. When a transfer is performed, specifies transfer source/destination address and size of transfer.
SPRS (Set process status)	Specifies initialization values for normal processing line count, maximum error line count, etc., and abort if error line count exceeds maximum.
SYS (System)	Assigns specific system parameters such as image memory organization, bus cycle mode, word length of a line, etc. Also initializes internal μPD72185 parameter table.
TRO (Transfer operation)	Performs data transfer/composition for image buffer specified by IMB command.

* CFE interrupt is generated if a CEMPT or CFULL response is returned.

RESPONSES

The μPD72185 has four types of responses: confirmation, error, statistical, and special. Table 13 describes the response types; table 14 describes the responses.

Table 13. Response Types

Type	Function	Response
Confirmation	Reports normal completion of processing requested by a command	BCDOK, BDCOK,ECDOK, EDCOK, FILLOK, LCDOK, LDCOK, MODOK, MSKOK, POK, RCDOK, RDCOK, SCDBOK, SIMBOK, SOK, SYSOK, TAGPAT, TRNOK, VEROK
Error	Returned when an error occurs during processing requested by a command.	BLABT, CMDERR, DBLCRQ LNABT
Statistical	Returns statistical information in response to a command.	PRSTBL
Special	Other than above.	CEMPT, CFULL, CLBTBL

Table 14. List of Responses

Name	Function
BCDOK (Block code okay)	Indicates normal termination of encoding by BLO command. Sends back to host CPU: number of lines processed; start address of image data buffer following processed image data buffer; start address and start bit position of code buffer following processed code buffer.
BDCOK (Block decode okay)	Indicates normal termination of decoding by BLO command. Sends back to host CPU: number of lines processed; start address of image data buffer following processed image data buffer; start address and start bit position of code buffer following processed code buffer.
BLABT (Block abort)	Indicates that during decoding by BLO command, processing was aborted because error line count exceeded maximum value set by SPRS command. Sends back to host CPU: number of lines processed; start address of image buffer following processed image buffer; start address and start bit position of code buffer following processed code buffer.
CEMPT (CDB empty)	Indicates specified code buffer has become empty during decoding. At this point, the μPD72185 enters the CFE interrupt state and subsequently accepts only SYS, SCDB, CNT, ABT, RPRS, and RCLB commands. If other commands are issued, a CFEERR response is returned.
CFEERR (CDB full/empty error)	In the CFE interrupt state, indicates a command other than SYS, SCDB, CNT, ABT, RPRS, or RCLB has been issued.

Table 14. List of Responses (cont)

Name	Function
CFULL (CDB full)	Indicates specified code buffer has become full during encoding. At this point, the μPD72185 enters the CFE interrupt state and subsequently accepts only SYS, SCDB, CNT, ABT, RPRS, and RCLB commands. If other commands are issued, a CFEERR response is returned.
CLBTBL (CLBTBL table)	Reports compression line buffer contents in response to RCLB command.
CMDERR (Command error)	Indicates that there is no command corresponding to input command code.
DBLCRQ (Double CRQ error)	Indicates receipt of duplicate command requests during processing, and notifies host CPU that processing being executed is invalidated.
ECDOK (EOL code okay)	Indicates EOL code has been added and output to code buffer by EOL command. Sends back to host CPU: start address and start bit position of code buffer following processed code buffer.
EDCOK (EOL decode okay)	Indicates detection of EOL code in code buffer by EOL command. Sends back to host CPU: address and position of bit following detected EOL code.
FILLOK (FILL okay)	Indicates that the number of fill bits specified by a FILL command have been output. Sends back to host CPU: start address and bit position of buffer code following fill bits.
LCDOK (Line code okay)	Indicates normal termination of encoding by LNO command. Sends back to host CPU: number of lines remaining in image buffer; start address of image buffer following processed image buffer; start address and start bit position of code buffer following processed code buffer.
LDCOK (Line decode okay)	Indicates normal termination of decoding by LNO command. Sends back to host CPU: number of lines remaining in image buffer; start address of image buffer following processed image buffer; start address and start bit position of code buffer following processed code buffer.
LNABT (Line abort)	Indicates that during execution of decoding by LNO command, processing was aborted because error line count exceeded maximum value set by SPRS command. Sends back to host CPU: number of lines remaining in image buffer; start address of image buffer following processed image buffer; start address and start bit position of code buffer following processed code buffer.

Table 14. List of Responses (cont)

Name	Function
MODOK (MOD okay)	Indicates normal termination of MOD command processing.
MSKOK (Mask okay)	Indicates normal termination of processing by MSK command. Sends back to host CPU: start address of next image buffer to be processed.
POK (Process okay)	When the μPD72185 is in continuous processing mode, and the object of execution by an ABT command is BLO, LNO, RTAG, EOL, or RTC, then POK indicates continuous processing mode has been discontinued. Sends back to host CPU: start address and start bit position of code buffer following processed code buffer.
PRSTBL (Process status table)	Reports contents of statistical information table before it is initialized by SPRS command. Also reports current contents of table in response to RPRS command.
RCDOK (RTC code okay)	Indicates RTC code has been added and output to code buffer by RTC command. Sends back to host CPU: start address and start bit position of code buffer following processed code buffer.
RDCOK (RTC decode okay)	Indicates detection of RTC code in code buffer by RTC command. Sends back to host CPU: address and position of bit following detected RTC code.
SCDBOK (SCDB okay)	Indicates normal termination of SCDB command processing.
SIMBOK (SIMB okay)	Indicates normal termination of SIMB command processing.
SOK (Set okay)	Indicates that when a CNT or ABT command has been issued and the command to be executed does not exist, the μPD72185 has terminated processing.
SYSOK (SYS okay)	Indicates normal termination of SYS command processing.
TAGPAT (Tag pattern)	Indicates tag pattern specified by an RTAG command has been read. Sends back to host CPU: start address of code buffer following read tag pattern and start bit position of that code buffer.
TRNOK (Transfer okay)	Indicates normal termination of data transfer/composition processing by TRO command. Sends back to host CPU: next transfer source/destination address.
VEROK (RVER okay)	Returns firmware version to the host CPU.

SYSTEM CONFIGURATION

Figure 17 is a diagram of low-end and high-end system configurations.

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Figure 17. System Configurations