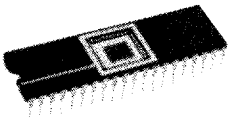
RDC-19220 SERIES

16-BIT MONOLITHIC TRACKING RESOLVER (and LVDT)-TO-DIGITAL CONVERTERS



DESCRIPTION

The RDC-19220 Series are low cost versatile 16-bit monolithic state-of-the-art Resolver(and LVDT)-to-Digital Converters. These single chip converters are available in small 40 pin DDIP, 28 pin DDIP, or 44 pin J-Lead packages and offer programmable features such as resolution, bandwidth, and velocity output scaling.

Resolution programming allows selection of 10-, 12-, 14-, or 16-bit, with accuracies to 2.3 min. This feature combines the high tracking rate of a 10-bit converter with the precision and low speed velocity resolution of a 16-bit converter in one package.

The velocity output (VEL) from the RDC-19220 Series, which can be used to replace a tachometer, is a 4 V signal referenced to ground with a linearity of 0.75% of output voltage. The full scale value of VEL is set by the user with a single resistor.

RDC-19220 Series converters are available with operating temperature ranges of 0° to +70°C, -40° to +85°C, and -55° to +125°C, and military processing is available (consult factory).

APPLICATIONS

With its low cost, small size, high accuracy, and versatile performance, the RDC-19220 Series converters are ideal for use in modern high performance industrial and military control systems. Typical applications include motor control, radar antenna positioning, machine tool control, robotics, and process control.

FEATURES

- *+5 Volt Only Option*
- *Only 5 External Passive Components*
- *Programmable:*
  - *Resolution: 10-, 12-, 14-, or 16-Bit*
  - *Bandwidth: to 1200 Hz*
  - *Tracking: to 2300 RPS*
- *Differential Resolver and LVDT Input Modes*
- *Velocity Output Eliminates Tachometer*
- *Built-In-Test ($\overline{BIT}$) Output, No 180° Hangup*
- *Small Size: 28 or 40 Pin DDIP or 44 Pin J-Lead Package*
- *-55° to +125°C Operating Temperature*

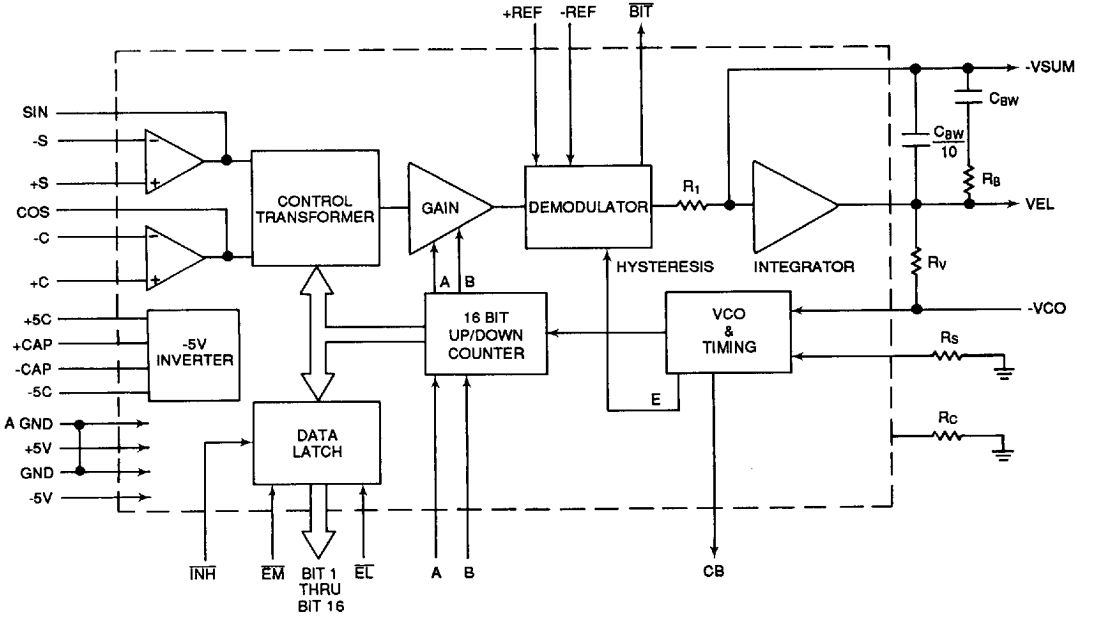


FIGURE 1. RDC-19220 SERIES BLOCK DIAGRAM

TABLE 1. RDC-19220 SPECIFICATIONS
These specs apply over the rated power supply, temperature, and reference frequency ranges; and 10% signal amplitude variation & 10% harmonic distortion.

PARAMETER	UNIT	VALUE
RESOLUTION	Bits	10, 12 , 14, or 16
ACCURACY	Min	8, 4, or 2 + 1 LSB (note 3)
REPEATABILITY	LSB	1 max
DIFFERENTIAL LINEARITY	LSB	1 max in the 16th bit
REFERENCE		(+REF, -REF)
Type		Differential
Voltage: differential	V	±10 max
single ended	V	±5 max
overload	V	±25 continuous, 100 transient
Frequency	Hz	DC to 40,000 (note 4)
Input Impedance	Ohm	10M min //20 pf
SIGNAL INPUT		(+S, -S, SIN, +C, -C, COS)
Type		Resolver, differential, groundbased
Voltage: operating	Vrms	2 ±15%
overload	V	±25 continuous
Input impedance	Ohm	10M min //10 pf.
DIGITAL INPUT/OUTPUT		
Logic Type		TTL/CMOS compatible
Inputs		Logic 0 = 0.8V max. Logic 1 = 2.0V min. Loading =10µa max P.U. current source to +5 V //5pF max. CMOS transient protected
Inhibit ($\overline{INH}$)		Logic 0 inhibits; Data stable within 0.3 µS
Enable Bits 1 to 8 ($\overline{EM}$)		Logic 0 enables; Data stable
Enable Bits 9 to 16 ($\overline{EL}$)		within 150 nS Logic 1 = High Impedance Data High Z within 100 nS
Resolution and Mode Control(A & B) (see notes 1 and 2.)		Mode B A Resolution resolver 0 0 10 bits " 0 1 12 bits " 1 0 14 bits " 1 1 16 bits LVDT -5 V 0 8 bits " 0 -5 V 10 bits " 1 -5 V 12 bits " -5 V -5 V 14 bits
Outputs		
Parallel Data (1-16)		10, 12, 14, or 16 parallel lines; natural binary angle, positive logic (see note 2)
Converter Busy (CB)		0.25 to 0.75 µs positive pulse leading edge initiates counter update.
Zero Index	(ZI)	Logic 1 at all 0s [$\overline{ENL}$ to -5 V]; LSBs are enabled

NOTES: 1. Unused data bits are set to logic "0".
2. In LVDT mode, Bit 16 is LSB for 14-Bit resolution or Bit 12 is LSB for 10-Bit resolution.
3. Accuracy in LVDT mode is 0.15% + 1LSB of full scale.
4. See text for higher tracking rates and carrier frequencies, which depend on R_S and R_C selection.
5. See text, General Setup Considerations.

TABLE 1. RDC-19220 SPECIFICATIONS (continued)

PARAMETER	UNIT	VALUE
DIGITAL INPUT/OUTPUT (continued)		
Outputs (continued)		
Built-in-Test ($\overline{BIT}$)		Logic 0 for BIT condition. ±100 LSBs of error with a filter of 500 µS, Loss-of-Signal (LOS), or Loss-of-Reference (LOR).
Drive Capability		50 pF + Logic 0; 1 TTL load, 1.6 mA at 0.4 V max Logic 1; 10 TTL loads, -0.4 mA at 2.8 V min Logic 0; 100 mV max driving CMOS Logic 1; +5 V supply minus 100 mV min driving CMOS High Z; 10 uA //5 pF max

DYNAMIC CHARACTERISTICS		(at maximum bandwidth)			
Resolution	bits	10	12	14	16
Tracking Rate (min)(note 4)	rps	1152	288	72	18
Bandwidth(Closed Loop)	Hz	1200	1200	600	300
Ka	$1/sec^2$	5.7M	5.7M	1.4M	360k
A_1	1/sec	19.5	19.5	4.9	1.2
A_2	1/sec	295k	295k	295k	295k
A	1/sec	2400	2400	1200	600
B	1/sec	1200	1200	600	300
Acceleration (1LSB lag)	deg/s^2	2M	500k	30k	2k
Settling Time(179° step)	msec	2	8	20	50

VELOCITY CHARACTERISTICS			
Polarity		Positive for increasing angle	
Voltage Range(Full Scale)	V	±4 (at nominal ps)	
Scale Factor Error	%	10 typ	20max
Scale Factor TC	PPM/C	100 typ	200 max
Reversal Error	%	0.75 typ	1.3 max
Linearity	%	0.25 typ	0.50 max
Zero Offset	mv	5 typ	10 max
Zero Offset TC	µV/C	15 typ	30max
Load	kΩ		8 max

POWER SUPPLIES		(note 5)	
Nominal Voltage	V	+5	-5
Voltage Range	%	± 5	+5, -20
Max Volt. w/o Damage	V	+7	-7
Current	mA	14 typ,22 max	

TEMPERATURE RANGE		
Operating		
-30X	°C	0 to +70
-20X	°C	-40 to +85
-10X	°C	-55 to +125
Storage	°C	-65 to +150

PHYSICAL CHARACTERISTICS			
Size: 40 pin DDIP	in	2.0 x 0.6 x 0.2 (50.8 x 15.24 x 5.08)	
28 pin DDIP	(mm)	1.4 x 0.6 x 0.2 (35.56 x 15.24 x 5.08)	
44 pin J-Lead		0.690 square (17.526)	
		Plastic	Ceramic
Weight: 40 pin DDIP	oz	0.21 (5.95)	0.24 (6.80)
28 pin DDIP	(g)	0.15 (4.25)	0.16 (4.54)
44 pin J-Lead		0.08 (2.27)	0.065 (1.84)

THEORY OF OPERATION

The RDC-19220 series of converters are single CMOS custom monolithic chips. They are implemented using the latest IC technology which merges precision analog circuitry with digital logic to form a complete high-performance tracking resolver-to-digital converter. For user flexibility and convenience, the converter bandwidth, dynamics, and velocity scaling are externally set with passive components.

FIGURE 1 is the Functional Block Diagram of RDC-19220 Series. The converter operates with ±5 Vdc power supplies. Analog signals are referenced to analog ground, which is at ground potential. The converter is made up of two main sections; a converter and a digital Interface. The converter front end consists of sine and cosine differential input amplifiers. These inputs are protected to ±25 V with 2 kΩ resistors and diode clamps to the ±5 Vdc supplies. These amplifiers feed the high accuracy Control Transformer (CT). Its other input is the 16-bit digital angle ϕ. Its output is an analog error angle, or difference angle, between the two inputs. The CT performs the ratiometric trigonometric computation of $SIN\theta COS\phi - COS\theta SIN\phi = SIN(\theta-\phi)$ using amplifiers, switches, logic, and capacitors in precision ratios. **Note:** The transfer function of the CT is normally trigonometric, but in LDVT-mode the transfer function is triangular (linear) and could thereby convert any linear transducer output.

The converter accuracy is limited by the precision of the computing elements in the CT. In these converters ratioed capacitors are used in the CT, instead of the more conventional precision ratioed resistors. Capacitors used as computing elements with op-amps need to be sampled to eliminate voltage drifting. Therefore, the circuits are sampled at a high rate (67 kHz) to eliminate this drifting and at the same time to cancel out the op-amp offsets.

The error processing is performed using the industry standard technique for type II tracking R/D converters. The dc error is integrated yielding a velocity voltage which in turn drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which together with the velocity integrator forms a type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above. The settings of the various error processor gains and break frequencies are done with external resistors and capacitors so that the converter loop dynamics can be easily controlled by the user.

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its Transfer Function Block Diagrams and its Bode Plots (open and closed loop). These are shown in FIGURES 2, 3, and 4. The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where A is the gain coefficient and $A^2 = A_1A_2$
and B is the frequency of lead compensation

The components of gain coefficient are error gradient, integrator gain, and VCO gain. These can be broken down as follows:

- Error Gradient = 0.011 volts per LSB (CT+Error Amp+Demod with 2Vrms input)

- Integrator gain = $\frac{C_SF_S}{1.1C_{BW}}$ volts per second per volt

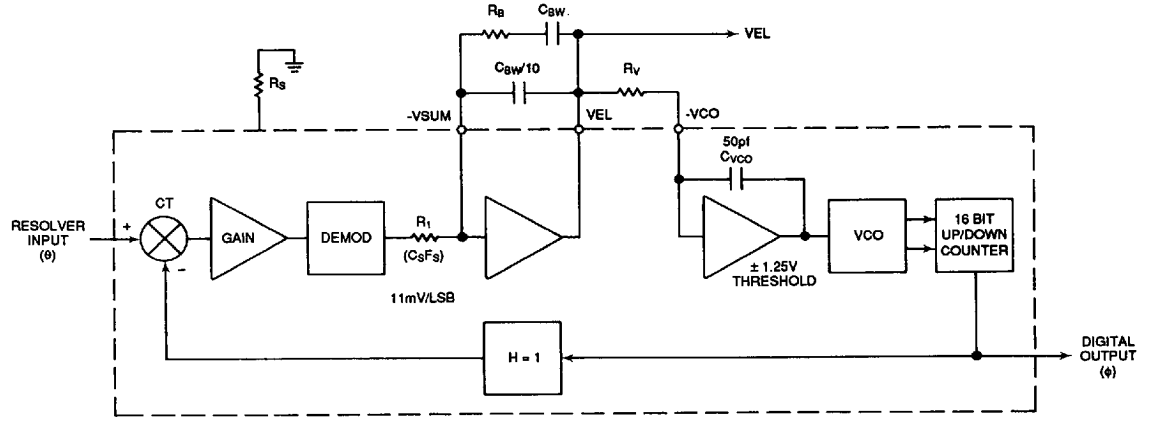


FIGURE 2. TRANSFER FUNCTION BLOCK DIAGRAM #1

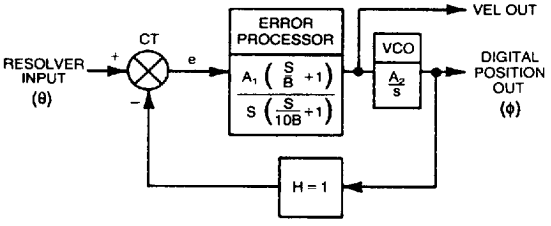


FIGURE 3. TRANSFER FUNCTION BLOCK DIAGRAM #2

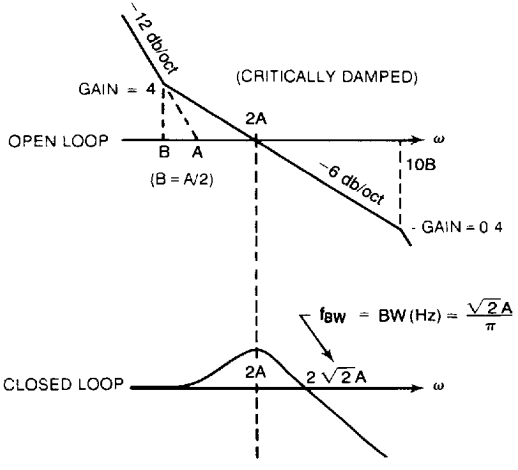


FIGURE 4. BODE PLOTS

- VCO Gain = $\frac{1}{1.25 R_V C_{VCO}}$ LSBs per second per volt

where: $C_S = 10$ pF
$F_S = 67$ kHz when $R_S = 30$ kΩ
$F_S = 100$ kHz when $R_S = 20$ kΩ
$F_S = 134$ kHz when $R_S = 15$ kΩ
$C_{VCO} = 50$ pF

R_V, R_B, and C_{BW} are selected by the user to set velocity scaling and bandwidth.

GENERAL SETUP CONSIDERATIONS

DDC has external component selection software which considers all the criteria below, and in a simple fashion, asks the key parameters (carrier frequency, resolution, bandwidth, and tracking rate) to derive the external component value.

The following recommendations should be considered when hooking up the RDC-19220 Series R/D converters:

1) Power supplies are ±5 Vdc. For lowest noise performance it is recommended that a 10 µF or larger cap be connected from each supply to ground near the converter package.

2) Resolver inputs and velocity output are referenced to A GND. This pin should be connected to GND near the converter package. Digital currents flowing through ground will not disturb the analog signals.

3) The $\overline{BIT}$ output which is active low is activated by an error of about 100 LSBs. During normal operation for step inputs or on power up a large error can exist. Connecting the $\overline{BIT}$ output back to the resolution control lines, A and B, which would change the resolution of the converter down, would make the converter settle out faster. The converter bandwidth is independent of the resolution.

4) Setup of bandwidth and velocity scaling for the optimized critically damped case should proceed as follows:

   - Select the desired f_{BW}(closed loop), based on overall system dynamics.

   - Select $f_{carrier} \geq 3.5\ f_{BW}$

   - Compute $R_V = 55k\Omega \times \frac{\{\text{For the converter max tracking rate value, see the row indicated in Table 3.}\}}{\text{Application max rate}}$

   - Compute $C_{BW}(pf) = \frac{3.2 \times F_S\,(Hz) \times 10^8}{R_V \times (f_{BW})^2}$

   - Where F_S = 67 kHz for $R_S = 27$ kΩ
     100 kHz for $R_S = 20$ kΩ
     134 kHz for $R_S = 15$ kΩ

- Compute $R_B = \frac{0.9}{C_{BW} \times f_{BW}}$

- Compute $\frac{C_{BW}}{10}$

5) Selecting a f_{BW} that is too low relative to the maximum application tracking rate can create a spin-around condition in which the converter never settles. The relationship to insure against spin-around is as follows:

TABLE 2. TRACKING/BW RELATIONSHIP	
RPS (max)/ BW	RESOLUTION
2	10
0.9	12
0.35	14
0.15	16

6a) **For RDC-19222:**
When using the built-in -5 V inverter: connect pin 2 to 26, pin 17 to 22, a 10 µF/10 Vdc capacitor from pin 23 (negative terminal) to pin 25 (positive terminal), and a 47 µF/10 Vdc capacitor from -5 V to GND. The current drain from the +5 V supply doubles. No external -5 V supply is needed.

6b) **For RDC-19223:**
When using the built-in -5 V inverter: connect pin 2 to 22, pin 10 to 18, a 10 µF/10 Vdc capacitor from pin 19 (negative terminal) to pin 21 (positive terminal), and a 47 µF/10 Vdc capacitor from -5 V to GND. The current drain from the +5 V supply doubles. No external -5 V supply is needed.

HIGHER TRACKING RATES AND CARRIER FREQUENCIES.

Tracking rate (nominally 4 V) is limited by two factors: velocity voltage saturation and maximum internal clock rate (nominally 1,333,333 Hz). An understanding of their interaction is essential to extending performance.

The General Setup Considerations section makes note of the selection of R_V for the desired velocity scaling. R_V is the input resistor to an inverting integrator with a 50 pF nominal feedback capacitor. When it integrates to -1.25 V, the converter counts up 1 LSB and when it integrates to +1.25 V, the converter counts down 1 LSB. When a count is taken, a charge is dumped on the capacitor; such that, the voltage on it changes 1.25 V in a direction to bring it to 0 V. The output counts per second per volt input is therefore:

$$\frac{1}{(R_V \times 50pF \times 1.25)}$$

As an example:
Calculate R_V for the maximum counting rate, at a VEL voltage of 4 V.

For a 12-bit converter there are 2^{12} or 4096 counts per rotation. 1,333,333/4096 = 325 rotations per second or 333,333 counts per second per volt.

$$R_V = \frac{1}{(333{,}333 \times 50pF \times 1.25)} = 48k \text{ ohms}$$

The maximum rate capability of the RDC-19220 is set by R_S. When R_S = 27 kΩ it is nominally 1,333,333 counts/sec, which equates to 325 rps (rotations per second). The converter maximum tracking rate can be increased 50% in the 16- and 14-bit modes and 100% in the 12- and 10-bit modes by increasing the supply current from 12 to 15 mA (by using an R_C = 23 kΩ); and by increasing the sampling rate by changing R_S to 20 kΩ for 16- and 14-bit resolution or to 15 kΩ for 12- and 10-bit resolution. (See TABLE 3.)

The maximum carrier frquency can, in the same way, increase from: 5 to 10 kHz in the 16-bit mode, 7 to 14 kHz in the 14-bit mode, 11 to 32 kHz in the 12-bit mode, and 20 to 40 kHz in the 10-bit mode. (See TABLE 4.)

The maximum tracking rate and carrier frequency for full performance are set by the power supply current control resistor (R_C) per the following tables:

TABLE 3. MAX TRACKING RATE (MIN) IN RPS					
R_C	R_S	RESOLUTION			
		10	12	14	16
30k or open	27 k	1152	288	72	18
23 k	20 k	1728	432	108	27
23 k	15 k	2304	576	*	*

*Not recommended

Depending on the resolution, select one of the values from this row, for use in converter max tracking rate formula. (See previous page for formula.)

TABLE 4. CARRIER FREQUENCY (MAX) IN KHZ					
R_C	R_S	RESOLUTION			
		10	12	14	16
30k or open	27 k	20	11	7	5
23 k	27 k	24	12	11	7
23 k	20 k	34	24	14	10
23 k	15 k	40	32	*	*

*Not recommended

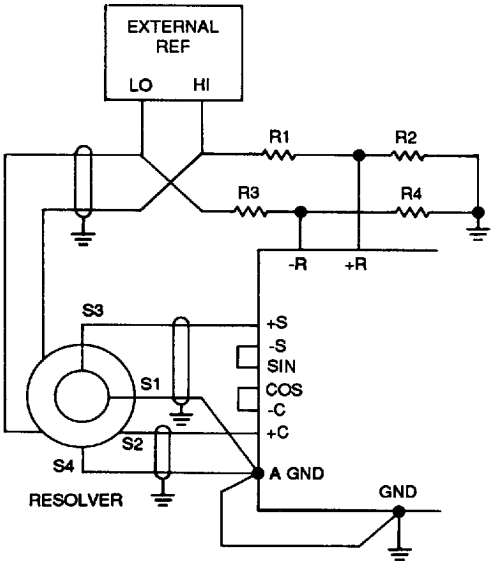
Carrier frequency should be 1/10, or less, of the sampling frquency in order to have many samples per carrier cycle. The converter will work with reduced quadrature rejection at a carrier frequency up to 1/4 the sampling frequency. Carrier frequency should be at least 3.5 times the BW in order to eliminate the chance of jitter.

REDUCED POWER SUPPLY CURRENTS

When R_S = 27 kΩ , and the tracking is not being pushed, power supply current can be cut from 14 to 9 mA by setting R_C = 53 kΩ.

TYPICAL INPUTS

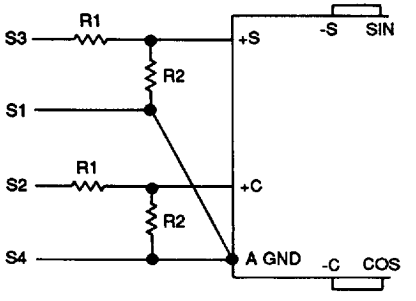
FIGURES 5 through 8 illustrate typical input configurations.



Notes:

1. Resistors selected to limit V_{ref} peak to between 1 V and 4 V.
2. If External Reference LO is grounded, then R3 and R4 are not needed, and -R is connected to GND.

FIGURE 5. TYPICAL HOOK-UP, 2V RESOLVER, DIRECT INPUT

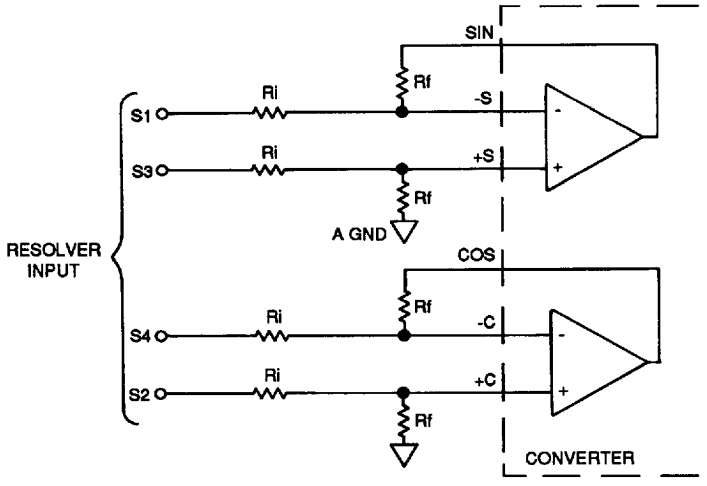


$$\frac{R2}{R1+R2} = \frac{2}{X\ Volt}$$

R1 + R2 should not load the Resolver too much; it is recommended to use a R2 =10 k.

R1 + R2 Ratio Errors will result in Angular Errors, 2 cycle, 0.1% Ratio Error = 0.029° Peak Error.

FIGURE 6. TYPICAL HOOK-UP, X- VOLT RESOLVER, DIRECT INPUT

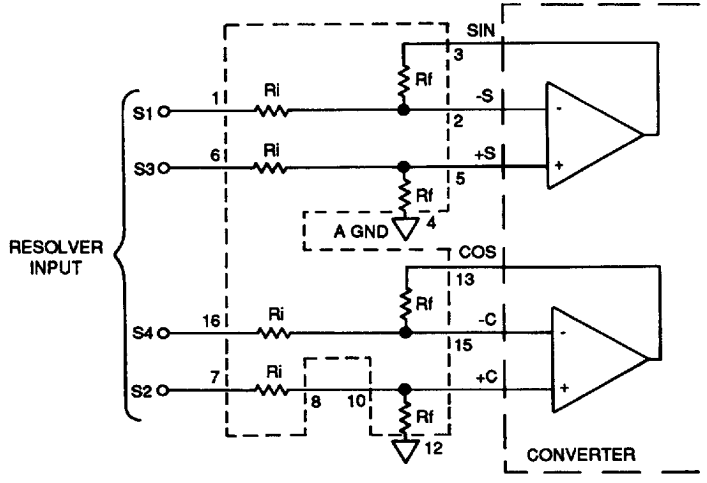


$\frac{Ri}{Rf}$ X 2 Vrms = Resolver L-L rms voltage

Rf ≥ 6 kΩ

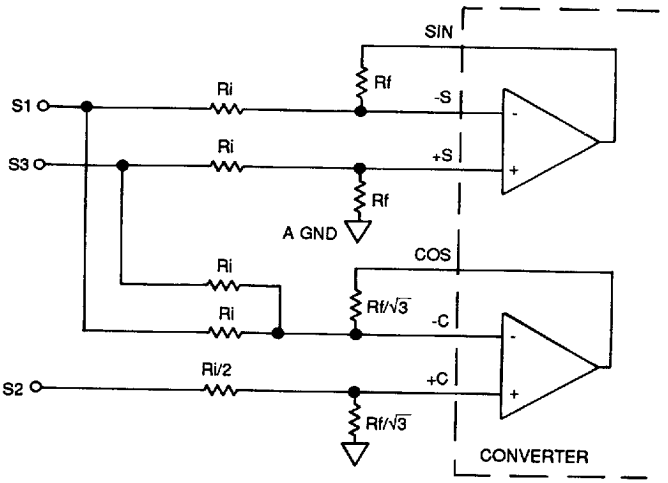
S1 and S3, S2 and S4, and RH and RL should be ideally twisted shielded, with the shield tied to GND at the converter.

FIGURE 7A. DIFFERENTIAL RESOLVER INPUT



S1 and S3, S2 and S4, and RH and RL should be ideally twisted shielded, with the shield tied to GND at the converter.
For DDC-49530: Ri = 70.8 kΩ, 11.8 V input, synchro or resolver.
For DDC-49590: Ri = 270 kΩ, 90 V input, synchro or resolver.
Maximum addition error is 1 minute.

FIGURE 7B. DIFFERENTIAL RESOLVER INPUT, USING DDC-49530 (11.8 V) OR DDC-49590 (90 V)

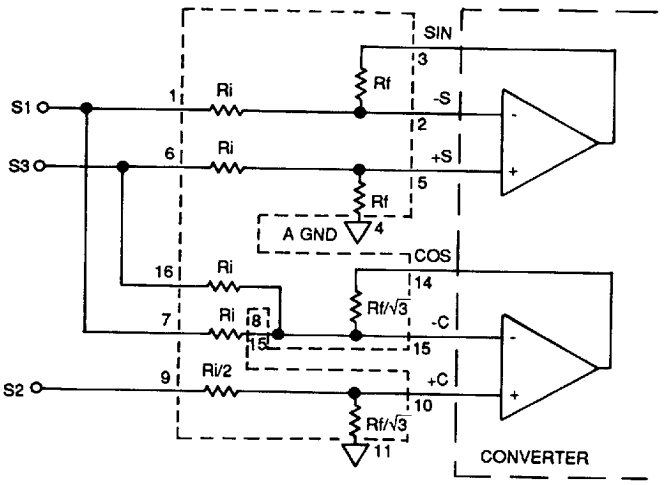


$\frac{Ri}{Rf}$ X 2 Vrms = Synchro L-L rms voltage

Rf ≥ 6 kΩ

S1, S2, and S3 should be triple twisted shielded; RH and RL should be twisted shielded. In both cases the shield should be tied to GND at the converter.

FIGURE 8A. SYNCHRO INPUT



S1, S2, and S3 should be triple twisted shielded; RH and RL should be twisted shielded. In both cases the shield should be tied to GND at the converter.
90 V input = DDC-49590: Ri = 270 kΩ, 90 V input, synchro or resolver.
11.8 V input = DDC-49530: Ri = 70.8 kΩ, 11.8 V input, synchro or resolver.
Maximum addition error is 1 minute.

FIGURE 8B. SYNCHRO INPUT, USING DDC-49530 (11.8 V) OR DDC-49590 (90 V)

DC INPUTS

As noted in TABLE 1 the RDC-19220 will accept dc inputs. It is necessary to set the REF input to dc by tying +REF to +5 V and -REF to GND or -5 V.

VELOCITY TRIMMING

RDC-19220 Series specifications for velocity scaling, reversal error, and offset are contained in TABLE 1. Velocity scaling and offset are externally trimmable for applications requiring tighter specifications than those available from the standard unit. FIGURE 9 shows the setup for trimming these parameters with external pots. It should also be noted that when the resolution is changed, VEL Scaling is also changed. Since the VEL output is from an integrator with capacitor feedback, the VEL voltage cannot change instantaneously. Therefore, when changing resolution while moving, there will be a transient with a magnitude proportional to the velocity and a duration determined by the converter bandwidth. This transient **does not** effect position data.

ADDITIONAL ERROR SOURCES

Quadrature voltages in a resolver or synchro are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. A digital position error will result due to the interaction of this quadrature voltage and a reference phase shift between the converter signal and reference inputs. The magnitude of this error is given in the following formula:

Magnitude of Error = (Quadrature Voltage/F.S.signal) * tan (α)

Where:

Magnitude of Error is in radians
Quadrature Voltage is in volts
Full Scale signal is in volts
α = signal to REF phase shift

An example of the magnitude of error is as follows:

Let: Quadrature Voltage = 11.8 mV
Let: F.S. signal = 11.8 V
Let:: $\alpha = 6^{\circ}$

Then: Magniture of Error = 0.36 min ≡ 1 LSB in the 16th bit.
Note: Quadrature is composed of static quadrature which is specified by the synchro or resolver supplier plus the speed voltage which is determined by the following formula:

Speed Voltage=(rotational speed/carrier frequency * F.S.signal

Where:

Speed Voltage is the quadrature due to rotation.
Rotation speed is the rps (rotations per second) of the synchro or resolver.

Carrier frequency is the REF in Hz.
A circuit to LEAD or LAG the reference into the converter in order to compensate for phase-shift is illustrated in FIGURE 10.

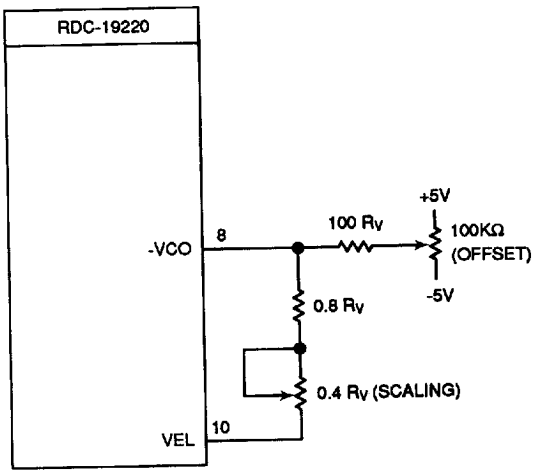
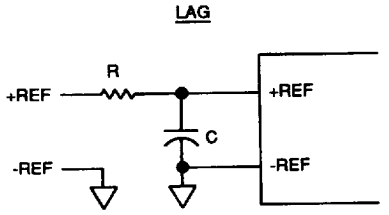
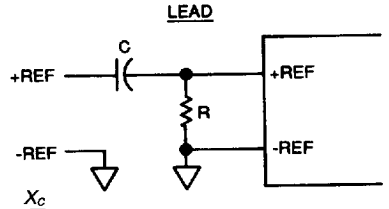


FIGURE 9. VELOCITY TRIMMING





$$\tan \varphi = \frac{X_c}{R}$$

Where φ = desired phase-shift

$$X_c = \frac{1}{2\pi fc}$$

Where f = carrier frequency
Where c = capacitance

FIGURE 10. PHASE-SHIFT COMPENSATION

LVDT MODE

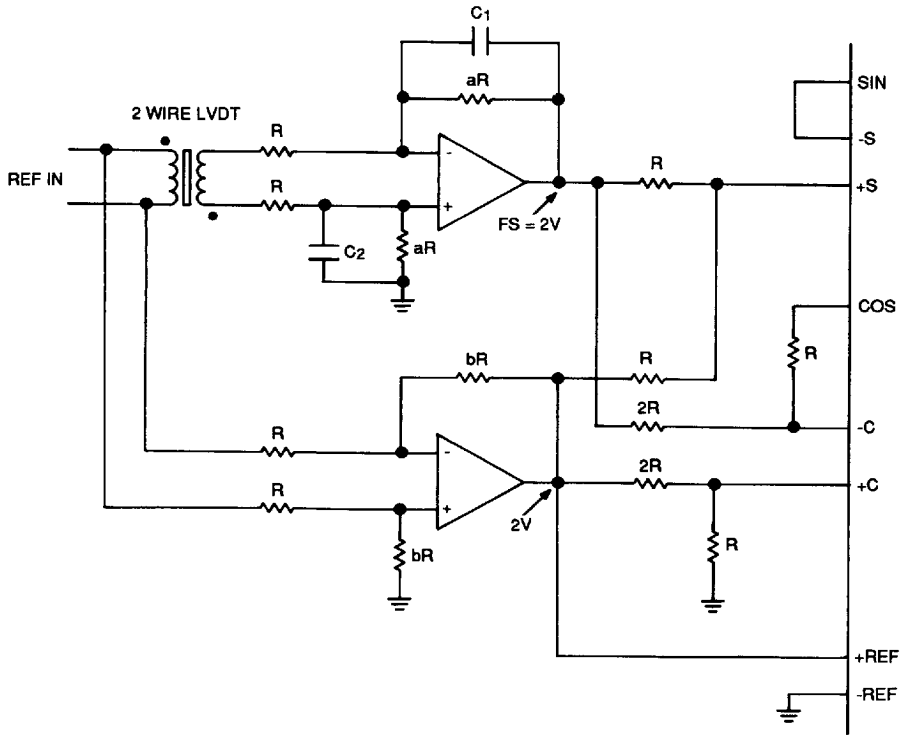
As shown in TABLE 1 the RDC-19220 Series units can be made to operate as LVDT-to-digital converters by connecting Resolution Control inputs A and B to "0," "1," or the -5 volt supply. In this mode the RDC-19220 Series functions as a ratiometric tracking linear converter. When linear ac inputs are applied from a LVDT the converter operates over one quarter of its range. This results in two less bits of resolution for LVDT mode than are provided in resolver mode.

FIGURE 11B shows a direct LVDT 1 Vrms full scale input. Some LDVT output signals will need to be scaled to be compatible with the converter input. FIGURE 11C is a schematic of an input scaling circuit applicable to 3-wire LVDTs. The value of the scaling constant "a" is selected to provide an input of 2 Vrms at full stroke of the LVDT. The value of scaling constant "b" is selected to provide an input of 1 Vrms at null of the LVDT. Suggested components for implementing the input scaling circuit are a quad op amp, such as a 4741 type, and precision film resistors of 0.1% tolerance. FIGURE 11A illustrates a 2-wire LVDT configuration.

Data output of the RDC-19220 Series is Binary Coded in LVDT mode. The most negative stroke of the LVDT is represented by ALL ZEROS and the most positive stroke of the LVDT is represented by ALL ONES. The most significant 2 bits (2 MSBs) may be used as overrange indicators. Positive overrange is indicated by code "01" and negative overrange is indicated by code "11" (see TABLE 5).

TABLE 5. LVDT OUTPUT CODE

LVDT OUTPUT	MSB			LSB
+ over full travel	01	xxxx	xxxx	xxxx
+ full travel -1LSB	00	1111	1111	1111
+ 0.5 travel	00	1100	0000	0000
+ 1LSB	00	1000	0000	0001
null	00	1000	0000	0000
- 1LSB	00	0111	1111	1111
- 0.5 travel	00	0100	0000	0000
- full travel	00	0000	0000	0000
- over full travel	11	xxxx	xxxx	xxxx



$C_1 = C_2$, set for phase lag = phase lead through the LVDT.

FIGURE 11A. 2-WIRE LVDT DIRECT INPUT

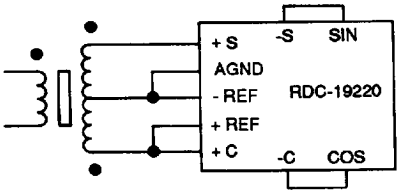
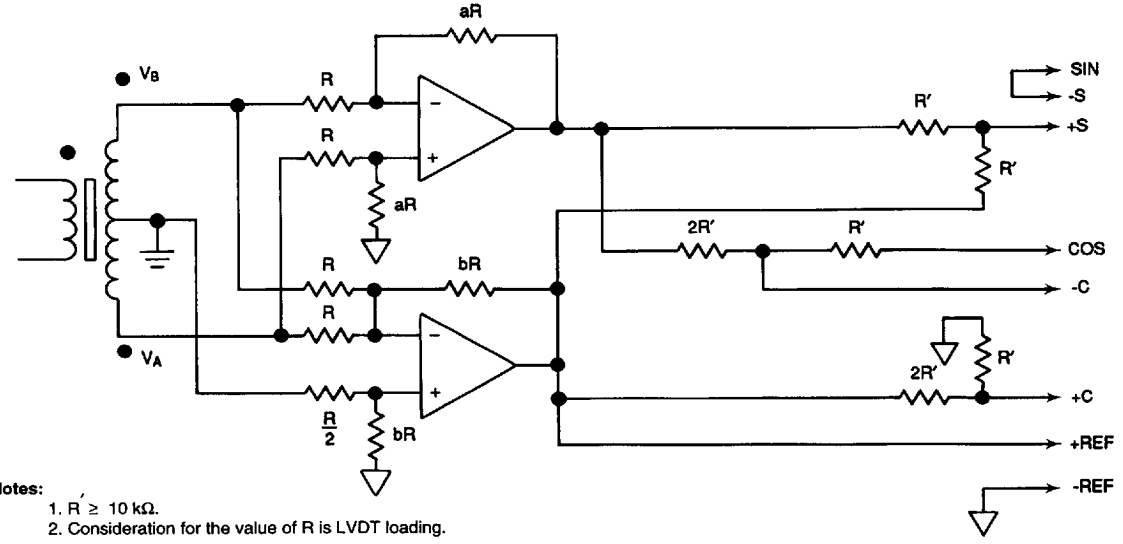
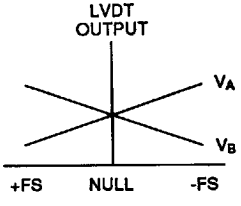


FIGURE 11B. 3-WIRE LVDT DIRECT INPUT



Notes:
1. R′ ≥ 10 kΩ.
2. Consideration for the value of R is LVDT loading.



$$b = \frac{1}{V_{A_{null}}} = \frac{1}{V_{B_{null}}}$$

$$a = \frac{2}{(V_A - V_B)_{max}}$$

$$SIN = 1 + \frac{a}{2}(V_A - V_B)$$

$$COS = 1 - \frac{a}{2}(V_A - V_B)$$

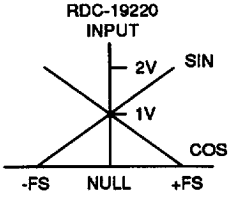


FIGURE 11C. 3-WIRE LVDT SCALING CIRCUIT

INHIBIT, ENABLE, and CB TIMING

The Inhibit (INH) signal is used to freeze the digital output angle in the transparent output data latch while data is being transferred. Application of an Inhibit signal does not interfere with the continuous tracking of the converter. As shown in FIGURE 12, angular output data is valid 300 ns maximum after the application of the negative inhibit pulse.

Output angle data is enabled onto the tri-state data bus in two bytes. Enable MSBs ($\overline{EM}$) is used for the most significant 8 bits and Enable LSBs ($\overline{EL}$) is used for the least significant 8 bits. As shown in FIGURE 13, output data is valid 150 ns maximum after the application of a negative enable pulse. The tri-state data bus returns to the high impedance state 100 ns maximum after the rising edge of the enable signal.

The Converter Busy (CB) signal indicates that the tracking converter output angle is changing 1 LSB. As shown in FIGURE 14, output data is valid 150 ns maximum after the middle of the CB pulse. CB pulse width is 1/40 Fs, which is nominally 375 ns.

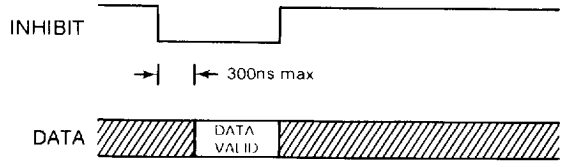


FIGURE 12. INHIBIT TIMING

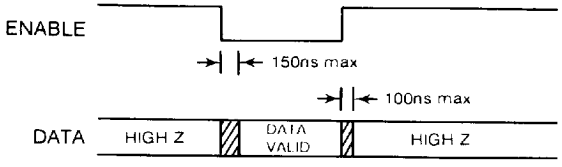


FIGURE 13. ENABLE TIMING

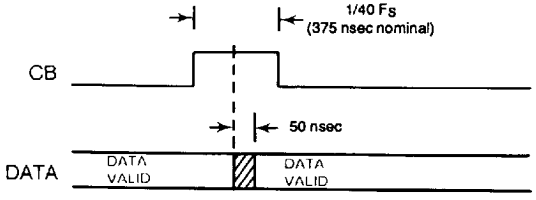


FIGURE 14. CONVERTER BUSY TIMING

BUILT-IN-TEST ($\overline{BIT}$)

The Built-In-Test output ($\overline{BIT}$) monitors the level of error from the demodulator. This signal is the difference in the input and output angles and ideally should be zero, if it exceeds approximately 55 LSBs (of the selected resolution) the logic level at $\overline{BIT}$ will change from a logic 1 to a logic 0.

This condition will occur during a large step and reset after the converter settles out. $\overline{BIT}$ will also change to logic 0 for an over-velocity condition, because the converter loop cannot maintain input-output or and if the converter malfunctions where it cannot maintain the loop at a null. $\overline{BIT}$ will also be set low for a detected Loss-of-Signal (LOS) and/or a Loss-of-Reference (LOR).

LOS will be detected if both sin and cos input voltages are less than 800 mV peak. LOR will be detected if the differential reference voltage is less than 20 mV peak.

ENCODER EMULATION

The RDC-19220 can be made to emulate incremental optical encoder output signals, where such an interface is desired. This is accomplished by tying $\overline{EL}$ to -5 V, whereby CB becomes Zero Index (ZI) Logic 1 at all 0s, the LSB+1 becomes A, and the exclusive-or of the LSB and LSB+1 becomes B emulating A QUAD B signals as illustrated in FIGURE 15A. Also, the LSB byte is enabled.

FIGURE 15B illustrates a more detailed circuit with delays and filtering to eliminate potential glitch due to data skew and rise/fall differences caused by logic loading.

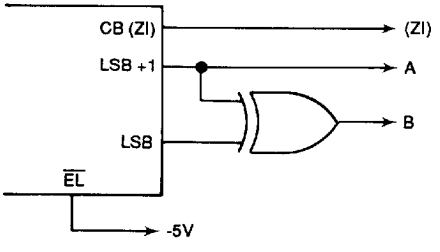
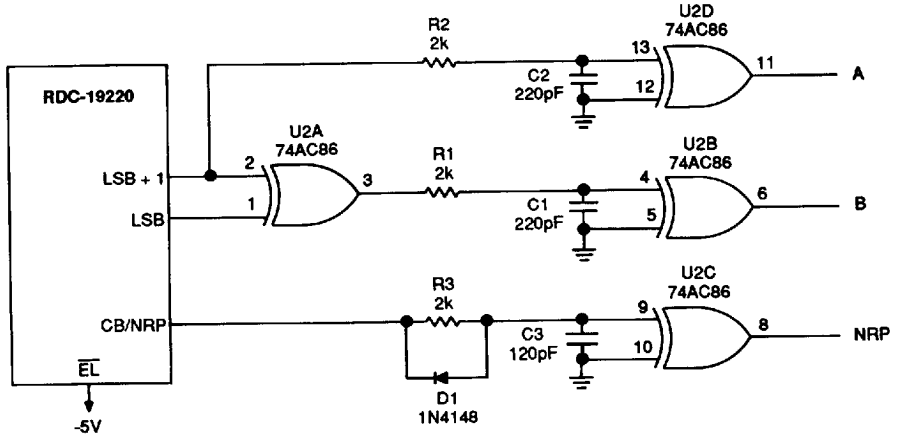


FIGURE 15A. INCREMENTAL ENCODER EMULATION



NOTE: CMOS LOGIC IS RECOMMENDED. TTL AND TTL COMPATABLE LOGIC WILL SKEW THE DELAYS.

FIGURE 15B. FILTERED/BUFFERED ENCODER EMULATOR CIRCUIT

TYPICAL -5 VOLT CIRCUITS

Since the 28 and 40 pin DDIP RDC-19220 and RDC-19221 do not have a pinout for the -5 V inverter, it may be necessary to create a -5 V from other supplies on the board. FIGURE 16 illustrates several possibilities.

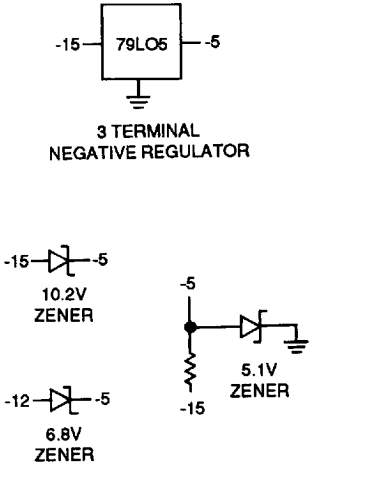


FIGURE 16. TYPICAL -5 VOLT CIRCUITS

PIN OUT FUNCTION TABLES BY MODEL NUMBER

The following tables detail pin out funcitons by the DDC model number. Note that while both the RDC-19220 and the RDC-19223 are 40 pin packages, they differ in functional offerings.

The RDC-19220 has differential inputs but requires both ±5 V power supplies.

The 28 pin RDC-19221 has single-ended inputs, and requires both ±5 V power supplies, and the output is only available in two 8-bit bytes.

The RDC-19222 has differential inputs and can be used with +5 V only.

The RDC-19223 can be used with +5 V only, but has single-ended inputs.

TABLE 7. PIN OUT (40 PIN) RDC-19220

#	NAME	DESCRIPTION	#	NAME	DESCRIPTION
1	A	Resolution Control	40	+5 V	Power Supply
2	B	Resolution Control	39	$\overline{EL}$	Enable LSBs (see note)
3	$\overline{INH}$	Inhibit	38	Bit 16	LSB
4	+REF	+Reference Input	37	Bit 8	
5	-REF	-Reference Input	36	Bit 15	
6	-VCO	Neg VCO Input	35	Bit 7	
7	-VSUM	Vel Sum Point	34	Bit 14	
8	VEL	Velocity Output	33	Bit 6	
9	+C	Signal Input	32	Bit 13	
10	COS	Signal Input	31	Bit 5	
11	-C	Signal Input	30	Bit 12	
12	+S	Signal Input	29	Bit 4	
13	+SIN	Signal Input	28	Bit 11	
14	-S	Signal Input	27	Bit 3	
15	-5V	Power Supply	26	Bit 10	
16	R_S	Sampling Set	25	Bit 2	
17	R_C	Current Set	24	Bit 9	
18	$\overline{EM}$	Enable MSBs	23	Bit 1	MSB
19	A GND	Analog Ground	22	CB	Converter Busy
20	GND	Ground	21	$\overline{BIT}$	Built-In-Test

TABLE 6. PIN OUT (44 PIN, +5 V ONLY) RDC-19222

#	NAME	#	NAME
1	$\overline{EL}$	44	Bit 16 (LSB)
2	+5V	43	Bit 8
3	A	42	Bit 15
4	B	41	Bit 7
5	$\overline{INH}$	40	Bit 14
6	+REF	39	Bit 6
7	-REF	38	Bit 13
8	-VCO	37	Bit 5
9	-VSUM	36	Bit 12
10	VEL	35	Bit 4
11	+C	34	Bit 11
12	COS	33	Bit 3
13	-C	32	Bit 10
14	+S	31	Bit 2
15	SIN	30	Bit 9
16	-S	29	Bit 1 (MSB)
17	-5V	28	CB
18	R_S	27	$\overline{BIT}$
19	R_C	26	+5C (+5 V)
20	$\overline{EM}$	25	+CAP
21	A GND	24	GND
22	-5C(-5 V)	23	-CAP

Notes:
1. When -5 V is applied to pin 1 ($\overline{EL}$), Converter Busy (CB) becomes Zero Index (ZI).
2. When using the built-in -5 V inverter: connect pin 2 to 26, pin 17 to 22, and a 10 µF/10Vdc capacitor from pin 23 (negative terminal) to pin 25 (positive terminal). Connect a 47 µF/10 Vdc capacitor from -5 V to GND. The current drain from the +5 V supply doubles. No external -5 V supply is needed.

TABLE 8. PIN OUT (40 PIN, +5 V ONLY) RDC-19223

#	NAME	#	NAME
1	$\overline{EL}$	40	Bit 16 (LSB)
2	+5V	39	Bit 8
3	A	38	Bit 15
4	B	37	Bit 7
5	$\overline{INH}$	36	Bit 14
6	+REF	35	Bit 6
7	-REF	34	Bit 13
8	-VCO	33	Bit 5
9	-VSUM	32	Bit 12
10	VEL	31	Bit 4
11	+C	30	Bit 11
12	+S	29	Bit 3
13	-5V	28	Bit 10
14	-R_S	27	Bit 2
15	R_C	26	Bit 9
16	$\overline{EM}$	25	Bit 1 (MSB)
17	A GND	24	CB
18	-5C (-5V)	23	$\overline{BIT}$
19	-CAP	22	+5C (+5 V)
20	GND	21	+CAP

Notes:
1. When -5 V is applied to pin 1 ($\overline{EL}$), Converter Busy (CB) becomes Zero Index (ZI).
2. When using the -5 V inverter: connect pin 2 to 22, pin 13 to 18, and a 10 µF/10 Vdc capacitor from pin 19 (negative terminal) to pin 21 (positive terminal). Connect a 47 µF/10 Vdc capacitor from -5 V to GND. The current drain from the +5 V supply doubles. No external -5 V supply is needed..
3. Signal inputs are single-ended.

TABLE 9. PIN OUT (28 PIN) RDC-19221			
#	NAME	#	NAME
1	B	28	A
2	$\overline{INH}$	27	+5 V
3	+REF	26	$\overline{EL}$
4	-REF	25	Bits 8/16 (LSB)
5	-VCO	24	Bits 7/15
6	-VSUM	23	Bits 6/14
7	VEL	22	Bits 5/13
8	+C	21	Bits 4/12
9	+S	20	Bits 3/11
10	-5V	19	Bits 2/10
11	R_S	18	Bits 1(MSB) /9
12	R_C	17	CB
13	$\overline{EM}$	16	BIT
14	A GND	15	GND

Note:
When -5 V is applied to pin 26 ($\overline{EL}$), Converter Busy(CB) becomes Zero Index (ZI).

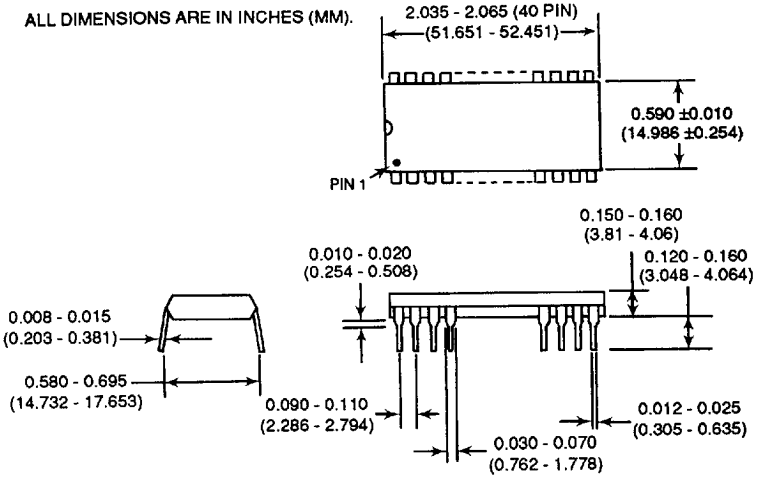


FIGURE 17. RDC-19220/RDC-19223 (40 PIN DDIP) PLASTIC PACKAGE MECHANICAL OUTLINE

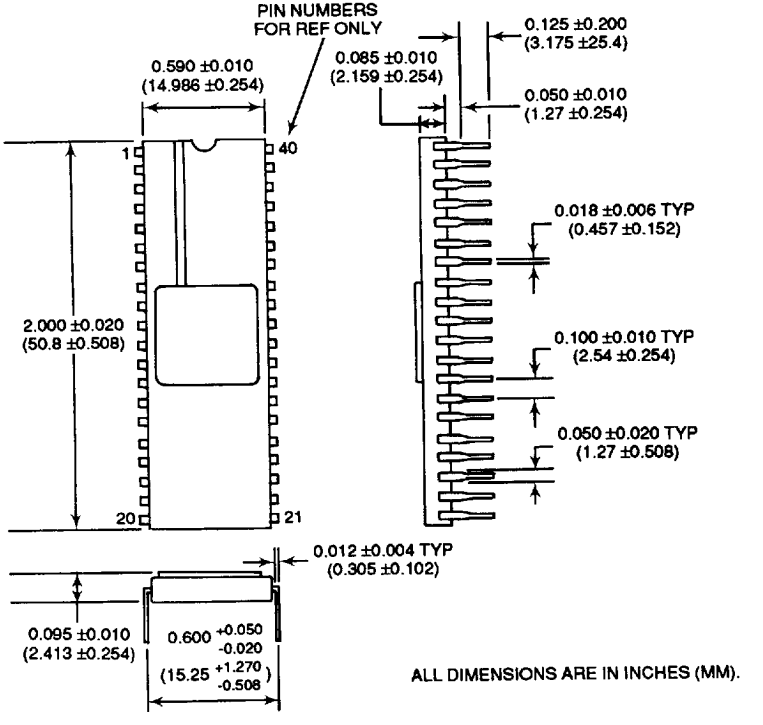


FIGURE 18. RDC-19220/RDC-19223 (40 PIN DDIP) CERAMIC PACKAGE MECHANICAL OUTLINE

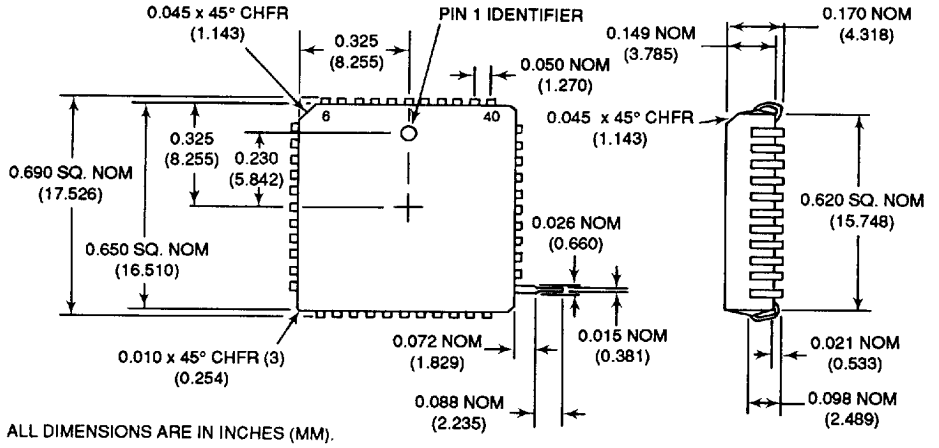


FIGURE 19. RDC-19222 (44 PIN PLASTIC J-LEAD) MECHANICAL OUTLINE

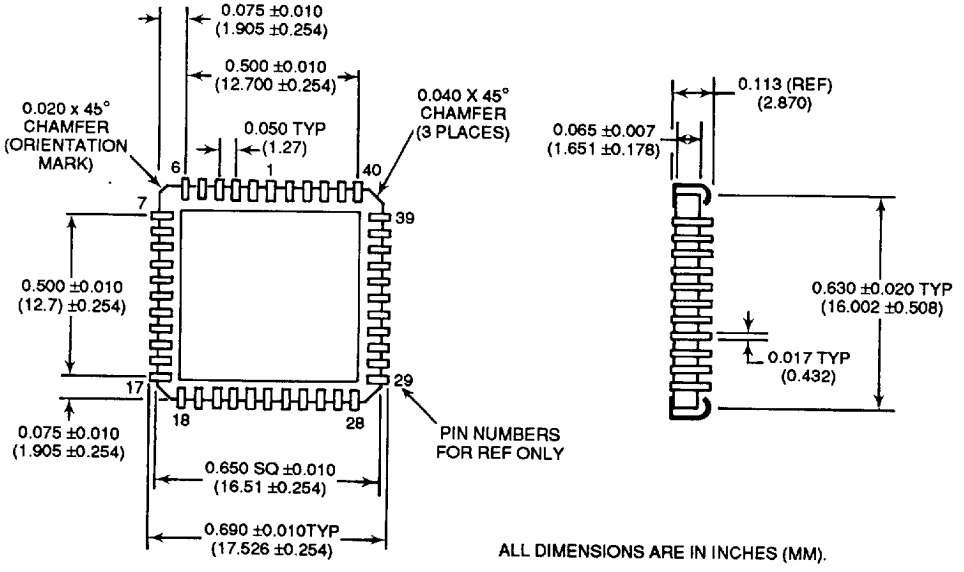


FIGURE 20. RDC-19222 (44 PIN CERAMIC J-LEAD) MECHANICAL OUTLINE

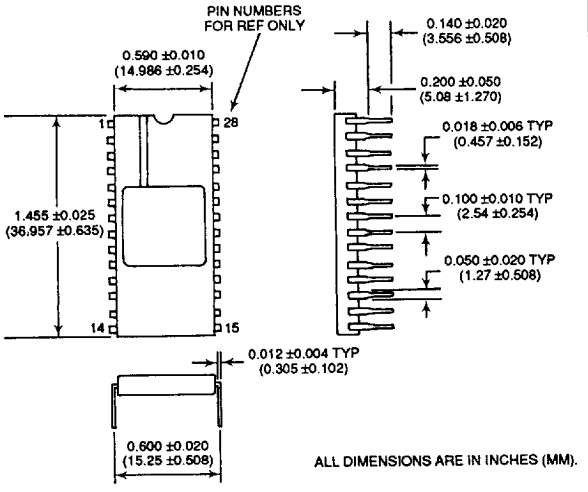


FIGURE 21. RDC-19221 (28 PIN CERAMIC DDIP) MECHANICAL OUTLINE

TABLE 10. FRONT-END THIN-FILM RESISTOR NETWORKS (See FIGURE 23)

SYMBOL	ABS VALUE	TOL (%)	REL TO	REL VALUE	TOL (%)	TCR (PPM)
DDC-49530 RESISTOR VALUES (11.8 V Inputs)						
R1	70.8 k	0.1				25
R2			R1	12 k	0.02	2
R3			R4	12 k	0.02	2
R4			R1	70.8 k	0.02	2
R5			R1	70.8 k	0.02	2
R6			R1	35.4 k	0.02	2
R7			R6	6.9282 k	0.02	2
R8			R6	5.0718 k	0.02	2
R9			R11	5.0718 k	0.02	2
R10			R11	6.9282 k	0.02	2
R11			R1	70.8 k	0.02	2
DDC-49590 RESISTOR VALUES (90 V Inputs)						
R1	270 k	0.1				25
R2			R1	6 k	0.02	2
R3			R4	6 k	0.02	2
R4			R1	270 k	0.02	2
R5			R1	270 k	0.02	2
R6			R1	135 k	0.02	2
R7			R6	3.4641 k	0.02	2
R8			R6	2.5359 k	0.02	2
R9			R11	2.5359 k	0.02	2
R10			R11	3.4641 k	0.02	2
R11			R1	270 k	0.02	2

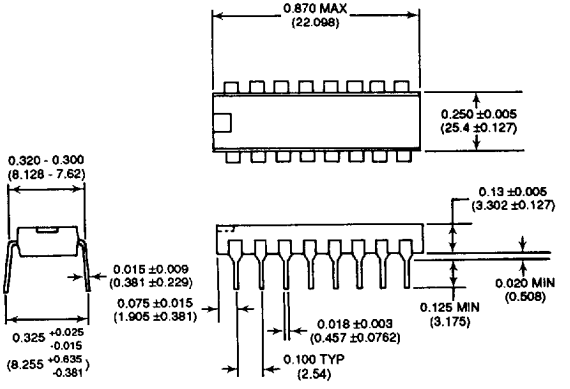


FIGURE 22. 16 PIN DIP THIN-FILM RESISTOR NETWORK MECHANICAL OUTLINE (DDC-49530, DDC-49590)

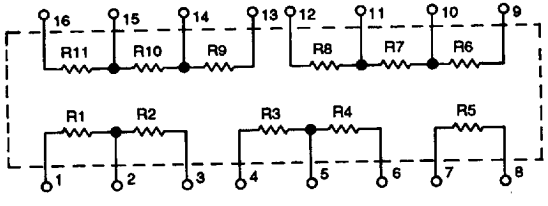


FIGURE 23. DDC-49530 AND DDC-49590 LAYOUT AND RESISTOR VALUES (See TABLE 10.)

ORDERING INFORMATION

RDC- 19220 - 3 0 2

Accuracy:
- 1 = 8 min + 1 LSB (-301 and -201 only)
- 2 = 4 min + 1 LSB
- 3 = 2 min + 1 LSB

Reliability:
- 0 = Standard DDC Procedures
- 1 = Fully Compliant to MIL-STD-883 (Package Type 0 and 2 only)
- 2 = 168 Hour Burn-in at 125°C (-55 to +125°C only)

Operating Temperature Range:
- 1 = -55 to +125°C
- 2 = -40 to +85°C
- 3 = 0 to +70°C

Package:
- 0 = 40 pin DDIP*
- 1 = 28 pin DDIP*
- 2 = 44 pin J-Lead* with +5 Volt only option
- 3 = 40 pin DDIP* with +5 Volt only option

*plastic for -20X and -30X, ceramic for -1XX

Note: DDC reserves the right to supply ceramic packages in place of plastic packages.

THIN-FILM RESISTOR NETWORKS:

DDC-49530 = 11.8 V inputs
DDC-49590 = 90 V inputs

Consult factory for External Component Selection Software

D

4678769 0009723 9T7