PRELIMINARY

P4C1982/P4C1982L
P4C1981/P4C1981L
ULTRA HIGH SPEED 16K x 4 CMOS STATIC RAMS

FEBRUARY 1988

FEATURES

- Full CMOS, 6T Cell
- High Speed (Equal Access and Cycle Times)
  —20/25/30/35/45 ns (Commercial)
  —25/30/35/45/55 ns (Military)
- Low Power Operation (Commercial/Military)
  —550/660 mW Active
  —193/220 mW Standby (TTL Input)
  —83/110 mW Standby (CMOS Input) P4C1981/82
  —1.1/5.5 mW Standby (CMOS Input) P4C1981L/82L
- Output Enable and Dual Chip Enable Functions
- 5V ± 10% Power Supply
- Data Retention with 2.0V Supply, 10 μA Typical Current
- Separate Inputs and Outputs
  —P4C1981/L Input Data at Outputs during Write
  —P4C1982/L Outputs in High Z during Write
- Fully TTL Compatible Inputs and Outputs
- Produced with PACE Technology™
- Standard Pinout (JEDEC Approved)
  —28-Pin 300 mil DIP, SOJ
  —28-Pin 350×550 mil LCC

DESCRIPTION

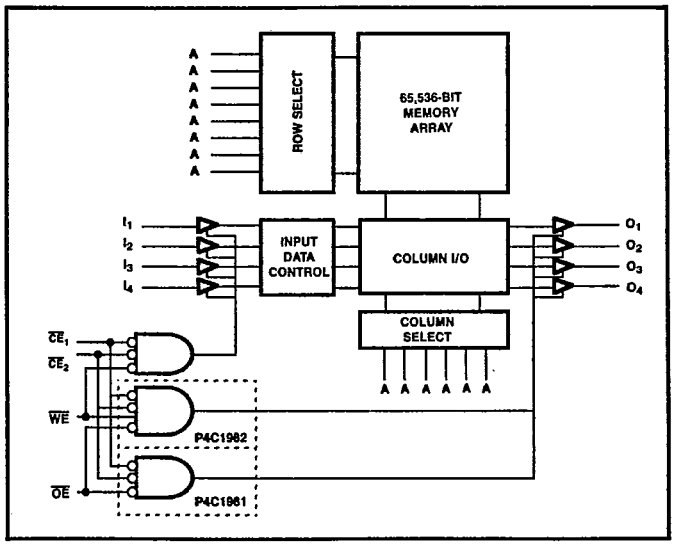
The P4C1982/L and P4C1981/L are 65,536-bit (16K x 4) ultra high speed static RAMs similar to the P4C198, but with separate data I/O pins. The P4C1981/L feature a transparent write operation when $\overline{OE}$ is low; the outputs of the P4C1982/L are in high impedance during the write cycle. All devices have low power standby modes. The RAMs operate from a single 5V ±10% tolerance power supply. With battery backup, data integrity is maintained for supply voltages down to 2.0V. Current drain is typically 10 μA from a 2.0V supply.

Access times as fast as 20 nanoseconds are available, permitting greatly enhanced system operating speeds.

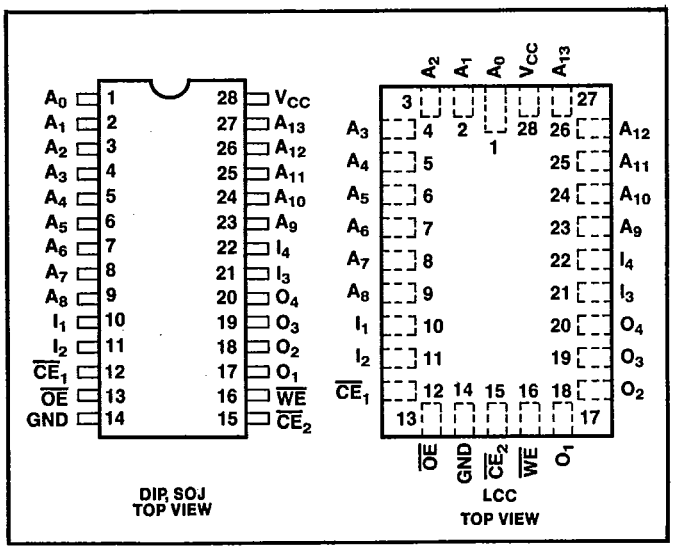
CMOS is utilized to reduce power consumption to a low 550 mW active, 193 mW standby. For the P4C1982L and P4C1981L, power is only 1.1 mW standby with CMOS input levels. The P4C1982/L and P4C1981/L are members of a family of PACE RAM™ products offering super fast access times never before available at these complexity levels in TTL-compatible bipolar or CMOS technologies. The P4C1982/L and P4C1981/L are manufactured with PACE Technology™.

The P4C1982/L and P4C1981/L are available in 28-pin 300 mil DIP and SOJ, and in 28-pin 350×550 mil LCC packages providing excellent board level densities.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	−0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	−0.5 to V_{CC}+0.5	V
T_A	Operating Temperature	−55 to +125	°C

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	−55 to +125	°C
T_{STG}	Storage Temperature	−65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade[2]	Ambient Temperature	GND	V_{CC}
Military	−55 to +125°C	0V	5.0V ±10%

Grade[2]	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ±10%

DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

Symbol	Parameter	Test Conditions		P4C1981 P4C1982		P4C1981L P4C1982L		Unit
				Min.	Max.	Min.	Max.	
V_{IH}	Input High Voltage			2.2	V_{CC}+0.5	2.2	V_{CC}+0.5	V
V_{IL}	Input Low Voltage			−0.5[3]	0.8	−0.5[3]	0.8	V
V_{HC}	CMOS Input High Voltage			V_{CC}−0.2	V_{CC}+0.5	V_{CC}−0.2	V_{CC}+0.5	V
V_{LC}	CMOS Input Low Voltage			−0.5[3]	0.2	−0.5[3]	0.2	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Min., I_{IN} = −18 mA		—	−1.2	—	−1.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +10 mA, V_{CC} = Min. I_{OL} = +8 mA, V_{CC} = Min.		— —	0.5 0.4	— —	0.5 0.4	V
V_{OLC}	Output Low Voltage (CMOS Load)	I_{OLC} = +100 µA, V_{CC} = Min.			0.2		0.2	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = −4 mA, V_{CC} = Min.		2.4	—	2.4	—	V
V_{OHC}	Output High Voltage (CMOS Load)	I_{OHC} = −100 µA, V_{CC} = Min.		V_{CC}−0.2	—	V_{CC}−0.2	—	V
I_{LI}	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	Mil. Com'l.	−10 −5	+10 +5	−5 −2	+5 +2	µA
I_{LO}	Output Leakage Current	V_{CC} = Max., $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	Mil. Com'l.	−10 −5	+10 +5	−5 −2	+5 +2	µA
I_{CC}	Dynamic Operating Current	V_{CC} = Max., f = Max., Outputs Open	Mil. Com'l.	— —	120 100	— —	120 100	mA
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE}$ ≥ V_{IH}, V_{CC} = Max., f = Max., Outputs Open	Mil. Com'l.	— —	40 35	— —	40 35	mA
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE}$ ≥ V_{HC}, V_{CC} = Max., f = 0, Outputs Open, V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}	Mil. Com'l.	— —	20 15	— —	1.0 0.2	mA

Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than −3.0V and −100mA, respectively, are permissible for pulse widths up to 20 ns.

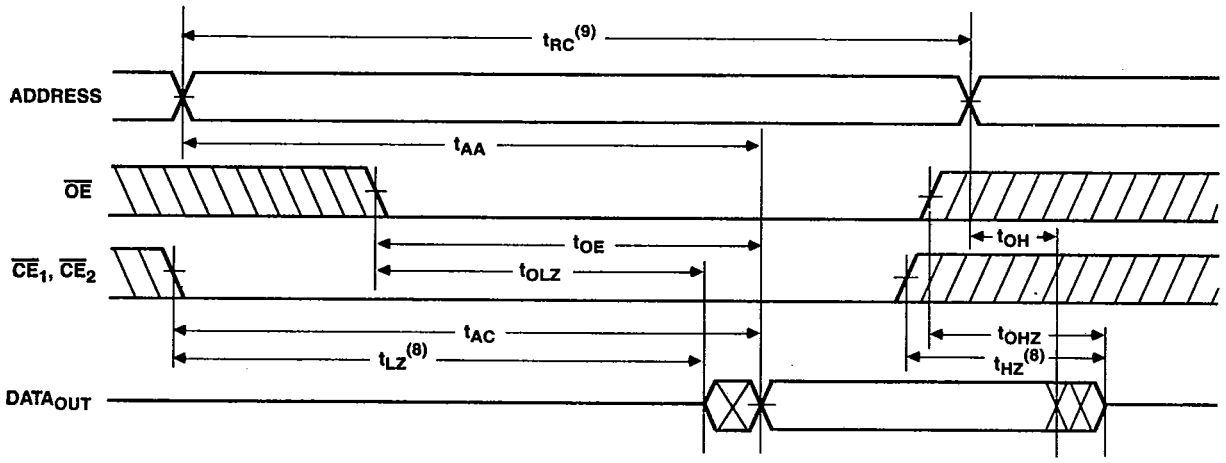
AC ELECTRICAL CHARACTERISTICS—READ CYCLE

(V_{CC} = 5V ±10%, All Temperature Ranges)[2]

Symbol	Parameter	-20*		-25		-30		-35		-45		-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	20		25		30		35		45		55		ns
t_{AA}	Address Access Time		20		25		30		35		45		55	ns
t_{AC}	Chip Enable Access Time		20		25		30		35		45		55	ns
t_{OH}	Output Hold from Address Change	3		3		3		3		3		3		ns
t_{LZ}	Chip Enable to Output in Low Z	2		2		3		3		3		3		ns
t_{HZ}	Chip Disable to Output in High Z		10		10		13		15		15		20	ns
t_{OE}	Output Enable Low to Data Valid		12		15		18		21		27		35	ns
t_{OLZ}	Output Enable Low to Output in Low Z	2		2		3		3		3		3		ns
t_{OHZ}	Output Enable High to Output in High Z		8		10		12		14		15		20	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		20		25		25		25		30		30	ns

* V_{CC} = 5V ± 5% for -20

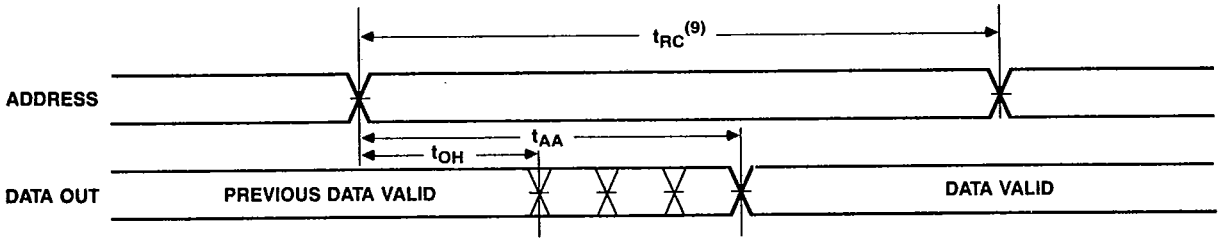
READ CYCLE NO. 1 ($\overline{OE}$ controlled)[4]



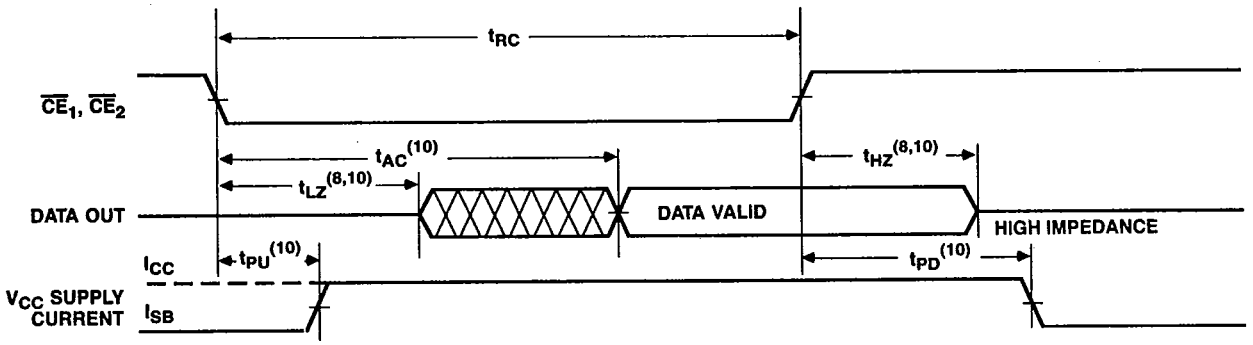
Notes:

4. $\overline{WE}$ is high for READ cycle.
5. $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{OE}$ are low READ cycle.
6. $\overline{OE}$ is low for the cycle.
7. ADDRESS must be valid prior to, or coincident with, $\overline{CE_1}$ and $\overline{CE_2}$ transition low.
8. Transition is measured ±200mV from steady state voltage prior to change, with loading as specified in Figure 1.
9. Read Cycle Time is measured from the last valid address to the first transitioning address.

READ CYCLE NO. 2 (ADDRESS controlled)[4,5]



READ CYCLE NO. 3 ($\overline{CE}_1$, $\overline{CE}_2$ controlled)[4,6,7]



Note:

10. Transitions caused by a chip enable control have similar delays irrespective of whether $\overline{CE}_1$ or $\overline{CE}_2$ causes them.

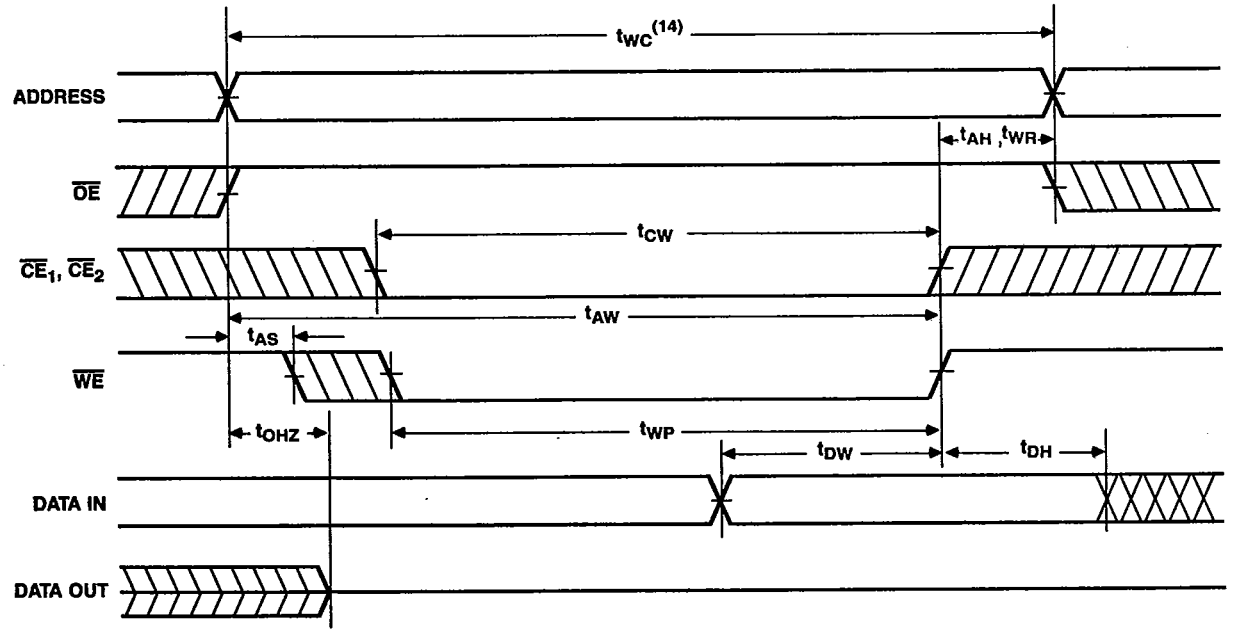
AC ELECTRICAL CHARACTERISTICS—WRITE CYCLE

(V_{CC} = 5V ±10%, All Temperature Ranges)[2]

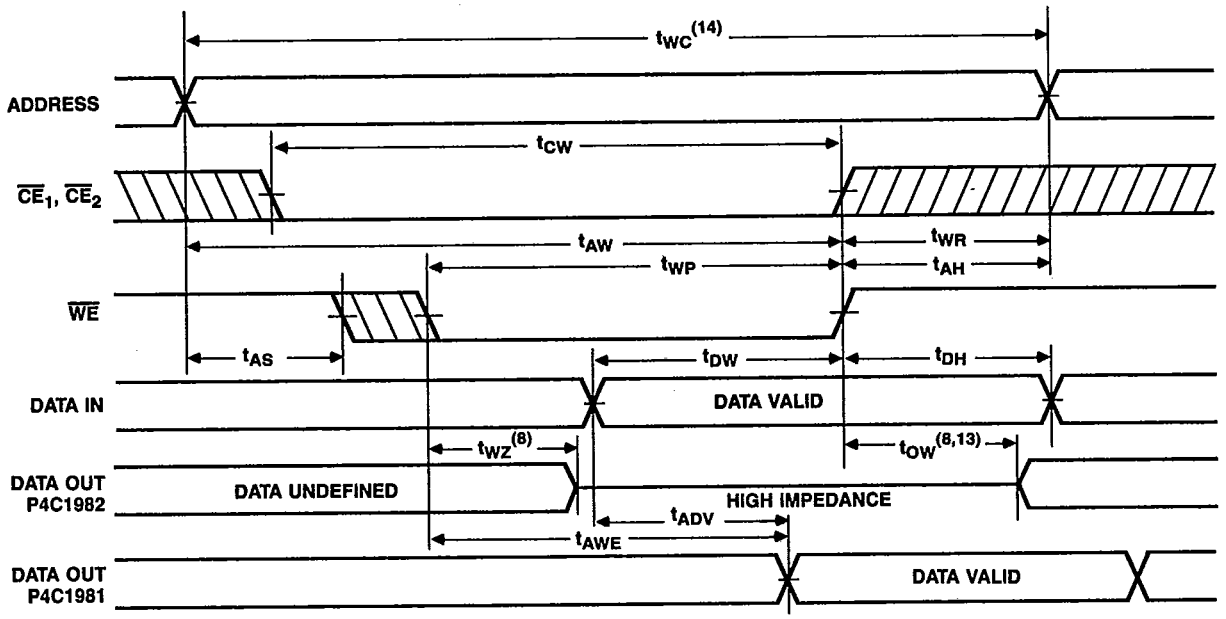
Symbol	Parameter	-20*		-25		-30		-35		-45		-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	15		20		25		30		40		50		ns
t_{CW}	Chip Enable Time to End of Write	15		20		25		30		35		40		ns
t_{AW}	Address Valid to End of Write	15		20		25		25		35		40		ns
t_{AS}	Address Set-up Time	0		0		0		0		0		0		ns
t_{WP}	Write Pulse Width	15		20		25		25		35		40		ns
t_{WR}	Write Recovery Time	0		0		0		0		0		0		ns
t_{AH}	Address Hold Time	0		0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	10		13		15		15		20		25		ns
t_{DH}	Data Hold Time	0		0		0		0		3		5		ns
t_{WZ}	Write Enable to Output in High Z (P4C1982)		8		10		10		10		15		20	ns
t_{OW}	Output Active from End of Write (P4C1982)	2		2		3		3		3		3		ns
t_{AWE}	Write Enable to Data-out Valid (P4C1981)		18		20		25		30		35		40	ns
t_{ADV}	Data-in Valid to Data-out Valid (P4C1981)		18		20		25		30		35		40	ns

* V_{CC} = 5V ± 5% for -20

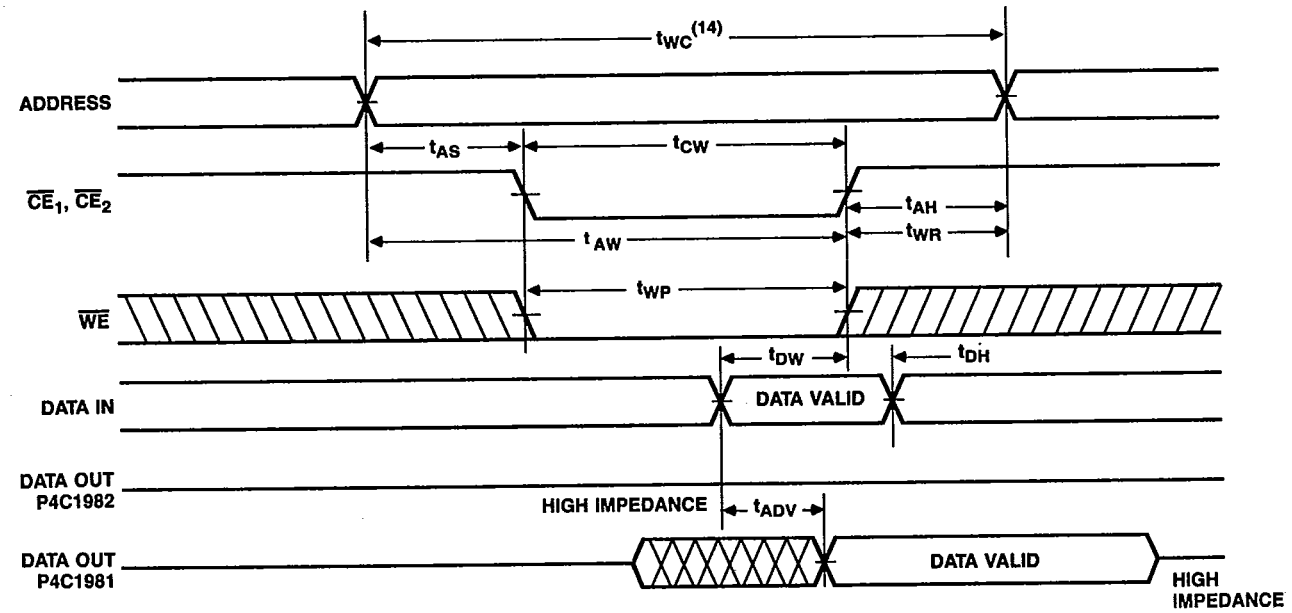
WRITE CYCLE NO. 1 (With $\overline{OE}$ high)



WRITE CYCLE NO. 2 ($\overline{WE}$ controlled)[11,12]



WRITE CYCLE NO. 3 ($\overline{CE}_1$, $\overline{CE}_2$ controlled)[11,12]



Notes:

11. $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{WE}$ must be low for WRITE cycle.
12. $\overline{OE}$ is low for this WRITE cycle.
13. If $\overline{CE}_1$ or $\overline{CE}_2$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
14. Write Cycle Time is measured from the last valid address to the first transitioning address.

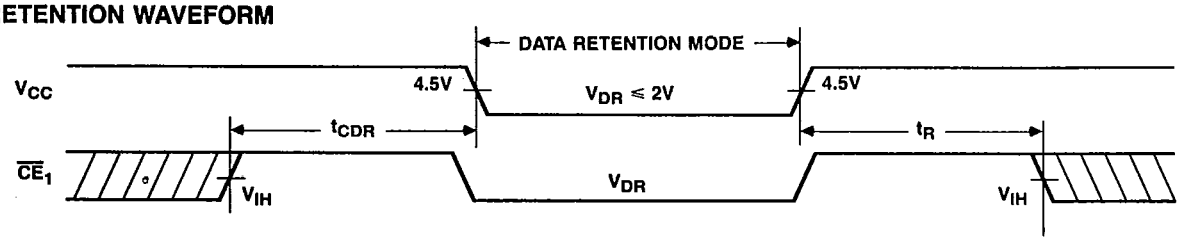
DATA RETENTION CHARACTERISTICS (P4C1981L and P4C1982L only)

(All Temperature Ranges)

Symbol	Parameter	Test Condition	Min.	Typ.* V_{CC} = 2.0V	Typ.* V_{CC} = 3.0V	Max. V_{CC} = 2.0V	Max. V_{CC} = 3.0V	Unit
V_{DR}	V_{CC} for Data Retention		2.0					V
I_{CCDR}	Data Retention Current	Mil.		10	15	600	900	µA
		Com'l.		10	15	150	225	
t_{CDR}	Chip Deselect to Data Retention Time	$\overline{CE} \geq V_{CC}-0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	0					ns
t_R†	Operation Recovery Time		t_{RC}‡					ns

* T_A = +25°C.
‡ t_{RC} = Read Cycle Time.
† This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

TRUTH TABLE P4C1981/L (P4C1982/L)

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	Mode	Output
H	X	X	X	Standby	High Z
X	H	X	X	Standby	High Z
L	L	H	H	Output Inhibit	High Z
L	L	H	L	READ	D_{OUT}
L	L	L	H	WRITE	High Z
L	L	L	L	WRITE	D_{IN} (High Z)

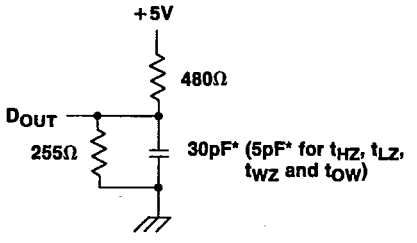


Figure 1. Output Load

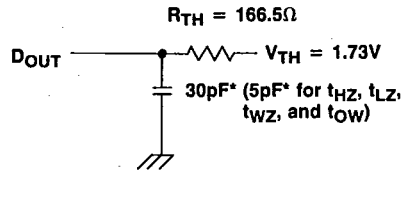


Figure 2. Thevenin Equivalent

Note:
Due to the ultra-high speed of the P4C1981/L and P4C1982/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

CAPACITANCES[15]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF

Symbol	Parameter	Conditions	Typ.	Unit
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

Note:
15. This parameter is sampled and not 100% tested.

SELECTION GUIDE

The P4C1981/L and P4C1982/L are available in the following temperature range, speed and package options.

Temperature Range	Package \ Speed (ns)	20	25	30	35	45	55
Commercial	Plastic DIP	-20PC	-25PC	-30PC	-35PC	-N/A	N/A
	Plastic SOJ	-20JC	-25JC	-30JC	-35JC	N/A	N/A
	Sidebrazed DIP	-20CC	-25CC	-30CC	-35CC	-45CC	N/A
	LCC	-20DL	-25LC	-30LC	-35LC	-45LC	N/A
Military Temp.	Sidebrazed DIP	N/A	-25CM	-30CM	-35CM	-45CM	-55CM
	LCC	N/A	-25LM	-30LM	-35LM	-45LM	-55LM
Military Processed*	Sidebrazed DIP	N/A	-25CMB	-30CMB	-35CMB	-45CMB	-55CMB
	LCC	N/A	-25LMB	-30LMB	-35LMB	-45LMB	-55LMB

* Military temperature range with MIL-STD-883 Revision C, Class B processing.
N/A = Not Available

To order these parts, refer to the section on Ordering Information.