Lattice Semiconductor Corporation

Product Brief
January 15, 2002

ORCA® Series 4 Field-Programmable Gate Arrays

Introduction

Built on the Series 4 reconfigurable embedded system-on-chip (SoC) architecture, Lattice introduces its new family of generic field-programmable gate arrays (FPGA). The high-performance and highly versatile architecture brings a new dimension to bringing network system designs to market in less time than ever before. This new device family offers many new features and architectural enhancements not available in any earlier FPGA generations. Bringing together highly flexible SRAM-based programmable logic, powerful system features, a rich hierarchy of routing and interconnect resources, and meeting multiple interface standards, the Series 4 FPGA accommodates the most complex and high-performance intellectual property (IP) network designs.

Programmable Features

- High-performance platform design:
  - — 0.16 µm 7-level metal technology.
  - — Internal performance of >250 MHz.
  - — I/O performance of >420 MHz.
  - — Meets multiple I/O interface standards.
  - — 1.5 V operation (30% less power than 1.8 V operation) translates to greater performance.
- Traditional I/O selections:
  - — LVTTL and LVCMOS (3.3 V, 2.5 V, and 1.8 V) I/Os.
  - — Per pin-selectable I/O clamping diodes provide 3.3 V PCI compliance.
  - — Individually programmable drive capability: 24 mA sink/12 mA source, 12 mA sink/6 mA source, or 6 mA sink/3 mA source.
  - — Two slew rates supported (fast and slew-limited).
  - — Fast-capture input latch and input flip-flop (FF)/latch for reduced input setup time and zero hold time.
  - — Fast open-drain drive capability.
  - — Capability to register 3-state enable signal.
  - — Off-chip clock drive capability.
  - — Two-input function generator in output path.
- New programmable high-speed I/O:
  - — Single-ended: GTL, GTL+, PECL, SSTL3/2 (class I and II), HSTL (Class I, III, and IV), ZBT, and DDR.
  - — Double-ended: LDVS, bused-LVDS, and LVPECL. Programmable (on/off) internal parallel termination (100 Ω) also supported for these I/Os.

Table 1. *ORCA* Series 4—Available FPGA Logic

Device	Rows	Columns	PFUs	User I/O	LUTs	EBR Blocks	EBR Bits (K)	Usable* Gates (K)
OR4E2	26	24	624	400	4,992	8	74	260—515
OR4E4	36	36	1296	576	10,368	12	111	380—800
OR4E6	46	44	2024	720	16,192	16	147	515—1095

* The usable gate counts range from a logic-only gate count to a gate count assuming 20% of the PFUs/SLICs being used as RAMs. The logic-only gate count includes each PFU/SLIC (counted as 108 gates/PFU), including 12 gates per LUT/FF pair (eight per PFU) and 12 gates per SLIC/FF pair (one per PFU). Each of the four PIO groups are counted as 16 gates (three FFs, fast-capture latch, output logic, CLK, and I/O buffers). PFUs used as RAM are counted at four gates per bit, with each PFU capable of implementing a 32 x 4 RAM (or 512 gates) per PFU. Embedded block RAM (EBR) is counted as four gates per bit, plus each block has an additional 25 K gates. 7 K gates are used for each PLL and 50K gates for the embedded system bus and microprocessor interface logic. Both the EBR and PLLs are conservatively utilized in the gate count calculations.

Note: Devices are not pinout compatible with *ORCA* Series 2/3.

Programmable Features (continued)

- New capability to (de)multiplex I/O signals:
  - — New double data rate on both input and output at rates up to 350 MHz (700 MHz effective rate).
  - — New 2x and 4x downlink and uplink capability per I/O (i.e., 50 MHz internal to 200 MHz I/O).
- Enhanced twin-quad programmable function unit (PFU):
  - — Eight 16-bit look-up tables (LUTs) per PFU.
  - — Nine user registers per PFU, one following each LUT and organized to allow two nibbles to act independently, plus one extra for arithmetic operations.
  - — New register control in each PFU has two independent programmable clocks, clock enables, local set/reset, and data selects.
  - — New LUT structure allows flexible combinations of LUT4, LUT5, new LUT6, 4 to 1 MUX, new 8 to 1 MUX, and ripple mode arithmetic functions in the same PFU.
  - — 32 x 4 RAM per PFU, configurable as single- or dual-port. Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using the SLIC decoders as bank drivers.
  - — Soft-wired LUTs (SWL) allow fast cascading of up to three levels of LUT logic in a single PFU through fast internal routing, which reduces routing congestion and improves speed.
  - — Flexible fast access to PFU inputs from routing.
  - — Fast-carry logic and routing to all four adjacent PFUs for nibble-, byte-wide, or longer arithmetic functions, with the option to register the PFU carry-out.
- Abundant high-speed buffered and nonbuffered routing resources provide 2x average speed improvements over previous architectures.
- Hierarchical routing optimized for both local and global routing with dedicated routing resources. This results in faster routing times with predictable and efficient performance.
- SLIC provides eight 3-statable buffers, up to 10-bit decoder, and *PAL*™-like and-or-invert (AOI) in each programmable logic cell.
- Improved built-in clock management with programmable phase-locked loops (PPLLs) provide optimum clock modification and conditioning for phase, frequency, and duty cycle from 20 MHz up to 420 MHz. Multiplication of the input frequency up to 64x, and division of the input frequency down to 1/64x, is possible.
- New 200 MHz embedded quad-port RAM blocks, two read ports, two write ports, and two sets of byte lane enables. Each embedded RAM block can be configured as:
  - — 1-512 x 18 (quad-port, two read/two write) with optional built in arbitration.
  - — 1-256 x 36 (dual-port, one read/one write).
  - — 1-1K x 9 (dual-port, one read/one write).
  - — 2-512 x 9 (dual-port, one read/one write for each).
  - — 2 RAMS with arbitrary number of words whose sum is 512 or less by 18 (dual-port, one read/one write).
  - — Supports joining of RAM blocks.
  - — Two 16 x 8-bit content addressable memory (CAM) support.
  - — FIFO 512 x 18, 256 x 36, 1K x 9 or dual 512 x 9.
  - — Constant multiply (8 x 16 or 16 x 8).
  - — Dual-variable multiply (8 x 8).
- Embedded 32-bit internal system bus plus 4-bit parity interconnects FPGA logic, microprocessor interface (MPI), embedded RAM blocks, and embedded standard cell blocks with 100 MHz bus performance. Included are built-in system registers that act as the control and status center for the device.
- Built-in testability:
  - — Full boundary scan (*IEEE* ® 1149.1 and Draft 1149.2 joint test access group (JTAG)).
  - — Programming and readback through boundary scan port compliant to *IEEE* Draft 1532:D1.7.
  - — TS_ALL testability function to 3-state all I/O pins.
  - — New temperature-sensing diode.
- New cycle stealing capability allows a typical 15% to 40% internal speed improvement after final place and route. This feature also enables compliance with many setup/hold and clock-to-out I/O specifications, and may provide reduced ground bounce for output buses by allowing flexible delays of switching output buffers.

System Features

- PCI local bus compliant.
- Improved *PowerPC*® /PowerQUICC MPC860 and *PowerPC* II MPC8260 high-speed synchronous microprocessor interface can be used for configuration, readback, device control, and device status, as well as for a general-purpose interface to the FPGA logic, RAMs, and embedded standard cell blocks. Glueless interface to synchronous *PowerPC* processors with user-configurable address space is provided.
- New embedded *AMBA*™ specification 2.0 AHB system bus (*ARM* ™ processor) facilitates communication among the microprocessor interface, configuration logic, embedded block RAM, FPGA logic, and embedded standard cell blocks.
- New network PLLs meet ITU-T G.811 specifications and provide clock conditioning for DS-1/E-1 and STS-3/STM-1 applications.
- Variable size bused readback of configuration data capability with the built-in microprocessor interface and system bus.
- Internal, 3-state, bidirectional buses with simple control provided by the SLIC.
- New clock routing structures for global and local clocking significantly increases speed and reduces skew (<200 ps for OR4E4).
- New local clock routing structures allow creation of localized clock trees.
- Two new edge clock routing structures allow up to six high-speed clocks on each edge of the device for improved setup/hold and clock-to-out performance.
- New double-data rate (DDR) and zero-bus turnaround (ZBT) memory interfaces support the latest high-speed memory interfaces.
- New 2x/4x uplink and downlink I/O capabilities interface high-speed external I/Os to reduced speed internal logic.
- Meets universal test and operations PHY interface for ATM (UTOPIA) Levels 1, 2, and 3. Also meets proposed specifications for UTOPIA level 4, POS-PHY Level 3 (2.5 Gbits/s), and POS-PHY 4 (10 Gbits/s) interface standards for packet-over-SONET as defined by the Saturn Group.
- *ORCA* Foundry development system software s upported by industry-standard CAE tools for design entry, synthesis, simulation, and timing analysis.

System Features (continued)

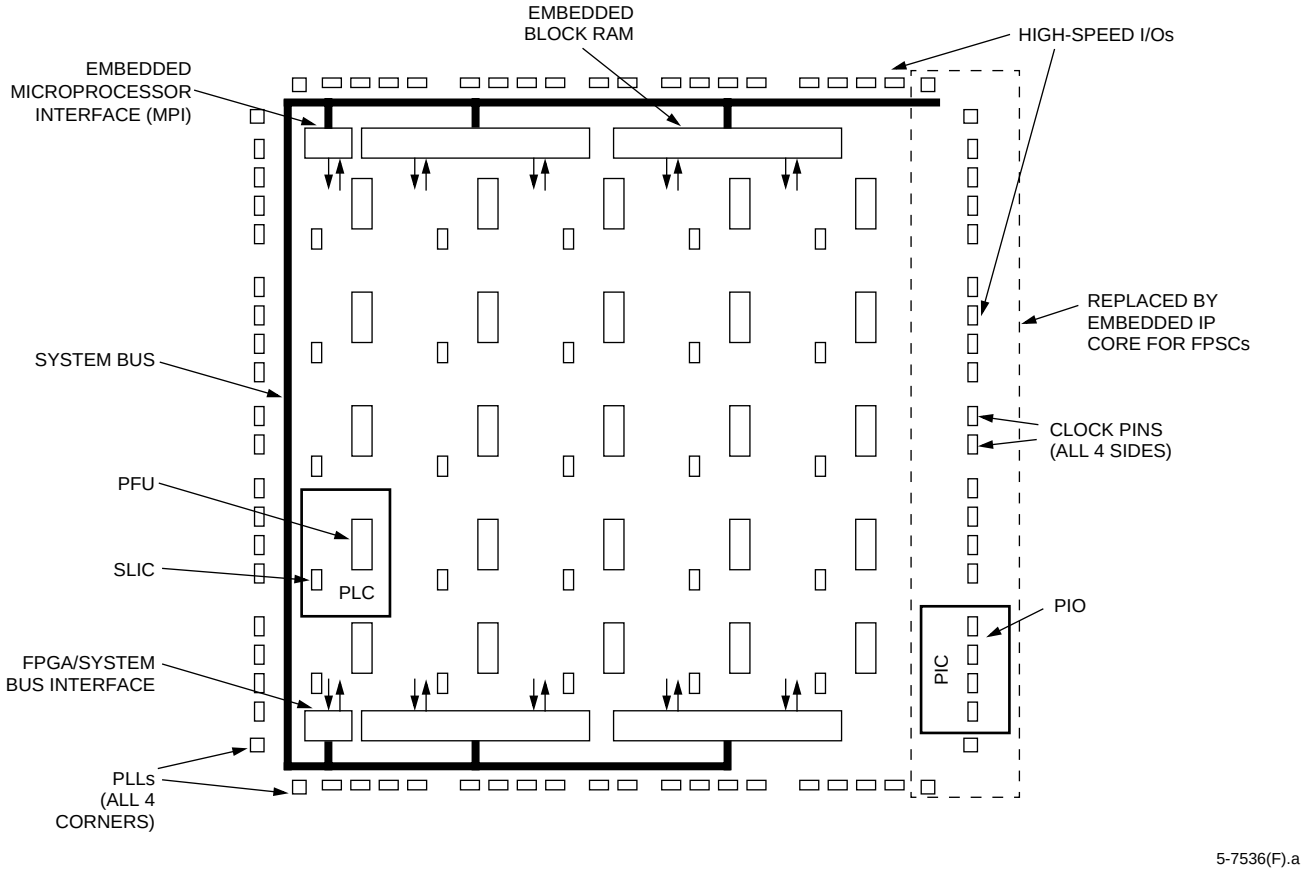
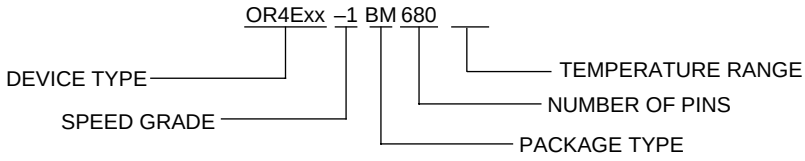


Figure 1. Series 4 FPGA Block Diagram

Ordering Information



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OR4Exx, –1 Speed Grade, 680-pin Plastic Ball Grid Array Multilayer (PBGAM)

Table 2. Device Type Options

Device	Voltage
OR4Exx	1.5 V internal 3.3 V/2.5 V/1.8 V/1.5 V I/O

Table 3. Temperature Options

Symbol	Description	Ambient Temperature
(Blank)	Industrial	–40 ˚C to +85 ˚C

Note: Device junction temperature of –40 ˚C to +125 ˚C are recommended.

Table 4. Package Options

Symbol	Description
BA	Plastic Ball Grid Array (PBGA)
BC	Enhanced Ball Grid Array (EBGA)
BM	Plastic Ball Grid Array, Multilayer (PBGAM)

Table 5. *ORCA* OR4EXX Series Package Matrix (Speed Grade)

Devices	256-Pin FSBGA(BA)	352-Pin PBGA(BA)	416-Pin PBGAM(BA)	432-Pin EBGA(BC)	680-Pin PBGAM(BM)
OR4E2	–1, –2, –3	–1, –2, –3	–1, –2, –3	–1, –2, –3	–1, –2, –3
OR4E4	—	–1, –2, –3	–1, –2, –3	–1, –2, –3	–1, –2, –3
OR4E6	—	–1, –2, –3	—	–1, –2, –3	–1, –2, –3

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