LT1182/LT1183

CCFL/LCD Contrast Dual Switching Regulator

June 1994

FEATURES

- Wide Input Voltage Range: 3V to 30V
- Low Quiescent Current: 4.5mA per Regulator
- High Switching Frequency: 200kHz
- CCFL Switch: 1.25A /LCD Switch: 625mA
- Grounded or Floating Bulb Configurations
- Open Bulb Protection
- Positive or Negative Contrast Capability

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Automotive Displays
- Retail Terminals

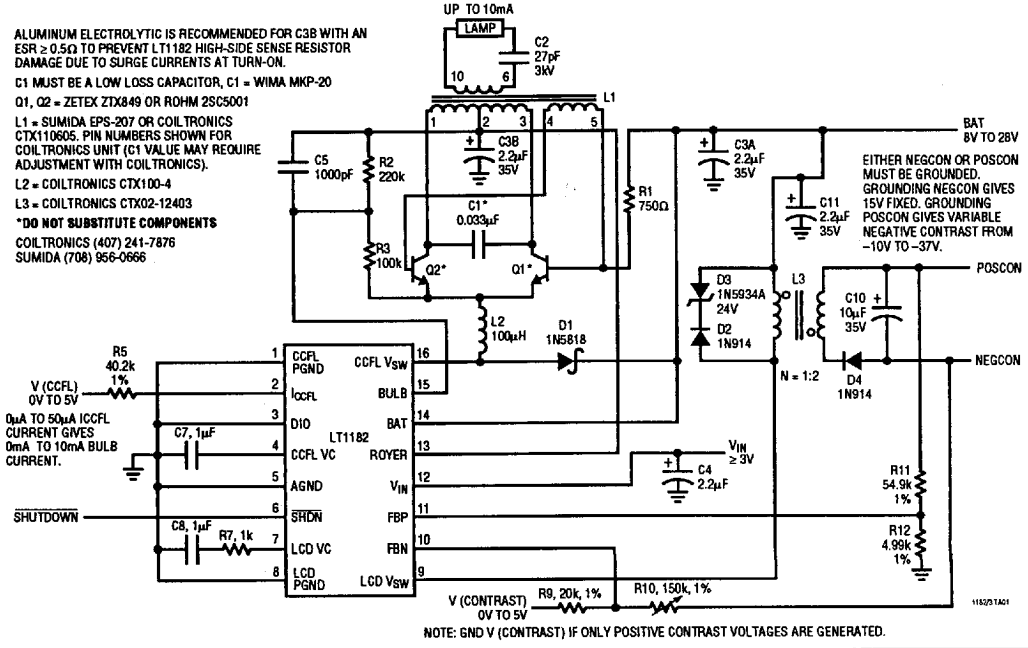
DESCRIPTION

The LT1182/LT1183 are dual current-mode switching regulators that provide the control function for Cold Cathode Fluorescent Lighting and Liquid Crystal Display Contrast. Two high current, high efficiency switches are included on the die along with an oscillator, reference, output drive logic, control blocks and protection circuitry. The LT1183 brings out the internal reference and ties the inputs of the LCD contrast error amplifier together in comparison to the LT1182. The LT1182/LT1183 are available in 16-pin narrow body SOIC and 16-pin plastic DIP.

The LT1182/LT1183 operate with supply voltages from 3V to 30V and draw only 9mA quiescent current. A shutdown pin reduces total supply current to less than 50µA for

TYPICAL APPLICATION

90% Efficient Floating CCFL Configuration with Dual Polarity LCD Contrast



NOTE: GND V (CONTRAST) IF ONLY POSITIVE CONTRAST VOLTAGES ARE GENERATED.

DESCRIPTION

standby operation. A 200kHz switching frequency minimizes the size of required magnetic components. The use of current-mode switching techniques with cycle by cycle limiting gives high reliability and simple loop frequency compensation.

The CCFL regulator typically drives an inductor that acts as a switched-mode current source for a current-driven Royer class converter with efficiencies as high as 90%. The control loop forces the CCFL PWM to modulate the inductor's average current to maintain constant current in the lamp. The constant current value, and thus lamp intensity, is programmable. This drive technique provides a wide range of intensity control. A unique bulb current programming block allows either grounded or floating bulb configurations. Grounded circuits directly sense one-half of actual bulb current. Floating circuits directly sense Royer primary-side supply current. Floating circuits provide differential drive to the bulb and significantly reduce the loss from stray bulb to frame capacitance, thereby extending illumination range.

The LCD Contrast regulator is typically configured as a flyback converter and generates a bias supply for contrast control. The supply's variable output permits adjustment of display contrast. A unique error amplifier and the choice of flyback allows either positive or negative LCD Contrast voltages to be generated with minor circuit changes.

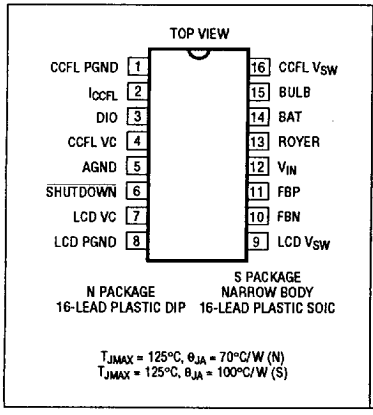
The LT1184 will be available in the near future which provides only the CCFL function. Consult factory for further details.

ABSOLUTE MAXIMUM RATINGS

V_{IN}, BAT, Royer, Bulb 30V
CCFL V_{SW}, LCD V_{SW} 55V
Shutdown 6V
I_{CCFL} Input Current 10mA
DIO Input Current 100mA
FBN Pin Current ..... ±2mA

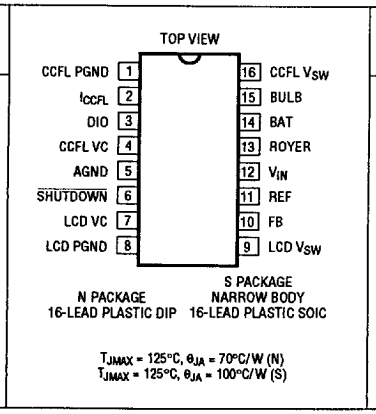
Operating Ambient Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature (Note 1) ..... 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LT1182CN
LT1182CS



ORDER PART NUMBER

LT1183CN
LT1183CS

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 5V, BAT = Royer = Bulb = 12V, CCFL VC = LCD VC = 0.5V, CCFL V_{SW} = LCD V_{SW} = ICCFL = $\overline{\text{Shutdown}}$ = Open, DIO = FBN = FBP = GND, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Supply Current	3V ≤ V_{IN} ≤ 30V	●		9	14	mA
$I_{\overline{SHDN}}$	$\overline{\text{Shutdown}}$ Supply Current	$\overline{\text{Shutdown}}$ = 0V, CCFL VC = LCD VC = Open (Note 2)			40	60	µA
	$\overline{\text{Shutdown}}$ Input Bias Current	$\overline{\text{Shutdown}}$ = 0V, CCFL VC = LCD VC = Open			3		µA
	$\overline{\text{Shutdown}}$ Threshold Voltage		●	0.7	0.85	1.0	V
f	Switching Frequency	Measured at CCFL V_{SW}, I_{SW} = 50mA, FBN = FBP = 1V CCFL VC = LCD VC = Open, ICCFL = 100µA	 ●		200 200		kHz kHz
DC(MAX)	Maximum Switch Duty Cycle	Measured at CCFL V_{SW} and LCD V_{SW}			85		%
	Input Operating Voltage		●	3.0		30	V
BV	Switch Breakdown Voltage	I_{SW} = 2mA, Measured at CCFL V_{SW} and LCD V_{SW}	●	55	70		V
	CCFL Switch Leakage Current	V_{SW} = 12V V_{SW} = 30V				2.0 5.0	µA µA
	LCD Switch Leakage Current	V_{SW} = 12V V_{SW} = 30V				2.0 5.0	µA µA
	I_{CCFL} Summing Voltage	3V ≤ V_{IN} ≤ 30V	 ●		0.45 0.45		V V
	ΔI_{CCFL} Summing Voltage for ΔInput Programming Current	I_{CCFL} = 0µA to 100µA			3		mV
	CCFL VC Offset Sink Current		●		0		µA
	ΔCCFL VC Source Current for ΔI_{CCFL} Programming Current	I_{CCFL} = 0µA to 100µA	●		5		µA/µA
	CCFL VC to DIO Current Servo Ratio	DIO = 5mA Out of Pin, Current Measured at CCFL VC		97	100	103	µA/mA
	CCFL VC Low Clamp Voltage	Royer = 1A			0.1		V
	CCFL VC High Clamp Voltage	I_{CCFL} = 100µA			2.0		V
	CCFL VC Switching Threshold	CCFL V_{SW} DC = 0%			0.95		V
	CCFL High-Side Sense Current Transfer Ratio	Royer = 1A, Current Measured at CCFL VC CCFL VC = 1.5V		480	500	520	µA/A
	CCFL High-Side Sense Line Regulation	Royer = 1A, BAT = 5V to 30V CCFL VC = 1.5V			0.1		%/V
	CCFL High-Side Sense Supply Current	Measured at BAT, Royer	●		120		µA
	Bulb Protect Servo Voltage	I_{CCFL} = 100µA, CCFL VC = 0µA at 1.5V	●	6.65	7.0	7.35	V
	Bulb Input Bias Current	I_{CCFL} = 100µA, CCFL VC = 0µA at 1.5V			5		µA
I_{LIM1}	CCFL Switch Current Limit	Duty Cycle = 50% Duty Cycle = 80% (Note 3)	● ●	1.25 1.05	2.0 1.7	3.0 2.6	A A
V_{SAT1}	CCFL Switch On Resistance	CCFL I_{SW} = 1A	●		0.6	1.0	Ω
$\frac{\Delta I_Q}{\Delta I_{SW1}}$	Supply Current Increase During CCFL Switch On Time	CCFL I_{SW} = 1A			25		mA/A
	Switch Minimum On Time	Measured at CCFL V_{SW} and LCD V_{SW}			0.45		µs
REF1	LCD FBP Reference Voltage	Measured at FBP of LCD Error Amplifier, FBN = 1V, LCD VC = 0.8V	 ●	1.224	1.244 1.244	1.264	V V
	FBP Voltage Line Regulation	3V ≤ V_{IN} ≤ 30V, LCD VC = 0.8V	●		0.01		%/V
	FBP Input Bias Current	FBP = REF1, FBN = 1V, LCD VC = 0.8V	 ●		0.35 0.35	0.75 1.1	µA µA
	LCD FBN Offset Voltage	Measured at FBN of LCD Error Amplifier, FBP = GND, LCD VC = 0.8V	 ●	−15	−10 −10	−5	mV mV
	FBN Voltage Line Regulation	3V ≤ V_{IN} ≤ 30V	●		0.01		%/V

13

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 5V, BAT = Royer = Bulb = 12V, CCFL VC = LCD VC = 0.5V, CCFL V_{SW} = LCD V_{SW} = ICCFL = $\overline{\text{Shutdown}}$ = Open, DIO = FBN = FBP = GND, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	FBN Input Bias Current	FBN = FBN Offset Voltage, FBP = GND, LCD VC = 0.8V		−2.0	−1.0		µA
			●	−3.0	−1.0		µA
g_m	FBP to LCD VC Transconductance	ΔI LCD VC = ±25µA, LCD VC = 1.5V, FBN = 1V			1000		µmhos
			●		1000		µmhos
	FBN to LCD VC Transconductance	ΔI LCD VC = ±25µA, LCD VC = 1.5V, FBP = GND			900		µmhos
			●		900		µmhos
	LCD Error Amplifier Source Current	FBP = FBN = 1V or 0.25V			100		µA
			●		100		µA
	LCD Error Amplifier Sink Current	FBP = FBN = 1.5V or −0.25V			90		µA
			●		90		µA
	LCD VC High Clamp Voltage	FBP = FBN = 1V			2		V
	LCD VC Low Clamp Voltage	FBP = FBN = 1.5V			0.1		V
	LCD VC Switching Threshold	FBP = FBN = 1V, LCD V_{SW} DC = 0%			0.95		V
V_{REF}	Reference Voltage	Measured at REF (Pin 11) on LT1183		1.224	1.244	1.264	V
			●		1.244		V
	Reference Output Impedance	Measured at REF (Pin 11) on LT1183			30		Ω
	V_{REF} – ICCFL Summing Voltage			0.782	0.794	0.806	V
			●		0.794		V
I_{LIM2}	LCD Switch Current Limit	Duty Cycle = 50%	●	0.625	1.0	1.5	A
		Duty Cycle = 80% (Note 3)	●	0.50	0.85	1.3	A
V_{SAT2}	LCD Switch On Resistance	LCD I_{SW} = 0.5A	●		0.9	1.5	Ω
$\frac{\Delta I_Q}{\Delta I_{SW2}}$	Supply Current Increase During LCD Switch On Time	LCD I_{SW} = 0.5A			25		mA/A

The ● denotes specifications which apply over the specified operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LT1182CN/LT1183CN: $T_J = T_A + (P_D \times 70°C/W)$

LT1182CS/LT1183CS: $T_J = T_A + (P_D \times 100°C/W)$

Note 2: Does not include switch leakage.

Note 3: For duty cycles (DC) between 50% and 80%, minimum guaranteed switch current is given by $I_{LIM} = 0.833\ (2 - DC)$ for the CCFL regulator and $I_{LIM} = 0.417\ (2 - DC)$ for the LCD Contrast regulator due to internal slope compensation circuitry.

PIN FUNCTIONS

LT1182

CCFL PGND: This pin is the emitter of an internal NPN power switch. CCFL switch current flows through this pin and allows for internal switch current sensing. Separate analog and power grounds have been provided for the CCFL and LCD regulators in order to minimize interaction.

ICCFL: This pin is the input to the CCFL bulb current programming circuit. This pin is internally regulated to 450mV and accepts an input current signal of 0µA to 100µA full scale which is converted to a 0µA to 500µA source current at the CCFL VC pin. By regulating the I_{CCFL} pin, the input programming current can be set with DAC, PWM or potentiometer control.

DIO: This pin is the common connection between the cathode and anode of two internal diodes. DIO is used in a grounded-bulb configuration and connects directly to the low voltage side of the bulb. Bi-directional bulb current flows in the DIO pin and thus, the diodes conduct alternately on half cycles. Bulb current is controlled by monitoring one-half of the bulb current. The diode conducting on negative half cycles has one-tenth of its current di-

PIN FUNCTIONS

verted to the CCFL VC pin and nulls against the source current provided by the bulb current programmer circuit. The compensation capacitor on the CCFL VC pin acts not only to provide loop compensation but also to provide an averaging function to the rectified sinusoidal bulb current. This scheme reduces the number of loop compensation components and allows for faster loop transient response in comparison to previously published circuits. If a floating bulb configuration is used, this pin should be tied to ground.

CCFL VC: This pin is the output of the bulb current programmer circuit and the input of the current comparator for the CCFL regulator. It is used for frequency compensation, bulb current averaging for grounded-bulb circuits and current limiting. The voltage on the CCFL VC pin determines the current trip level for switch turnoff. During normal operation this pin sits at a voltage between 0.95V (zero switch current) and 2.0V (maximum switch current). This pin has a high impedance output, so the voltage can be clamped externally for adjusting current limit. Loop frequency compensation is typically performed with a series R/C network to ground.

AGND: This is the low current analog ground for the chip. It also acts as the sense for the LCD dual input error amplifier. External feedback divider networks which terminate to ground and frequency compensation components on the VC pins which terminate to ground should connect directly to this pin for best performance.

$\overline{\text{Shutdown}}$: Pulling this pin low causes complete regulator shutdown with quiescent current reduced to about 40μA. The threshold voltage for this pin is about 0.85V. If this pin is not used, it can be left to float high or pulled to a logic high level (max. of 6V). Allowing the pin to float high to provide active operation should be carefully evaluated as capacitive coupling into the pin from switching transients could cause erratic operation.

LCD VC: This pin is the output of the LCD Contrast dual input error amplifier and the input of the current comparator for the LCD Contrast regulator. It is used for frequency compensation and current limiting. The voltage on the LCD VC pin determines the current trip level for switch turnoff. During normal operation, this pin sits at a voltage between 0.95V (zero switch current) and 2.0V (maximum switch current). The LCD VC pin is a high impedance current output (g_m) error amplifier, so the voltage can be clamped externally for adjusting current limit. Loop frequency compensation is typically performed with a series R/C network to ground.

LCD PGND: This pin is the emitter of an internal NPN power switch. LCD Contrast switch current flows through this pin and allows for internal switch current sensing. Separate analog and power grounds have been provided for the CCFL and LCD regulators in order to minimize interaction.

LCD V_{SW}: This pin is the collector of the internal NPN power switch for the LCD Contrast regulator. The power switch is guaranteed to provide a minimum of 625mA. Fast switching times and high efficiency are obtained by using a driver loop to automatically adapt base drive current to the minimum required to keep the switch in a quasi-saturation state. The ratio of switch current to driver current is about 40:1.

FBN: This pin is the noninverting terminal for the negative contrast control error amplifier. The inverting terminal is offset from ground by –10mV to define the error amplifier output state under start-up conditions. The FBN pin acts as a summing junction for a resistor divider network. Input bias current for this pin is typically –1μA.

FBP: This pin is the inverting terminal for the positive contrast control error amplifier. The noninverting terminal is tied to an internal 1.24V reference. Input bias current for this pin is typically 0.5μA.

V_{IN}: This is the supply pin for the LT1182/LT1183. The IC accepts an input voltage range of 3V minimum to 30V maximum with little change in quiescent operating current (zero switch current) as a low dropout internal regulator provides a 2.4V supply for the majority of the internal circuitry. Supply current increases as each PWM's switch current increases at a rate approximately 1/40 of each switch current. This corresponds to a forced Beta of 40 for each switch. Undervoltage lockout is incorporated by sensing the saturation of the lateral PNP pass transistor which drives the 2.4V regulator. Remote collectors on this

13

PIN FUNCTIONS

transistor conduct current and lock out the switch for input voltages below about 2.5V. No hysteresis is used to maximize the useful range of input voltage. The typical input voltage used is a 3.3V or 5V logic supply.

Royer: This pin connects to the center-tapped primary of the Royer converter and is used in conjunction with the BAT pin in a floating-bulb configuration where bulb current is controlled by directly sensing Royer primary-side supply current. This pin is the inverting terminal of a high-side current sense amplifier. The typical quiescent current is 60μA into the pin. If the CCFL regulator is not being used in a floating bulb configuration, the Royer and BAT pins should be tied together.

BAT: This pin connects to the battery voltage from which the CCFL Royer converter and LCD Contrast flyback converter operate. This voltage is typically higher than the V_{IN} supply voltage but can be equal or less than V_{IN}. However, the BAT voltage must be at least 2V greater than the internal 2.4V regulator. This pin is used in conjunction with the Royer pin for floating bulb configurations. This pin is the noninverting terminal of a high-side current sense amplifier. The typical quiescent current is 60μA into the pin. The BAT and Royer pins monitor the voltage across an internal 0.1Ω top-side current sense resistor. A 0A to 1A Royer supply current translates into an input signal range of 0mV to 100mV for the current sense amplifier. This 0mV to 100mV signal range is converted to a 0μA to 500μA sink current at the CCFL VC pin to null against the source current provided by the bulb current programmer circuit. The BAT pin also connects to the top side of an internal clamp between the BAT and Bulb pins.

Bulb: This pin connects to the low side of an internal 7V threshold voltage comparator between the BAT and Bulb pins. This pin can be used to set a maximum threshold voltage level across the primary side of the Royer converter. This reduces the maximum output under start-up conditions or open bulb conditions, thereby easing transformer voltage rating requirements. The Bulb pin is connected to the junction of an external resistor divider network. The divider network connects from the center tap of the Royer transformer to the top side of the Royer inductor. A capacitor across the top of the divider network serves to filter out switching ripple and allows a time constant to be set for determining how quickly the comparator activates. When the comparator is activated, this transfers the Royer converter from current mode operation into voltage mode operation.

CCFL V_{SW}: This pin is the collector of the internal NPN power switch for the CCFL regulator. The power switch is guaranteed to provide a minimum of 1.25A. Fast switching times and high efficiency are obtained by using a driver loop to automatically adapt base drive current to the minimum required to keep the switch in a quasi-saturation state. The ratio of switch current to driver current is about 40:1.

LT1183

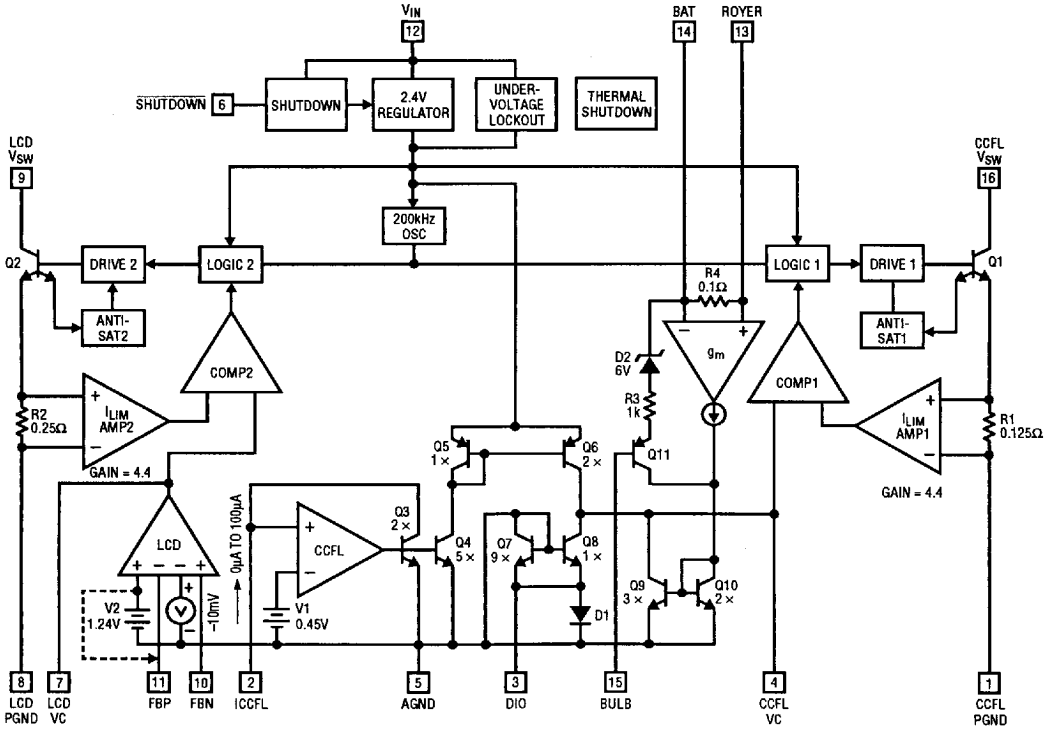
All functions and pins on the LT1183 are equivalent to the LT1182 with the exception of pins 10 and 11. On the LT1182, pin 10 is FBN and pin 11 is FBP. On the LT1183, pin 10 changes to FB and pin 11 changes to REF.

FB: This pin is the common connection between the noninverting terminal for the negative contrast control error amplifier and the inverting terminal for the positive contrast control error amplifier. In comparison to the LT1182, the FBN and the FBP pins have been internally tied together and brought out as one pin.

REF: This pin brings out the internal 1.24V reference and can be used for negative contrast control with an external resistor divider network. The REF pin has an output impedance of about 30Ω. The resistors in the divider network should be chosen to limit reference drive current to less than a few hundred microamps; otherwise reference regulation will be degraded. The REF pin may also be used to generate the maximum programming current for the ICCFL pin by placing a resistor between the pins. PWM or DAC control may then be used to subtract from the maximum programming current.

BLOCK DIAGRAM

LT1182/LT1183 CCFL/LCD Contrast Top Level Block Diagram



LT1183: FBP AND FBN ARE TIED TOGETHER TO PIN 10
REFERENCE IS BROUGHT OUT TO PIN 11

1182/83 BD

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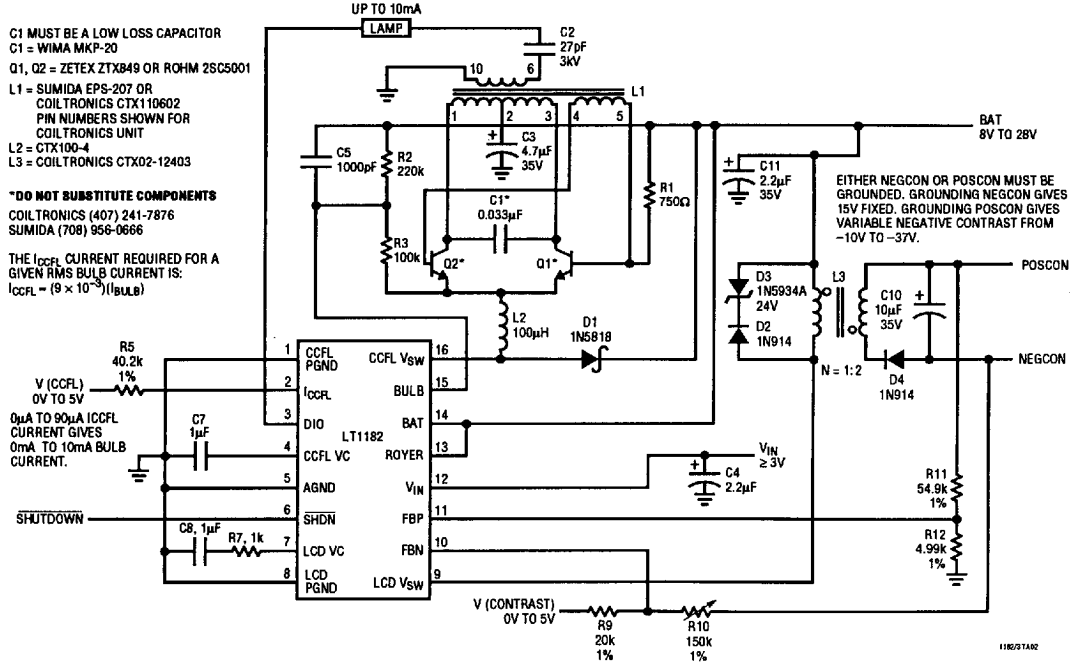
TYPICAL APPLICATION

90% Efficient Grounded CCFL configuration with Dual Polarity LCD Contrast



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