ESS Technology, Inc.

ES1920
AC'97 Rev 2.0/PC98 Audio CODEC
Data Sheet

DESCRIPTION

The ES1920 CODEC is a fully compliant AC'97 Rev. 2.0 CODEC and mixer for a digital audio controller embodied in a single mixed-signal chip. The ES1920 is designed for use with ESS Technology's PCI audio solution, the Maestro™ family of digital audio controllers. The ESS AC'97 CODEC enables higher quality PC audio, lower BOM cost, and greater design flexibility.

The ES1920 is available in an industry-standard 48-pin Low Quad Flat Pack (LQFP).

FEATURES

- Single, high-performance, mixed-signal, 18-bit stereo VLSI chip
- Meets or exceeds AC'97 analog performance specification
- AC-Link TDM digital serial interface to a Maestro Digital Audio Controller
- Supports notebook plus docking station architecture and AC-3 6-speaker configuration

Record and Playback Features

- Full-duplex stereo operation for simultaneous record and playback
- 18-bit stereo ADC and DAC
- 48 kHz sample rate
- Recording multiplexer with 4 stereo inputs: line, CD, video, and aux, plus mic, mono-mix, stereo-mix, and phone
- 3D stereo enhancement
- 91 dB SNR ADC, 92 dB SNR DAC
- CODEC highlights: ultra-low filter ripple, low crosstalk, and improved Vref

Inputs/Outputs

- True line-level out
- Stereo out with volume control
- Mono out with volume control
- 4 stereo analog inputs with 5-bit volume controls for each channel
- 2 mic inputs; selectable
- Mono PC_BEEP and phone inputs
- Input mixer for 4 stereo, mic, and DAC inputs

Power

- Low power modes
- 3.3 V digital interface

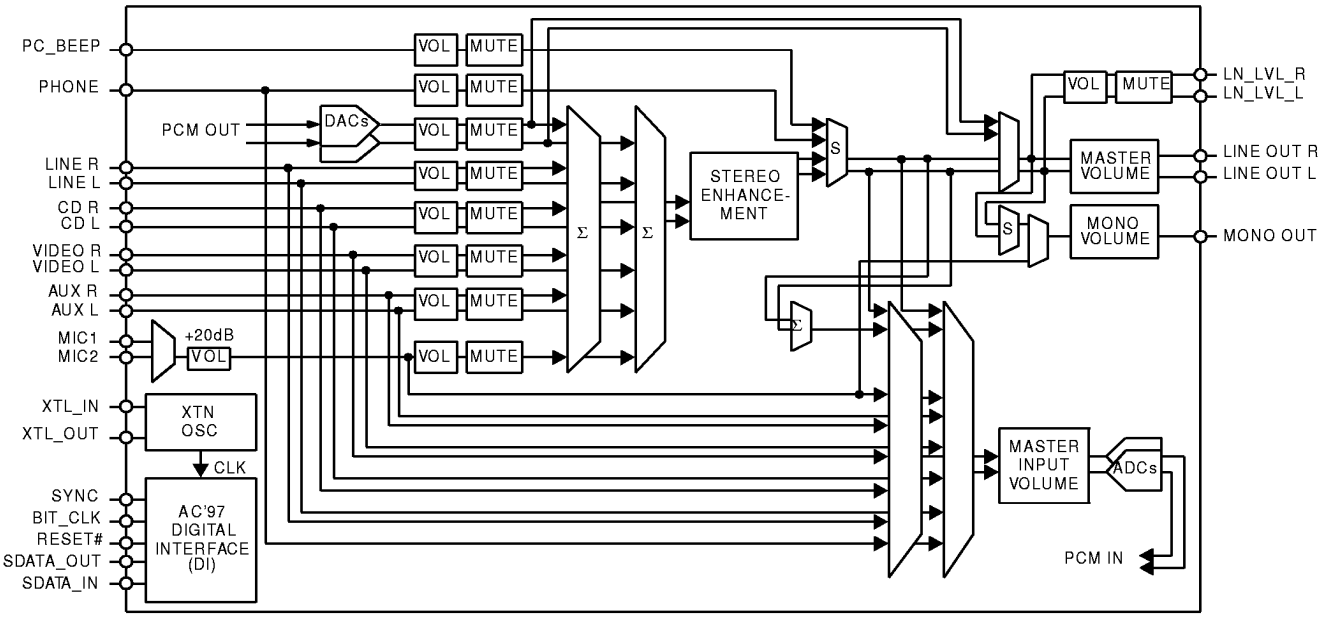
Compatibility

- Meets Intel Audio Codec '97 Rev. 1.03 and 2.0 specifications
- Meets Microsoft PC97 1.0, PC98 1.0, PC99 (draft) specifications

APPLICATIONS

- Motherboard Audio
- PCI Sound Card
- 3D Audio
- Audio/Modem Combo Card
- Notebook Audio

BLOCK DIAGRAM



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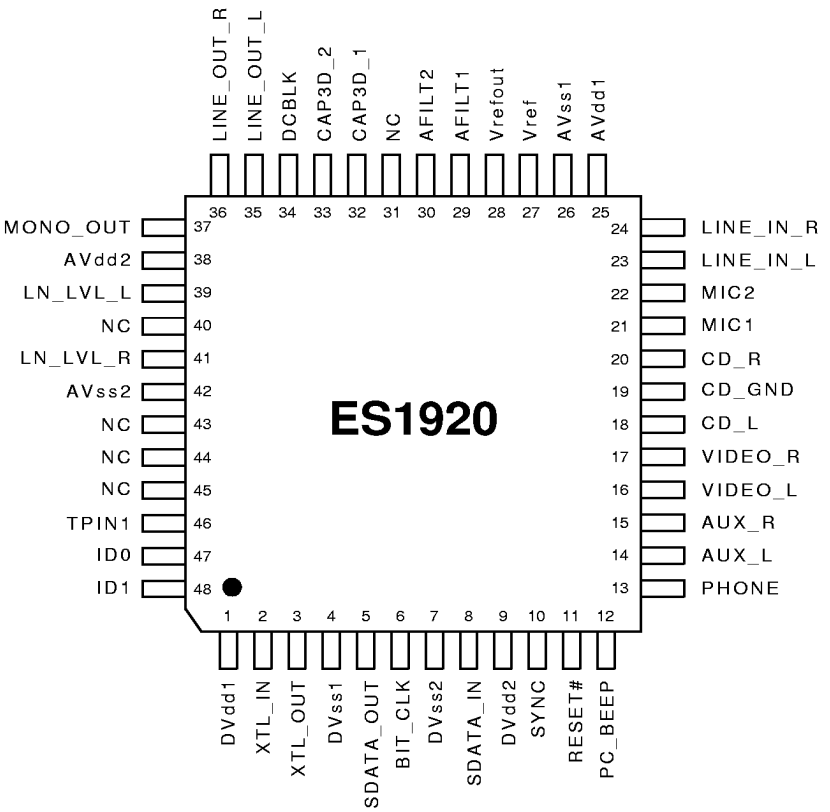
PINOUT



Pin 33 (NC) is bonded internally to pin 29 (AFILT1).

Figure 1 ES1920 Pinout

PIN DESCRIPTION

Name	Number	I/O	Description
DVdd[2:1]	1,9	I	Digital VDD.
XTL_IN	2	I	Oscillator input (24.576 MHz).
XTL_OUT	3	O	Oscillator output.
DVss[2:1]	4,7	I	Digital ground.
SDATA_OUT	5	I	Serial data in.
BIT_CLK	6	O	Serial data clock (12.288 MHz).
SDATA_IN	8	O	Serial data out.
SYNC	10	I	Fixed rate sample sync (48 kHz).
RESET#	11	I	Hardware reset.
PC_BEEP	12	I	PC speaker input.
PHONE	13	I	Telephone speaker input.
AUX_L	14	I	Aux left channel input.
AUX_R	15	I	Aux right channel input.
VIDEO_L	16	I	Video left channel input.
VIDEO_R	17	I	Video right channel input.
CD_L	18	I	CD left channel input.
CD_GND	19	I	CD ground.
CD_R	20	I	CD right channel input.
MIC1	21	I	First microphone input.
MIC2	22	I	Second microphone input.
LINE_IN_L	23	I	Line-In left channel input.
LINE_IN_R	24	I	Line-In right channel input.
AVdd[2:1]	25,38	I	Analog VDD.
AVss[2:1]	26,42	I	Analog ground.
Vref (cap)	27	I/O	Mic reference voltage filter capacitor (2.5 V).
Vrefout	28	O	Mic reference voltage output (2.5 V, 1.25 mA).
AFILT[2:1]	30:29	O	Anti-Aliasing filter.
CAP3D_1	32	O	3D stereo capacitor port.
CAP3D_2	33	I	3D stereo capacitor port.
DCBLK	34	I	DC decoupling capacitor.
LINE_OUT_L	35	O	Line-Out left channel output.
LINE_OUT_R	36	O	Line-Out right channel output.
MONO_OUT	37	O	Mono output.
LN_LVL_L	39	O	True line-level out left.
LN_LVL_R	41	I	True line-level out right.
TPIN1	46	I/O	Test pin for serial and CODEC interface.
ID[1:0]	48:47	I	CODEC ID. Internally pulled-down.
NC	31,40, 43,44,45	–	No connection.

REGISTERS

The ES1920 has 17 16-bit registers, addressable on even-byte boundaries. Access to odd registers is invalid and ignored by the ES1920. This section provides a summary of the mixer registers followed by a detailed description of each register.

Table 1 Mixer Register Summary [a]

Reg	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Remark
00h	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	Reset
02h	Mute	x	Master volume left [5:0]						x	x	Master volume right [5:0]						Master output volume
04h	Mute	x	Line-Level volume left [5:0]						x	x	Line-Level volume right [5:0]						Line-Level output volume
06h	Mute	x	x	x	x	x	x	x	x	x	Mono volume [5:0]						Mono output volume
0Ah	Mute	x	x	x	x	x	x	x	x	x	x	PC beep volume [3:0]				x	PC_BEEP volume
0Ch	Mute	x	x	x	x	x	x	x	x	x	x	Phone volume [4:0]					Phone
0Eh	Mute	x	x	x	x	x	x	x	x	20 dB	x	Mic volume [4:0]					Mic volume
10h	Mute	x	x	Line in volume left [4:0]					x	x	x	Line in volume right [4:0]					Line in volume
12h	Mute	x	x	CD volume left [4:0]					x	x	x	CD volume right [4:0]					CD volume
14h	Mute	x	x	Video volume left [4:0]					x	x	x	Video volume right [4:0]					Video volume
16h	Mute	x	x	Aux volume left [4:0]					x	x	x	Aux volume right [4:0]					Aux volume
18h	Mute	x	x	PCM out volume left [4:0]					x	x	x	PCM out volume right [4:0]					PCM out volume
1Ah	x	x	x	x	x	Record select left [2:0]			x	x	x	x	x	Record select right [2:0]			Record select
1Ch	Mute	x	x	x	Record gain left [3:0]				x	x	x	x	Record gain right [3:0]				Record gain
20h	POP	x	3D	x	x	x	MIX	MS	LPBK	x	x	x	x	x	x	x	General purpose
26h	x	x	Power-down mode [5:0]						x	x	x	R	REF	ANL	DAC	ADC	Power-down control/status
28h	ID1	ID0	x	Reserved				x	x	x	Reserved		x	R	x	x	Extended audio ID

a. The ES1920 outputs the x's in this table as 0's.

Register Detailed Descriptions

The following section describes the mixer registers in detail.

Reset **(00h, R/W)**

0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Write any value to this register to reset the ES1920 registers. Reading this register returns the default hardware configuration, 3800h.

Output Volume Control Registers

These registers control the master volume output of the ES1920. Table 2 shows the relationship between the master volume bits and the attenuation value for registers 02h, 04h, and 06h.

Table 2 Volume Attenuation

Mute	MX5	MX4	MX3	MX2	MX1	MX0	Attenuation
0	0	0	0	0	0	0	0 dB
0	0	0	0	0	0	1	-1.5 dB
0	0	0	0	0	1	0	-3.0 dB
0	0	0	0	0	1	1	-4.5 dB
continued....							
0	0	1	1	1	1	0	-45.0 dB
0	0	1	1	1	1	1	-46.5 dB
0	1	X	X	X	X	X	-46.5 dB
1	X	X	X	X	X	X	- ∞dB

Master Output Volume Control **(02h, R/W)**

Mute	x	Master volume left [5:0]						x	x	Master volume right [5:0]					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls the master playback volume. The maximum setting (00h) corresponds to 0 dB attenuation, with each step adding -1.5 dB attenuation down to the minimum -46.5 dB attenuation (1Fh). See Table 2, "Volume Attenuation," on page 6.

The AC'97 specification requires 5 bits of master volume resolution for both the left (bits 12:8) and right (bits 4:0) channels. In addition, the AC'97 specification allows for an optional sixth bit of resolution (bits 13 and 5). The ES1920 uses 5 bits of resolution, but interprets a 1 written to the optional sixth bit.

When a 1 is written to the optional sixth bit, the data written to the other 5 bits is ignored and stuffed with 1's instead, setting the volume to the minimum value, -46.5 dB.

When read, bits 13 and 5 always read 0.

On reset, this register assumes the value of 8000h.

Bit Definitions:

Bits	Name	Description
15	Mute	1 = Mute enabled. Set master volume at -∞ dB. 0 = Mute disabled.
14	–	Don't care.
13:8	ML[5:0]	Sets the volume level for the LINE_L output. ML[5] is always 0 when read. If a 1 is written to this bit, the values written for bits 12:8 ignored and are stuffed with 1's instead.
7:6	–	Don't care.
5:0	MR[5:0]	Sets the volume level for the LINE_R output. MR[5] is always 0 when read. If a 1 is written to this bit, the values written for bits 4:0 ignored and are stuffed with 1's instead.

Line-Level Output Volume Control **(04h, R/W)**

Mute	x	Line-Level volume left [5:0]						x	x	Line-Level volume right [5:0]					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls the line-level playback volume. The maximum setting (00h) corresponds to 0 dB attenuation, with each step adding -1.5 dB attenuation down to the minimum -46.5 dB attenuation (1Fh). See Table 2, "Volume Attenuation," on page 6.

The AC'97 specification recommends 5 bits of line-level volume resolution for both the left (bits 12:8) and right (bits 4:0) channels. In addition, the AC'97 specification allows for an optional sixth bit of resolution (bits 13 and 5). The ES1920 only uses 5 bits of resolution, but interprets a 1 written to the optional sixth bit.

When a 1 is written to the optional sixth bit, the data written to the other 5 bits is ignored and stuffed with 1's instead, setting the volume to the minimum value, -46.5 dB.

When read, bits 13 and 5 always read 0.

On reset, this register assumes the value of 8000h.

Bit Definitions:

Bits	Name	Description
15	Mute	1 = Mute enabled. Set line-level volume at -∞ dB. 0 = Mute disabled.
14	–	Don't care.
13:8	LL[5:0]	Sets the volume level for the LN_LVL_L output. LL[5] is always 0 when read. If a 1 is written to this bit, the values written for bits 12:8 ignored and are stuffed with 1's instead.
7:6	–	Don't care.
5:0	LR[5:0]	Sets the volume level for the LN_LVL_R output. LR[5] is always 0 when read. If a 1 is written to this bit, the values written for bits 4:0 ignored and are stuffed with 1's instead.

Mono Output Volume Control (06h, R/W)

Mute	x	x	x	x	x	x	x	x	x	Mono volume [5:0]					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls the master playback volume for the mono out. The maximum setting (00h) corresponds to 0 dB attenuation, with each step adding -1.5 dB attenuation down to the minimum -46.5 dB attenuation (1Fh). See Table 2, "Volume Attenuation," on page 6.

The AC'97 specification requires 5 bits of mono volume resolution (bits 4:0). In addition, the AC'97 specification allows for an optional sixth bit of resolution (bit 5). The ES1920 only uses 5 bits of resolution, but interprets a 1 written to the optional sixth bit.

When a 1 is written to the optional sixth bit, the data written to the other 5 bits is ignored and stuffed with 1's instead, setting the volume to the minimum value, -46.5 dB.

When read, bit 5 always reads 0.

On reset, this register assumes the value of 8000h.

Bits Definitions:

Bits	Name	Description
15	Mute	1 = Mute enabled. Set mono volume at -∞ dB. 0 = Mute disabled.
14:6	–	Don't care.
5:0	MM[5:0]	Sets the volume level for the MONO_OUT output. MM[5] is always 0 when read. If a 1 is written to this bit, the values written for bits 4:0 ignored and are stuffed with 1's instead.

PC_BEEP Volume (0Ah, R/W)

Mute	x	x	x	x	x	x	x	x	x	x	PC beep volume				x
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register level controls the volume level for the PC beep input. The maximum setting (00h) corresponds to 0 dB attenuation, with each step adding -3 dB attenuation down to the minimum -45 dB attenuation (0Fh). See Table 3, "PC Beep Volume Attenuation," on page 7.

PC_BEEP supports motherboard implementations. The intention of routing PC_BEEP through the ES1920 mixer is to eliminate the requirement for an on-board speaker by guaranteeing a connection to speakers connected through the output jack. In order for this to be viable the PC_BEEP signal needs to reach the output jack at all times.

NOTE: It is required that PC_BEEP be routed to the left and right line outputs even when the ES1920 is in a RESET state. This is so that Power On Self Test (POST) codes can be heard by the user in case of a hardware problem with the PC. This can be accomplished with a high impedance path to the outputs without any attenuation. For further PC_BEEP implementation details please refer to the AC'97 Technical FAQ sheet.

Table 3 PC Beep Volume Attenuation

Mute	PV3	PV2	PV1	PV0	Attenuation
0	0	0	0	0	0 dB
0	0	0	0	1	-3.0 dB
0	0	0	1	0	-6.0 dB
0	0	0	1	1	-9.0 dB
continued....					
0	1	1	1	1	-45.0 dB
1	X	X	X	X	- ∞dB

On reset this register assumes the value of 8000h.

Bits Definitions:

Bits	Name	Description
15	Mute	1 = Mute enabled. Set PC beep volume at -∞ dB. 0 = Mute disabled.
14:5	–	Don't care.
4:1	PBV[3:0]	Sets the volume level for the PC beep input.
0	–	Don't care.

Analog Mixer Input Gain Registers

These registers control the volume for each of the analog inputs. The maximum setting (00h) corresponds to 12 dB gain. Each step adds -1.5 dB attenuation down to the minimum -34.5 dB attenuation (1Fh). Table 4 shows the relationship between the volume bits and the attenuation value for registers 0Ch, 0Eh, 10h, 12h, 14h, 16h, and 18h.

Table 4 Analog Mixer Input Volume Attenuation

Mute	GX4	GX3	GX2	GX1	GX0	Attenuation
0	0	0	0	0	0	12.0 dB
0	0	0	0	0	1	10.5 dB
0	0	0	0	1	0	9.0 dB
continued...						
0	0	1	0	0	0	0 dB
0	0	1	0	0	1	-1.5 dB
0	0	1	0	1	0	-3.0 dB
continued....						
0	1	1	1	1	0	-33.0 dB
0	1	1	1	1	1	-34.5 dB
1	X	X	X	X	X	- ∞dB

Phone Volume (0Ch, R/W)

Mute	x	x	x	x	x	x	x	x	x	x	Phone volume				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls the volume for the phone input. The Phone input is a mono input. See Table 4, “Analog Mixer Input Volume Attenuation,” on page 7.

On reset, this register assumes the value of 8008h.

Bits Definitions:

Bits	Name	Description
15	Mute	In Extended mode, Mute applies only to the left channel. 1 = Mute enabled. Set Phone volume at -∞ dB. 0 = Mute disabled.
14:5	–	Don’t care.
4:0	PV[4:0]	Sets the volume level for the PHONE input.

Mic Volume (0Eh, R/W)

Mute	x	x	x	x	x	x	x	x	20 dB	x	Mic volume				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls the volume for the microphone input. The mic input is a mono input. See Table 4, “Analog Mixer Input Volume Attenuation,” on page 7.

On reset, this register assumes the value of 8008h.

Bits Definitions:

Bits	Name	Description
15	Mute	In Extended mode, Mute applies only to the left channel. 1 = Mute enabled. Set Mic volume at -∞ dB. 0 = Mute disabled.
14:7	–	Don’t care.
6	20 dB	1 = 20 dB boost enabled. 0 = 20 dB boost disabled.
5	–	Don’t care.
4:0	MV[4:0]	Sets the volume level for the Mic input. In Extended mode this applies only to the right channel.

Line In Volume (10h, R/W)

Mute	x	x	Line in volume left					x	x	x	Line in volume right				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls the Line In volume. See Table 4, “Analog Mixer Input Volume Attenuation,” on page 7.

On reset, this register assumes the value of 8808h.

Bits Definitions:

Bits	Name	Description
15	Mute	1 = Mute enabled. Set Line in volume at -∞ dB. 0 = Mute disabled.
14:13	–	Don’t care.
12:8	LIL[4:0]	Sets the volume level for the LINE_IN_L input.
7:5	–	Don’t care.
4:0	LIR[4:0]	Sets the volume level for the LINE_IN_R input.

CD Volume (12h, R/W)

Mute	x	x	CD volume left					x	x	x	CD volume right				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls the CD volume. See Table 4, “Analog Mixer Input Volume Attenuation,” on page 7.

On reset, this register assumes the value of 8808h.

Bits Definitions:

Bits	Name	Description
15	Mute	1 = Mute enabled. Set CD volume at -∞ dB. 0 = Mute disabled.
14:13	–	Don’t care.
12:8	CDL[4:0]	Sets the volume level for the CD_L input.
7:5	–	Don’t care.
4:0	CDR[4:0]	Sets the volume level for the CD_R input.

Video Volume (14h, R/W)

Mute	x	x	Video volume left					x	x	x	Video volume right				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls the Video volume. See Table 4, “Analog Mixer Input Volume Attenuation,” on page 7.

On reset, this register assumes the value of 8808h.

Bits Definitions:

Bits	Name	Description
15	Mute	1 = Mute enabled. Set Video volume at -∞ dB. 0 = Mute disabled.
14:13	–	Don’t care.
12:8	VL[4:0]	Sets the volume level for the VIDEO_L input.
7:5	–	Don’t care.
4:0	VR[4:0]	Sets the volume level for the VIDEO_R input.

Aux Volume (16h, R/W)

Mute	x	x	Aux volume left					x	x	x	Aux volume right				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls the Auxiliary volume. See Table 4, “Analog Mixer Input Volume Attenuation,” on page 7.

On reset, this register assumes the value of 8808h.

Bits Definitions:

Bits	Name	Description
15	Mute	1 = Mute enabled. Set Aux volume at -∞ dB. 0 = Mute disabled.
14:13	–	Don’t care.
12:8	AL[4:0]	Sets the volume level for the AUX_L input.
7:5	–	Don’t care.
4:0	AR[4:0]	Sets the volume level for the AUX_R input.

PCM Out Volume (18h, R/W)

Mute	x	x	PCM out volume left					x	x	x	PCM out volume right				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls the PCM Out volume. See Table 4, “Analog Mixer Input Volume Attenuation,” on page 7.

On reset, this register assumes the value of 8808h.

Bits Definitions:

Bits	Name	Description
15	Mute	1 = Mute enabled. Set PCM out volume at -∞ dB. 0 = Mute disabled.
14:13	–	Don’t care.
12:8	PCML [4:0]	Sets the volume level for the PCM output.
7:5	–	Don’t care.
4:0	PCMR [4:0]	Sets the volume level for the PCM output.

Record Select (1Ah, R/W)

x	x	x	x	x	Record select left			x	x	x	x	x	Record select right		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register selects record sources for the left and right channel.

On reset, this register assumes the value of 0000h.

Bits Definitions:

Bits	Name	Description
15:11	–	Don’t care.
10:8	RSL[2:0]	Selects left channel record source:

bit 10	bit 9	bit 8	source
0	0	0	Mic (default)
0	0	1	CD left
0	1	0	Video left
0	1	1	Aux left
1	0	0	Line left
1	0	1	Stereo mix left
1	1	0	Mono mix
1	1	1	Phone

7:5	–	Don’t care.
7:5	RSR[2:0]	Selects right channel record source:

bit 2	bit 1	bit 0	source
0	0	0	Mic (default)
0	0	1	CD right
0	1	0	Video right
0	1	1	Aux right
1	0	0	Line right
1	0	1	Stereo mix right
1	1	0	Mono mix
1	1	1	Phone

Record Gain (1Ch, R/W)

Mute	x	x	x	Record gain left				x	x	x	x	Record gain right			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register sets the volume level for the record input. The minimum setting (00h) corresponds to 0 dB gain. Each step adds 1.5 dB gain up to the maximum 22.5 dB gain (0Fh). Table 5 shows the relationship between the record volume bits and the gain value for register 1Ch.

Table 5 Record Mixer Output Volume Gain

Mute	GX3	GX2	GX1	GX0	Attenuation
0	0	0	0	0	0 dB
0	0	0	0	1	1.5 dB
0	0	0	1	0	3.0 dB
continued....					
0	1	1	1	0	21.0 dB
0	1	1	1	1	22.5 dB
1	X	X	X	X	- ∞dB

On reset, this register assumes the value of 8000h.

Bits Definitions:

Bits	Name	Description
15	Mute	1 = Mute enabled. Set Record gain at -∞ dB. 0 = Mute disabled.
14:12	–	Don't care.
11:8	RGL[3:0]	Sets the volume level for the Record input left.
7:4	–	Don't care.
3:0	RGR[3:0]	Sets the volume level for the Record input right.

General Purpose (20h, R/W)

POP	x	3D	x	x	x	MIX	MS	LPBK	x	x	x	x	x	x	x
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register controls a number of miscellaneous functions. This register should be read before writing to generate a mask for only the bit(s) that need to be changed. On reset, this register assumes the value of 0000h.

Bits Definitions:

Bits	Name	Description
15	POP	Optional PCM out 3D bypass path control. 1 = pre 3D. 0 = post 3D.
14	–	Don't care.
13	3D	3D stereo enhancement control. 1 = on. 0 = off.
12:10	–	Don't care.
9	MIX	Mono output select: 1 = Mic. 0 = Mixer.
8	MS	Microphone selector: 1 = Mic2. 0 = Mic1.
7	LPBK	This bit enables loopback of the ADC output to the DAC input without involving the AC-Link. This allows for full system performance measurements. 1 = Enable ADC/DAC loopback mode. 0 = Disable ADC/DAC loopback mode.
6:0	–	Don't care.

Power-down Control/Status (26h, R/W)

x	x	Power-down mode				x	x	x	R	REF	ANL	DAC	ADC
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register is used to program power-down states and monitor the readiness of selected subsystems.

The ES1920 implements six of the eight power management bits in the AC'97 specification (the three remaining bits concern headphone amplifier, and modem CODEC).

When bit 3 is high, the ADC, DAC, analog mixer, and Vref subsections are powered down. When bit 3 is reset to 0, the ES1920 can resume its previous state as the context of bits PR2:0 are preserved. Though the context is preserved for bits PR2:0, bits 3:0 show the actual power-down status.

When the AC-Link "CODEC ready" bit (SDATA_IN slot 0 bit 15) is a 1, it indicates that the AC-Link and the ES1920 control and status registers are fully operational. The Maestro Digital Controller must check bits 4:0 to determine exactly which subsections are ready.

Bits 7:0 are read-only. Writes will have no effect on these bits.

Bits 3:0 are all 0 after a cold reset. As each subsection becomes ready to resume normal operation, the corresponding bit becomes a 1.

This register is not affected by a write to the reset register.

Bit Definitions:

Bits	Name	Description
15:14	–	Don't care.
13	PR5	1 = Digital section powered down with all clocks disabled. This bit can be cleared by a cold reset only. 0 = Digital section powered up.
12	PR4	1 = Digital section powered down with oscillator enabled. The analog mixer can still function. The 24.576 oscillator still runs. This bit can be cleared by either a cold or a warm reset. The digital section powers up quickly as the oscillator is still running. 0 = Digital section powered up.
11	PR3	1 = Analog mixer powered down (Vref off). In this case, the ADCs, DACs, Mixer, and Vref are also powered down; however, the state of PR2:0 are preserved. 0 = Analog mixer powered up.
10	PR2	This section is powered down when PR3 = 1, but the state of PR2 is preserved. 1 = Analog mixer powered down with reference generator still enabled. 0 = Analog mixer powered up.
9	PR1	This section is powered down when PR3 = 1, but the state of PR1 is preserved. 1 = PCM out DACs powered down. 0 = PCM out DACs powered up.
8	PR0	This section is powered down when PR3 = 1, but the state of PR0 is preserved. 1 = PCM in ADCs, input volume control, and input mux powered down. 0 = PCM in ADCs and input mux powered up.
7:4	–	READ-ONLY. Don't care.
4	–	READ-ONLY. Reserved.
3	REF	READ-ONLY. VREF is up to nominal level.
2	ANL	READ-ONLY. Analog mixers, etc. ready.
1	DAC	READ-ONLY. DAC section ready to accept data.
0	ADC	READ-ONLY. ADC section ready to transmit data.

Extended Audio Register

The ES1920 may be configured as a primary or secondary chip by pins 47 and 48 (ID[1:0]). These pins correspond directly to bits 1:0 for SDATA_OUT slot 0. In primary mode, the BIT_CLK pin remains an output; in secondary mode, it is configured as an input. Because of this, the primary chip has to drive the BIT_CLK to the digital controller and the secondary chips. Powering down the primary chip also disables the operation of the secondary chips. In a multiple chip setup, SDATA_OUT, BIT_CLK, SYNC, and RESET# are common to all the chips, including the digital controller. However, each ES1920 has a dedicated DSDATA_IN connection to the digital controller. For example; if there are one primary and two secondary ES1920s, the digital controller requires 3 separate SDATA_IN pins. The primary and secondary ES1920s use the same slot data for PCM playback, but the PCM recordings may be different, since there are dedicated SDATA_INs.

Extended Audio ID **(28h, R)**

ID1	ID0	x	Reserved	x	x	x	Reserved	x	R	x	x
15	14	13	12 11 10 9	8	7	6	5 4	3	2	1	0

This register is used to identify the extended audio features that are supported (in addition to the original AC'97 features identified by reading the Reset register).

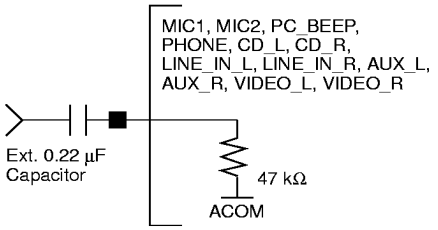
On reset, this register assumes the value of 0001h.

Bit Definitions:

Bits	Name	Description
15:14	ID[1:0]	CODEC configuration indicator. bit 15 bit 14 configuration 0 0 Primary CODEC
13	–	Don't care.
12:9	–	Reserved.
8:6	–	Don't care.
5:4	–	Reserved.
3	–	Don't care.
2	–	Reserved.
1:0	–	Don't care.

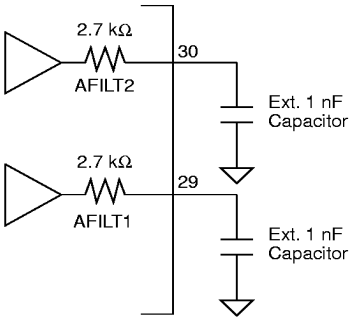
EXTERNAL COMPONENTS INTERFACE

Analog Input

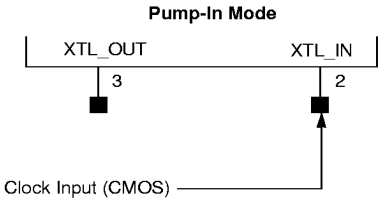


Use low-cost 0.22 μF ceramic capacitors for the full audio range of 20 Hz to 20 kHz. However, 0.1 μF may be used with good results for an audio range of 33 Hz to 20 kHz. Most PC speakers have a low frequency response above 50 Hz.

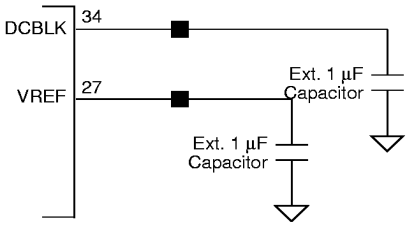
Anti-Aliasing Filter



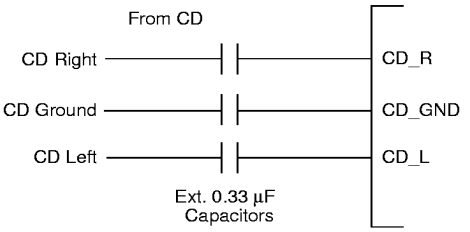
Oscillator Connection



Reference Voltage Filtering

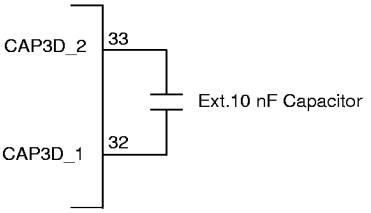


CD Input

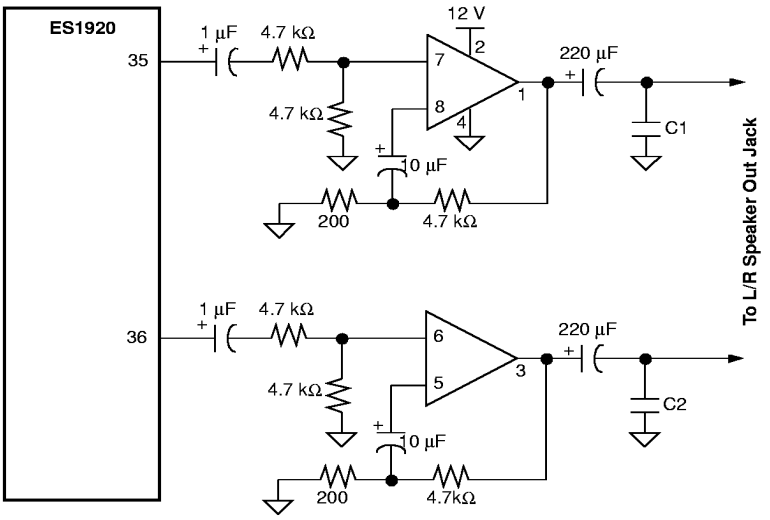


Use low-cost 0.33 μF ceramic capacitors for the full audio range of 20 Hz to 20 kHz. However, 0.1 μF may be used with good results for an audio range of 50 Hz to 20 kHz. Most PC speakers have a low frequency response above 50 Hz.

Stereo Enhancement Capacitor



APPLICATION NOTE



Notes:

1. The op amps are in a single package. Part Number NJM2073 from New Japan Radio or NJR. The op amps have internal feedback.
2. The op amps are not stable under 26 dB of gain; check data sheet for gain calculation.
3. C1 and C2: 600 to 100 pF.

Figure 2 Low Cost Power Amp

ELECTRICAL CHARACTERISTICS

All voltages are in volts, current in mA and timing in ns unless otherwise specified. Specifications are guaranteed by design and characterization. They are subjected to production testing at ESS' discretion.
(@ VDD = 5.0V, 25°C)

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. There are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Absolute Maximum Ratings

Ratings	Symbol	Value	Units
Analog supply voltage range	VA	-0.3 to 6.0	V
Digital supply voltage range	VD	-0.3 to 6.0	V
Input or output voltage	VIN	-0.5 to VDD + 0.5	V
Operating temperature range	TA	0 to 70	°C
Storage temperature range	TSTG	-40 to 125	°C

Thermal Characteristics

The ES1920 is designed to operate at case temperatures less than 70° C.

Operating Conditions

The ES1920 digital and analog characteristics operate under the following conditions:

VDD	4.75 V to 5.25 V (at 5 V)
AVD	4.75 V to 5.25 V (at 5 V)
TA	25°

Recommended DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Digital Supply Voltage	VDD 5V	4.75	5.0	5.25	V
Alternate Digital Supply Voltage	VDD 3.3V	3.15	3.3	5.25	V
Analog Supply Voltage	AVD	4.75	5.0	5.25	V
Ambient Temperature	T_{amb}	0	25	70	°C
I/O latchup Current (VDD < V < VSS)	Iklu	100			mA
Electrostatic Protection (100pF, 1.5kΩ)	Vesd	2			kV

Power Consumption

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Digital Supply Current	I_{VDD}	Power Up Power Down		20 10		mA µA
Analog Supply Current	I_{AVD}	Power Up Power Down		65 10		mA µA

Digital Characteristics (at VDD = 5.0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Low Level Input Current	Iil	Vin = VSS	-10		10	µA
High Level Input Current	Iih	Vin = VDD	-10		10	µA
Tristate Output Leakage Current	Ioz	Vout = VDD/VSS	-10		10	µA
Low Level Input Voltage	Vil	TTL-static			0.8	V
High Level Input Voltage	Vih	TTL-static	2.0			V
Low Level Output Voltage	Vol	TTL-static			0.4	V
High Level Output Voltage	Voh	TTL-static	2.4			V
Input Capacitance	Cin	1 MHz @ 0V			5	pF
Output Capacitance	Cout	1 MHz @ 0V			5	pF
Output Current Drive	SDATA_IN BIT_CLK				12	mA

ANALOG PERFORMANCE CHARACTERISTICS

The standard test conditions apply unless otherwise noted.

$T_{ambient}$ = 25°C, AVdd = DVdd = 5.0 V ±5%; Input Voltage Levels: Logic Low = 0.8 V, Logic High = 2.4 V;
1 kHz input sine wave; Sample Frequency = 48 kHz; 0 dB = 1 Vrms, 10 kΩ / 50 pF load,
Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB attenuation; tone and 3D disabled)

Parameter		Min.	Typ.	Max.	Units
Full Scale Input Voltage:	Line Inputs Mic Inputs[a]	– –	1.0 0.1	– –	
Full Scale Output Voltage:	Line Output	–	1.0	–	Vrms
Analog S/N:	CD to LINE_OUT Other to LINE_OUT	90 90	– –	– –	dB
Analog Frequency Response[b]		20	–	20K	Hz
Digital S/N[c]	DAC ADC	87 85	92 91	– –	dB
Total Harmonic Distortion:	Line Output[d]	–	0.007	0.02	%
DAC & ADC Frequency Response[e]	DAC ADC	0 20		20K 21K	Hz
Stop Band	DAC ADC	28 26.4			kHz
Transition Band	DAC ADC	20 21.6		28 26.4	kHz
Stop Band Rejection[f]		-74			dB
Out-of-Band Rejection[g]		–	-40	–	dB
Group Delay[h]		–	0.63	–	mS
Power Supply Rejection Ratio (1 kHz)		–	40	–	dB
Crosstalk Between Input Channels		–	–	-80	dB
Spurious Tone Reduction		–	-100	–	dB
Attenuation, Gain Step Size		–	1.5	–	dB
Analog Input Impedance		40	47	–	kΩ
CD Input Impedance		25	33	–	kΩ
Input Capacitance		–	15	–	pF
Vrefout		–	2.5	–	V

a. With +20 dB Boost on, 1.0 Vrms with Boost off
b. ±1 dB limits
c. The ratio of the rms output level with 1 kHz full scale input to the rms output level with all zeros into the digital input. Measured “A wtd” over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
d. 0 dB gain, 20 kHz BW, 48 kHz Sample Frequency
e. ±0.25 dB limits max, ±0.1 dB typical
f. Stop Band rejection determines filter requirements to 70 kHz. Out-of-Band rejection determines audible noise.
g. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 kHz to 100 kHz, with respect to a 1 Vrms DAC output.
h. Group delay measured A-D-D-A

MISCELLANEOUS ANALOG PERFORMANCE CHARACTERISTICS

Mixer Specifications

(all specifications subject to change pending device characterization)

Parameter	Condition	Min.	Typ.	Max.	Units
General Input & Output Vol. Control Step			1.5		dB
PC_BEEP Vol. Control Step			3.0		dB
Mute Level			80		dB
Interchannel Gain Mismatch		-0.5		0.5	dB
Gain Drift			100		ppm/°C

Analog Characteristics

(Ta = 25°C, AVdd1, AVdd2, DVdd1, DVdd2 = 5 V, fs = 48 kHz)

ADCs & Analog Inputs

(Analog Source Impedance 50Ω)

Parameter	Condition	Min.	Typ.	Max.	Units
Resolution			16		Bits
Gain Error			±2	±5	%
Offset Error			±10		mV

DACs & Analog Outputs

Parameter	Condition	Min.	Typ.	Max.	Units
Resolution			16		Bits
Interchannel Gain Mismatch			0.1	0.2	dB
Gain Error				±5	%
Gain Drift			60		ppm/°C

AC-LINK TIMING

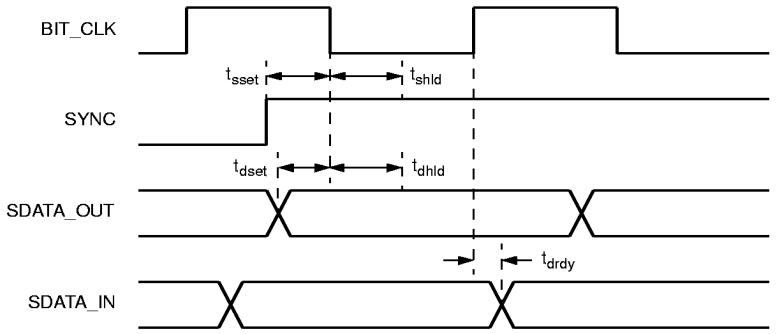


Figure 3 AC-Link Timing

Table 6 AC-Link Timing Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{sset}	BIT_CLK negative-edge to SYNC setup	15			ns
t_{shld}	BIT_CLK negative-edge to SYNC hold	5			ns
t_{dset}	BIT_CLK negative-edge to SDATA_OUT setup	15			ns
t_{dhld}	BIT_CLK negative-edge to SDATA_OUT hold	5			ns
t_{drdy}	BIT_CLK positive-edge to SDATA_IN ready			5	ns

ATE/VENDOR TEST MODE TIMING

ATE in Circuit test mode: The AC'97 CODEC enters the ATE in circuit test mode if SDATA_OUT is sampled high at the trailing edge of RESET#. When the AC'97 CODEC is in this mode BIT_CLK and SDATA_IN are driven to a high-impedance state.

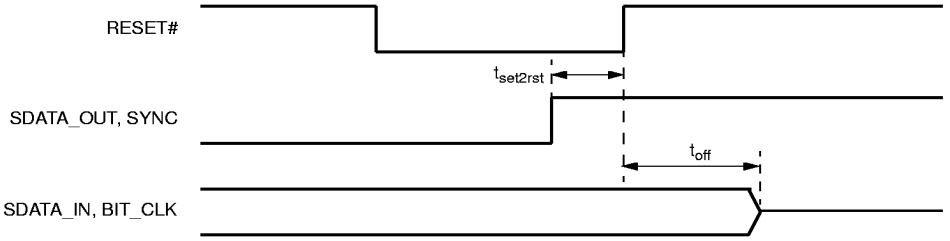
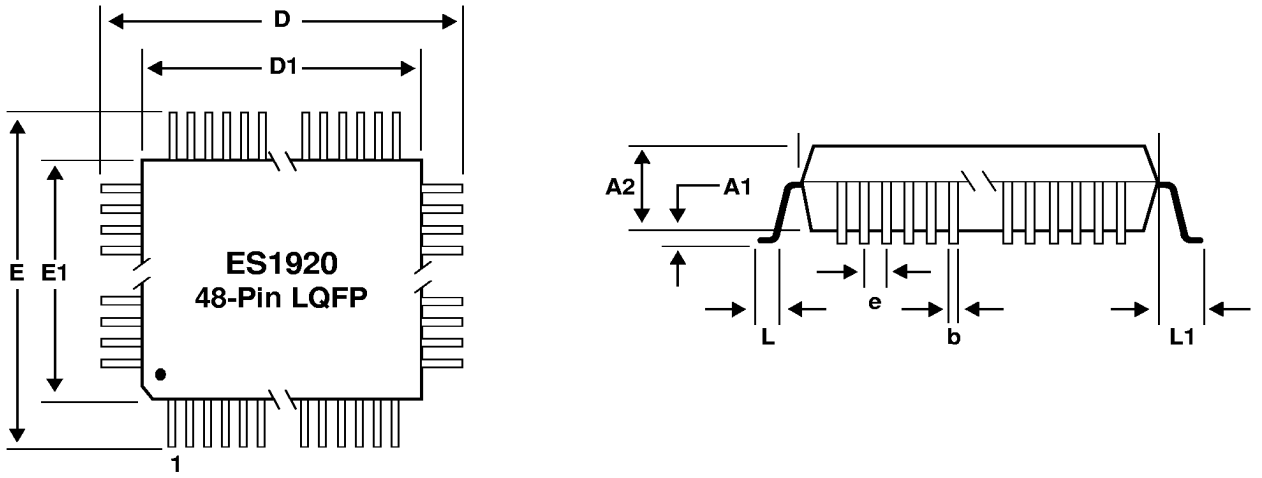


Figure 4 ATE/Vendor Test Mode Timing

Table 7 ATE/Vendor Test Mode Timing Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
$t_{set2rst}$	SDATA_OUT setup to RESET# positive-edge	30			ns
t_{off}	RESET# positive-edge to Hi-Z delay			140	ns

MECHANICAL DIMENSIONS



Symbol	Description	Millimeters		
		Min	Nom	Max
D	Lead to lead, X-axis	8.6	9.0	9.4
D1	Package's outside, X-axis	6.9	7.0	7.1
E	Lead to lead, Y-axis	8.6	9.0	9.4
E1	Package's outside, Y-axis	6.9	7.0	7.1
A1	Board standoff	-	0.1	-
A2	Package thickness	-	-	1.7
b	Lead width	0.13	-	0.28
e	Lead pitch	-	0.5	-
L	Foot length	0.3	0.5	0.7
L1	Lead length	-	1.0	-
-	Foot angle	0	-	10
-	Coplanarity	-	-	7
-	Leads in X-axis	-	12	-
-	Leads in Y-axis	-	12	-
-	Total leads	-	48	-
-	Package type	-	LQFP	-

Figure 5 Mechanical Dimensions