CAT521

Configured Digitally Programmable Potentiometer (DPP™): Programmable Voltage Applications

FEATURES

- **8-bit DPP configured as a programmable voltage source in DAC-like applications**
- **Buffered wiper output**
- **Non-volatile NVRAM memory wiper storage**
- **Output voltage range includes both supply rails**
- **1 LSB accuracy, high resolution**
- **Serial Microwire-like interface**
- **Single supply operation: 2.7V - 5.5V**
- **Setting read-back without effecting outputs**

APPLICATIONS

- **Automated product calibration**
- **Remote control adjustment of equipment**
- **Offset, gain and zero adjustments in self-calibrating and adaptive control systems**
- **Tamper-proof calibrations**
- **DAC (with memory) substitute**

DESCRIPTION

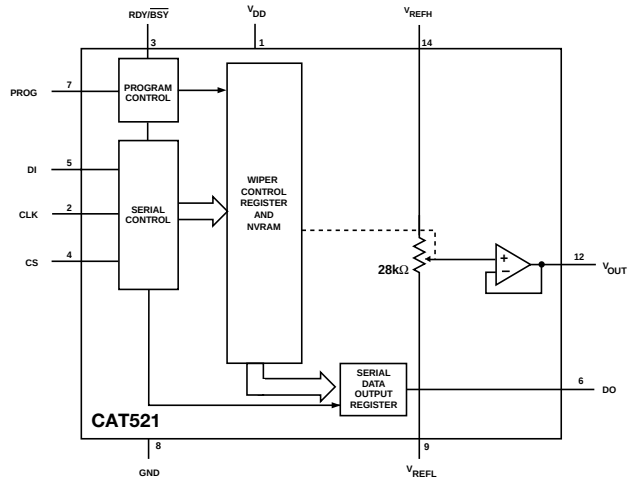
The CAT521 is a 8-bit digitally-programmable potentiometer (DPP™) configured for programmable voltage and DAC-like applications. Intended for final calibration of products such as camcorders, fax machines and cellular telephones on automated high volume production lines, it is also well suited for self-calibrating systems and for applications where equipment which requires periodic adjustment is either difficult to access or in a hazardous environment.

The programmable DPP has an output voltage range which includes both supply rails. The wiper is buffered by a rail to rail op amp. The wiper setting, stored in non-volatile NVRAM memory, is not lost when the device is powered down and is automatically reinstated when power is returned. The wiper can be dithered to test new output values without effecting the stored settings and stored settings can be read back without disturbing the DPP's output.

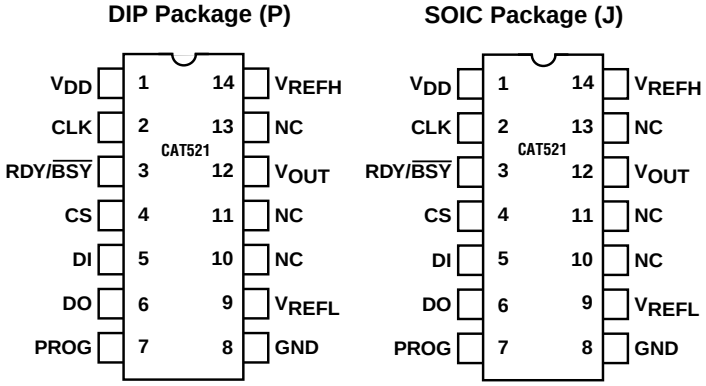
The CAT521 is controlled with a simple 3-wire, Microwire-like serial interface. A Chip Select pin allows several devices to share a common serial interface. Communication back to the host controller is via a single serial data line thanks to the CAT521 Tri-Stated Data Output pin. A RDY/$\overline{BSY}$ output working in concert with an internal low voltage detector signals proper operation of the non-volatile NVRAM memory Erase/Write cycle.

The CAT521 is available in 0°C to 70°C commercial and -40°C to 85°C industrial operating temperature ranges. Both 14-pin plastic DIP and surface mount packages are available.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



Doc. No. 2003, Rev. C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage*
- V_{DD} to GND ..... -0.5V to +7V

Inputs
- CLK to GND ..... -0.5V to V_{DD} +0.5V
- CS to GND ..... -0.5V to V_{DD} +0.5V
- DI to GND ..... -0.5V to V_{DD} +0.5V
- RDY/BSY to GND ..... -0.5V to V_{DD} +0.5V
- PROG to GND ..... -0.5V to V_{DD} +0.5V
- V_{REF}H to GND ..... -0.5V to V_{DD} +0.5V
- V_{REF}L to GND ..... -0.5V to V_{DD} +0.5V

Outputs
- D_0 to GND ..... -0.5V to V_{DD} +0.5V
- V_{OUT} 1– 4 to GND ..... -0.5V to V_{DD} +0.5V

Operating Ambient Temperature
- Commercial ('C' or Blank suffix) ..... 0°C to +70°C
- Industrial ('I' suffix) ..... -40°C to +85°C

Junction Temperature ..... +150°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering (10 sec max) ..... +300°C

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Absolute Maximum Ratings are limited values applied individually while other parameters are within specified operating conditions, and functional operation at any of these conditions is NOT implied. Device performance and reliability may be impaired by exposure to absolute rating conditions for extended periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Method
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(2)	Latch-Up	100		mA	JEDEC Standard 17

NOTES: 1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} + 1V.

POWER SUPPLY

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD1}	Supply Current (Read)	Normal Operating	—	400	600	µA
I_{DD2}	Supply Current (Write)	Programming, V_{DD} = 5V	—	1600	2500	µA
		V_{DD} = 3V	—	1000	1600	µA
V_{DD}	Operating Voltage Range		2.7	—	5.5	V

LOGIC INPUTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	Input Leakage Current	V_{IN} = V_{DD}	—	—	10	µA
I_{IL}	Input Leakage Current	V_{IN} = 0V	—	—	-10	µA
V_{IH}	High Level Input Voltage		2	—	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	—	0.8	V

LOGIC OUTPUTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High Level Output Voltage	I_{OH} = -40µA	V_{DD} -0.3	—	—	V
V_{IL}	Low Level Output Voltage	I_{OL} = 1 mA, V_{DD} = +5V	—	—	0.4	V
		I_{OL} = 0.4 mA, V_{DD} = +3V	—	—	0.4	V

POTENTIOMETER CHARACTERISTICS

V_{DD} = +2.7V to +5.5V, $V_{REF}H = V_{DD}$, $V_{REF}L$ = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{POT}	Potentiometer Resistance			28		kΩ
	R_{POT} to R_{POT} Match		—	±0.5	±1	%
	Pot Resistance Tolerance				±15	%
	Voltage on V_{REFH} pin		2.7		V_{DD}	V
	Voltage on V_{REFL} pin		OV		V_{DD} - 2.7	V
	Resolution			0.4		%
INL	Integral Linearity Error			0.5	1	LSB
DNL	Differential Linearity Error			0.25	0.5	LSB
R_{OUT}	Buffer Output Resistance				10	Ω
I_{OUT}	Buffer Output Current				3	mA
TC_{RPOT}	TC of Pot Resistance			300		ppm/°C
TC_{RATIO}	Ratiometric TC					ppm/°C
R_{ISO}	Isolation Resistance					Ω
V_N	Noise					nV/√Hz
C_H/C_L	Potentiometer Capacitances			8/8		pF
fc	Frequency Response	Passive Attenuator				MHz

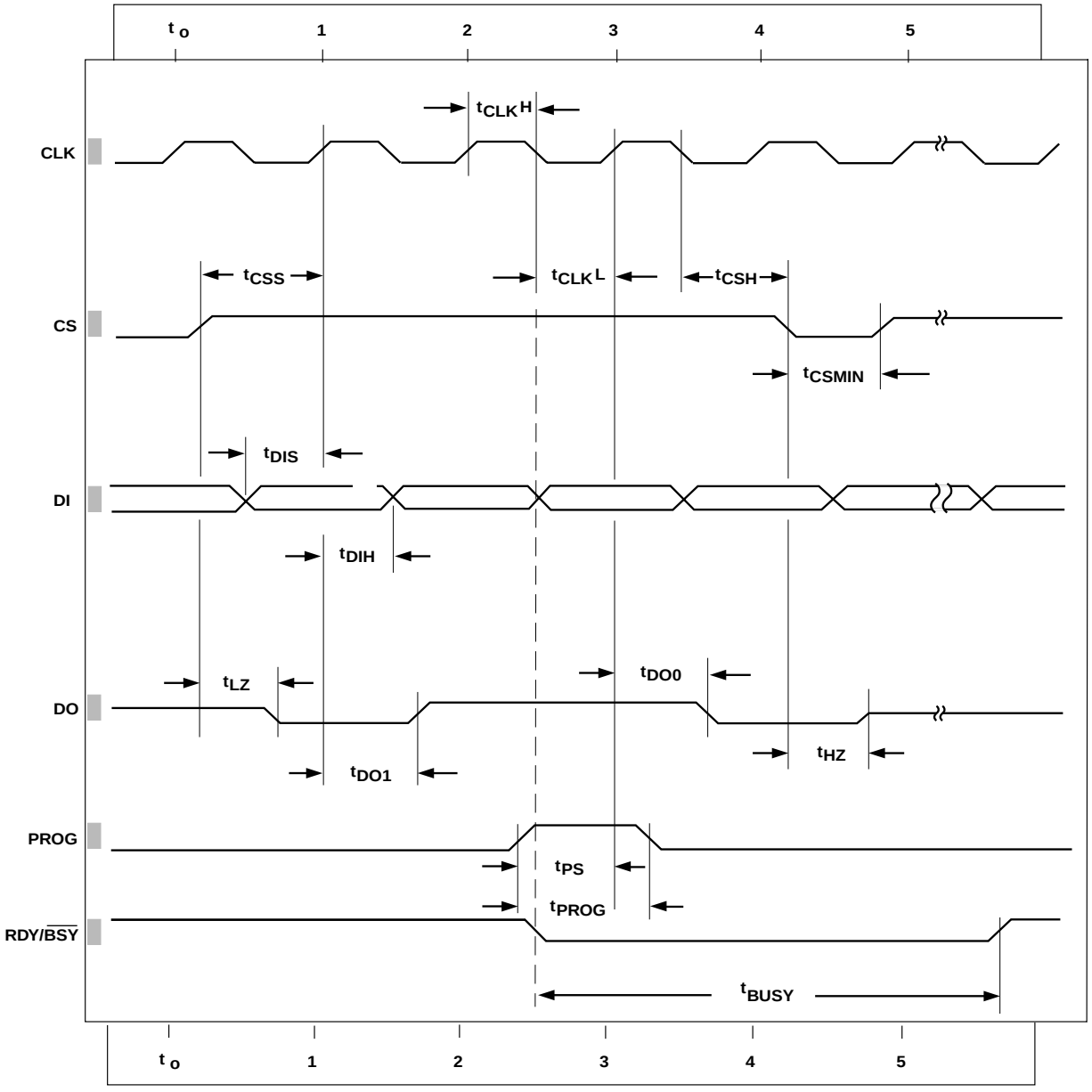
AC ELECTRICAL CHARACTERISTICS:

V_{DD} = +2.7V to +5.5V, $V_{REF}H = V_{DD}$, $V_{REF}L$ = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Digital						
t_{CSMIN}	Minimum CS Low Time		150	—	—	ns
t_{CSS}	CS Setup Time		100	—	—	ns
t_{CSH}	CS Hold Time	C_L=100pF, see note 1	0	—	—	ns
t_{DIS}	DI Setup Time		50	—	—	ns
t_{DIH}	DI Hold Time		50	—	—	ns
t_{DO1}	Output Delay to 1		—	—	150	ns
t_{DO0}	Output Delay to 0		—	—	150	ns
t_{HZ}	Output Delay to High-Z		—	400	—	ns
t_{LZ}	Output Delay to Low-Z		—	400	—	ns
t_{BUSY}	Erase/Write Cycle Time		—	4	5	ms
t_{PS}	PROG Setup Time		150	—	—	ns
t_{PROG}	Minimum Pulse Width		700	—	—	ns
$t_{CLK}H$	Minimum CLK High Time		500	—	—	ns
$t_{CLK}L$	Minimum CLK Low Time		300	—	—	ns
f_C	Clock Frequency		DC	—	1	MHz
Analog						
t_{DS}	DPP Settling Time to 1 LSB	C_{LOAD} = 10 pF, V_{DD} = +5V	—	3	10	µs
		C_{LOAD} = 10 pF, V_{DD} = +3V	—	6	10	µs

NOTES: 1. All timing measurements are defined at the point of signal crossing V_{DD} / 2.
2. These parameters are periodically sampled and are not 100% tested.

A. C. TIMING DIAGRAM



PIN DESCRIPTION

Pin	Name	Function
1	V_{DD}	Power supply positive
2	CLK	Clock input pin
3	RDY/$\overline{BSY}$	Ready/Busy output
4	CS	Chip select
5	DI	Serial data input pin
6	DO	Serial data output pin
7	PROG	EEPROM Programming Enable Input
8	GND	Power supply ground
9	V_{REFL}	Minimum DAC output voltage
10	NC	No Connect
11	NC	No Connect
12	V_{OUT}	DPP output
13	NC	No Connect
14	V_{REFH}	Maximum DPP 1 output voltage

DPP addressing is as follows:

DPP OUTPUT	A0	A1
V_{OUT}	1	0

DEVICE OPERATION

The CAT521 is a single 8-bit configured digitally programmable potentiometer (DPP™) whose output can be programmed to any one of 256 individual voltage steps. Once programmed, the output setting is retained in non-volatile memory and will not be lost when power is removed from the chip. Upon power up the DPP returns to the setting stored in non-volatile memory. The DPP can be written to and read from without effecting the output voltage during the read or write cycle. The output can also be adjusted without altering the stored output setting, which is useful for testing new output settings before storing them in memory.

DIGITAL INTERFACE

The CAT521 employs a 3 wire, Microwire-like serial control interface consisting of Clock (CLK), Chip Select (CS) and Data In (DI) inputs. For all operations, address and data are shifted in LSB first. In addition, all digital data must be preceded by a logic “1” as a start bit. The DPP address and data are clocked into the DI pin on the clock’s rising edge. When sending multiple blocks of information a minimum of two clock cycles is required between the last block sent and the next start bit.

Multiple devices may share a common input data line by selectively activating the CS control of the desired IC. Data Outputs (DO) can also share a common line because the DO pin is Tri-Stated and returns to a high impedance when not in use.

CHIP SELECT

Chip Select (CS) enables and disables the CAT521’s read and write operations. When CS is high data may be read to or from the chip, and the Data Output (DO) pin is active. Data loaded into the DPP control register will remain in effect until CS goes low. Bringing CS to a logic low returns all DPP outputs to the settings stored in non-volatile memory and switches DO to its high impedance Tri-State mode.

Because CS functions like a reset the CS pin has been desensitized with a 30 ns to 90 ns filter circuit to prevent noise spikes from causing unwanted resets and the loss of volatile data.

CLOCK

The CAT521 clock controls both data flow in and out of the device and non-volatile memory cell programming. Serial data is shifted into the DI pin and out of the DO pin on the clock’s rising edge. While it is not necessary for the clock to be running between data transfers, the clock must be operating in order to write to non-volatile memory, even though the data being saved may already be resident in the DPP wiper control register.

No clock is necessary upon system power-up. The CAT521 internal power-on reset circuitry loads data from non-volatile memory to the DPP without using the external clock.

As data transfers are edge triggered clean clock transitions are necessary to avoid falsely clocking data into the control register. Standard CMOS and TTL logic families work well in this regard and it is recommended that any mechanical switches used for breadboarding or device evaluation purposes be debounced by a flip-flop or other suitable debouncing circuit.

V_{REF}

V_{REF}, the voltage applied between pins V_{REFH} &V_{REFL}, sets the DPP's Zero to Full Scale output range where V_{REFL} = Zero and V_{REFH} = Full Scale. V_{REF} can span the full power supply range or just a fraction of it. In typical applications V_{REFH} &V_{REFL} are connected across the power supply rails. When using less than the full supply voltage be mindfull of the limits placed on V_{REFH} and V_{REFL} as specified in the References section of DC Electrical Characteristics.

READY/$\overline{\text{BUSY}}$

When saving data to non-volatile memory, the Ready/Busy ouput (RDY/$\overline{\text{BSY}}$) signals the start and duration of the non-volatile erase/write cycle. Upon receiving a command to store data (PROG goes high) RDY/$\overline{\text{BSY}}$ goes low and remains low until the programming cycle is complete. During this time the CAT521 will ignore any data appearing at DI and no data will be output on DO.

RDY/$\overline{\text{BSY}}$ is internally ANDed with a low voltage detector circuit monitoring V_{DD}. If V_{DD} is below the minimum value required for non-volatile programming, RDY/$\overline{\text{BSY}}$ will remain high following the program command indicating a failure to record the desired data in non-volatile memory.

DATA OUTPUT

Data is output serially by the CAT521, LSB first, via the Data Out (DO) pin following the reception of a start bit and two address bits by the Data Input (DI). DO becomes active whenever CS goes high and resumes its high impedance Tri-State mode when CS returns low. Tri-Stating the DO pin allows several 521s to share a single serial data line and simplifies interfacing multiple 521s to a microprocessor.

WRITING TO MEMORY

Programming the CAT521's non-volatile memory is accomplished through the control signals: Chip Select (CS) and Program (PROG). With CS high, a start bit followed by a two bit DPP address and eight data bits are clocked into the DPP wiper control register via the DI pin. Data enters on the clock's rising edge. The DPP output changes to its new setting on the clock cycle following D7, the last data bit.

Programming is accomplished by bringing PROG high sometime after the start bit and at least 150 ns prior to the rising edge of the clock cycle immediately following the D7 bit. Two clock cycles after the D7 bit the DPP wiper control register will be ready to receive the next set of address and data bits. The clock must be kept running throughout the programming cycle. Internal control circuitry takes care of generating and ramping up the programming voltage for data transfer to the non-volatile memory cells. The CAT521 non-volatile memory cells will endure over 1,000,000 write cycles and will retain data for a minimum of 100 years without being refreshed.

READING DATA

Each time data is transferred into the DPP wiper control register currently held data is shifted out via the D0 pin, thus in every data transaction a read cycle occurs. Note, however, that the reading process is destructive. Data must be removed from the register in order to be read. Figure 2 depicts a Read Only cycle in which no change occurs in the DPP's output. This feature allows µPs to poll DPPs for their current setting without disturbing the output voltage but it assumes that the setting being read is also stored in non-volatile memory so that it can be restored at the end of the read cycle. In Figure 2 CS returns low before the 13th clock cycle completes. In doing so the non-volatile memory's setting is reloaded into the DPP wiper control register. Since this value is

Figure 1. Writing to Memory

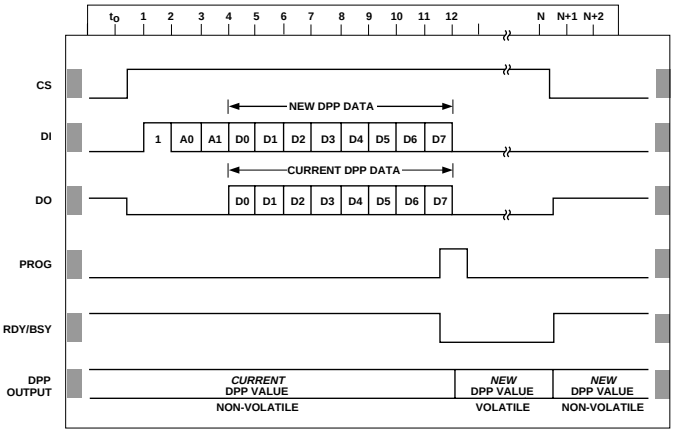
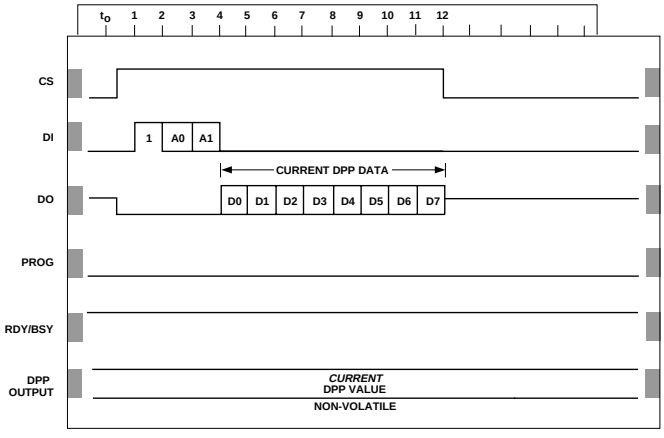


Figure 2. Reading from Memory



the same as that which had been there previously no change in the DPP's output is noticed. Had the value held in the control register been different from that stored in non-volatile memory then *a change would occur* at the read cycle's conclusion.

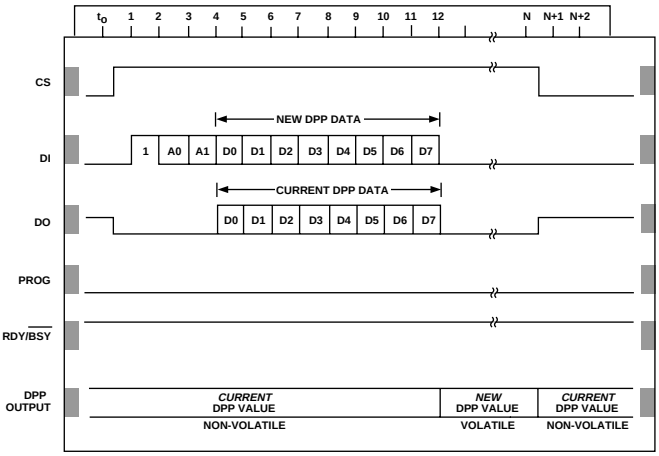
TEMPORARILY CHANGE OUTPUT

The CAT521 allows temporary changes in the DPP's output to be made without disturbing the settings retained in non-volatile memory. This feature is particularly useful when testing for a new output setting and allows for user adjustment of preset or default values without losing the original factory settings.

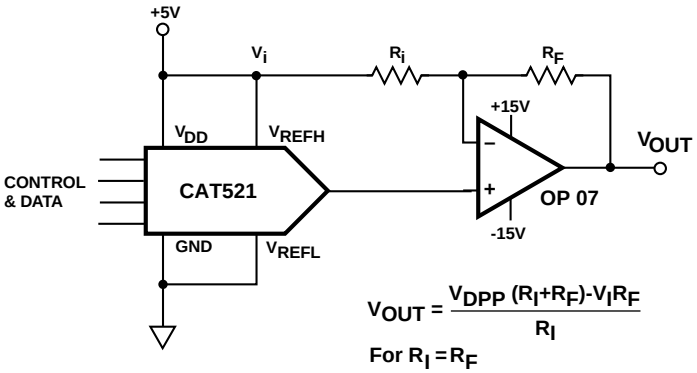
Figure 3 shows the control and data signals needed to effect a temporary output change. DPP settings may be changed as many times as required. The temporary setting remains in effect long as CS remains high. When CS returns low the DPP will return to the output value stored in non-volatile memory.

When it is desired to save a new setting acquired using this feature, the new value must be reloaded into the DPP wiper control register prior to programming. This is because the CAT521's internal control circuitry discards from the programming register the new data two clock cycles after receiving it if no PROG signal is received.

Figure 3. Temporary Change in Output



APPLICATION CIRCUITS



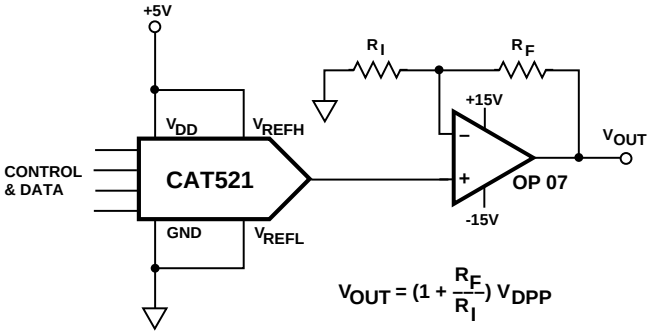
$$V_{OUT} = \frac{V_{DPP}(R_I+R_F)-V_I R_F}{R_I}$$

For $R_I = R_F$

$$V_{OUT} = 2V_{DPP} - V_I$$

DPP INPUT MSB	DPP INPUT LSB	DPP OUTPUT $V_{DPP} = \frac{CODE}{255}(V_{FS} - V_{ZERO}) + V_{ZERO}$; $V_{FS} = 0.99$ V; $V_{ZERO} = 0.01$ V	ANALOG OUTPUT $V_{REF} = 5$V; $R_I = R_F$
1111	1111	$\frac{255}{255}(.98\ V_{REF}) + .01\ V_{REF} = .990\ V_{REF}$	$V_{OUT} = +4.90$V
1000	0000	$\frac{128}{255}(.98\ V_{REF}) + .01\ V_{REF} = .502\ V_{REF}$	$V_{OUT} = +0.02$V
0111	1111	$\frac{127}{255}(.98\ V_{REF}) + .01\ V_{REF} = .498\ V_{REF}$	$V_{OUT} = -0.02$V
0000	0001	$\frac{1}{255}(.98\ V_{REF} + .01\ V_{REF} = .014\ V_{REF}$	$V_{OUT} = -4.86$V
0000	0000	$\frac{0}{255}(.98\ V_{REF}) + .01\ V_{REF} = .010\ V_{REF}$	$V_{OUT} = -4.90$V

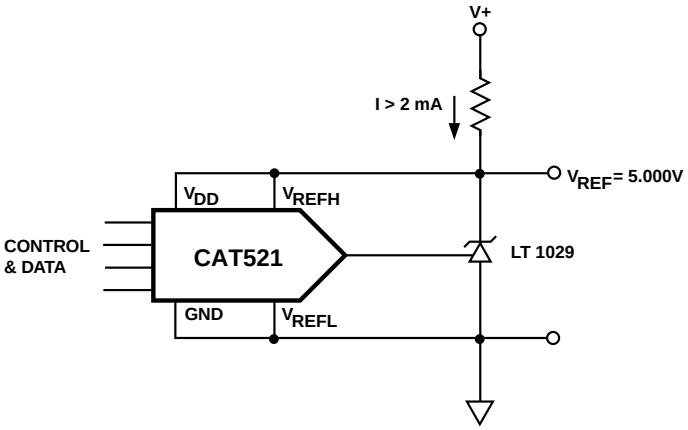
Bipolar DPP Output



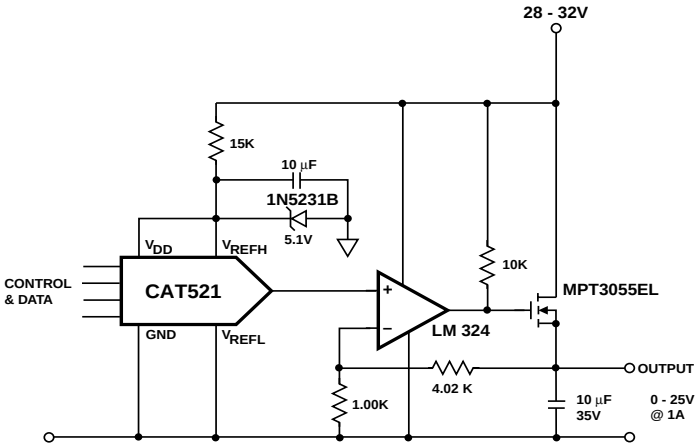
$$V_{OUT} = \left(1 + \frac{R_F}{R_I}\right) V_{DPP}$$

Amplified DPP Output

APPLICATION CIRCUITS (Cont.)

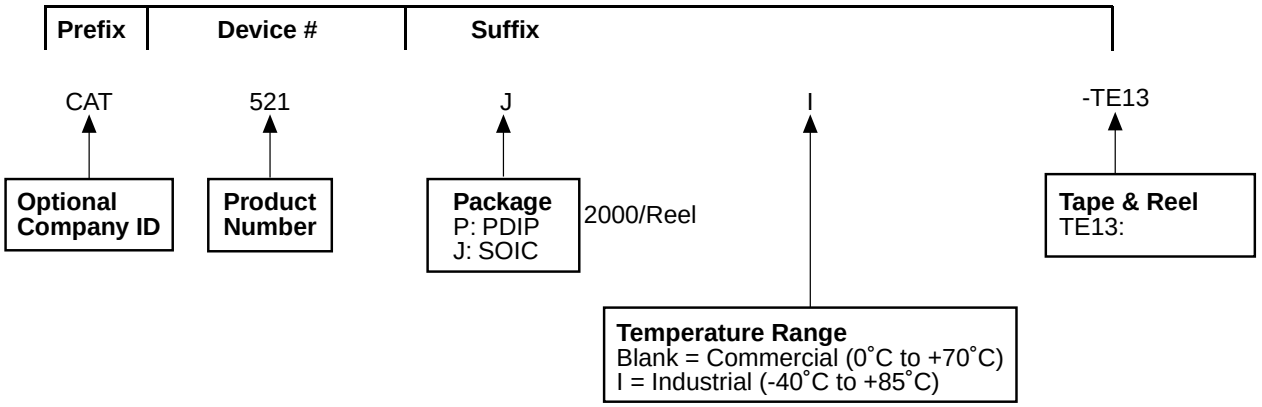


Digitally Trimmed Voltage Reference



Digitally Controlled Voltage Reference

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a CAT521JI-TE13 (SOIC, Industrial Temperature, Tape & Reel)

CATALYST

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CAT522

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FEATURES

- **Two 8-bit DPPs configured as programmable voltage sources in DAC-like applications**
- **Independent reference inputs**
- **Non-volatile NVRAM memory wiper storage**
- **Output voltage range includes both supply rails**
- **2 independently addressable buffered output wipers**
- **1 LSB accuracy, high resolution**
- **Serial Microwire-like interface**
- **Single supply operation: 2.7V - 5.5V**
- **Setting read-back without effecting outputs**

APPLICATIONS

- **Automated product calibration.**
- **Remote control adjustment of equipment**
- **Offset, gain and zero adjustments in self-calibrating and adaptive control systems.**
- **Tamper-proof calibrations.**
- **DAC (with memory) substitute.**

DESCRIPTION

The CAT522 is a dual, 8-bit digitally-programmable potentiometer (DPP™) configured for programmable voltage and DAC-like applications. Intended for final calibration of products such as camcorders, fax machines and cellular telephones on automated high volume production lines, it is also well suited for self-calibrating systems and for applications where equipment which requires periodic adjustment is either difficult to access or in a hazardous environment.

The CAT522 offers two independently programmable DPPs each having its own reference inputs and each capable of rail to rail output swing. The wipers are buffered by rail to rail opamps. Wiper settings, stored in non-volatile NVRAM memory, are not lost when the device is powered down and are automatically reinstated when power is returned. Each wiper can be dithered to test new output values without effecting the stored settings and stored settings can be read back without disturbing the DPP's output.

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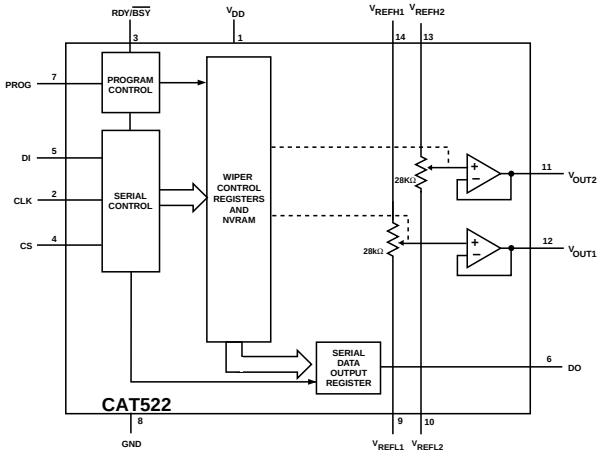
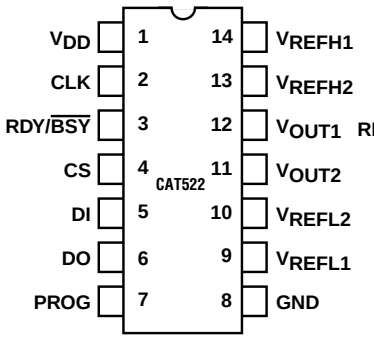
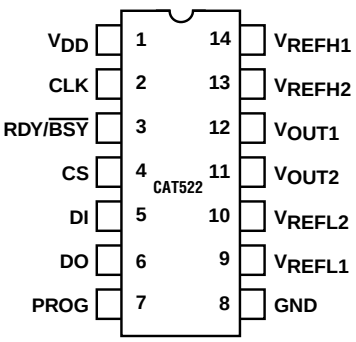


PIN CONFIGURATION

DIP Package (P)



SOIC Package (J)



Doc. No. 2004, Rev. B

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RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Method
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(2)	Latch-Up	100		mA	JEDEC Standard 17

NOTES: 1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} + 1V.

POWER SUPPLY

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD1}	Supply Current (Read)	Normal Operating	—	400	600	µA
I_{DD2}	Supply Current (Write)	Programming, V_{DD} = 5V	—	1600	2500	µA
		V_{DD} = 3V	—	1000	1600	µA
V_{DD}	Operating Voltage Range		2.7	—	5.5	V

LOGIC INPUTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	Input Leakage Current	V_{IN} = V_{DD}	—	—	10	µA
I_{IL}	Input Leakage Current	V_{IN} = 0V	—	—	-10	µA
V_{IH}	High Level Input Voltage		2	—	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	—	0.8	V

LOGIC OUTPUTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High Level Output Voltage	I_{OH} = -40µA	V_{DD} -0.3	—	—	V
V_{IL}	Low Level Output Voltage	I_{OL} = 1 mA, V_{DD} = +5V	—	—	0.4	V
		I_{OL} = 0.4 mA, V_{DD} = +3V	—	—	0.4	V

POTENTIOMETER CHARACTERISTICS

V_{DD} = +2.7V to +5.5V, $V_{REF}H = V_{DD}$, $V_{REF}L$ = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{POT}	Potentiometer Resistance			28		kΩ
	R_{POT} to R_{POT} Match		—	±0.5	±1	%
	Pot Resistance Tolerance				±15	%
	Voltage on V_{REFH} pin		2.7		V_{DD}	V
	Voltage on V_{REFL} pin		OV		V_{DD} - 2.7	V
	Resolution			0.4		%
INL	Integral Linearity Error			0.5	1	LSB
DNL	Differential Linearity Error			0.25	0.5	LSB
R_{OUT}	Buffer Output Resistance				10	Ω
I_{OUT}	Buffer Output Current				3	mA
TC_{RPOT}	TC of Pot Resistance			300		ppm/°C
TC_{RATIO}	Ratiometric TC					ppm/°C
R_{ISO}	Isolation Resistance					Ω
V_N	Noise					nV/√Hz
C_H/C_L	Potentiometer Capacitances			8/8		pF
fc	Frequency Response	Passive Attenuator				MHz

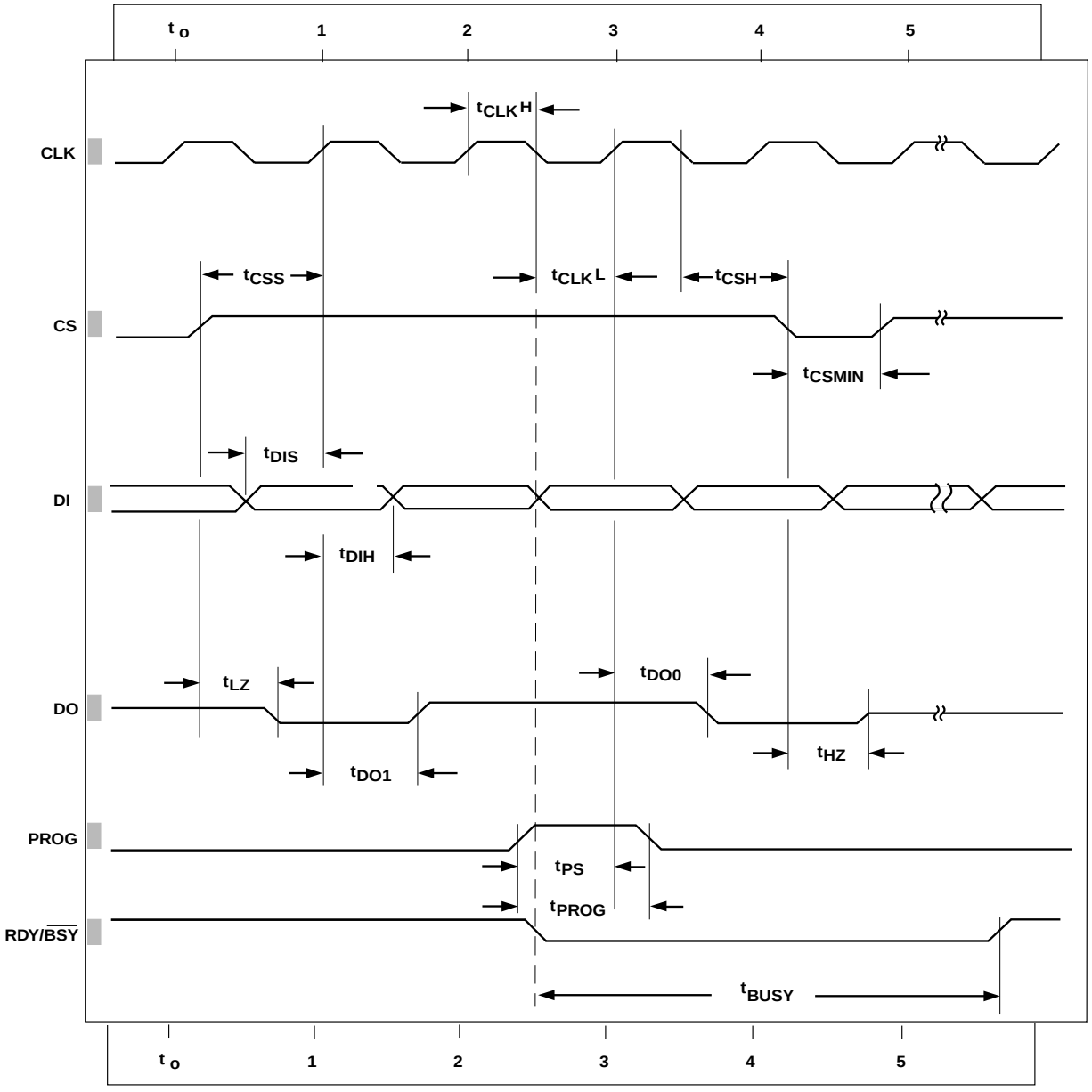
AC ELECTRICAL CHARACTERISTICS:

V_{DD} = +2.7V to +5.5V, $V_{REF}H = V_{DD}$, $V_{REF}L$ = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Digital						
t_{CSMIN}	Minimum CS Low Time		150	—	—	ns
t_{CSS}	CS Setup Time		100	—	—	ns
t_{CSH}	CS Hold Time	C_L=100pF, see note 1	0	—	—	ns
t_{DIS}	DI Setup Time		50	—	—	ns
t_{DIH}	DI Hold Time		50	—	—	ns
t_{DO1}	Output Delay to 1		—	—	150	ns
t_{DO0}	Output Delay to 0		—	—	150	ns
t_{HZ}	Output Delay to High-Z		—	400	—	ns
t_{LZ}	Output Delay to Low-Z		—	400	—	ns
t_{BUSY}	Erase/Write Cycle Time		—	4	5	ms
t_{PS}	PROG Setup Time		150	—	—	ns
t_{PROG}	Minimum Pulse Width		700	—	—	ns
$t_{CLK}H$	Minimum CLK High Time		500	—	—	ns
$t_{CLK}L$	Minimum CLK Low Time		300	—	—	ns
f_C	Clock Frequency		DC	—	1	MHz
Analog						
t_{DS}	DPP Settling Time to 1 LSB	C_{LOAD} = 10 pF, V_{DD} = +5V	—	3	10	µs
		C_{LOAD} = 10 pF, V_{DD} = +3V	—	6	10	µs

NOTES: 1. All timing measurements are defined at the point of signal crossing V_{DD} / 2.
2. These parameters are periodically sampled and are not 100% tested.

A. C. TIMING DIAGRAM



PIN DESCRIPTION

Pin	Name	Function
1	V_{DD}	Power supply positive
2	CLK	Clock input pin
3	RDY/$\overline{BSY}$	Ready/Busy output
4	CS	Chip select
5	DI	Serial data input pin
6	DO	Serial data output pin
7	PROG	EEPROM Programming Enable Input
8	GND	Power supply ground
9	V_{REFL1}	Minimum DPP 1 output voltage
10	V_{REFL2}	Minimum DPP 2 output voltage
11	V_{OUT2}	DPP 2 output
12	V_{OUT1}	DPP 1 output
13	V_{REFH2}	Maximum DPP 2 output voltage
14	V_{REFH1}	Maximum DPP 1 output voltage

DPP addressing is as follows:

DPP OUTPUT	A0	A1
V_{OUT1}	0	1
V_{OUT2}	1	1

DEVICE OPERATION

The CAT522 is a dual 8-bit configured digitally programmable potentiometer (DPP) whose outputs can be programmed to any one of 256 individual voltage steps. Once programmed, these output settings are retained in non-volatile memory and will not be lost when power is removed from the chip. Upon power up the DPPs return to the settings stored in non-volatile memory. Each DPP can be written to and read from independently without effecting the output voltage during the read or write cycle. Each output can also be adjusted without altering the stored output setting, which is useful for testing new output settings before storing them in memory.

DIGITAL INTERFACE

The CAT522 employs a 3 wire serial, Microwire-like control interface consisting of Clock (CLK), Chip Select (CS) and Data In (DI) inputs. For all operations, address and data are shifted in LSB first. In addition, all digital data must be preceded by a logic “1” as a start bit. The DPP address and data are clocked into the DI pin on the clock’s rising edge. When sending multiple blocks of information a minimum of two clock cycles is required between the last block sent and the next start bit.

Multiple devices may share a common input data line by selectively activating the CS control of the desired IC. Data Outputs (DO) can also share a common line because the DO pin is Tri-Stated and returns to a high impedance when not in use.

CHIP SELECT

Chip Select (CS) enables and disables the CAT522’s read and write operations. When CS is high data may be read to or from the chip, and the Data Output (DO) pin is active. Data loaded into the DPP control registers will remain in effect until CS goes low. Bringing CS to a logic low returns all DPP outputs to the settings stored in non-volatile memory and switches DO to its high impedance Tri-State mode.

Because CS functions like a reset the CS pin has been desensitized with a 30 ns to 90 ns filter circuit to prevent noise spikes from causing unwanted resets and the loss of volatile data.

CLOCK

The CAT522’s clock controls both data flow in and out of the IC and non-volatile memory cell programming. Serial data is shifted into the DI pin and out of the DO pin on the clock’s rising edge. While it is not necessary for the clock to be running between data transfers, the clock must be operating in order to write to non-volatile memory, even though the data being saved may already be resident in the DPP wiper control register.

No clock is necessary upon system power-up. The CAT522’s internal power-on reset circuitry loads data from non-volatile memory to the DPPs without using the external clock.

As data transfers are edge triggered clean clock transitions are necessary to avoid falsely clocking data into the control registers. Standard CMOS and TTL logic families work well in this regard and it is recommended that any mechanical switches used for breadboarding or device evaluation purposes be debounced by a flip-flop or other suitable debouncing circuit.

V_{REF}

V_{REF}, the voltage applied between pins V_{REFH} &V_{REFL}, sets the configured DPP's Zero to Full Scale output range where V_{REFL} = Zero and V_{REFH} = Full Scale. V_{REF} can span the full power supply range or just a fraction of it. In typical applications V_{REFH} &V_{REFL} are connected across the power supply rails. When using less than the full supply voltage be mindful of the limits placed on V_{REFL} and V_{REFL} as specified in the References section of DC Electrical Characteristics.

READY/$\overline{\text{BUSY}}$

When saving data to non-volatile memory, the Ready/Busy ouput (RDY/$\overline{\text{BSY}}$) signals the start and duration of the non-volatile erase/write cycle. Upon receiving a command to store data (PROG goes high) RDY/$\overline{\text{BSY}}$ goes low and remains low until the programming cycle is complete. During this time the CAT522 will ignore any data appearing at DI and no data will be output on DO.

RDY/$\overline{\text{BSY}}$ is internally ANDed with a low voltage detector circuit monitoring V_{DD}. If V_{DD} is below the minimum value required for non-volatile programming, RDY/$\overline{\text{BSY}}$ will remain high following the program command indicating a failure to record the desired data in non-volatile memory.

DATA OUTPUT

Data is output serially by the CAT522, LSB first, via the Data Out (DO) pin following the reception of a start bit and two address bits by the Data Input (DI). DO becomes active whenever CS goes high and resumes its high impedance Tri-State mode when CS returns low. Tri-Stating the DO pin allows several 522s to share a single serial data line and simplifies interfacing multiple 522s to a microprocessor.

WRITING TO MEMORY

Programming the CAT522's non-volatile memory is accomplished through the control signals: Chip Select (CS) and Program (PROG). With CS high, a start bit followed by a two bit DPP address and eight data bits are clocked into the DPP wiper control register via the DI pin. Data enters on the clock's rising edge. The DPP output changes to its new setting on the clock cycle following D7, the last data bit.

Programming is accomplished by bringing PROG high sometime after the start bit and at least 150 ns prior to the rising edge of the clock cycle immediately following the D7 bit. Two clock cycles after the D7 bit the DPP wiper control register will be ready to receive the next set of address and data bits. The clock must be kept running throughout the programming cycle. Internal control circuitry takes care of generating and ramping up the programming voltage for data transfer to the non-volatile cells. The CAT522's non-volatile memory cells will endure over 1,000,000 write cycles and will retain data for a minimum of 100 years without being refreshed.

READING DATA

Each time data is transferred into a DPP control register currently held data is shifted out via the D0 pin, thus in every data transaction a read cycle occurs. Note, however, that the reading process is destructive. Data must be removed from the register in order to be read. Figure 2 depicts a Read Only cycle in which no change occurs in the DPP's output. This feature allows µPs to poll DPPs for their current setting without disturbing the output voltage but it assumes that the setting being read is also stored in non-volatile memory so that it can be restored at the end of the read cycle. In Figure 2 CS returns low before the 13th clock cycle completes. In doing so the non-volatile memory setting is reloaded into the DPP wiper control register. Since this value is the

Figure 1. Writing to Memory

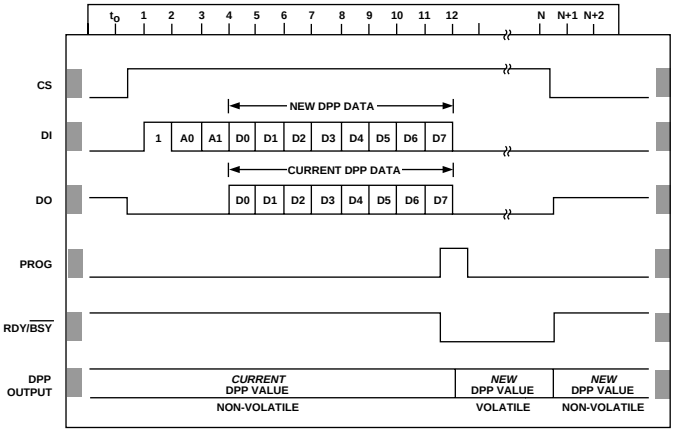
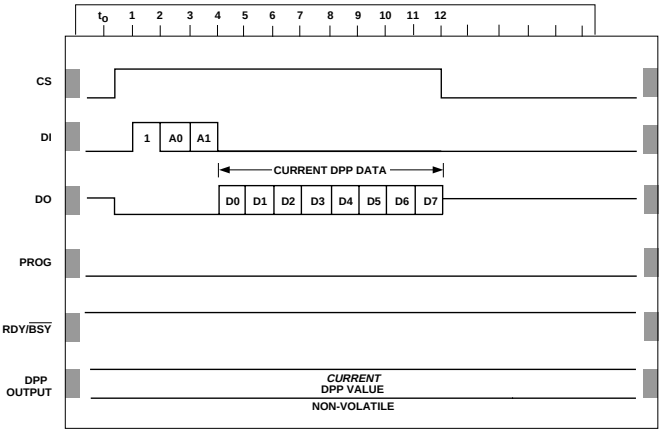


Figure 2. Reading from Memory



same as that which had been there previously no change in the DPP's output is noticed. Had the value held in the control register been different from that stored in non-volatile memory then *a change would occur* at the read cycle's conclusion.

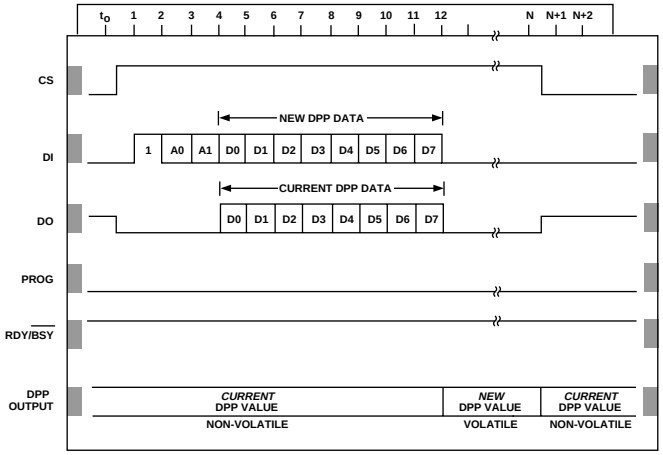
TEMPORARILY CHANGE OUTPUT

The CAT522 allows temporary changes in DPP's output to be made without disturbing the settings retained in non-volatile memory. This feature is particularly useful when testing for a new output setting and allows for user adjustment of preset or default values without losing the original factory settings.

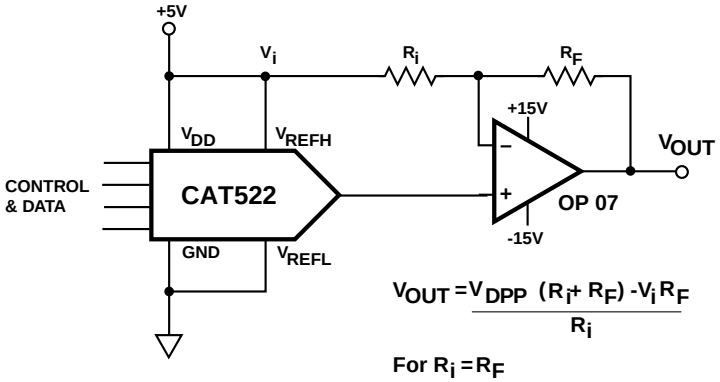
Figure 3 shows the control and data signals needed to effect a temporary output change. DPP wiper settings may be changed as many times as required and can be made to any of the two DPPs in any order or sequence. The temporary setting(s) remain in effect long as CS remains high. When CS returns low all two DPPs will return to the output values stored in non-volatile memory.

When it is desired to save a new setting acquired using this feature, the new value must be reloaded into the DPP wiper control register prior to programming. This is because the CAT522's internal control circuitry discards from the programming register the new data two clock cycles after receiving it if no PROG signal is received.

Figure 3. Temporary Change in Output



APPLICATION CIRCUITS



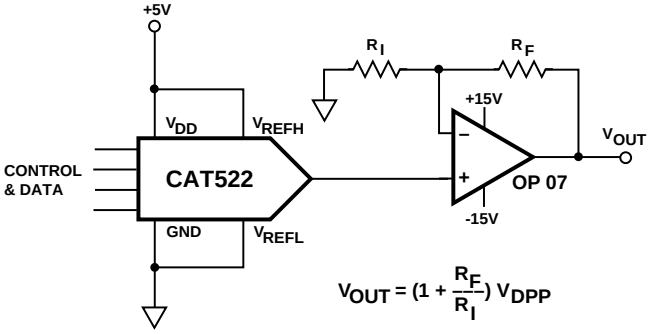
$$V_{OUT} = \frac{V_{DPP}\,(R_i + R_F) - V_i R_F}{R_i}$$

For $R_i = R_F$

$$V_{OUT} = 2V_{DPP} - V_i$$

DPP INPUT MSB	DPP INPUT LSB	DPP OUTPUT $V_{DPP} = \frac{CODE}{255}(V_{FS} - V_{ZERO}) + V_{ZERO}$; $V_{FS} = 0.99\,V_{REF}$; $V_{ZERO} = 0.01\,V_{REF}$	ANALOG OUTPUT $V_{REF} = 5V$, $R_I = R_F$
1111	1111	$\frac{255}{255}(.98\,V_{REF}) + .01\,V_{REF} = .990\,V_{REF}$	$V_{OUT} = +4.90V$
1000	0000	$\frac{128}{255}(.98\,V_{REF}) + .01\,V_{REF} = .502\,V_{REF}$	$V_{OUT} = +0.02V$
0111	1111	$\frac{127}{255}(.98\,V_{REF}) + .01\,V_{REF} = .498\,V_{REF}$	$V_{OUT} = -0.02V$
0000	0001	$\frac{1}{255}(.98\,V_{REF}) + .01\,V_{REF} = .014\,V_{REF}$	$V_{OUT} = -4.86V$
0000	0000	$\frac{0}{255}(.98\,V_{REF}) + .01\,V_{REF} = .010\,V_{REF}$	$V_{OUT} = -4.90V$

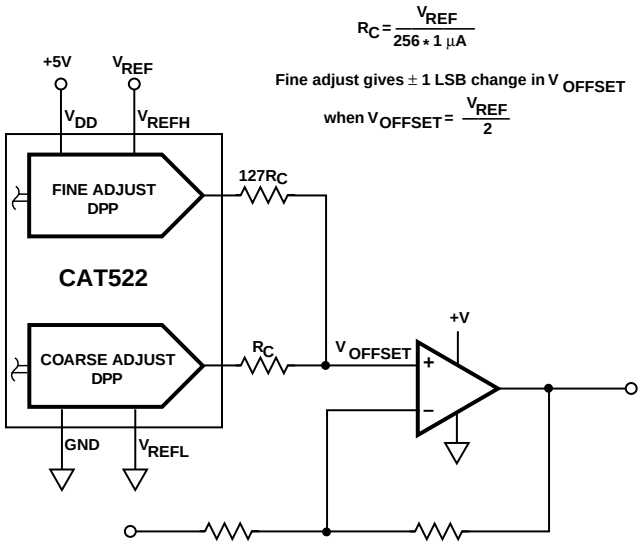
Bipolar DPP Output



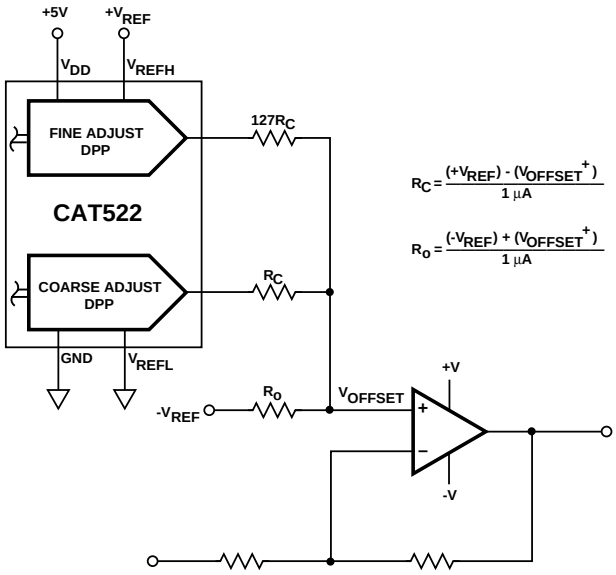
$$V_{OUT} = \left(1 + \frac{R_F}{R_I}\right) V_{DPP}$$

Amplified DPP Output

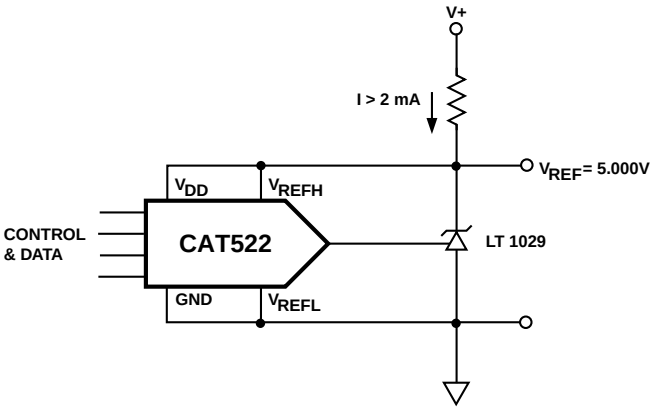
APPLICATION CIRCUITS (Cont.)



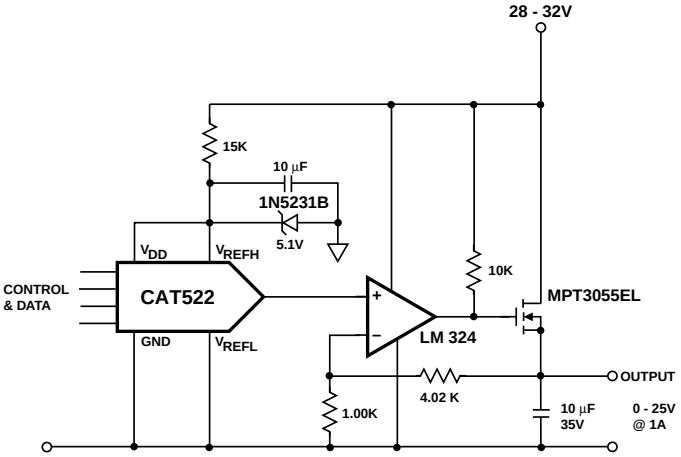
Coarse-Fine Offset Control by Averaging DPP Outputs for Single Power Supply Systems



Coarse-Fine Offset Control by Averaging DPP Outputs for Dual Power Supply Systems

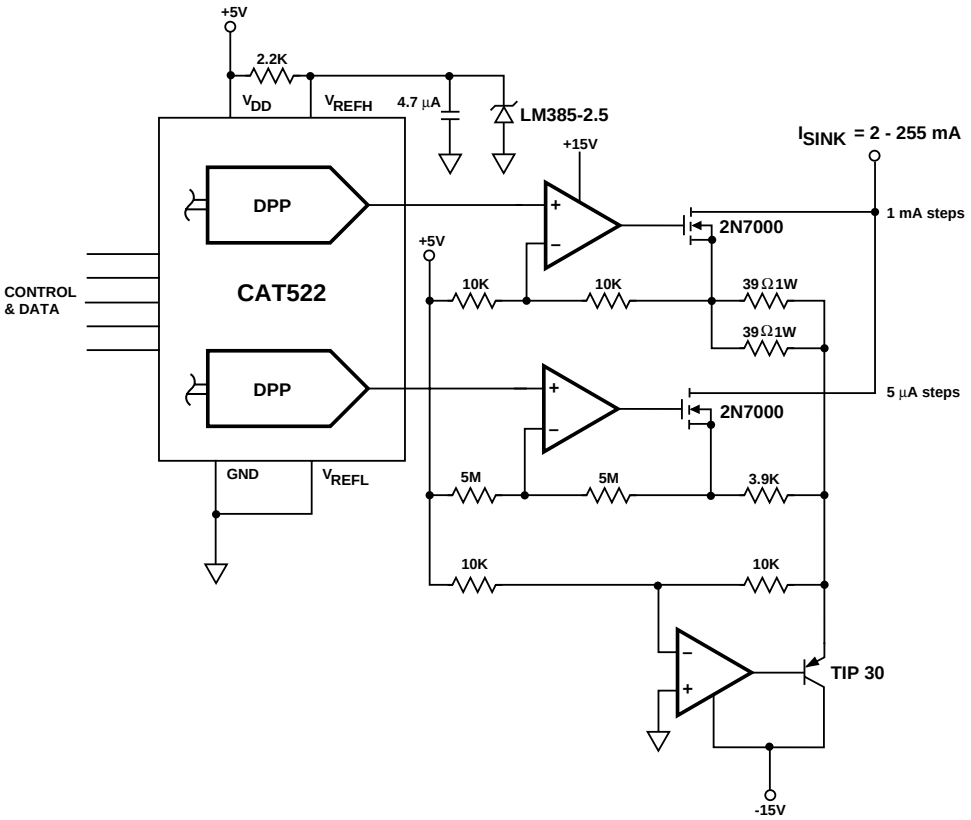


Digitally Trimmed Voltage Reference

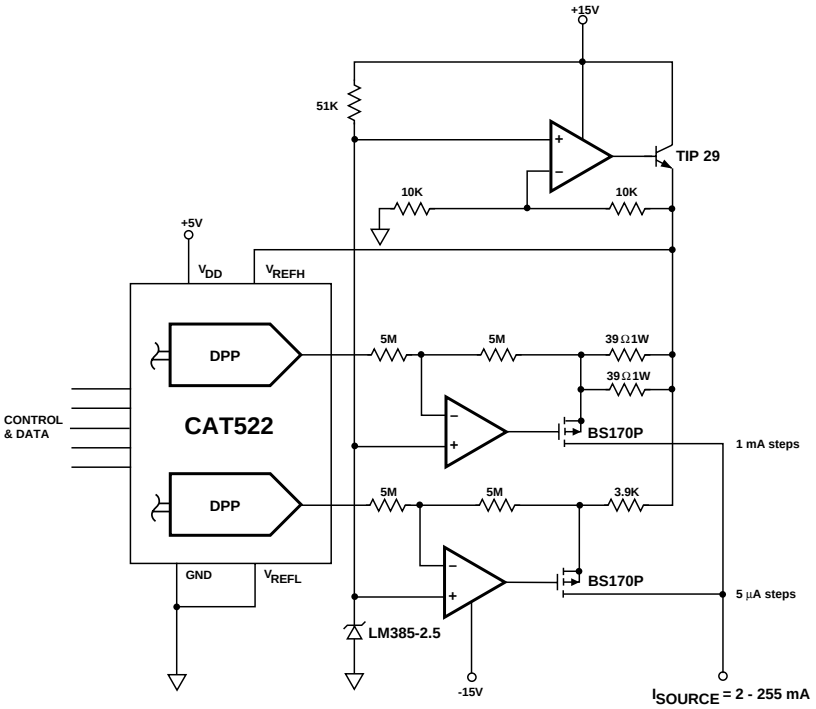


Digitally Controlled Voltage Reference

APPLICATION CIRCUITS (Cont.)

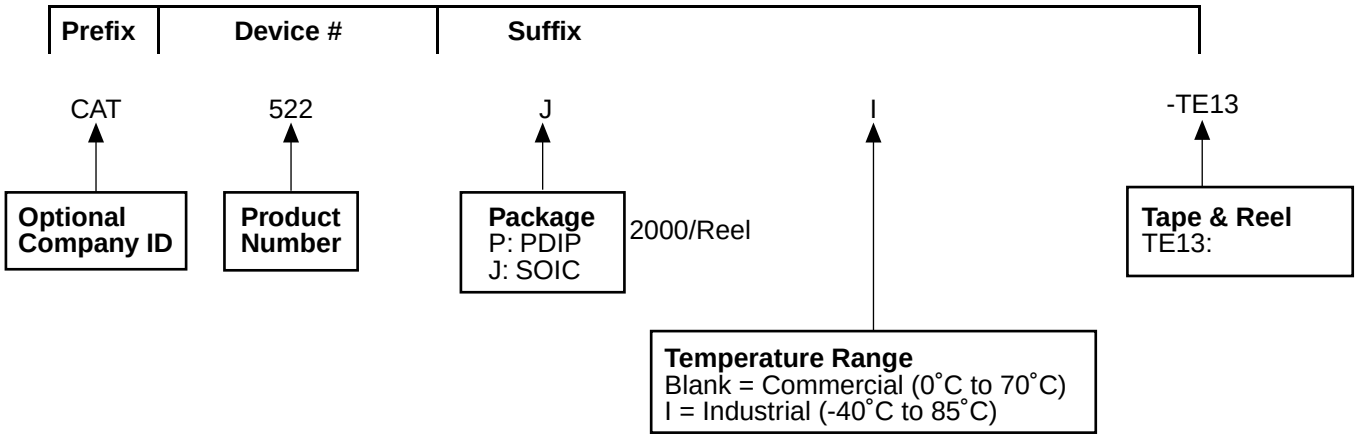


Current Sink with 4 Decades of Resolution



Current Source with 4 Decades of Resolution

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a CAT522JI-TE13 (SOIC, Industrial Temperature, Tape & Reel)

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Publication #: 2004
Revison: B
Issue date: 03/21/02
Type: Final

CAT523

Configured Digitally Programmable Potentiometer (DPP™): Programmable Voltage Applications

FEATURES

- **Two 8-bit DPPs configured as programmable voltage sources in DAC-like applications**
- **Common reference inputs**
- **Non-volatile NVRAM memory wiper storage**
- **Output voltage range includes both supply rails**
- **2 independently addressable buffered output wipers**
- **1 LSB accuracy, high resolution**
- **Serial microwire-like interface**
- **Single supply operation: 2.7V - 5.5V**
- **Setting read-back without effecting outputs**

APPLICATIONS

- **Automated product calibration.**
- **Remote control adjustment of equipment**
- **Offset, gain and zero adjustments in self-calibrating and adaptive control systems.**
- **Tamper-proof calibrations.**
- **DAC (with memory) substitute**

DESCRIPTION

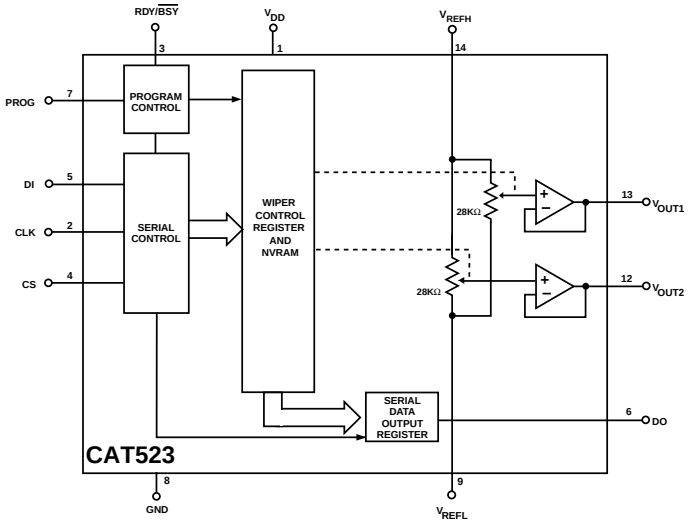
The CAT523 is a dual, 8-bit digitally-programmable potentiometer (DPP™) configured for programmable voltage and DAC-like applications. Intended for final calibration of products such as camcorders, fax machines and cellular telephones on automated high volume production lines, it is also well suited for systems capable of self calibration, and applications where equipment which is either difficult to access or in a hazardous environment, requires periodic adjustment.

The two independently programmable DPPs have a common output voltage range which includes both supply rails. The wipers are buffered by rail to rail op amps. Wiper settings, stored in non-volatile NVRAM memory, are not lost when the device is powered down and are automatically reinstated when power is returned. Each wiper can be dithered to test new output values without effecting the stored settings and stored settings can be read back without disturbing the DPP's output.

Control of the CAT523 is accomplished with a simple 3-wire, Microwire-like serial interface. A Chip Select pin allows several CAT523's to share a common serial interface and communication back to the host controller is via a single serial data line thanks to the CAT523's Tri-Stated Data Output pin. A RDY/$\overline{BSY}$ output working in concert with an internal low voltage detector signals proper operation of non-volatile NVRAM memory Erase/Write cycle.

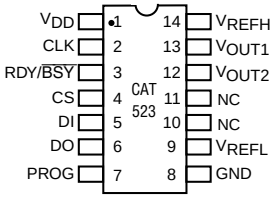
The CAT523 is available in the 0°C to 70°C Commercial and -40°C to + 85°C Industrial operating temperature ranges and offered in 14-pin plastic DIP and SOIC mount packages.

FUNCTIONAL DIAGRAM

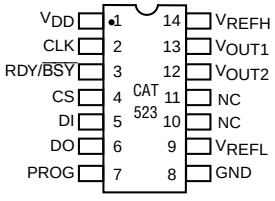


PIN CONFIGURATION

DIP Package (P)



SOIC Package (J)



Doc. No. 2005, Rev. B

ABSOLUTE MAXIMUM RATINGS

Supply Voltage*	
V_{DD} to GND	-0.5V to +7V
Inputs	
CLK to GND	-0.5V to V_{DD} +0.5V
CS to GND	-0.5V to V_{DD} +0.5V
DI to GND	-0.5V to V_{DD} +0.5V
RDY/BSY to GND	-0.5V to V_{DD} +0.5V
PROG to GND	-0.5V to V_{DD} +0.5V
V_{REF}H to GND	-0.5V to V_{DD} +0.5V
V_{REF}L to GND	-0.5V to V_{DD} +0.5V
Outputs	
D_0 to GND	-0.5V to V_{DD} +0.5V
V_{OUT} 1– 4 to GND	-0.5V to V_{DD} +0.5V
Operating Ambient Temperature	
Commercial ('C' or Blank suffix)	0°C to +70°C
Industrial ('I' suffix)	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Soldering (10 sec max)	+300°C

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Absolute Maximum Ratings are limited values applied individually while other parameters are within specified operating conditions, and functional operation at any of these conditions is NOT implied. Device performance and reliability may be impaired by exposure to absolute rating conditions for extended periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Method
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(2)	Latch-Up	100		mA	JEDEC Standard 17

NOTES: 1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} + 1V.

POWER SUPPLY

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD1}	Supply Current (Read)	Normal Operating	—	400	600	µA
I_{DD2}	Supply Current (Write)	Programming, V_{DD} = 5V	—	1600	2500	µA
		V_{DD} = 3V	—	1000	1600	µA
V_{DD}	Operating Voltage Range		2.7	—	5.5	V

LOGIC INPUTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	Input Leakage Current	V_{IN} = V_{DD}	—	—	10	µA
I_{IL}	Input Leakage Current	V_{IN} = 0V	—	—	-10	µA
V_{IH}	High Level Input Voltage		2	—	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	—	0.8	V

LOGIC OUTPUTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High Level Output Voltage	I_{OH} = -40µA	V_{DD} -0.3	—	—	V
V_{IL}	Low Level Output Voltage	I_{OL} = 1 mA, V_{DD} = +5V	—	—	0.4	V
		I_{OL} = 0.4 mA, V_{DD} = +3V	—	—	0.4	V

POTENTIOMETER CHARACTERISTICS

V_{DD} = +2.7V to +5.5V, $V_{REF}H = V_{DD}$, $V_{REF}L$ = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{POT}	Potentiometer Resistance			28		kΩ
	R_{POT} to R_{POT} Match		—	±0.5	±1	%
	Pot Resistance Tolerance				±15	%
	Voltage on V_{REFH} pin		2.7		V_{DD}	V
	Voltage on V_{REFL} pin		OV		V_{DD} - 2.7	V
	Resolution			0.4		%
INL	Integral Linearity Error			0.5	1	LSB
DNL	Differential Linearity Error			0.25	0.5	LSB
R_{OUT}	Buffer Output Resistance				10	Ω
I_{OUT}	Buffer Output Current				3	mA
TC_{RPOT}	TC of Pot Resistance			300		ppm/°C
TC_{RATIO}	Ratiometric TC					ppm/°C
R_{ISO}	Isolation Resistance					Ω
V_N	Noise					nV/√Hz
C_H/C_L	Potentiometer Capacitances			8/8		pF
fc	Frequency Response	Passive Attenuator				MHz

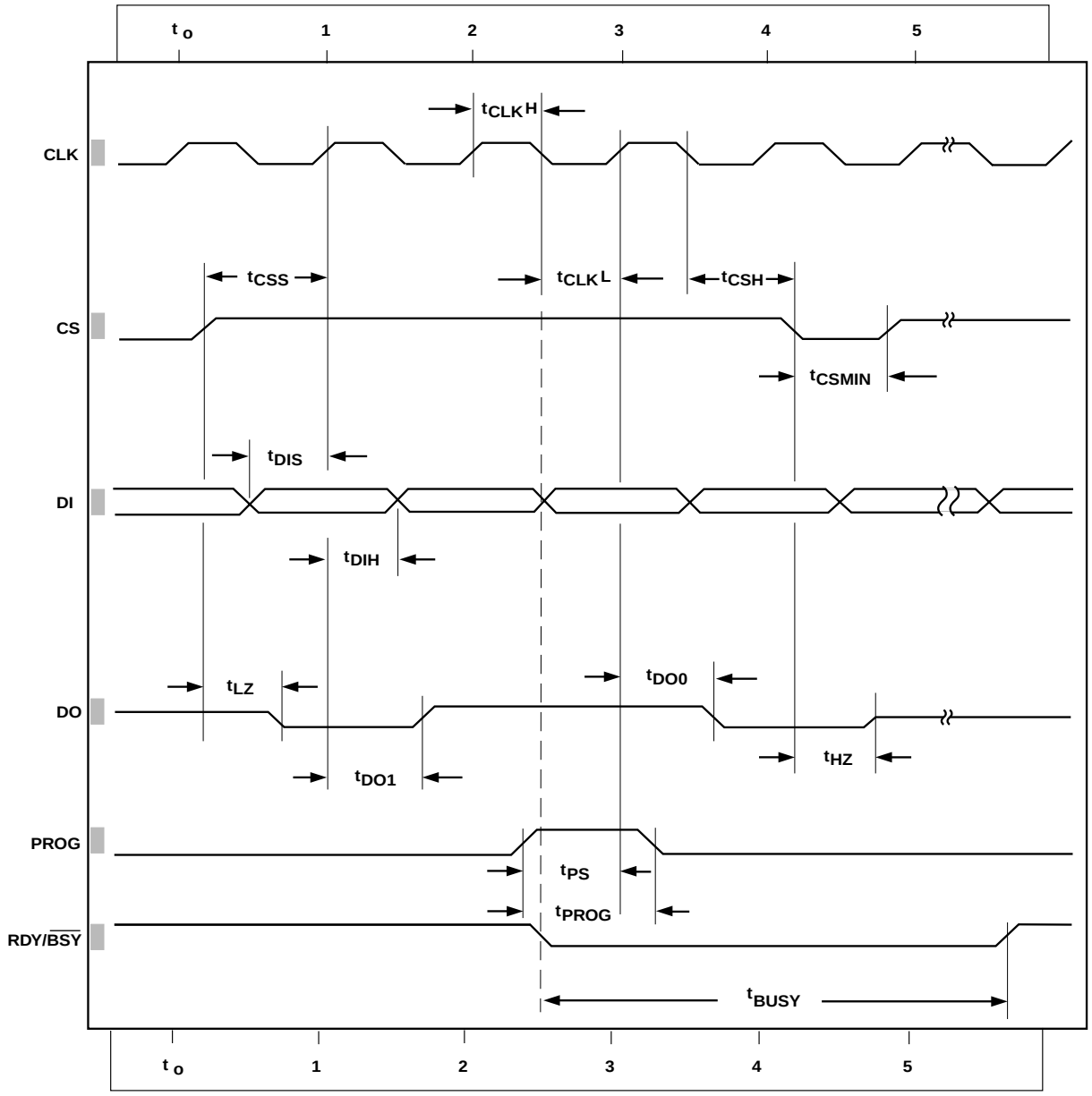
AC ELECTRICAL CHARACTERISTICS:

V_{DD} = +2.7V to +5.5V, $V_{REF}H = V_{DD}$, $V_{REF}L$ = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Digital						
t_{CSMIN}	Minimum CS Low Time		150	—	—	ns
t_{CSS}	CS Setup Time		100	—	—	ns
t_{CSH}	CS Hold Time	C_L=100pF, see note 1	0	—	—	ns
t_{DIS}	DI Setup Time		50	—	—	ns
t_{DIH}	DI Hold Time		50	—	—	ns
t_{DO1}	Output Delay to 1		—	—	150	ns
t_{DO0}	Output Delay to 0		—	—	150	ns
t_{HZ}	Output Delay to High-Z		—	400	—	ns
t_{LZ}	Output Delay to Low-Z		—	400	—	ns
t_{BUSY}	Erase/Write Cycle Time		—	4	5	ms
t_{PS}	PROG Setup Time		150	—	—	ns
t_{PROG}	Minimum Pulse Width		700	—	—	ns
$t_{CLK}H$	Minimum CLK High Time		500	—	—	ns
$t_{CLK}L$	Minimum CLK Low Time		300	—	—	ns
f_C	Clock Frequency		DC	—	1	MHz
Analog						
t_{DS}	DPP Settling Time to 1 LSB	C_{LOAD} = 10 pF, V_{DD} = +5V	—	3	10	µs
		C_{LOAD} = 10 pF, V_{DD} = +3V	—	6	10	µs

NOTES: 1. All timing measurements are defined at the point of signal crossing V_{DD} / 2.
2. These parameters are periodically sampled and are not 100% tested.

A. C. TIMING DIAGRAM



PIN DESCRIPTION

Pin	Name	Function
1	V_{DD}	Power supply positive.
2	CLK	Clock input pin.Clock input pin.
3	RDY/$\overline{BSY}$	Ready/Busy Output
4	CS	Chip Select
5	DI	Serial data input pin.
6	DO	Serial data output pin.
7	PROG	EEPROM Programming Enable Input
8	GND	Power supply ground.
9	V_{REFL}	Minimum DPP output voltage.
10	NC	No Connect.
11	NC	No Connect.
12	V_{OUT2}	DPP output channel 2.
13	V_{OUT1}	DPP output channel 1.
14	V_{REFH}	Maximum DPP output voltage.

DPP addressing is as follows:

DPP OUTPUT	A0	A1
V_{OUT1}	0	0
V_{OUT2}	1	0

DEVICE OPERATION

The CAT523 is a dual 8-bit configured digitally programmable potentiometer (DPP) whose outputs can be programmed to any one of 256 individual voltage steps. Once programmed, these output settings are retained in non-volatile memory and will not be lost when power is removed from the chip. Upon power up the DPPs return to the settings stored in non-volatile memory. Each DPP can be written to and read from independently without effecting the output voltage during the read or write cycle. Each output can also be temporarily adjusted without changing the stored output setting, which is useful for testing new output settings before storing them in memory.

DIGITAL INTERFACE

The CAT523 employs a 3 wire, Microwire-like, serial control interface consisting of Clock (CLK), Chip Select (CS) and Data In (DI) inputs. For all operations, address and data are shifted in LSB first. In addition, all digital data must be preceded by a logic “1” as a start bit. The DPP address and data are clocked into the DI pin on the clock’s rising edge. When sending multiple blocks of information a minimum of two clock cycles is required between the last block sent and the next start bit.

Multiple devices may share a common input data line by selectively activating the CS control of the desired IC. Data Outputs (DO) can also share a common line because the DO pin is Tri-Stated and returns to a high impedance when not in use.

CHIP SELECT

Chip Select (CS) enables and disables the CAT523’s read and write operations. When CS is high data may be read to or from the chip, and the Data Output (DO) pin is active. Data loaded into the DPP control registers will remain in effect until CS goes low. Bringing CS to a logic low returns all DPP outputs to the settings stored in non-volatile memory and switches DO to its high impedance Tri-State mode.

Because CS functions like a reset the CS pin has been equipped with a 30 ns to 90 ns filter circuit to prevent noise spikes from causing unwanted resets and the loss of volatile data.

CLOCK

The CAT523’s clock controls both data flow in and out of the IC and non-volatile memory cell programming. Serial data is shifted into the DI pin and out of the DO pin on the clock’s rising edge. While it is not necessary for the clock to be running between data transfers, the clock must be operating in order to write to non-volatile memory, even though the data being saved may already be resident in the DPP wiper control register.

No clock is necessary upon system power-up. The CAT523’s internal power-on reset circuitry loads data from non-volatile memory to the DPPs without using the external clock.

As data transfers are edge triggered clean clock transitions are necessary to avoid falsely clocking data into the control registers. Standard CMOS and TTL logic families work well in this regard and it is recommended that any mechanical switches used for breadboarding or device evaluation purposes be debounced by a flip-flop or other suitable debouncing circuit.

V_{REF}

V_{REF}, the voltage applied between pins V_{REFH} and V_{REFL}, sets the DPP's Zero to Full Scale output range where V_{REFL} = Zero and V_{REFH} = Full Scale. V_{REF} can span the full power supply range or just a fraction of it. In typical applications V_{REFH} and V_{REFL} are connected across the power supply rails. When using less than the full supply voltage V_{REFH} is restricted to voltages between V_{DD} and $V_{DD}/2$ and V_{REFL} to voltages between GND and $V_{DD}/2$.

READY/$\overline{\text{BUSY}}$

When saving data to non-volatile memory, the Ready/Busy output (RDY/$\overline{\text{BSY}}$) signals the start and duration of the non-volatile erase/write cycle. Upon receiving a command to store data (PROG goes high) RDY/$\overline{\text{BSY}}$ goes low and remains low until the programming cycle is complete. During this time the CAT523 will ignore any data appearing at DI and no data will be output on DO.

RDY/$\overline{\text{BSY}}$ is internally ANDed with a low voltage detector circuit monitoring V_{DD}. If V_{DD} is below the minimum value required for non-volatile programming, RDY/$\overline{\text{BSY}}$ will remain high following the program command indicating a failure to record the desired data in non-volatile memory.

DATA OUTPUT

Data is output serially by the CAT523, LSB first, via the Data Out (DO) pin following the reception of a start bit and two address bits by the Data Input (DI). DO becomes active whenever CS goes high and resumes its high impedance Tri-State mode when CS returns low. Tri-Stating the DO pin allows several 523s to share a single serial data line and simplifies interfacing multiple 523s to a microprocessor.

WRITING TO MEMORY

Programming the CAT523's non-volatile memory is accomplished through the control signals: Chip Select (CS) and Program (PROG). With CS high, a start bit followed by a two bit DPP address and eight data bits are clocked into the DPP control register via the DI pin. Data enters on the clock's rising edge. The DPP output changes to its new setting on the clock cycle following D7, the last data bit.

Programming is achieved by bringing PROG high for a minimum of 3 ms. PROG must be brought high sometime after the start bit and at least 150 ns prior to the rising edge of the clock cycle immediately following the D7 bit. Two clock cycles after the D7 bit the DAC control register will be ready to receive the next set of address and data bits. The clock must be kept running throughout the programming cycle. Internal control circuitry takes care of ramping the programming voltage for data transfer to the non-volatile memory cells. The CAT523's non-volatile memory cells will endure over 100,000 write cycles and will retain data for a minimum of 100 years without being refreshed.

READING DATA

Each time data is transferred into a DPP wiper control register currently held data is shifted out via the D0 pin, thus in every data transaction a read cycle occurs. Note, however, that the reading process is destructive. Data must be removed from the register in order to be read. Figure 2 depicts a Read Only cycle in which no change occurs in the DPP's output. This feature allows µPs to poll DPPs for their current setting without disturbing the output voltage but it assumes that the setting being read is also stored in non-volatile memory so that it can be restored at the end of the read cycle. In Figure 2 CS returns low before the 13th clock cycle completes. In doing so the non-volatile memory setting is reloaded into the DPP wiper control register.

Figure 1. Writing to Memory

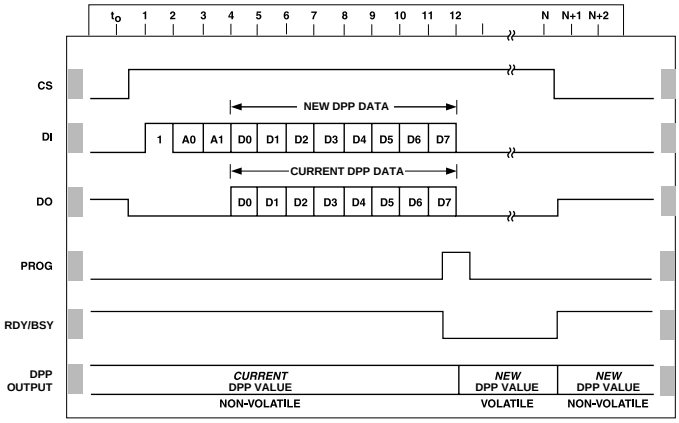
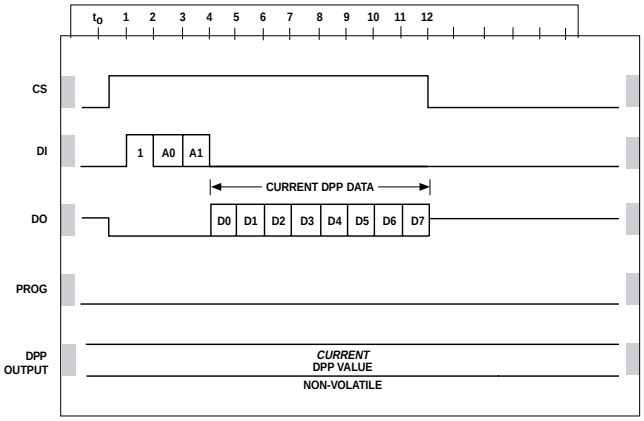


Figure 2. Reading from Memory



Since this value is the same as that which had been there previously no change in the DPP's output is noticed. Had the value held in the control register been different from that stored in non-volatile memory then *a change would occur* at the read cycle's conclusion.

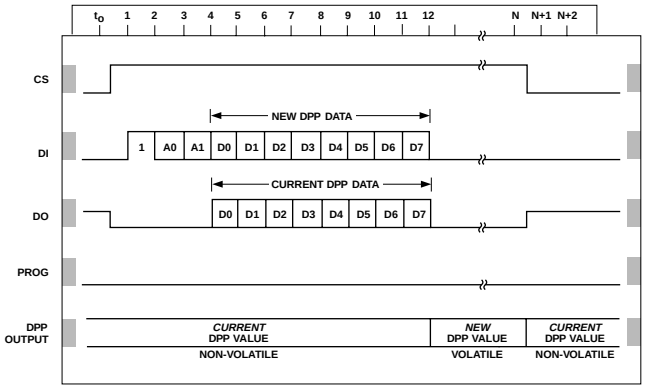
TEMPORARILY CHANGE OUTPUT

The CAT523 allows temporary changes in DPP's output to be made without disturbing the settings retained in non-volatile memory. This feature is particularly useful when testing for a new output setting and allows for user adjustment of preset or default values without losing the original factory settings.

Figure 3 shows the control and data signals needed to effect a temporary output change. DPP wiper settings may be changed as many times as required and can be made to any of the two DPPs in any order or sequence. The temporary setting(s) remain in effect long as CS remains high. When CS returns low all two DPPs will return to the output values stored in non-volatile memory.

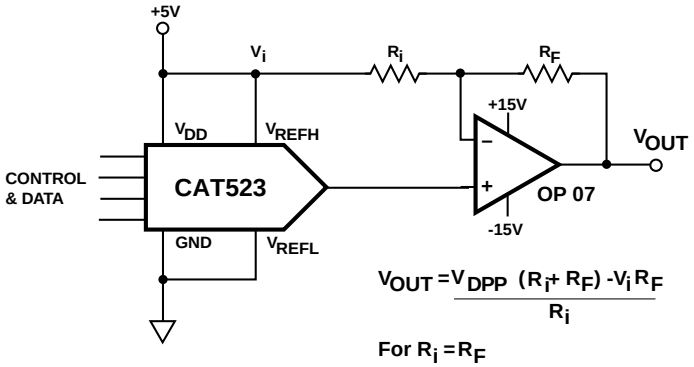
When it is desired to save a new setting acquired using this feature, the new value must be reloaded into the DPP wiper control register prior to programming. This is because the CAT523's internal control circuitry discards the new data from the programming register two clock cycles after receiving it (after reception is complete) if no PROG signal is received.

Figure 3. Temporary Change in Output

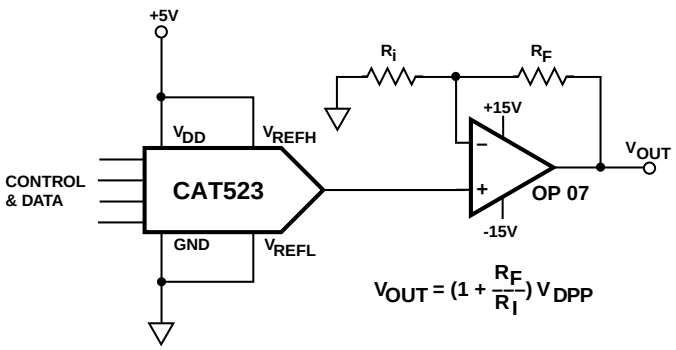


APPLICATION CIRCUITS

DPP INPUT MSB LSB	DPP OUTPUT $V_{DPP} = \frac{CODE}{255}(V_{FS} - V_{ZERO}) + V_{ZERO}$ $V_{FS} = 0.99\,V_{REF}$ $V_{ZERO} = 0.01\,V_{REF}$	ANALOG OUTPUT $V_{REF} = 5V$ $R_I = R_F$
1111 1111	$\frac{255}{255}(.98\,V_{REF}) + .01\,V_{REF} = .990\,V_{REF}$	$V_{OUT} = +4.90V$
1000 0000	$\frac{128}{255}(.98\,V_{REF}) + .01\,V_{REF} = .502\,V_{REF}$	$V_{OUT} = +0.02V$
0111 1111	$\frac{127}{255}(.98\,V_{REF}) + .01\,V_{REF} = .498\,V_{REF}$	$V_{OUT} = -0.02V$
0000 0001	$\frac{1}{255}(.98\,V_{REF}) + .01\,V_{REF} = .014\,V_{REF}$	$V_{OUT} = -4.86V$
0000 0000	$\frac{0}{255}(.98\,V_{REF}) + .01\,V_{REF} = .010\,V_{REF}$	$V_{OUT} = -4.90V$

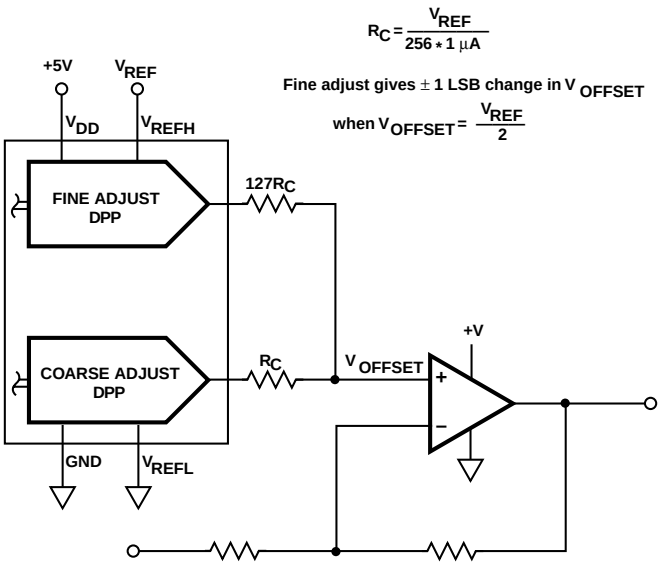


Bipolar DPP Output

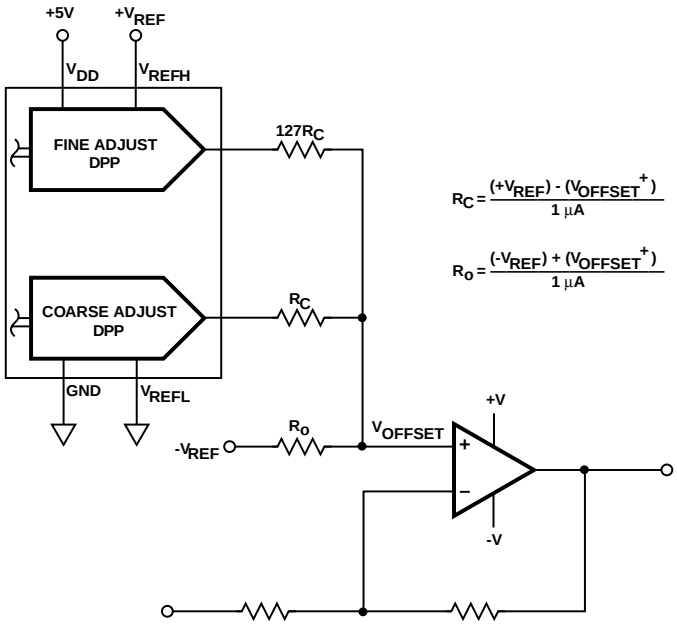


Amplified DPP Output

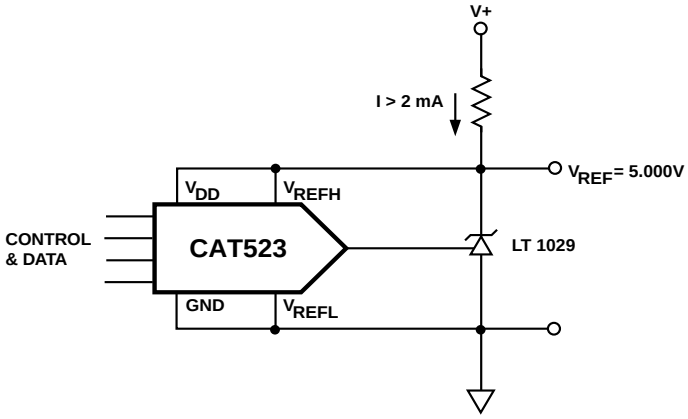
APPLICATION CIRCUITS (Cont.)



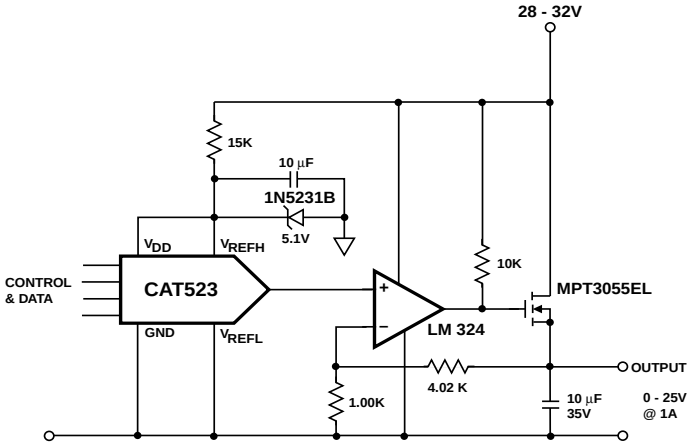
Coarse-Fine Offset Control by Averaging DPP Outputs for Single Power Supply Systems



Coarse-Fine Offset Control by Averaging DPP Outputs for Dual Power Supply Systems

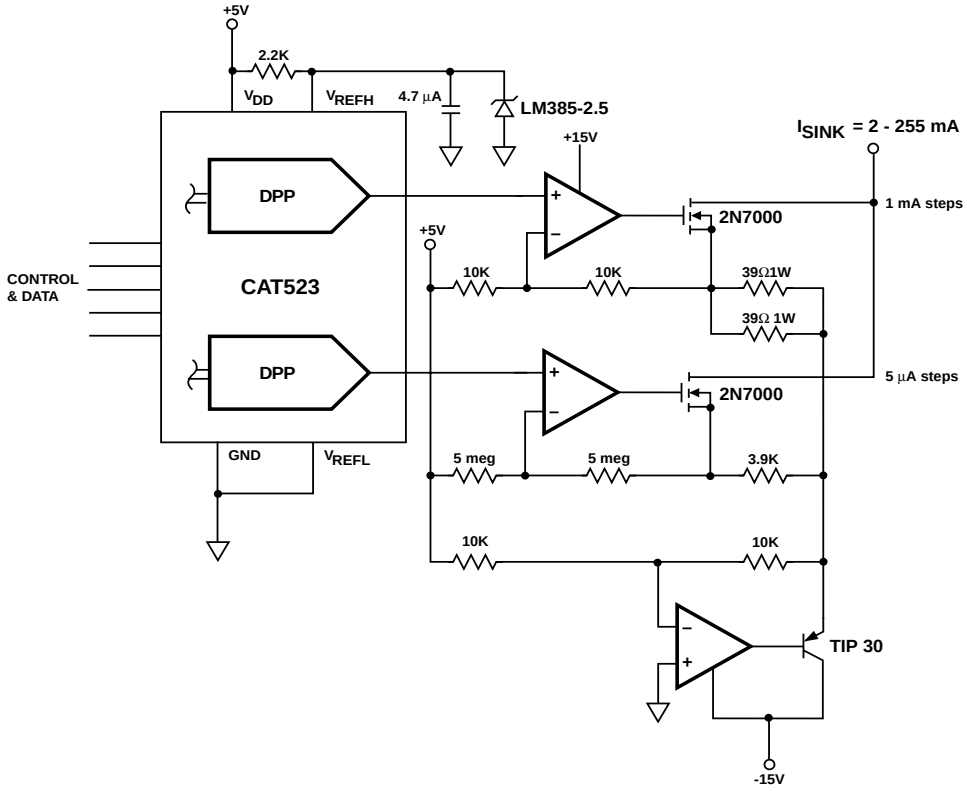


Digitally Trimmed Voltage Reference

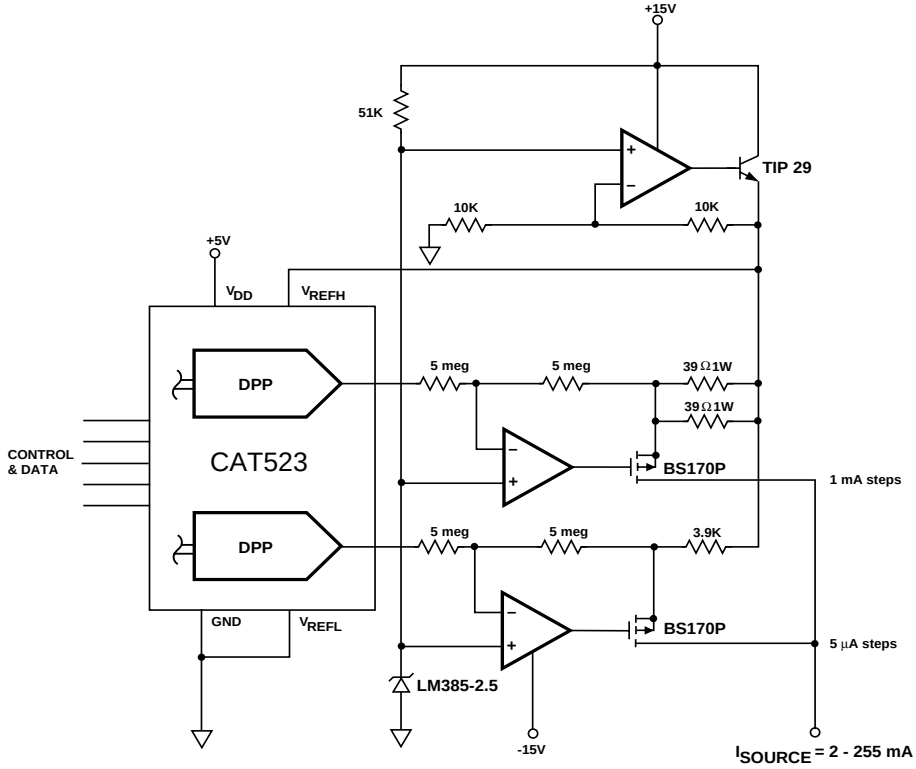


Digitally Controlled Voltage Reference

APPLICATION CIRCUITS (Cont.)

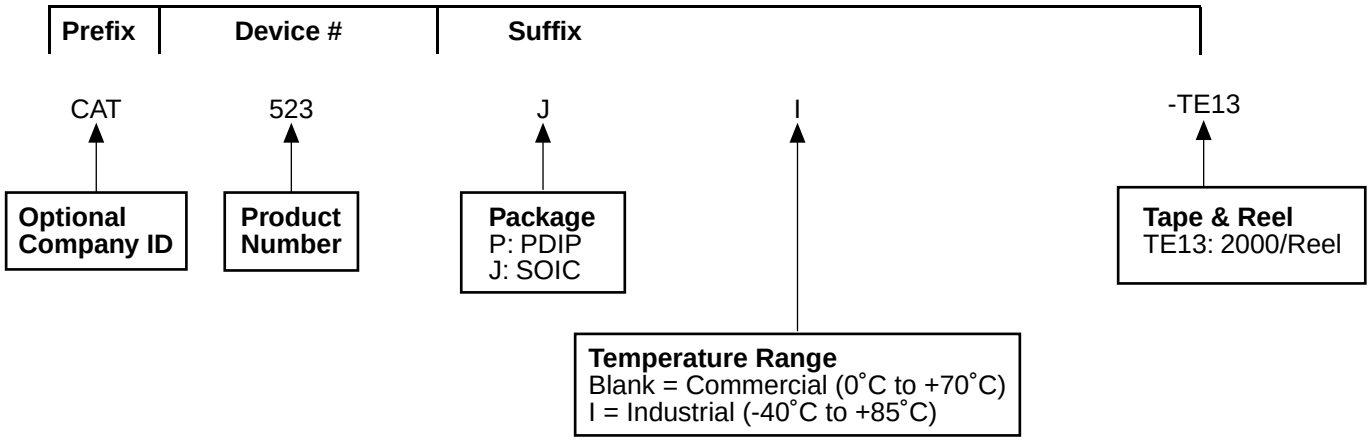


Current Sink with 4 Decades of Resolution



Current Source with 4 Decades of Resolution

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a CAT523JI-TE13 (SOIC, Industrial Temperature, Tape & Reel)

Catalyst Semiconductor, Inc.
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Publication #: 2005
Revison: B
Issue date: 3/22/02
Type: Final

CAT524

Configured Digitally Programmable Potentiometer (DPP™): Programmable Voltage Applications

FEATURES

- **Four 8-bit DPPs configured as programmable voltage sources in DAC-like applications**
- **Common reference inputs**
- **Buffered wiper outputs**
- **Non-volatile NVRAM memory wiper storage**
- **Output voltage range includes both supply rails**
- **4 independently addressable buffered output wipers**
- **1 LSB accuracy, high resolution**
- **Serial Microwire-like interface**
- **Single supply operation: 2.7V - 5.5V**
- **Setting read-back without effecting outputs**

APPLICATIONS

- **Automated product calibration**
- **Remote control adjustment of equipment**
- **Offset, gain and zero adjustments in self-calibrating and adaptive control systems**
- **Tamper-proof calibrations**
- **DAC (with memory) substitute**

DESCRIPTION

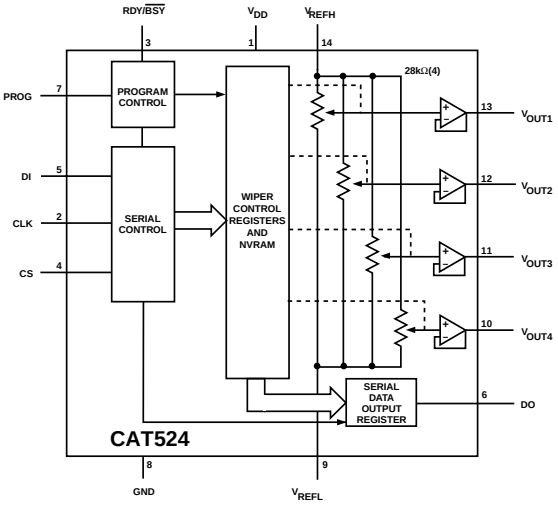
The CAT524 is a quad, 8-bit digitally-programmable potentiometer (DPP™) configured for programmable voltage and DAC-like applications. Intended for final calibration of products such as camcorders, fax machines and cellular telephones on automated high volume production lines, it is also well suited for self-calibrating systems and for applications where equipment which requires periodic adjustment is either difficult to access or in a hazardous environment.

The four independently programmable DPPs have an output range which includes both supply rails. The wipers are buffered by rail to rail op amps. Wiper settings, stored in non-volatile NVRAM memory, are not lost when the device is powered down and are automatically reinstated when power is returned. Each wiper can be dithered to test new output values without effecting the stored settings, and stored settings can be read back without disturbing the DPP's output.

The CAT524 is controlled with a simple 3-wire serial, Microwire-like interface. A Chip Select pin allows several devices to share a common serial interface. Communication back to the host controller is via a single serial data line thanks to the Tri-Stated CAT524 Data Output pin. A RDY/$\overline{BSY}$ output working in concert with an internal low voltage detector signals proper operation of the non-volatile NVRAM memory Erase/Write cycle.

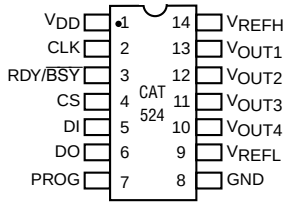
The CAT524 is available in the 0˚C to 70˚C commercial and -40˚C to 85˚C industrial operating temperature ranges. Both 14-pin plastic DIP and SOIC packages are offered.

FUNCTIONAL DIAGRAM

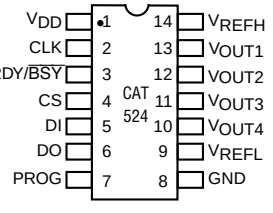


PIN CONFIGURATION

DIP Package (P)



SOIC Package (J)



Doc. No. 2006, Rev. B

ABSOLUTE MAXIMUM RATINGS

Supply Voltage*	
V_{DD} to GND	-0.5V to +7V
Inputs	
CLK to GND	-0.5V to V_{DD} +0.5V
CS to GND	-0.5V to V_{DD} +0.5V
DI to GND	-0.5V to V_{DD} +0.5V
RDY/BSY to GND	-0.5V to V_{DD} +0.5V
PROG to GND	-0.5V to V_{DD} +0.5V
V_{REF}H to GND	-0.5V to V_{DD} +0.5V
V_{REF}L to GND	-0.5V to V_{DD} +0.5V
Outputs	
D_0 to GND	-0.5V to V_{DD} +0.5V
V_{OUT} 1– 4 to GND	-0.5V to V_{DD} +0.5V

Operating Ambient Temperature	
Commercial ('C' or Blank suffix)	0°C to +70°C
Industrial ('I' suffix)	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Soldering (10 sec max)	+300°C

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Absolute Maximum Ratings are limited values applied individually while other parameters are within specified operating conditions, and functional operation at any of these conditions is NOT implied. Device performance and reliability may be impaired by exposure to absolute rating conditions for extended periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Method
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(2)	Latch-Up	100		mA	JEDEC Standard 17

NOTES: 1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} + 1V.

POWER SUPPLY

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD1}	Supply Current (Read)	Normal Operating	—	400	600	µA
I_{DD2}	Supply Current (Write)	Programming, V_{DD} = 5V	—	1600	2500	µA
		V_{DD} = 3V	—	1000	1600	µA
V_{DD}	Operating Voltage Range		2.7	—	5.5	V

LOGIC INPUTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	Input Leakage Current	V_{IN} = V_{DD}	—	—	10	µA
I_{IL}	Input Leakage Current	V_{IN} = 0V	—	—	-10	µA
V_{IH}	High Level Input Voltage		2	—	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	—	0.8	V

LOGIC OUTPUTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High Level Output Voltage	I_{OH} = -40µA	V_{DD} -0.3	—	—	V
V_{IL}	Low Level Output Voltage	I_{OL} = 1 mA, V_{DD} = +5V	—	—	0.4	V
		I_{OL} = 0.4 mA, V_{DD} = +3V	—	—	0.4	V

POTENTIOMETER CHARACTERISTICS

V_{DD} = +2.7V to +5.5V, $V_{REF}H = V_{DD}$, $V_{REF}L$ = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{POT}	Potentiometer Resistance			28		kΩ
	R_{POT} to R_{POT} Match		—	±0.5	±1	%
	Pot Resistance Tolerance				±15	%
	Voltage on V_{REFH} pin		2.7		V_{DD}	V
	Voltage on V_{REFL} pin		OV		V_{DD} - 2.7	V
	Resolution			0.4		%
INL	Integral Linearity Error			0.5	1	LSB
DNL	Differential Linearity Error			0.25	0.5	LSB
R_{OUT}	Buffer Output Resistance				10	Ω
I_{OUT}	Buffer Output Current				3	mA
TC_{RPOT}	TC of Pot Resistance			300		ppm/°C
TC_{RATIO}	Ratiometric TC					ppm/°C
R_{ISO}	Isolation Resistance					Ω
V_N	Noise					nV/√Hz
C_H/C_L	Potentiometer Capacitances			8/8		pF
fc	Frequency Response	Passive Attenuator				MHz

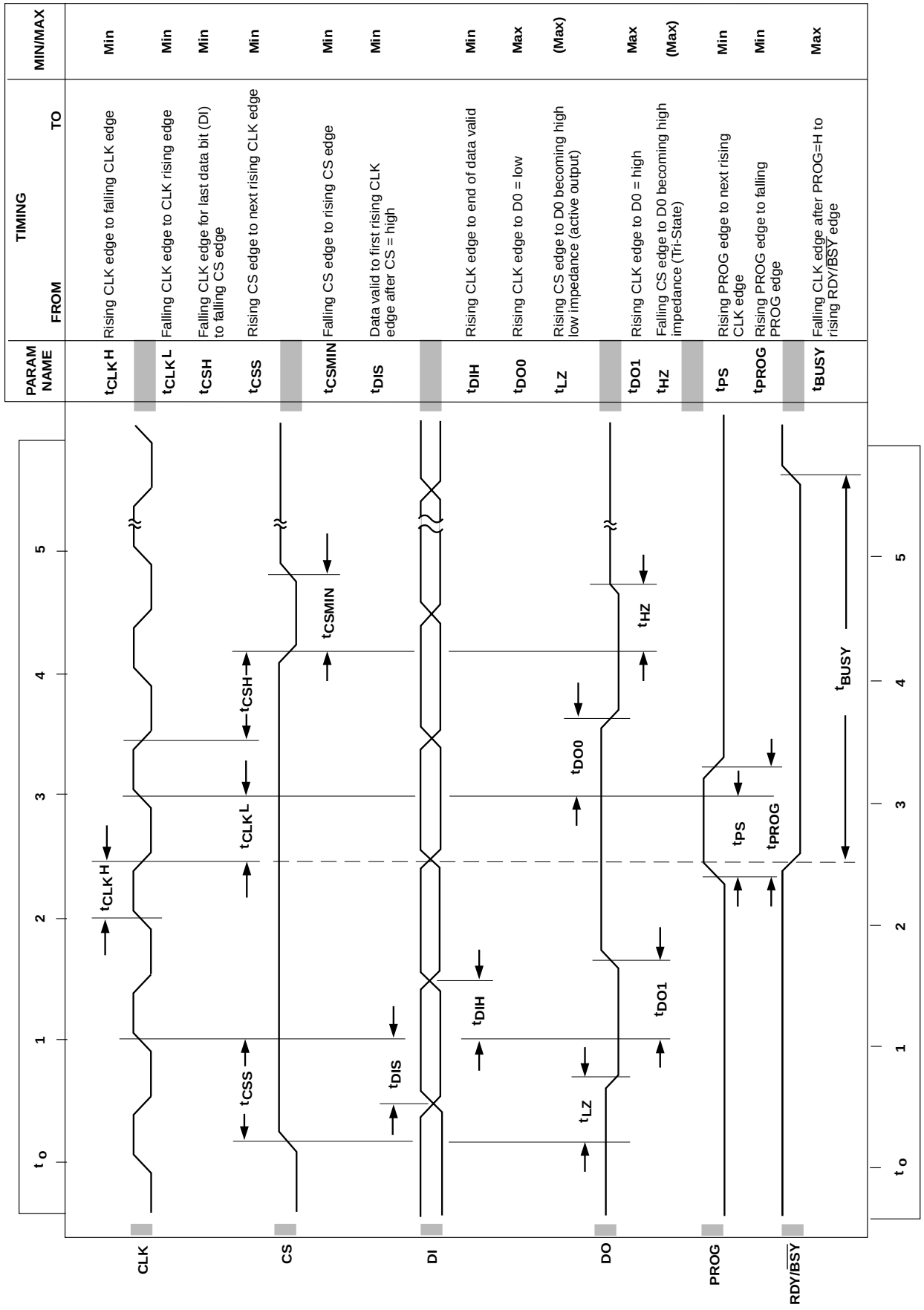
AC ELECTRICAL CHARACTERISTICS:

V_{DD} = +2.7V to +5.5V, $V_{REF}H = V_{DD}$, $V_{REF}L$ = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Digital						
t_{CSMIN}	Minimum CS Low Time		150	—	—	ns
t_{CSS}	CS Setup Time		100	—	—	ns
t_{CSH}	CS Hold Time	C_L=100pF, see note 1	0	—	—	ns
t_{DIS}	DI Setup Time		50	—	—	ns
t_{DIH}	DI Hold Time		50	—	—	ns
t_{DO1}	Output Delay to 1		—	—	150	ns
t_{DO0}	Output Delay to 0		—	—	150	ns
t_{HZ}	Output Delay to High-Z		—	400	—	ns
t_{LZ}	Output Delay to Low-Z		—	400	—	ns
t_{BUSY}	Erase/Write Cycle Time		—	4	5	ms
t_{PS}	PROG Setup Time		150	—	—	ns
t_{PROG}	Minimum Pulse Width		700	—	—	ns
$t_{CLK}H$	Minimum CLK High Time		500	—	—	ns
$t_{CLK}L$	Minimum CLK Low Time		300	—	—	ns
f_C	Clock Frequency		DC	—	1	MHz
Analog						
t_{DS}	DPP Settling Time to 1 LSB	C_{LOAD} = 10 pF, V_{DD} = +5V	—	3	10	µs
		C_{LOAD} = 10 pF, V_{DD} = +3V	—	6	10	µs

NOTES: 1. All timing measurements are defined at the point of signal crossing V_{DD} / 2.
2. These parameters are periodically sampled and are not 100% tested.

A. C. TIMING DIAGRAM



PIN DESCRIPTION

Pin	Name	Function
1	V_{DD}	Power supply positive.
2	CLK	Clock input pin.Clock input pin.
3	RDY/$\overline{BSY}$	Ready/Busy Output
4	CS	Chip Select
5	DI	Serial data input pin.
6	DO	Serial data output pin.
7	PROG	Non-volatile Memory Programming Enable Input
8	GND	Power supply ground.
9	V_{REFL}	Minimum DPP output voltage.
10	V_{OUT4}	DPP output channel 4.
11	V_{OUT3}	DPP output channel 3.
12	V_{OUT2}	DPP output channel 2.
13	V_{OUT1}	DPP output channel 1.
14	V_{REFH}	Maximum DPP output voltage.

DPP addressing is as follows:

DPP OUTPUT	A0	A1
V_{OUT1}	0	0
V_{OUT2}	1	0
V_{OUT3}	0	1
V_{OUT4}	1	1

DEVICE OPERATION

The CAT524 is a quad 8-bit configured digitally programmable potentiometer (DPP) whose outputs can be programmed to any one of 256 individual voltage steps. Once programmed, these output settings are retained in non-volatile memory and will not be lost when power is removed from the chip. Upon power up the DPPs return to the settings stored in non-volatile memory. Each DPP can be written to and read from independently without effecting the output voltage during the read or write cycle. Each output can also be temporarily adjusted without changing the stored output setting, which is useful for testing new output settings before storing them in memory.

DIGITAL INTERFACE

The CAT524 employs a 3 wire serial, Microwire-like control interface consisting of Clock (CLK), Chip Select (CS) and Data In (DI) inputs. For all operations, address and data are shifted in LSB first. In addition, all digital data must be preceded by a logic “1” as a start bit. The DPP address and data are clocked into the DI pin on the clock’s rising edge. When sending multiple blocks of information a minimum of two clock cycles is required between the last block sent and the next start bit.

Multiple devices may share a common input data line by selectively activating the CS control of the desired IC. Data Outputs (DO) can also share a common line because the DO pin is Tri-Stated and returns to a high impedance when not in use.

CHIP SELECT

Chip Select (CS) enables and disables the CAT524’s read and write operations. When CS is high data may be read to or from the chip, and the Data Output (DO) pin is active. Data loaded into the DPP control registers will remain in effect until CS goes low. Bringing CS to a logic low returns all DPP outputs to the settings stored in non-volatile memory and switches DO to its high impedance Tri-State mode.

Because CS functions like a reset the CS pin has been equipped with a 30 ns to 90 ns filter circuit to prevent noise spikes from causing unwanted resets and the loss of volatile data.

CLOCK

The CAT524’s clock controls both data flow in and out of the IC and non-volatile memory cell programming. Serial data is shifted into the DI pin and out of the DO pin on the clock’s rising edge. While it is not necessary for the clock to be running between data transfers, the clock must be operating in order to write to non-volatile memory, even though the data being saved may already be resident in the DPP wiper control register.

No clock is necessary upon system power-up. The CAT524’s internal power-on reset circuitry loads data from non-volatile memory to the DPPs without using the external clock.

As data transfers are edge triggered clean clock transitions are necessary to avoid falsely clocking data into the control registers. Standard CMOS and TTL logic families work well in this regard and it is recommended that any mechanical switches used for breadboarding or device evaluation purposes be debounced by a flip-flop or other suitable debouncing circuit.

V_{REF}

V_{REF}, the voltage applied between pins V_{REFH} and V_{REFL}, sets the configured DPP's Zero to Full Scale output range where V_{REFL} = Zero and V_{REFH} = Full Scale. V_{REF} can span the full power supply range or just a fraction of it. In typical applications V_{REFH} and V_{REFL} are connected across the power supply rails. When using less than the full supply voltage V_{REFH} is restricted to voltages between V_{DD} and $V_{DD}/2$ and V_{REFL} to voltages between GND and $V_{DD}/2$.

READY/$\overline{BUSY}$

When saving data to non-volatile memory, the Ready/Busy ouput (RDY/$\overline{BSY}$) signals the start and duration of the non-volatile erase/write cycle. Upon receiving a command to store data (PROG goes high) RDY/$\overline{BSY}$ goes low and remains low until the programming cycle is complete. During this time the CAT524 will ignore any data appearing at DI and no data will be output on DO.

RDY/$\overline{BSY}$ is internally ANDed with a low voltage detector circuit monitoring V_{DD}. If V_{DD} is below the minimum value required for non-volatile programming, RDY/$\overline{BSY}$ will remain high following the program command indicating a failure to record the desired data in non-volatile memory.

DATA OUTPUT

Data is output serially by the CAT524, LSB first, via the Data Out (DO) pin following the reception of a start bit and two address bits by the Data Input (DI). DO becomes active whenever CS goes high and resumes its high impedance Tri-State mode when CS returns low. Tri-Stating the DO pin allows several 524s to share a single serial data line and simplifies interfacing multiple 524s to a microprocessor.

WRITING TO MEMORY

Programming the CAT524's non-volatile memory is accomplished through the control signals: Chip Select (CS) and Program (PROG). With CS high, a start bit followed by a two bit DPP address and eight data bits are clocked into the DPP control register via the DI pin. Data enters on the clock's rising edge. The DPP output changes to its new setting on the clock cycle following D7, the last data bit.

Programming is achieved by bringing PROG high for a minimum of 3 ms. PROG must be brought high sometime after the start bit and at least 150 ns prior to the rising edge of the clock cycle immediately following the D7 bit. Two clock cycles after the D7 bit the DPP wiper control register will be ready to receive the next set of address and data bits. The clock must be kept running throughout the programming cycle. Internal control circuitry takes care of ramping the programming voltage for data transfer to the non-volatile cells. The CAT524 non-volatile memory cells will endure over 100,000 write cycles and will retain data for a minimum of 20 years without being refreshed.

READING DATA

Each time data is transferred into a DPP wiper control register currently held data is shifted out via the D0 pin, thus in every data transaction a read cycle occurs. Note, however, that the reading process is destructive. Data must be removed from the register in order to be read. Figure 2 depicts a Read Only cycle in which no change occurs in the DPP's output. This feature allows µPs to poll DPPs for their current setting without disturbing the output voltage but it assumes that the setting being read is also stored in non-volatile memory so that it can be restored at the end of the read cycle. In Figure 2 CS returns low before the 13th clock cycle completes. In doing so the non-volatile memory setting is reloaded into the DPP wiper control register.

Figure 1. Writing to Memory

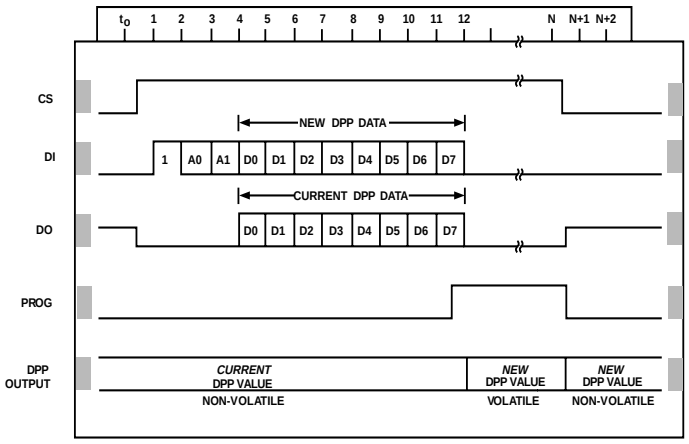
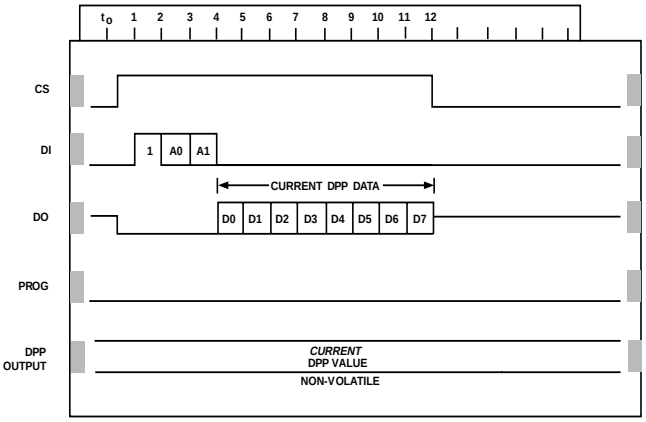


Figure 2. Reading from Memory



Since this value is the same as that which had been there previously no change in the DPP's output is noticed. Had the value held in the control register been different from that stored in non-volatile memory then *a change would occur* at the read cycle's conclusion.

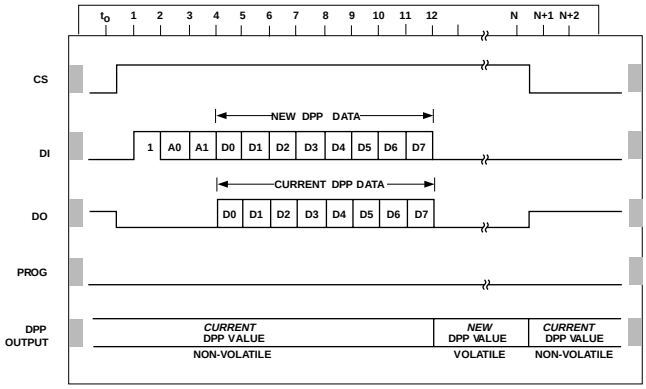
TEMPORARILY CHANGE OUTPUT

The CAT524 allows temporary changes in DPP's output to be made without disturbing the settings retained in non-volatile memory. This feature is particularly useful when testing for a new output setting and allows for user adjustment of preset or default values without losing the original factory settings.

Figure 3 shows the control and data signals needed to effect a temporary output change. DPP wiper settings may be changed as many times as required and can be made to any of the four DPPs in any order or sequence. The temporary setting(s) remain in effect long as CS remains high. When CS returns low all four DPPs will return to the output values stored in non-volatile memory.

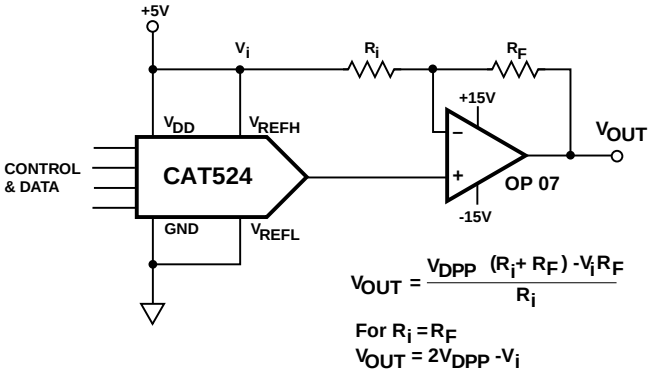
When it is desired to save a new setting acquired using this feature, the new value must be reloaded into the DPP control register prior to programming. This is because the CAT524's internal control circuitry discards the new data from the programming register two clock cycles after receiving it (after reception is complete) if no PROG signal is received.

Figure 3. Temporary Change in Output

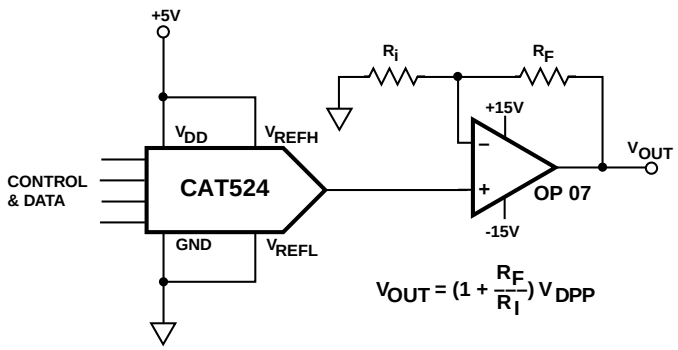


APPLICATION CIRCUITS

DPP INPUT MSB	DPP INPUT LSB	DPP OUTPUT $V_{DPP} = \frac{CODE}{255}(V_{FS} - V_{ZERO}) + V_{ZERO}$ $V_{FS} = 0.99\,V_{REF}$ $V_{ZERO} = 0.01\,V_{REF}$	ANALOG OUTPUT $V_{REF} = 5V$ $R_I = R_F$
1111	1111	$\frac{255}{255}(.98\,V_{REF}) + .01\,V_{REF} = .990\,V_{REF}$	$V_{OUT} = +4.90V$
1000	0000	$\frac{128}{255}(.98\,V_{REF}) + .01\,V_{REF} = .502\,V_{REF}$	$V_{OUT} = +0.02V$
0111	1111	$\frac{127}{255}(.98\,V_{REF}) + .01\,V_{REF} = .498\,V_{REF}$	$V_{OUT} = -0.02V$
0000	0001	$\frac{1}{255}(.98\,V_{REF}) + .01\,V_{REF} = .014\,V_{REF}$	$V_{OUT} = -4.86V$
0000	0000	$\frac{0}{255}(.98\,V_{REF}) + .01\,V_{REF} = .010\,V_{REF}$	$V_{OUT} = -4.90V$

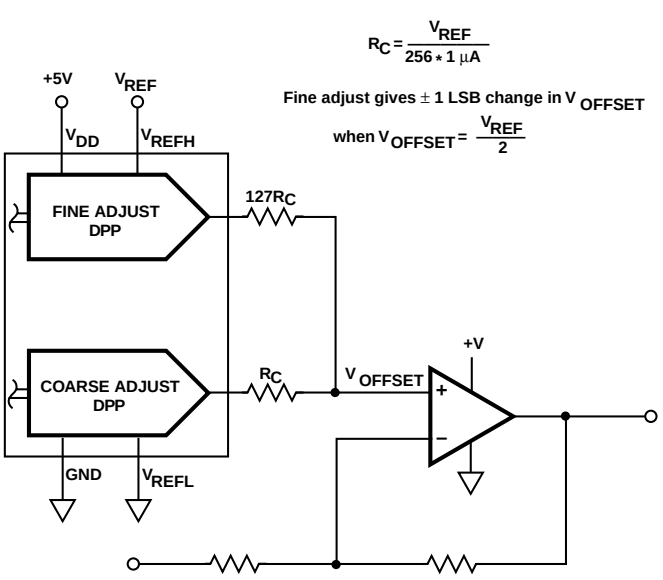


Bipolar DPP Output

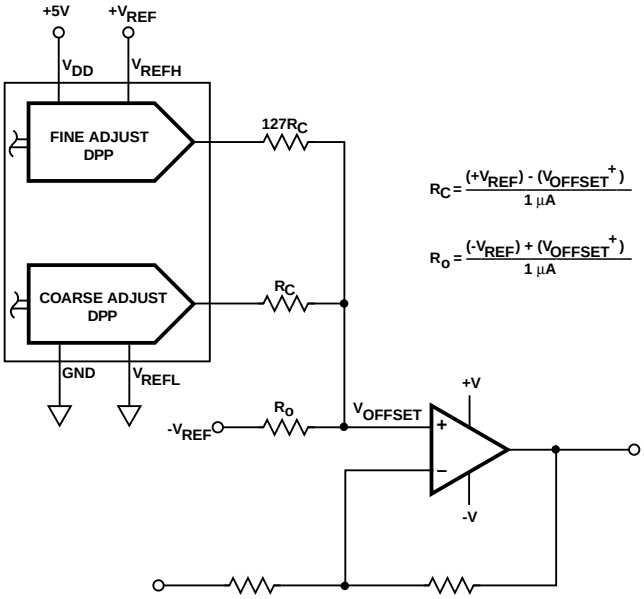


Amplified DPP Output

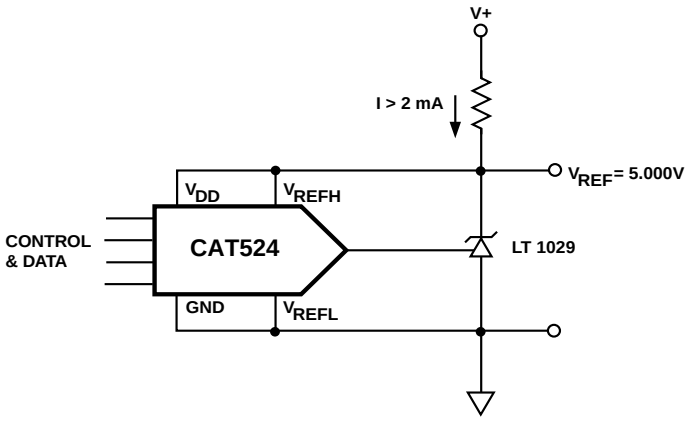
APPLICATION CIRCUITS (Cont.)



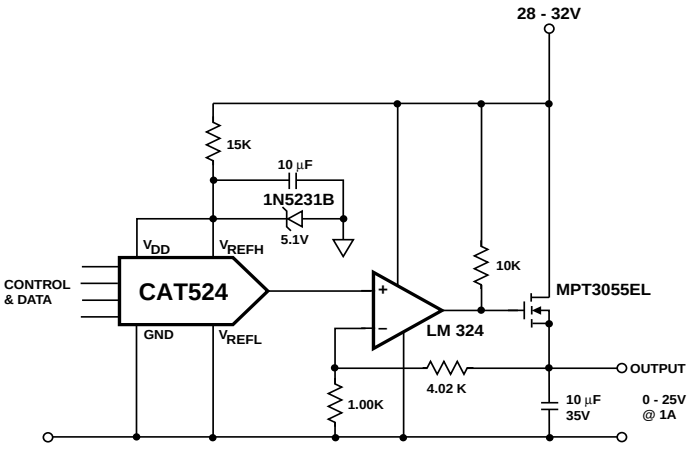
Coarse-Fine Offset Control by Averaging DPP Outputs for Single Power Supply Systems



Coarse-Fine Offset Control by Averaging DPP Outputs for Dual Power Supply Systems

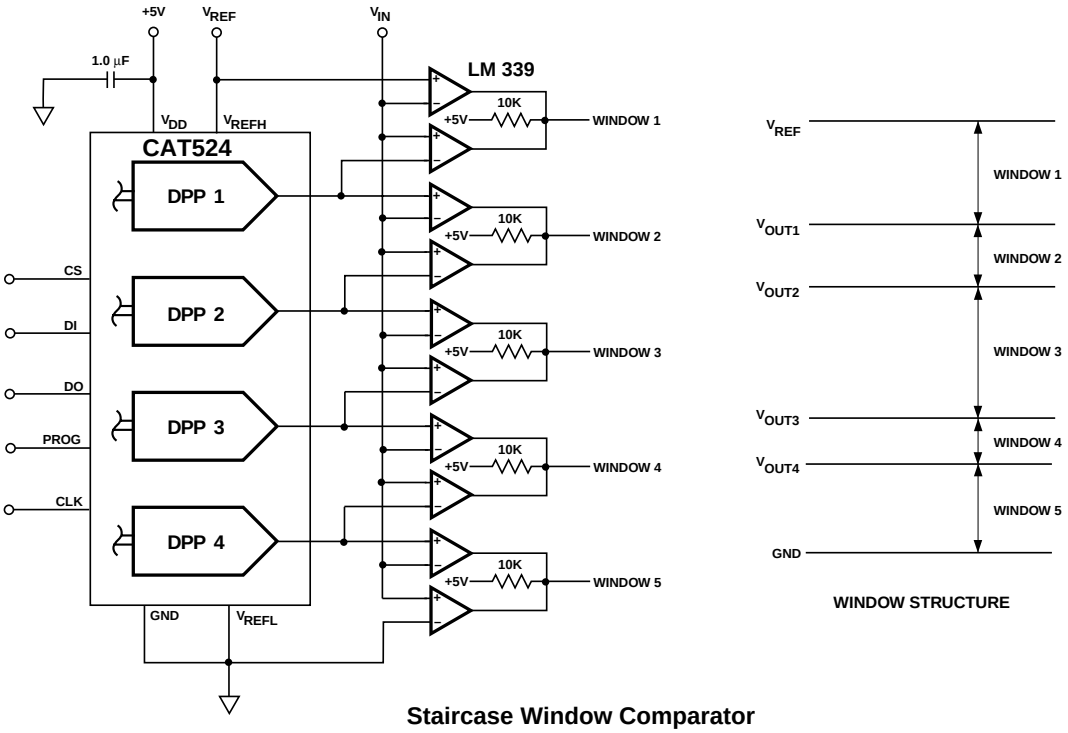


Digitally Trimmed Voltage Reference

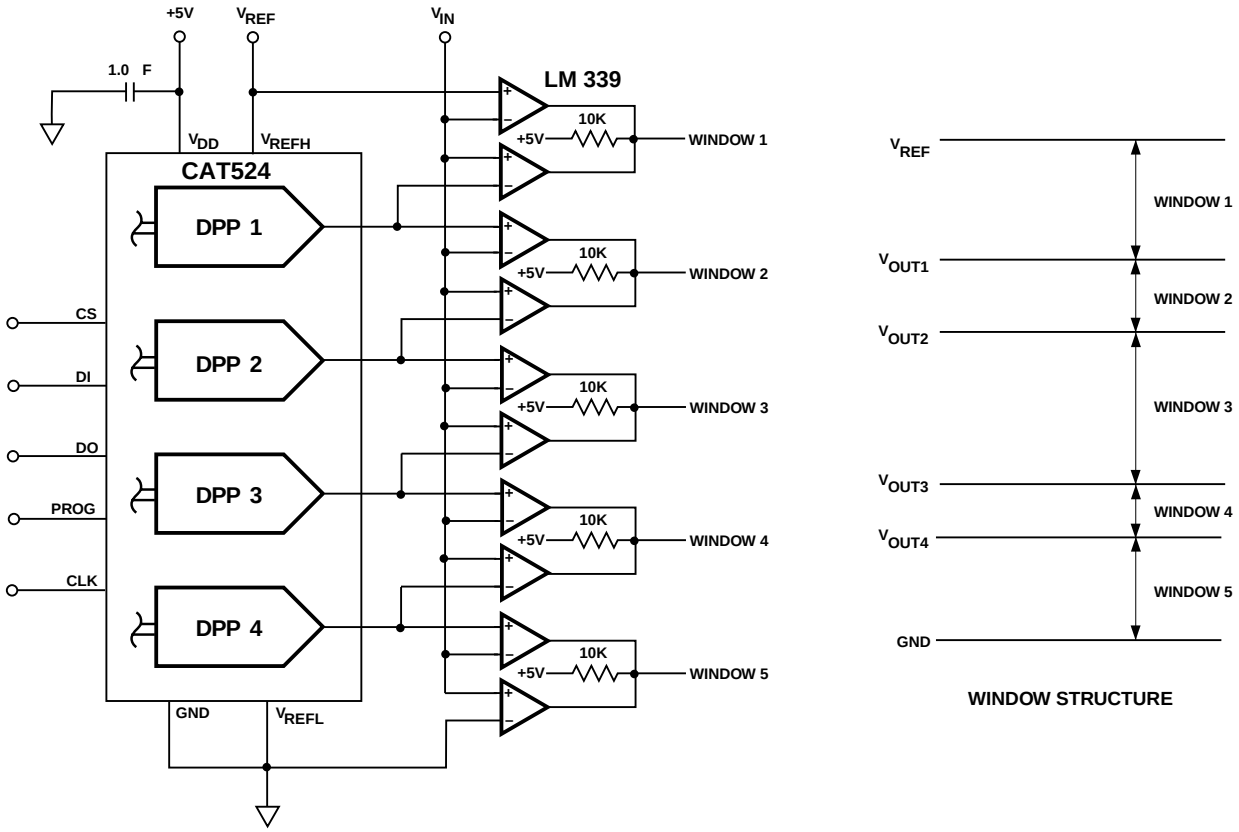


Digitally Controlled Voltage Reference

APPLICATION CIRCUITS (Cont.)

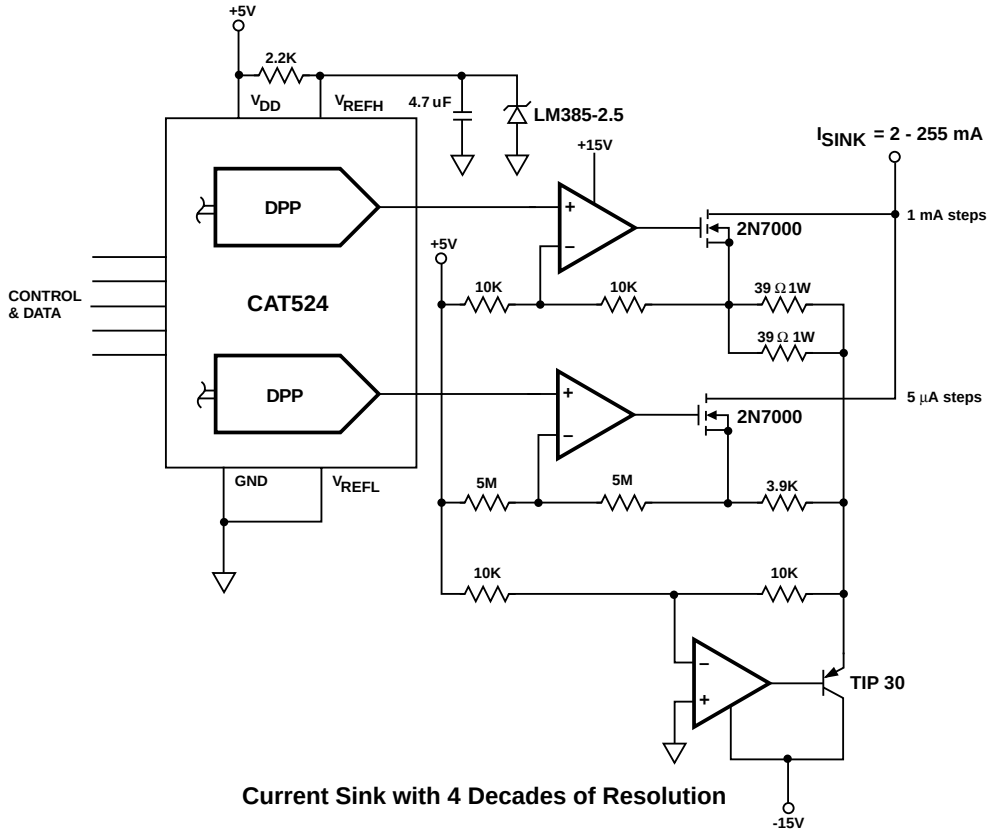


Staircase Window Comparator

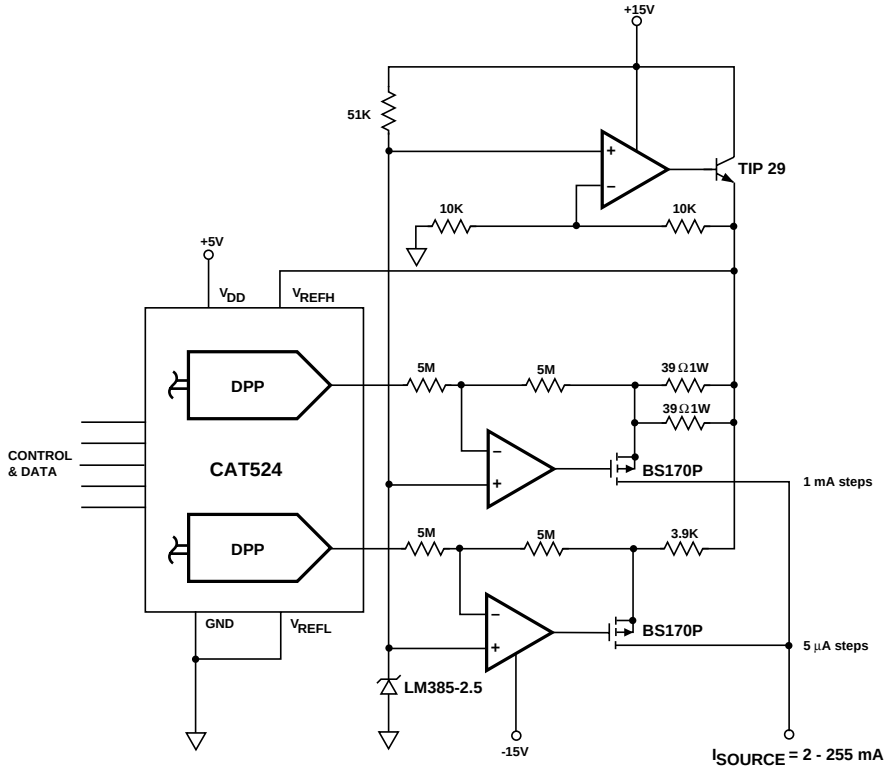


Overlapping Window Comparator

APPLICATION CIRCUITS (Cont.)

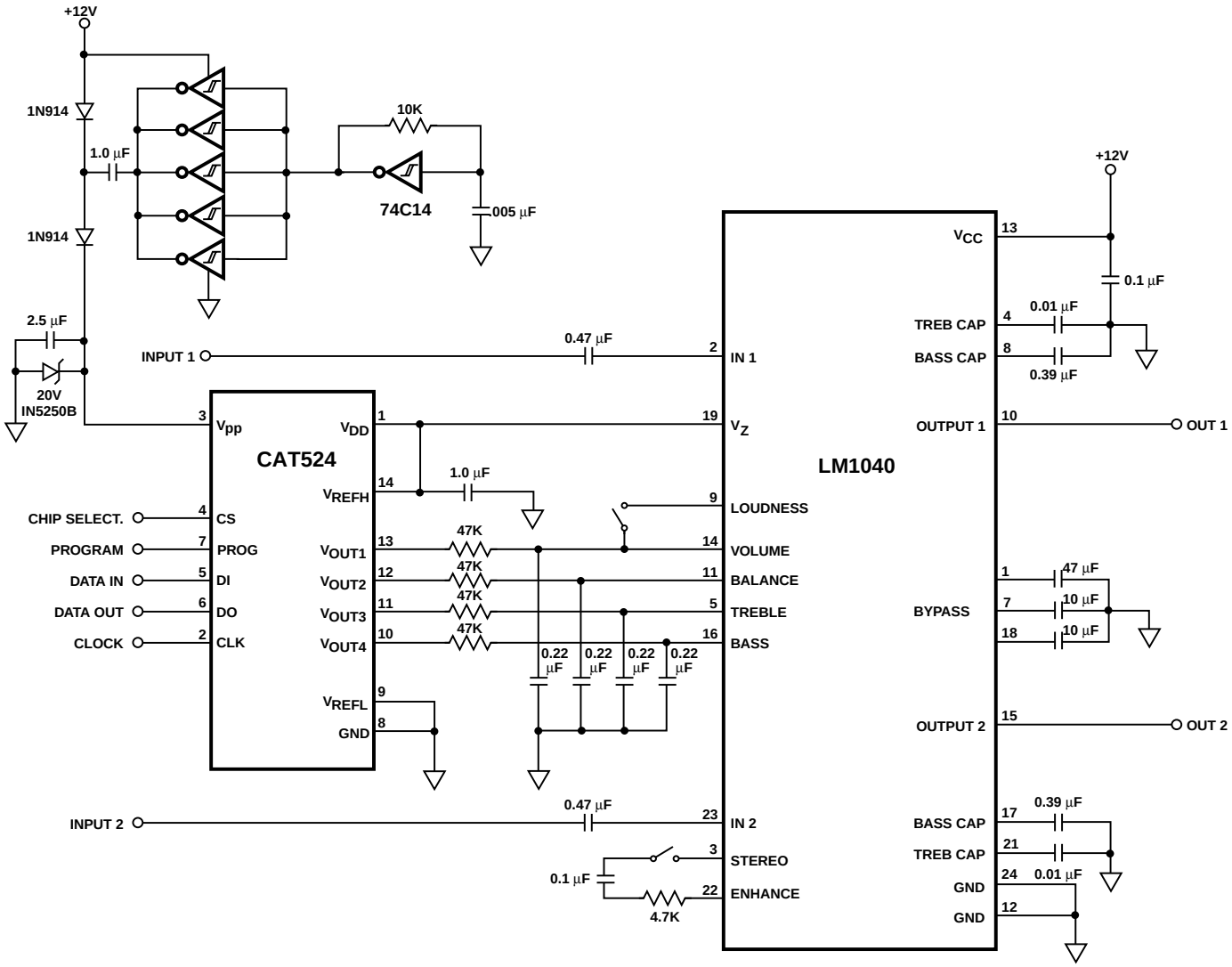


Current Sink with 4 Decades of Resolution



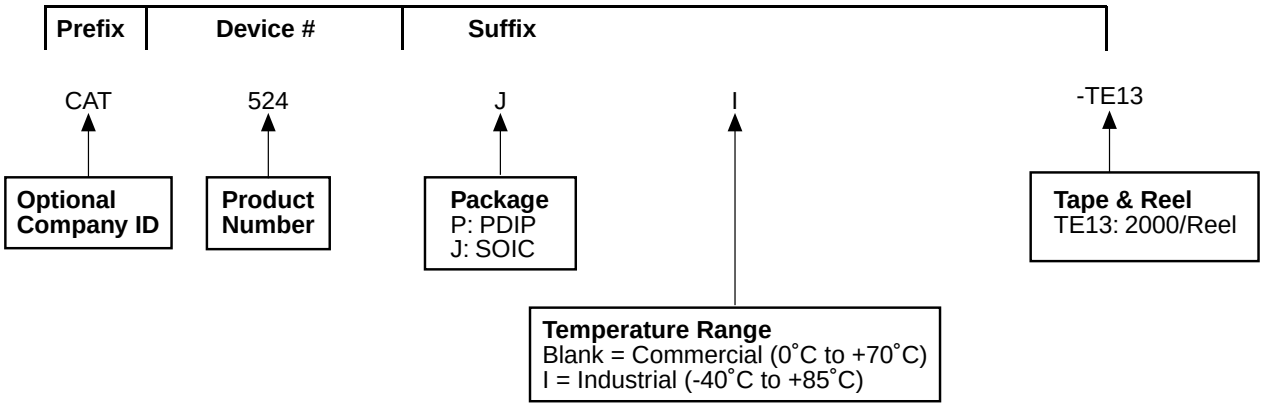
Current Source with 4 Decades of Resolution

APPLICATION CIRCUITS (Cont.)



Digital Stereo Control

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a CAT524JI-TE13 (SOIC, Industrial Temperature, Tape & Reel)

CATALYST

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Revison: B
Issue date: 03/22/02
Type: Final

CAT525

Configured Digitally Programmable Potentiometer (DPP™): Programmable Voltage Applications

FEATURES

- **Four 8-bit DPPs configured as programmable voltage sources in DAC-like applications**
- **Independent reference inputs**
- **Buffered wiper outputs**
- **Non-volatile NVRAM memory wiper storage**
- **Output voltage range includes both supply rails**
- **4 independently addressable buffered output wipers**
- **1 LSB accuracy, high resolution**
- **Serial Microwire-like interface**
- **Single supply operation: 2.7V - 5.5V**
- **Setting read-back without effecting outputs**

APPLICATIONS

- **Automated product calibration**
- **Remote control adjustment of equipment**
- **Offset, gain and zero adjustments in self-calibrating and adaptive control systems**
- **Tamper-proof calibrations**
- **DAC (with memory) substitute**

DESCRIPTION

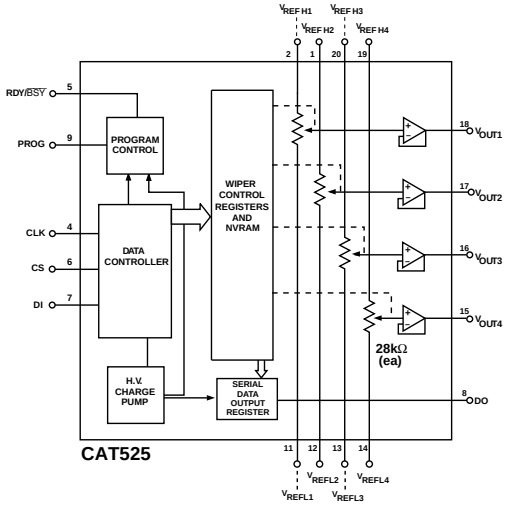
The CAT525 is a quad 8-bit digitally programmable potentiometer (DPP™) configured for programmable voltage and DAC-like applications. Intended for final calibration of products such as camcorders, fax machines and cellular telephones on automated high volume production lines and systems capable of self calibration, it is also well suited for applications were equipment requiring periodic adjustment is either difficult to access or located in a hazardous environment.

The CAT525 offers four independently programmable DPPs each having its own reference inputs and each capable of rail to rail output swing. The wipers are buffered by rail to rail op amps. Wiper settings, stored in non-volatile NVRAM memory, are not lost when the device is powered down and are automatically reinstated when power is returned. Each wiper can be dithered to test new output values without effecting the stored settings and stored settings can be read back without disturbing the DPP's output.

Control of the CAT525 is accomplished with a simple 3-wire, Microwire-like serial interface. A Chip Select pin allows several CAT525's to share a common serial interface and communications back to the host controller is via a single serial data line thanks to the CAT525's Tri-Stated Data Output pin. A RDY/$\overline{BSY}$ output working in concert with an internal low voltage detector signals proper operation of non-volatile NVRAM Memory Erase/Write cycle.

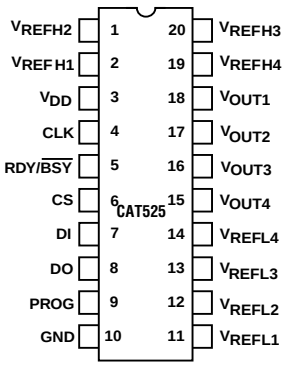
The CAT525 is available in the 0°C to 70°C commercial and -40°C to 85°C industrial operating temperature ranges and offered in 20-pin plastic DIP and surface mount packages.

FUNCTIONAL DIAGRAM

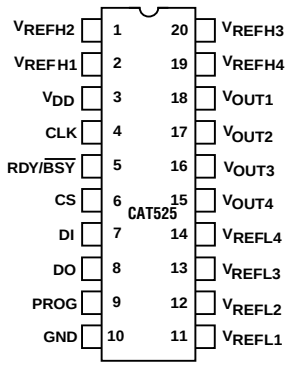


PIN CONFIGURATION

DIP Package (P)



SOIC Package (J)



Doc. No. 2001, Rev. B

ABSOLUTE MAXIMUM RATINGS

Supply Voltage*
- V_{DD} to GND ..... -0.5V to +7V

Inputs
- CLK to GND ..... -0.5V to V_{DD} +0.5V
- CS to GND ..... -0.5V to V_{DD} +0.5V
- DI to GND ..... -0.5V to V_{DD} +0.5V
- RDY/BSY to GND ..... -0.5V to V_{DD} +0.5V
- PROG to GND ..... -0.5V to V_{DD} +0.5V
- V_{REF}H to GND ..... -0.5V to V_{DD} +0.5V
- V_{REF}L to GND ..... -0.5V to V_{DD} +0.5V

Outputs
- D_0 to GND ..... -0.5V to V_{DD} +0.5V
- V_{OUT} 1– 4 to GND ..... -0.5V to V_{DD} +0.5V

Operating Ambient Temperature
- Commercial ('C' or Blank suffix) ..... 0°C to +70°C
- Industrial ('I' suffix) ..... -40°C to +85°C

Junction Temperature ..... +150°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering (10 sec max) ..... +300°C

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Absolute Maximum Ratings are limited values applied individually while other parameters are within specified operating conditions, and functional operation at any of these conditions is NOT implied. Device performance and reliability may be impaired by exposure to absolute rating conditions for extended periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Method
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(2)	Latch-Up	100		mA	JEDEC Standard 17

NOTES: 1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} + 1V.

POWER SUPPLY

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD1}	Supply Current (Read)	Normal Operating	—	400	600	µA
I_{DD2}	Supply Current (Write)	Programming, V_{DD} = 5V	—	1600	2500	µA
		V_{DD} = 3V	—	1000	1600	µA
V_{DD}	Operating Voltage Range		2.7	—	5.5	V

LOGIC INPUTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	Input Leakage Current	V_{IN} = V_{DD}	—	—	10	µA
I_{IL}	Input Leakage Current	V_{IN} = 0V	—	—	-10	µA
V_{IH}	High Level Input Voltage		2	—	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	—	0.8	V

LOGIC OUTPUTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High Level Output Voltage	I_{OH} = -40µA	V_{DD} -0.3	—	—	V
V_{IL}	Low Level Output Voltage	I_{OL} = 1 mA, V_{DD} = +5V	—	—	0.4	V
		I_{OL} = 0.4 mA, V_{DD} = +3V	—	—	0.4	V

POTENTIOMETER CHARACTERISTICS

V_{DD} = +2.7V to +5.5V, $V_{REF}H = V_{DD}$, $V_{REF}L$ = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{POT}	Potentiometer Resistance			28		kΩ
	R_{POT} to R_{POT} Match		—	±0.5	±1	%
	Pot Resistance Tolerance				±15	%
	Voltage on V_{REFH} pin		2.7		V_{DD}	V
	Voltage on V_{REFL} pin		OV		V_{DD} - 2.7	V
	Resolution			0.4		%
INL	Integral Linearity Error			0.5	1	LSB
DNL	Differential Linearity Error			0.25	0.5	LSB
R_{OUT}	Buffer Output Resistance				10	Ω
I_{OUT}	Buffer Output Current				3	mA
TC_{RPOT}	TC of Pot Resistance			300		ppm/°C
TC_{RATIO}	Ratiometric TC					ppm/°C
R_{ISO}	Isolation Resistance					Ω
V_N	Noise					nV/√Hz
C_H/C_L	Potentiometer Capacitances			8/8		pF
fc	Frequency Response	Passive Attenuator				MHz

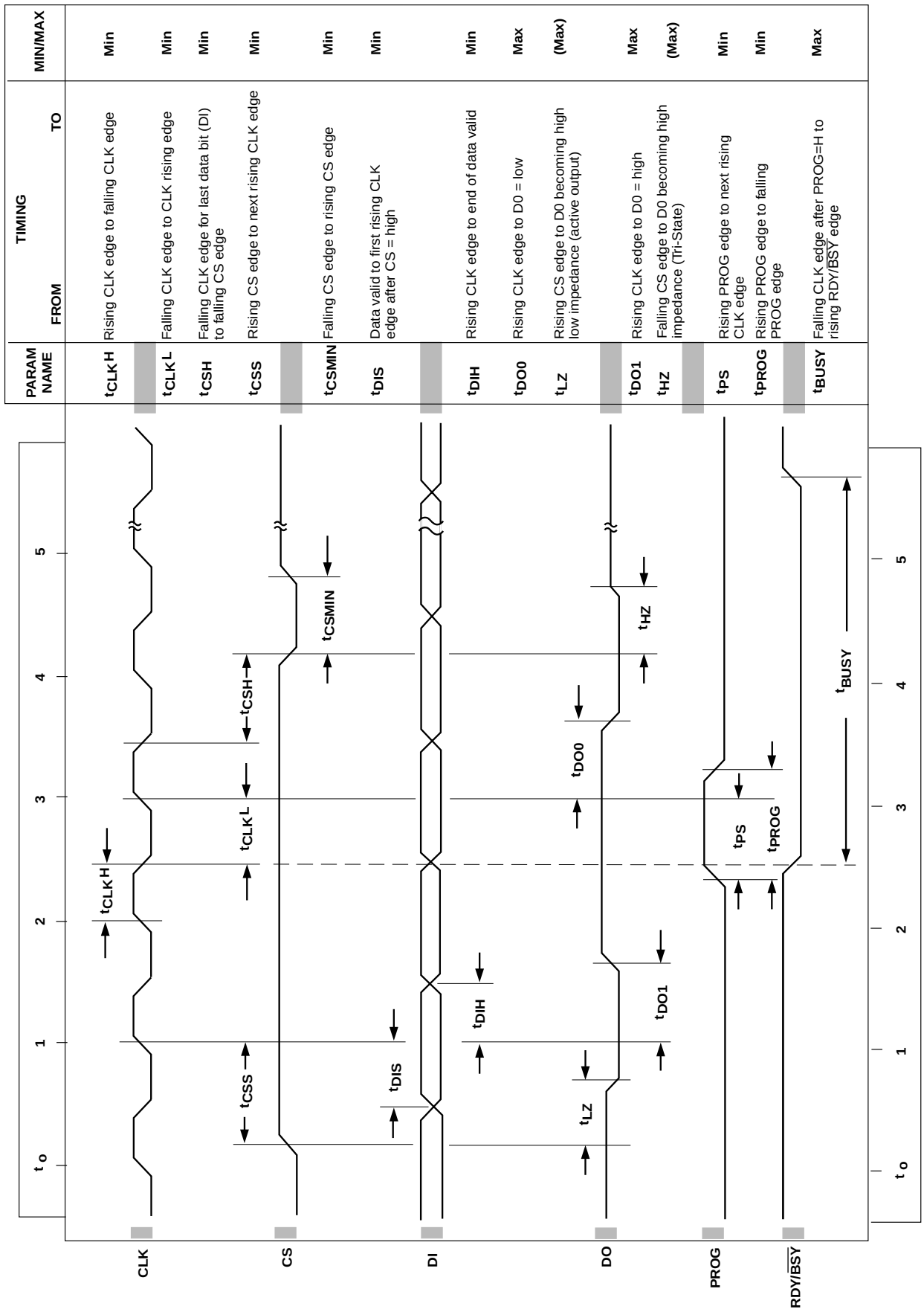
AC ELECTRICAL CHARACTERISTICS:

V_{DD} = +2.7V to +5.5V, $V_{REF}H = V_{DD}$, $V_{REF}L$ = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Digital						
t_{CSMIN}	Minimum CS Low Time		150	—	—	ns
t_{CSS}	CS Setup Time		100	—	—	ns
t_{CSH}	CS Hold Time	C_L=100pF, see note 1	0	—	—	ns
t_{DIS}	DI Setup Time		50	—	—	ns
t_{DIH}	DI Hold Time		50	—	—	ns
t_{DO1}	Output Delay to 1		—	—	150	ns
t_{DO0}	Output Delay to 0		—	—	150	ns
t_{HZ}	Output Delay to High-Z		—	400	—	ns
t_{LZ}	Output Delay to Low-Z		—	400	—	ns
t_{BUSY}	Erase/Write Cycle Time		—	4	5	ms
t_{PS}	PROG Setup Time		150	—	—	ns
t_{PROG}	Minimum Pulse Width		700	—	—	ns
$t_{CLK}H$	Minimum CLK High Time		500	—	—	ns
$t_{CLK}L$	Minimum CLK Low Time		300	—	—	ns
f_C	Clock Frequency		DC	—	1	MHz
Analog						
t_{DS}	DPP Settling Time to 1 LSB	C_{LOAD} = 10 pF, V_{DD} = +5V	—	3	10	µs
		C_{LOAD} = 10 pF, V_{DD} = +3V	—	6	10	µs

NOTES: 1. All timing measurements are defined at the point of signal crossing V_{DD} / 2.
2. These parameters are periodically sampled and are not 100% tested.

A. C. TIMING DIAGRAM



PIN DESCRIPTION

Pin	Name	Function
1	V_{REFH2}	Maximum DPP 2 output voltage
2	V_{REFH1}	Maximum DPP 1 output voltage
3	V_{DD}	Power supply positive
4	CLK	Clock input pin
5	RDY/$\overline{BSY}$	Ready/Busy output
6	CS	Chip select
7	DI	Serial data input pin
8	DO	Serial data output pin
9	PROG	Non-volatile Memory Programming Enable Input
10	GND	Power supply ground
11	V_{REFL1}	Minimum DPP 1 output voltage
12	V_{REFL2}	Minimum DPP 2 output voltage
13	V_{REFL3}	Minimum DPP 3 output voltage
14	V_{REFL4}	Minimum DPP 4 output voltage
15	V_{OUT4}	DPP 4 output
16	V_{OUT3}	DPP 3 output
17	V_{OUT2}	DPP 2 output
18	V_{OUT1}	DPP 1 output
19	V_{REFH4}	Maximum DPP 4 output voltage
20	V_{REFH3}	Maximum DPP 3 output voltage

CDPP/DPP addressing is as follows:

DPP OUTPUT	A0	A1
V_{OUT1}	0	0
V_{OUT2}	1	0
V_{OUT3}	0	1
V_{OUT4}	1	1

DEVICE OPERATION

The CAT525 is a quad 8-bit configured digitally programmable potentiometer (DPP/CDPP) whose outputs can be programmed to any one of 256 individual voltage steps. Once programmed, these output settings are retained in non-volatile memory and will not be lost when power is removed from the chip. Upon power up the DPPs return to the settings stored in non-volatile memory. Each confitured DPP can be written to and read from independently without effecting the output voltage during the read or write cycle. Each output can also be adjusted without altering the stored output setting, which is useful for testing new output settings before storing them in memory.

DIGITAL INTERFACE

The CAT525 employs a 3 wire serial, Microwire-like control interface consisting of Clock (CLK), Chip Select (CS) and Data In (DI) inputs. For all operations, address and data are shifted in LSB first. In addition, all digital data must be preceded by a logic “1” as a start bit. The DPP address and data are clocked into the DI pin on the clock’s rising edge. When sending multiple blocks of information a minimum of two clock cycles is required between the last block sent and the next start bit.

Multiple devices may share a common input data line by selectively activating the CS control of the desired IC. Data Outputs (DO) can also share a common line because the DO pin is Tri-Stated and returns to a high impedance when not in use.

CHIP SELECT

Chip Select (CS) enables and disables the CAT525’s read and write operations. When CS is high data may be read to or from the chip, and the Data Output (DO) pin is active. Data loaded into the DPP wiper control registers will remain in effect until CS goes low. Bringing CS to a logic low returns all DPP outputs to the settings stored in non-volatile memory and switches DO to its high impedance Tri-State mode.

Because CS functions like a reset the CS pin has been desensitized with a 30 ns to 90 ns filter circuit to prevent noise spikes from causing unwanted resets and the loss of volatile data.

CLOCK

The CAT525’s clock controls both data flow in and out of the IC and non-volatile memory cell programming. Serial data is shifted into the DI pin and out of the DO pin on the clock’s rising edge. While it is not necessary for the clock to be running between data transfers, the clock must be operating in order to write to non-volatile memory, even though the data being saved may already be resident in the DPP wiper control register.

No clock is necessary upon system power-up. The CAT525’s internal power-on reset circuitry loads data from non-volatile memory to the DPPs without using the external clock.

As data transfers are edge triggered clean clock transitions are necessary to avoid falsely clocking data into the control registers. Standard CMOS and TTL logic families work well in this regard and it is recommended that any mechanical switches used for breadboarding or device evaluation purposes be debounced by a flip-flop or other suitable debouncing circuit.

V_{REF}

V_{REF}, the voltage applied between pins V_{REFH} &V_{REFL}, sets the configured DPP's Zero to Full Scale output range where V_{REFL} = Zero and V_{REFH} = Full Scale. V_{REF} can span the full power supply range or just a fraction of it. In typical applications V_{REFH} &V_{REFL} are connected across the power supply rails. When using less than the full supply voltage be mindfull of the limits placed on V_{REFH} and V_{REFL} as specified in the References section of DC Electrical Characteristics.

READY/$\overline{BUSY}$

When saving data to non-volatile memory, the Ready/Busy ouput (RDY/$\overline{BSY}$) signals the start and duration of the erase/write cycle. Upon receiving a command to store data (PROG goes high) RDY/$\overline{BSY}$ goes low and remains low until the programming cycle is complete. During this time the CAT525 will ignore any data appearing at DI and no data will be output on DO.

RDY/$\overline{BSY}$ is internally ANDed with a low voltage detector circuit monitoring V_{DD}. If V_{DD} is below the minimum value required for EEPROM programming, RDY/$\overline{BSY}$ will remain high following the program command indicating a failure to record the desired data in non-volatile memory.

DATA OUTPUT

Data is output serially by the CAT525, LSB first, via the Data Out (DO) pin following the reception of a start bit and two address bits by the Data Input (DI). DO becomes active whenever CS goes high and resumes its high impedance Tri-State mode when CS returns low. Tri-Stating the DO pin allows several 525s to share a single serial data line and simplifies interfacing multiple 525s to a microprocessor.

WRITING TO MEMORY

Programming the CAT525's non-volatile memory is accomplished through the control signals: Chip Select (CS) and Program (PROG). With CS high, a start bit followed by a two bit DPP address and eight data bits are clocked into the DPP wiper control register via the DI pin. Data enters on the clock's rising edge. The DPP output changes to its new setting on the clock cycle following D7, the last data bit.

Programming is accomplished by bringing PROG high sometime after the start bit and at least 150 ns prior to the rising edge of the clock cycle immediately following the D7 bit. Two clock cycles after the D7 bit the DPP control register will be ready to receive the next set of address and data bits. The clock must be kept running throughout the programming cycle. Internal control circuitry takes care of generating and ramping up the programming voltage for data transfer to the non-volatile memory cells. The CAT525's non-volatile memory cells will endure over 100,000 write cycles and will retain data for a minimum of 20 years without being refreshed.

READING DATA

Each time data is transferred into a DPP wiper control register currently held data is shifted out via the D0 pin, thus in every data transaction a read cycle occurs. Note, however, that the reading process is destructive. Data must be removed from the register in order to be read. Figure 2 depicts a Read Only cycle in which no change occurs in the DPP's output. This feature allows µPs to poll DPPs for their current setting without disturbing the output voltage but it assumes that the setting being read is also stored in non-volatile memory so that it can be restored at the end of the read cycle. In Figure 2 CS returns low before the 13th clock cycle completes. In doing so the non-volatile memory setting is reloaded into the DPP wiper control register. Since this value is the

Figure 1. Writing to Memory

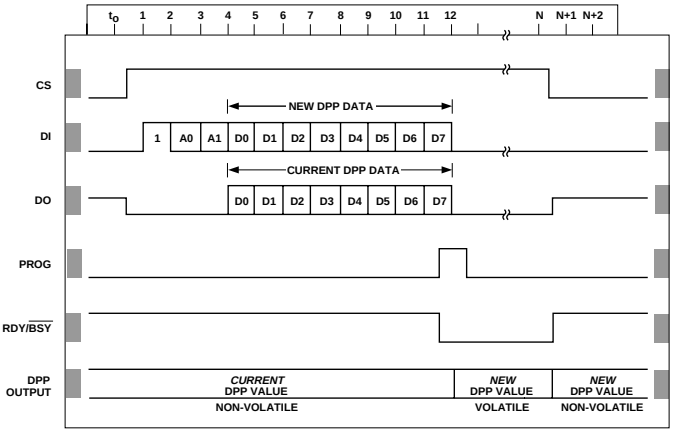
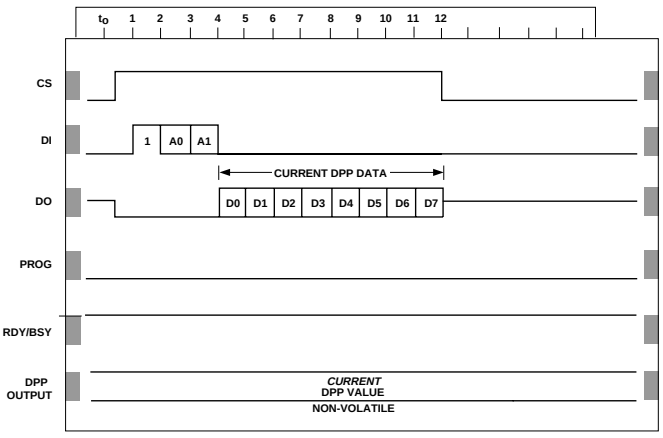


Figure 2. Reading from Memory



same as that which had been there previously no change in the DPP's output is noticed. Had the value held in the control register been different from that stored in non-volatile memory then *a change would occur* at the read cycle's conclusion.

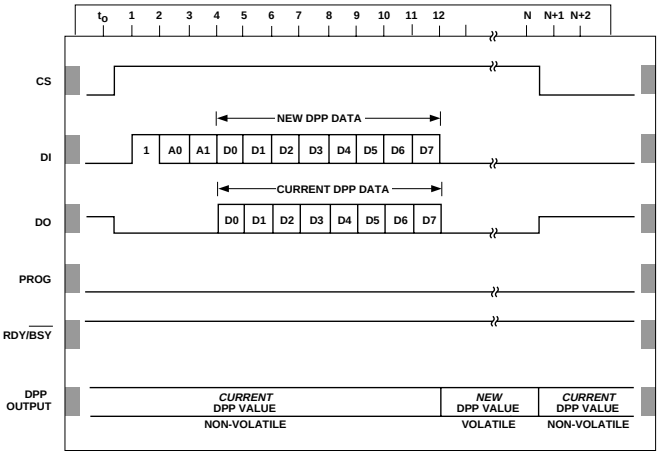
TEMPORARILY CHANGE OUTPUT

The CAT525 allows temporary changes in DPP's output to be made without disturbing the settings retained in non-volatile memory. This feature is particularly useful when testing for a new output setting and allows for user adjustment of preset or default values without losing the original factory settings.

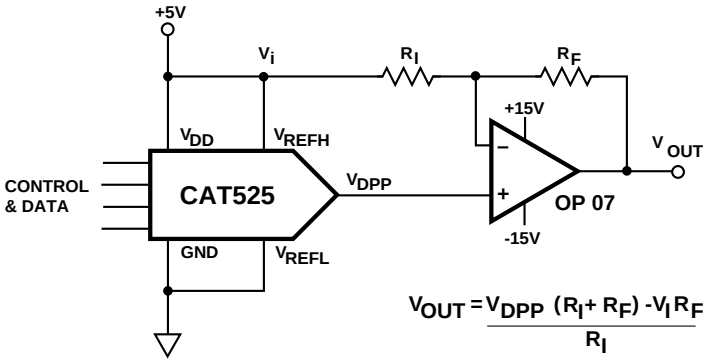
Figure 3 shows the control and data signals needed to effect a temporary output change. DPP settings may be changed as many times as required and can be made to any of the four DPPs in any order or sequence. The temporary setting(s) remain in effect long as CS remains high. When CS returns low all four DPPs will return to the output values stored in non-volatile memory.

When it is desired to save a new setting acquired using this feature, the new value must be reloaded into the DPP control register prior to programming. This is because the CAT525's internal control circuitry discards from the programming register the new data two clock cycles after receiving it if no PROG signal is received.

Figure 3. Temporary Change in Output



APPLICATION CIRCUITS



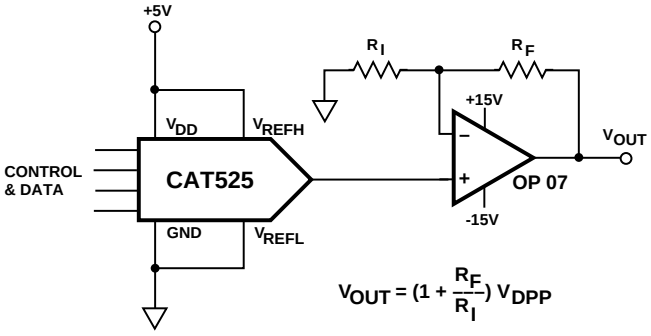
$$V_{OUT} = \frac{V_{DPP}\,(R_I + R_F) - V_I R_F}{R_I}$$

For $R_I = R_F$

$$V_{OUT} = 2V_{DPP} - V_I$$

DPP INPUT MSB	DPP INPUT LSB	DPP OUTPUT $V_{DPP} = \frac{CODE}{255}(V_{FS} - V_{ZERO}) + V_{ZERO}$; $V_{FS} = 0.99\,V_{REF}$; $V_{ZERO} = 0.01\,V_{REF}$	ANALOG OUTPUT $V_{REF} = 5V$; $R_I = R_F$
1111	1111	$\frac{255}{255}(.98\,V_{REF}) + .01\,V_{REF} = .990\,V_{REF}$	$V_{OUT} = +4.90V$
1000	0000	$\frac{128}{255}(.98\,V_{REF}) + .01\,V_{REF} = .502\,V_{REF}$	$V_{OUT} = +0.02V$
0111	1111	$\frac{127}{255}(.98\,V_{REF}) + .01\,V_{REF} = .498\,V_{REF}$	$V_{OUT} = -0.02V$
0000	0001	$\frac{1}{255}(.98\,V_{REF}) + .01\,V_{REF} = .014\,V_{REF}$	$V_{OUT} = -4.86V$
0000	0000	$\frac{0}{255}(.98\,V_{REF}) + .01\,V_{REF} = .010\,V_{REF}$	$V_{OUT} = -4.90V$

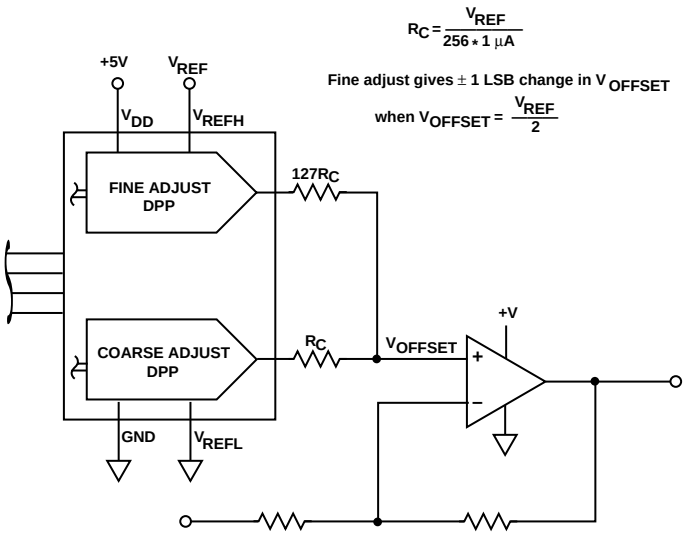
Bipolar DPP Output



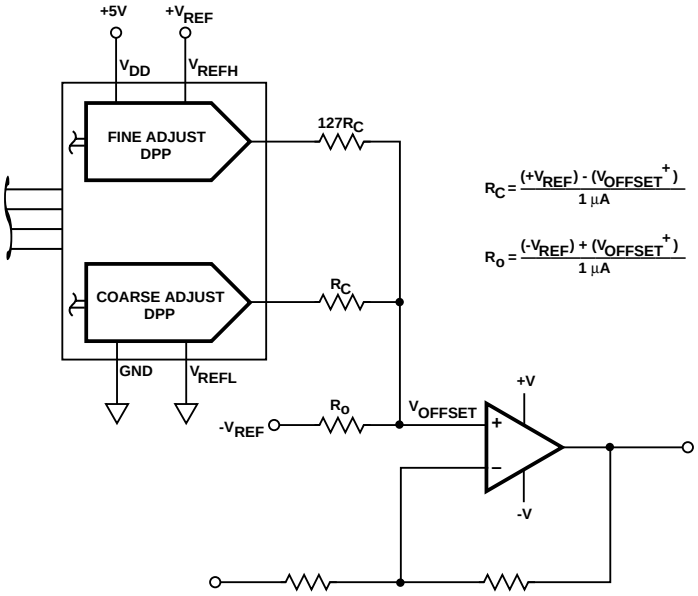
$$V_{OUT} = \left(1 + \frac{R_F}{R_I}\right) V_{DPP}$$

Amplified DPP Output

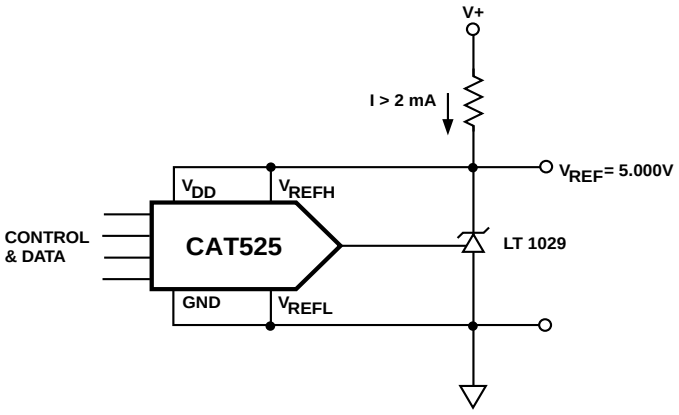
APPLICATION CIRCUITS (Cont.)



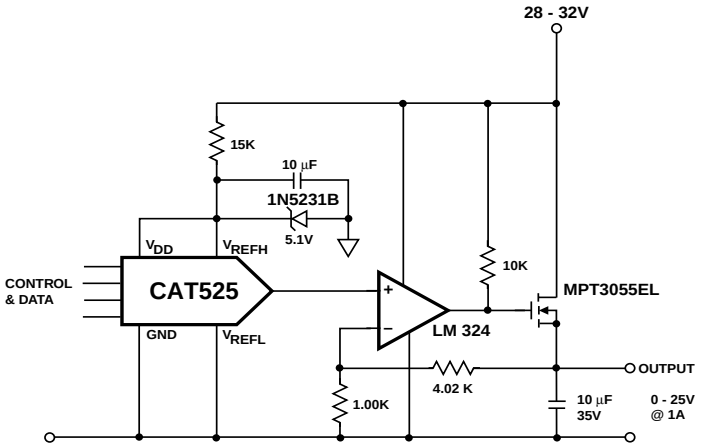
Coarse-Fine Offset Control by Averaging DPP Outputs for Single Power Supply Systems



Coarse-Fine Offset Control by Averaging DPP Outputs for Dual Power Supply Systems

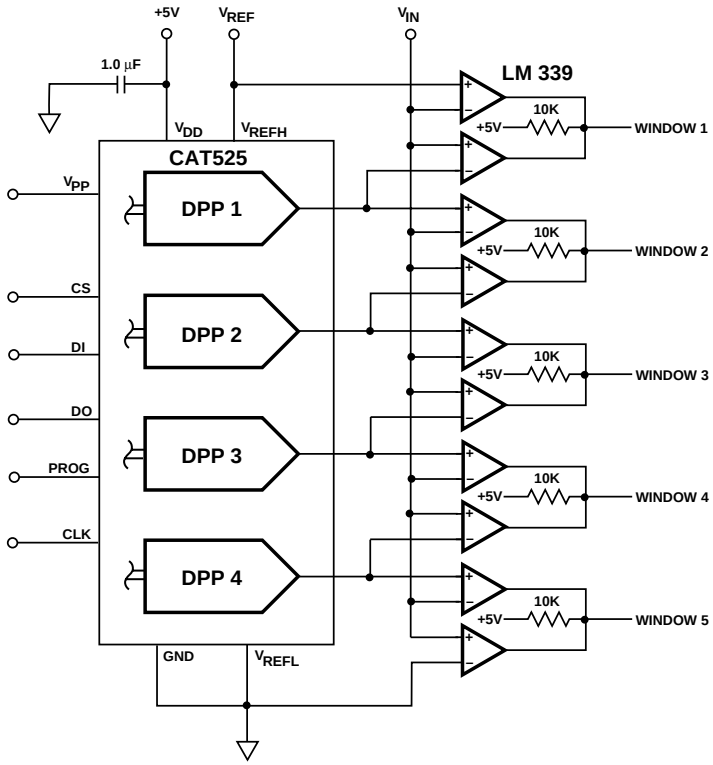


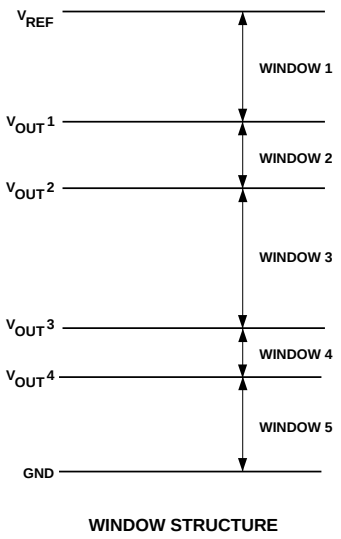
Digitally Trimmed Voltage Reference



Digitally Controlled Voltage Reference

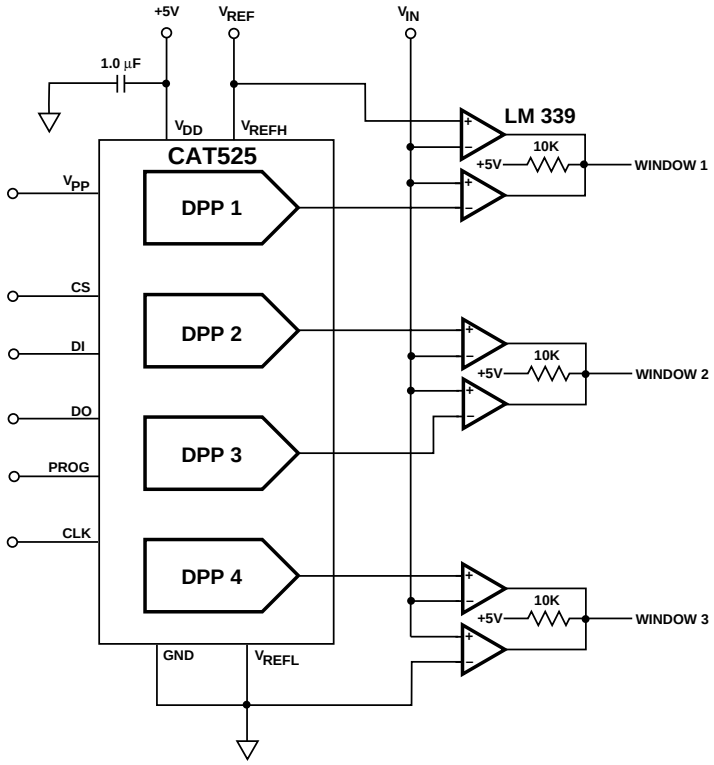
APPLICATION CIRCUITS (Cont.)

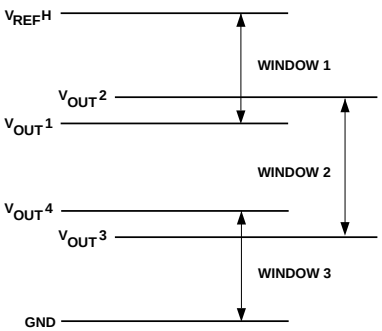




WINDOW STRUCTURE

Staircase Window Comparator

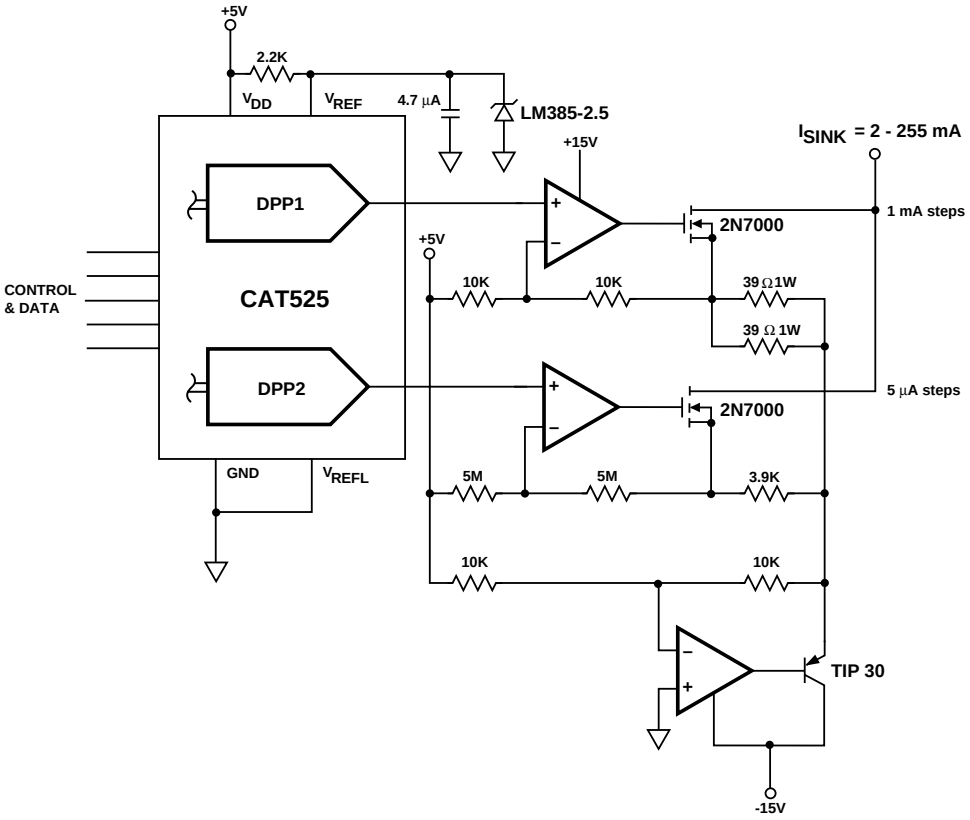




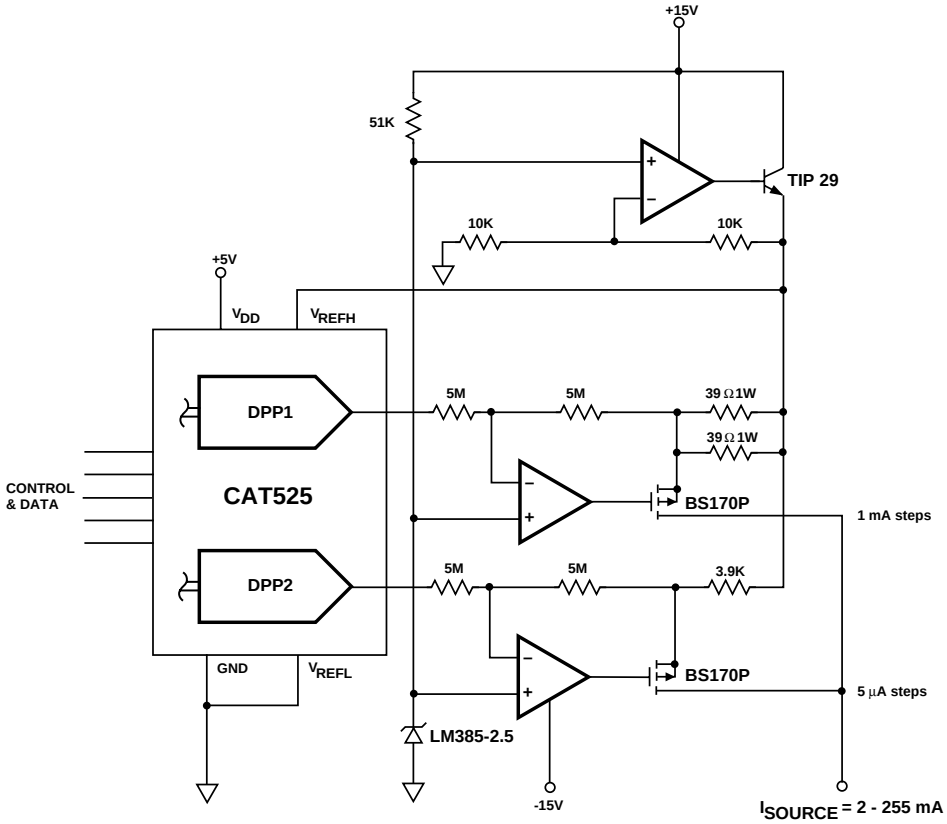
WINDOW STRUCTURE

Overlapping Window Comparator

APPLICATION CIRCUITS (Cont.)

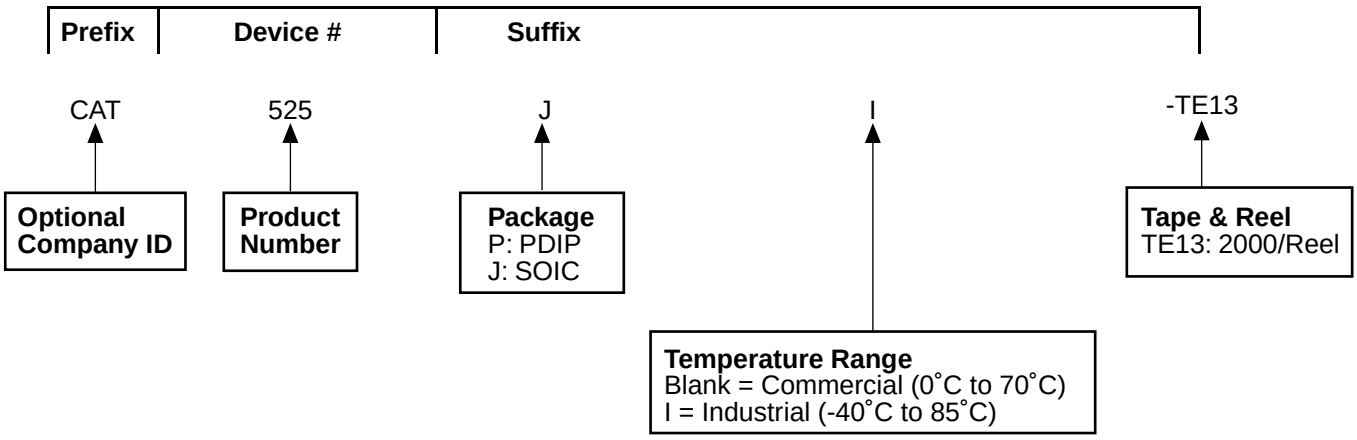


Current Sink with 4 Decades of Resolution



Current Source with 4 Decades of Resolution

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a CAT525JI-TE13 (SOIC, Industrial Temperature, Tape & Reel)

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Revison: B
Issue Date: 3/22/02
Type: Final

CAT5111

100-Tap Digitally Programmable Potentiometer (DPP™) with Buffered Wiper

FEATURES

- **100-position linear taper potentiometer**
- **Non-volatile NVRAM wiper storage; buffered wiper**
- **Low power CMOS technology**
- **Single supply operation: 2.5V-6.0V**
- **Increment up/down serial interface**
- **Resistance values: 10kΩ, 50kΩ and 100kΩ**
- **Available in PDIP, SOIC, TSSOP and MSOP packages**

APPLICATIONS

- **Automated product calibration**
- **Remote control adjustments**
- **Offset, gain and zero control**
- **Tamper-proof calibrations**
- **Contrast, brightness and volume controls**
- **Motor controls and feedback systems**
- **Programmable analog functions**

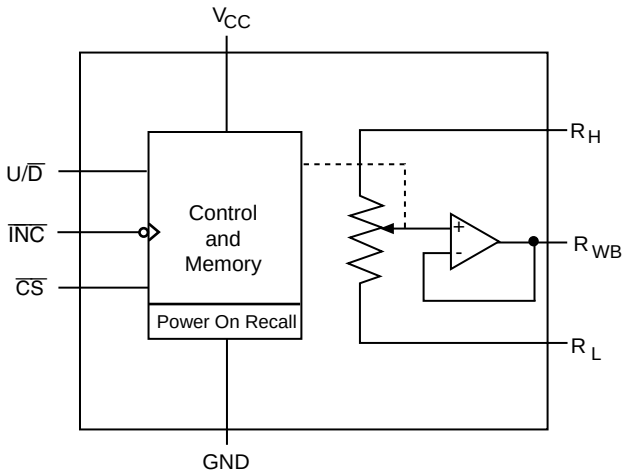
DESCRIPTION

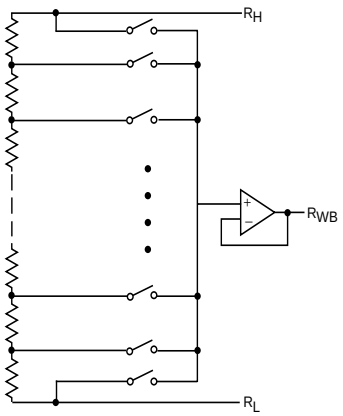
The CAT5111 is a single digitally programmable potentiometer (DPP™) designed as a electronic replacement for mechanical potentiometers and trim pots. Ideal for automated adjustments on high volume production lines, they are also well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous or remote environment.

The CAT5111 contains a 100-tap series resistor array connected between two terminals R_H and R_L. An up/down counter and decoder that are controlled by three input pins, determines which tap is connected to the wiper, R_{WB}. The CAT5111 wiper is buffered by an op amp that operates rail to rail. The wiper setting, stored in non-volatile NVRAM memory, is not lost when the device is powered down and is automatically recalled when power is returned. The wiper can be adjusted to test new system values without effecting the stored setting. Wiper-control of the CAT5111 is accomplished with three input control pins, $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$. The $\overline{INC}$ input increments the wiper in the direction which is determined by the logic state of the U/$\overline{D}$ input. The $\overline{CS}$ input is used to select the device and also store the wiper position prior to power down.

The digitally programmable potentiometer can be used as a three-terminal resistive divider or as a two-terminal variable resistor. DPPs bring variability and programmability to a broad range of applications and are used primarily to control, regulate or adjust a characteristic or parameter of an analog circuit.

FUNCTIONAL DIAGRAM

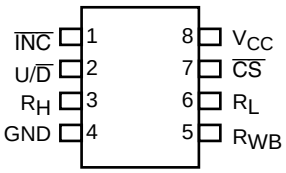




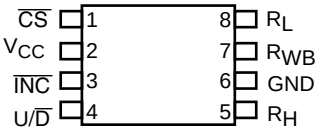
Electronic Potentiometer Implementation

PIN CONFIGURATION

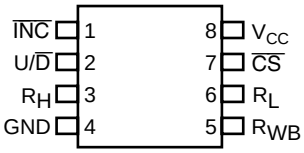
PDIP/SOIC Package



TSSOP Package



MSOP Package



PIN FUNCTIONS

Pin Name	Function
$\overline{INC}$	Increment Control
U/$\overline{D}$	Up/Down Control
R_H	Potentiometer High Terminal
GND	Ground
R_{WB}	Buffered Wiper Terminal
R_L	Potentiometer Low Terminal
$\overline{CS}$	Chip Select
V_{CC}	Supply Voltage

PIN DESCRIPTIONS

$\overline{INC}$: Increment Control Input

The $\overline{INC}$ input (on the falling edge) moves the wiper in the up or down direction determined by the condition of the U/$\overline{D}$ input.

U/$\overline{D}$: Up/Down Control Input

The U/$\overline{D}$ input controls the direction of the wiper movement. When in a high state and $\overline{CS}$ is low, any high-to-low transition on $\overline{INC}$ will cause the wiper to move one increment toward the R_H terminal. When in a low state and $\overline{CS}$ is low, any high-to-low transition on $\overline{INC}$ will cause the wiper to move one increment towards the R_L terminal.

R_H: High End Potentiometer Terminal

R_H is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the R_L terminal. Voltage applied to the R_H terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND.

R_{WB}: Wiper Potentiometer Terminal (Buffered)

R_{WB} is the buffered wiper terminal of the potentiometer. Its position on the resistor array is controlled by the control inputs, $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$.

R_L: Low End Potentiometer Terminal

R_L is the low end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the R_H terminal. Voltage applied to the R_L terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND. R_L and R_H are electrically interchangeable.

$\overline{CS}$: Chip Select

The chip select input is used to activate the control input of the CAT5111 and is active low. When in a high state, activity on the $\overline{INC}$ and U/$\overline{D}$ inputs will not affect or change the position of the wiper.

DEVICE OPERATION

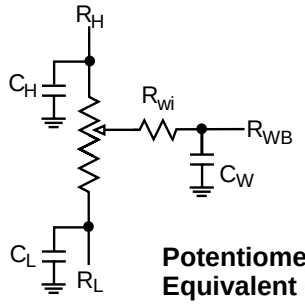
The CAT5111 operates like a digitally controlled potentiometer with R_H and R_L equivalent to the high and low terminals and R_{WB} equivalent to the mechanical potentiometer's wiper. There are 100 available tap positions including the resistor end points, R_H and R_L. There are 99 resistor elements connected in series between the R_H and R_L terminals. The wiper terminal is connected to one of the 100 taps and controlled by three inputs, $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$. These inputs control a seven-bit up/down counter whose output is decoded to select the wiper position. The selected wiper position can be stored in nonvolatile memory using the $\overline{INC}$ and $\overline{CS}$ inputs.

With $\overline{CS}$ set LOW the CAT5111 is selected and will respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ wil increment or decrement the wiper (depending on the state of the U/$\overline{D}$ input and seven-bit counter). The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH. When the CAT5111 is powered-down, the last stored wiper counter position is maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is set to the value stored.

With $\overline{INC}$ set low, the CAT5111 may be de-selected and powered down without storing the current wiper position in nonvolatile memory. This allows the system to always power up to a preset value stored in nonvolatile memory.

OPERATING MODES

$\overline{INC}$	$\overline{CS}$	U/$\overline{D}$	Operation
High to Low	Low	High	Wiper toward R_H
High to Low	Low	Low	Wiper toward R_L
High	Low to High	X	Store Wiper Position
Low	Low to High	X	No Store, Return to Standby
X	High	X	Standby



Potentiometer Equivalent Circuit

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
V_{CC} to GND	–0.5V to +7V
Inputs	
$\overline{CS}$ to GND	–0.5V to V_{CC} +0.5V
$\overline{INC}$ to GND	–0.5V to V_{CC} +0.5V
U/$\overline{D}$ to GND	–0.5V to V_{CC} +0.5V
R_H to GND	–0.5V to V_{CC} +0.5V
R_L to GND	–0.5V to V_{CC} +0.5V
R_{WB} to GND	–0.5V to V_{CC} +0.5V
Operating Ambient Temperature	
Commercial ('C' or Blank suffix)	0°C to +70°C
Industrial ('I' suffix)	– 40°C to +85°C
Junction Temperature	+150°C
Storage Temperature	–65°C to +150°C
Lead Soldering (10 sec max)	+300°C

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Absolute Maximum Ratings are limited values applied individually while other parameters are within specified operating conditions, and functional operation at any of these conditions is NOT implied. Device performance and reliability may be impaired by exposure to absolute rating conditions for extended periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Test Method	Min	Typ	Max	Units
V_{ZAP}(1)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000			Volts
I_{LTH}(1)(2)	Latch-Up	JEDEC Standard 17	100			mA
T_{DR}	Data Retention	MIL-STD-883, Test Method 1008	100			Years
N_{END}	Endurance	MIL-STD-883, Test Method 1003	1,000,000			Stores

DC Electrical Characteristics: V_{CC} = +2.5V to +6.0V unless otherwise specified

Power Supply

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Operating Voltage Range		2.5	—	6.0	V
I_{CC1}	Supply Current (Increment)	V_{CC} = 6V, f = 1MHz, I_W=0	—	—	200	µA
		V_{CC} = 6V, f = 250kHz, I_W=0	—	—	100	
I_{CC2}	Supply Current (Write)	Programming, V_{CC} = 6V	—	—	1	mA
		V_{CC} = 3V	—	—	500	µA
ISB_1 (2)	Supply Current (Standby)	CS=V_{CC}-0.3V	—	75	150	µA
		U/D, INC=V_{CC}-0.3V or GND				

Logic Inputs

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	Input Leakage Current	V_{IN} = V_{CC}	—	—	10	µA
I_{IL}	Input Leakage Current	V_{IN} = 0V	—	—	–10	µA
V_{IH1}	TTL High Level Input Voltage	4.5V ≤ V_{CC} ≤ 5.5V	2	—	V_{CC}	V
V_{IL1}	TTL Low Level Input Voltage		0	—	0.8	V
V_{IH2}	CMOS High Level Input Voltage	2.5V ≤ V_{CC} ≤ 6V	V_{CC} x 0.7	—	V_{CC} + 0.3	V
V_{IL2}	CMOS Low Level Input Voltage		-0.3	—	V_{CC} x 0.2	V

NOTES: (1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} + 1V
(3) I_W=source or sink
(4) These parameters are periodically sampled and are not 100% tested.

Potentiometer Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{POT}	Potentiometer Resistance	-10 Device		10		kΩ
		-50 Device		50		
		-00 Device		100		
	Pot Resistance Tolerance				±15	%
V_{RH}	Voltage on R_H pin		0		V_{CC}	V
V_{RL}	Voltage on R_L pin		0		V_{CC}	V
	Resolution			1		%
INL	Integral Linearity Error	$I_W \le 2\mu A$		0.5	1	LSB
DNL	Differential Linearity Error	$I_W \le 2\mu A$		0.25	0.5	LSB
R_{OUT}	Buffer Output Resistance	$.05V_{CC} \le V_{WB} \le .95V_{CC}$, V_{CC}=5V			1	Ω
I_{OUT}	Buffer Output Current	$.05V_{CC} \le V_{WB} \le .95V_{CC}$, V_{CC}=5V			3	mA
TC_{RPOT}	TC of Pot Resistance			300		ppm/ºC
TC_{RATIO}	Ratiometric TC			TBD		ppm/ºC
R_{ISO}	Isolation Resistance			TBD		Ω
$C_{RH}/C_{RL}/C_{RW}$	Potentiometer Capacitances			8/8/25		pF
fc	Frequency Response	Passive Attenuator, 10kΩ		1.7		MHz
$V_{WB(SWING)}$	Output Voltage Range	$I_{OUT} \le 100\mu A$, V_{CC}=5V	$0.01V_{CC}$		$.99V_{CC}$	

AC CONDITIONS OF TEST

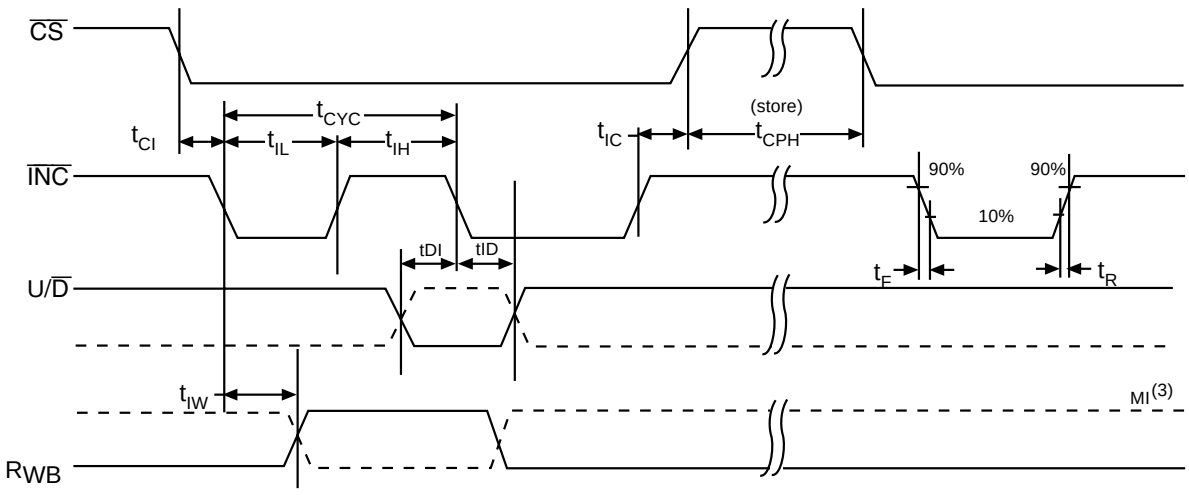
V_{CC} Range	$2.5V \le V_{CC} \le 6V$
Input Pulse Levels	$0.2V_{CC}$ to $0.7V_{CC}$
Input Rise and Fall Times	10ns
Input Reference Levels	$0.5V_{CC}$

AC OPERATING CHARACTERISTICS:

V_{CC} = +2.5V to +6.0V, $V_H = V_{CC}$, V_L = 0V, unless otherwise specified

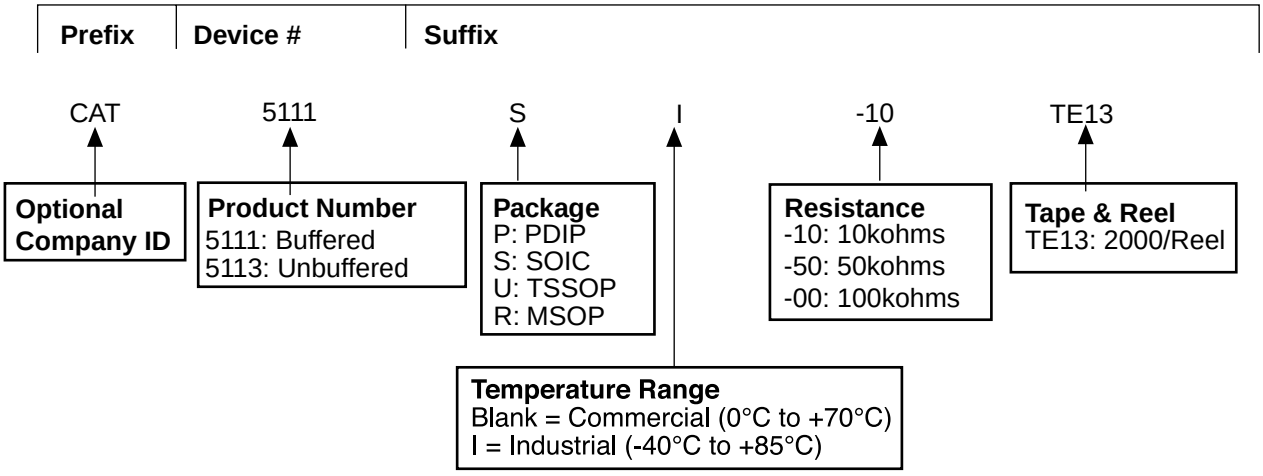
Symbol	Parameter	Min	Typ(1)	Max	Units
t_{CI}	$\overline{CS}$ to INC Setup	100	—	—	ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	50	—	—	ns
t_{ID}	U/$\overline{D}$ to $\overline{INC}$ Hold	100	—	—	ns
t_{IL}	$\overline{INC}$ LOW Period	250	—	—	ns
t_{IH}	$\overline{INC}$ HIGH Period	250	—	—	ns
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1	—	—	µs
t_{CPH}	$\overline{CS}$ Deselect Time (NO STORE)	100	—	—	ns
t_{CPH}	$\overline{CS}$ Deselect Time (STORE)	10	—	—	ms
t_{IW}	$\overline{INC}$ to V_{OUT} Change	—	1	5	µs
t_{CYC}	$\overline{INC}$ Cycle Time	1	—	—	µs
$t_{R,}$ t_F(2)	$\overline{INC}$ Input Rise and Fall Time	—	—	500	µs
t_{PU}(2)	Power-up to Wiper Stable	—	—	1	msec
t_{WR}	Store Cycle	—	5	10	ms

A. C. TIMING



(1) Typical values are for T_A=25˚C and nominal supply voltage.
(2) This parameter is periodically sampled and not 100% tested.
(3) MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a CAT5111 SI-10TE13 (SOIC, 10K Ohms, Industrial Temperature, Tape & Reel)

CATALYST

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Revison: I
Issue date: 04/17/02
Type: Final

CAT5112

32-Tap Digitally Programmable Potentiometer (DPP™) with Buffered Wiper

FEATURES

- **32-position linear taper potentiometer**
- **Non-volatile NVRAM wiper storage; buffered wiper**
- **Low power CMOS technology**
- **Single supply operation: 2.5V-6.0V**
- **Increment up/down serial interface**
- **Resistance values: 10kΩ, 50kΩ and 100kΩ**
- **Available in PDIP, SOIC, TSSOP and MSOP packages**

APPLICATIONS

- **Automated product calibration**
- **Remote control adjustments**
- **Offset, gain and zero control**
- **Tamper-proof calibrations**
- **Contrast, brightness and volume controls**
- **Motor controls and feedback systems**
- **Programmable analog functions**

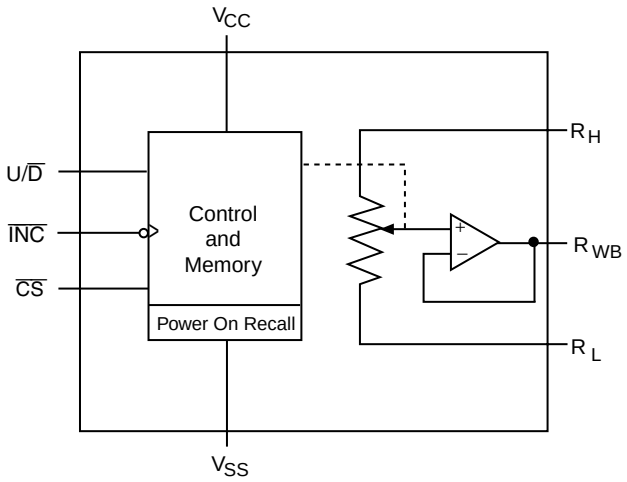
DESCRIPTION

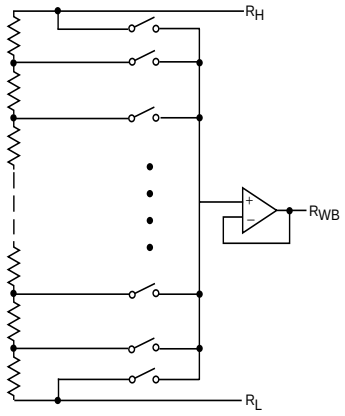
The CAT5112 is a single digitally programmable potentiometer (DPP™) designed as a electronic replacement for mechanical potentiometers and trim pots. Ideal for automated adjustments on high volume production lines, they are also well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous or remote environment.

The CAT5112 contains a 32-tap series resistor array connected between two terminals R_H and R_L. An up/down counter and decoder that are controlled by three input pins, determines which tap is connected to the wiper, R_{WB}. The CAT5112 wiper is buffered by an op amp that operates rail to rail. The wiper setting, stored in non-volatile NVRAM memory, is not lost when the device is powered down and is automatically recalled when power is returned. The wiper can be adjusted to test new system values without effecting the stored setting. Wiper-control of the CAT5112 is accomplished with three input control pins, $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$. The $\overline{INC}$ input increments the wiper in the direction which is determined by the logic state of the U/$\overline{D}$ input. The $\overline{CS}$ input is used to select the device and also store the wiper position prior to power down.

The digitally programmable potentiometer can be used as a three-terminal resistive divider or as a two-terminal variable resistor. DPPs bring variability and programmability to a broad range of applications and are used primarily to control, regulate or adjust a characteristic or parameter of an analog circuit.

FUNCTIONAL DIAGRAM



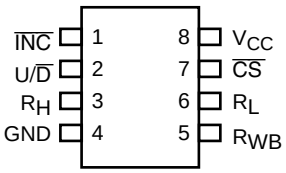


Electronic Potentiometer Implementation

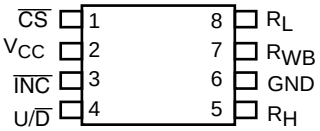
Doc. No. 2002, Rev. F

PIN CONFIGURATION

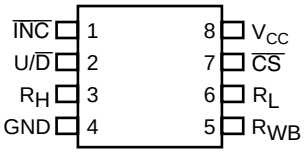
PDIP/SOIC Package



TSSOP Package



MSOP Package



PIN FUNCTIONS

Pin Name	Function
$\overline{INC}$	Increment Control
U/$\overline{D}$	Up/Down Control
R_H	Potentiometer High Terminal
GND	Ground
R_{WB}	Buffered Wiper Terminal
R_L	Potentiometer Low Terminal
$\overline{CS}$	Chip Select
V_{CC}	Supply Voltage

PIN DESCRIPTIONS

$\overline{INC}$: Increment Control Input

The $\overline{INC}$ input (on the falling edge) moves the wiper in the up or down direction determined by the condition of the U/$\overline{D}$ input.

U/$\overline{D}$: Up/Down Control Input

The U/$\overline{D}$ input controls the direction of the wiper movement. When in a high state and $\overline{CS}$ is low, any high-to-low transition on $\overline{INC}$ will cause the wiper to move one increment toward the R_H terminal. When in a low state and $\overline{CS}$ is low, any high-to-low transition on $\overline{INC}$ will cause the wiper to move one increment towards the R_L terminal.

R_H: High End Potentiometer Terminal

R_H is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the R_L terminal. Voltage applied to the R_H terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND.

R_{WB}: Wiper Potentiometer Terminal (Buffered)

R_{WB} is the buffered wiper terminal of the potentiometer. Its position on the resistor array is controlled by the control inputs, $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$.

R_L: Low End Potentiometer Terminal

R_L is the low end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the R_H terminal. Voltage applied to the R_L terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND. R_L and R_H are electrically interchangeable.

$\overline{CS}$: Chip Select

The chip select input is used to activate the control input of the CAT5112 and is active low. When in a high state, activity on the $\overline{INC}$ and U/$\overline{D}$ inputs will not affect or change the position of the wiper.

DEVICE OPERATION

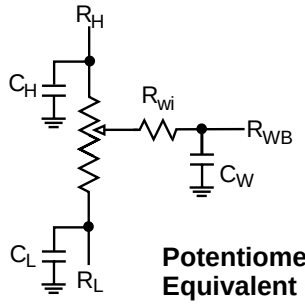
The CAT5112 operates like a digitally controlled potentiometer with R_H and R_L equivalent to the high and low terminals and R_{WB} equivalent to the mechanical potentiometer's wiper. There are 32 available tap positions including the resistor end points, R_H and R_L. There are 31 resistor elements connected in series between the R_H and R_L terminals. The wiper terminal is connected to one of the 32 taps and controlled by three inputs, $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$. These inputs control a five-bit up/down counter whose output is decoded to select the wiper position. The selected wiper position can be stored in nonvolatile memory using the $\overline{INC}$ and $\overline{CS}$ inputs.

With $\overline{CS}$ set LOW the CAT5112 is selected and will respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ wil increment or decrement the wiper (depending on the state of the U/$\overline{D}$ input and five-bit counter). The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH. When the CAT5112 is powered-down, the last stored wiper counter position is maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is set to the value stored.

With $\overline{INC}$ set low, the CAT5112 may be de-selected and powered down without storing the current wiper position in nonvolatile memory. This allows the system to always power up to a preset value stored in nonvolatile memory.

OPERATING MODES

$\overline{INC}$	$\overline{CS}$	U/$\overline{D}$	Operation
High to Low	Low	High	Wiper toward H
High to Low	Low	Low	Wiper toward L
High	Low to High	X	Store Wiper Position
Low	Low to High	X	No Store, Return to Standby
X	High	X	Standby



Potentiometer Equivalent Circuit

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- V_{CC} to GND: -0.5V to +7V

Inputs
- $\overline{CS}$ to GND: -0.5V to V_{CC} +0.5V
- $\overline{INC}$ to GND: -0.5V to V_{CC} +0.5V
- U/$\overline{D}$ to GND: -0.5V to V_{CC} +0.5V
- R_H to GND: -0.5V to V_{CC} +0.5V
- R_L to GND: -0.5V to V_{CC} +0.5V
- R_{WB} to GND: -0.5V to V_{CC} +0.5V

Operating Ambient Temperature
- Commercial ('C' or Blank suffix): 0°C to +70°C
- Industrial ('I' suffix): -40°C to +85°C

Junction Temperature: +150°C

Storage Temperature: -65°C to +150°C

Lead Soldering (10 sec max): +300°C

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Absolute Maximum Ratings are limited values applied individually while other parameters are within specified operating conditions, and functional operation at any of these conditions is NOT implied. Device performance and reliability may be impaired by exposure to absolute rating conditions for extended periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Test Method	Min	Typ	Max	Units
V_{ZAP}(1)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000			Volts
I_{LTH}(1)(2)	Latch-Up	JEDEC Standard 17	100			mA
T_{DR}	Data Retention	MIL-STD-883, Test Method 1008	100			Years
N_{END}	Endurance	MIL-STD-883, Test Method 1003	1,000,000			Stores

DC Electrical Characteristics: V_{CC} = +2.5V to +6.0V unless otherwise specified

Power Supply

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Operating Voltage Range		2.5	—	6.0	V
I_{CC1}	Supply Current (Increment)	V_{CC} = 6V, f = 1MHz, I_W=0	—	—	200	µA
		V_{CC} = 6V, f = 250kHz, I_W=0	—	—	100	
I_{CC2}	Supply Current (Write)	Programming, V_{CC} = 6V	—	—	1	mA
		V_{CC} = 3V	—	—	500	µA
ISB_1 (2)	Supply Current (Standby)	CS=V_{CC}-0.3V	—	75	150	µA
		U/D, INC=V_{CC}-0.3V or GND				

Logic Inputs

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	Input Leakage Current	V_{IN} = V_{CC}	—	—	10	µA
I_{IL}	Input Leakage Current	V_{IN} = 0V	—	—	–10	µA
V_{IH1}	TTL High Level Input Voltage	4.5V ≤ V_{CC} ≤ 5.5V	2	—	V_{CC}	V
V_{IL1}	TTL Low Level Input Voltage		0	—	0.8	V
V_{IH2}	CMOS High Level Input Voltage	2.5V ≤ V_{CC} ≤ 6V	V_{CC} x 0.7	—	V_{CC} + 0.3	V
V_{IL2}	CMOS Low Level Input Voltage		-0.3	—	V_{CC} x 0.2	V

NOTES: (1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} + 1V
(3) I_W=source or sink
(4) These parameters are periodically sampled and are not 100% tested.

Potentiometer Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{POT}	Potentiometer Resistance	-10 Device		10		kΩ
		-50 Device		50		
		-00 Device		100		
	Pot Resistance Tolerance				±15	%
V_{RH}	Voltage on R_H pin		0		V_{CC}	V
V_{RL}	Voltage on R_L pin		0		V_{CC}	V
	Resolution			1		%
INL	Integral Linearity Error	$I_W \le 2\mu A$		0.5	1	LSB
DNL	Differential Linearity Error	$I_W \le 2\mu A$		0.25	0.5	LSB
R_{OUT}	Buffer Output Resistance	$.05V_{CC} \le V_{WB} \le .95V_{CC}$, V_{CC}=5V			1	Ω
I_{OUT}	Buffer Output Current	$.05V_{CC} \le V_{WB} \le .95V_{CC}$, V_{CC}=5V			3	mA
TC_{RPOT}	TC of Pot Resistance			300		ppm/°C
TC_{RATIO}	Ratiometric TC			TBD		ppm/°C
R_{ISO}	Isolation Resistance			TBD		Ω
$C_{RH}/C_{RL}/C_{RW}$	Potentiometer Capacitances			8/8/25		pF
fc	Frequency Response	Passive Attenuator, 10kΩ		1.7		MHz
$V_{WB(SWING)}$	Output Voltage Range	$I_{OUT} \le 100\mu A$, V_{CC}=5V	$0.01V_{CC}$		$.99V_{CC}$	

AC CONDITIONS OF TEST

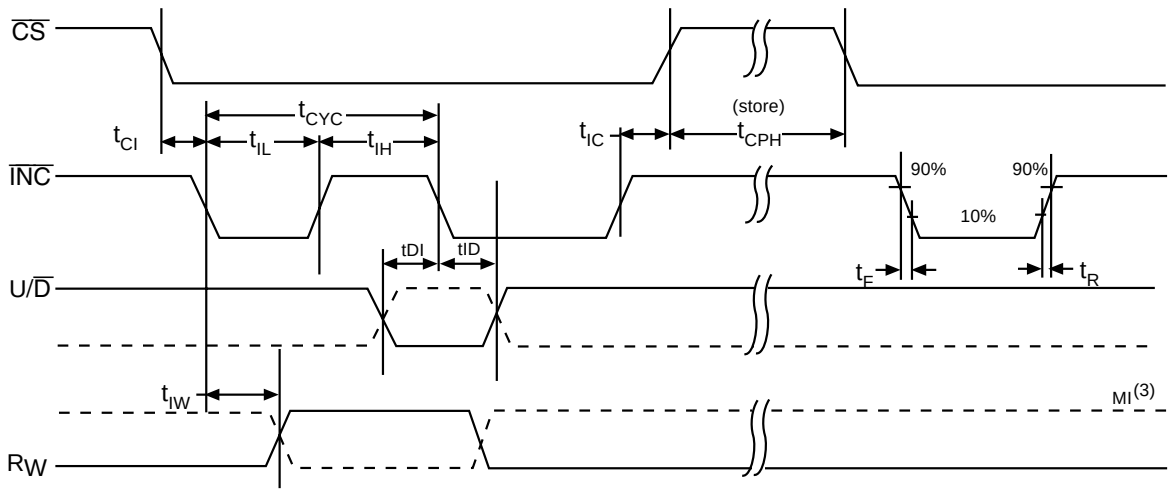
V_{CC} Range	$2.5V \le V_{CC} \le 6V$
Input Pulse Levels	$0.2V_{CC}$ to $0.7V_{CC}$
Input Rise and Fall Times	10ns
Input Reference Levels	$0.5V_{CC}$

AC OPERATING CHARACTERISTICS:

V_{CC} = +2.5V to +6.0V, $V_H = V_{CC}$, V_L = 0V, unless otherwise specified

Symbol	Parameter	Min	Typ(1)	Max	Units
t_{CI}	$\overline{CS}$ to INC Setup	100	—	—	ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	50	—	—	ns
t_{ID}	U/$\overline{D}$ to $\overline{INC}$ Hold	100	—	—	ns
t_{IL}	$\overline{INC}$ LOW Period	250	—	—	ns
t_{IH}	$\overline{INC}$ HIGH Period	250	—	—	ns
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1	—	—	µs
t_{CPH}	$\overline{CS}$ Deselect Time (NO STORE)	100	—	—	ns
t_{CPH}	$\overline{CS}$ Deselect Time (STORE)	10	—	—	ms
t_{IW}	$\overline{INC}$ to V_{OUT} Change	—	1	5	µs
t_{CYC}	$\overline{INC}$ Cycle Time	1	—	—	µs
$t_{R,}$ t_F(2)	$\overline{INC}$ Input Rise and Fall Time	—	—	500	µs
t_{PU}(2)	Power-up to Wiper Stable	—	—	1	msec
t_{WR}	Store Cycle	—	5	10	ms

A. C. TIMING



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(3) MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

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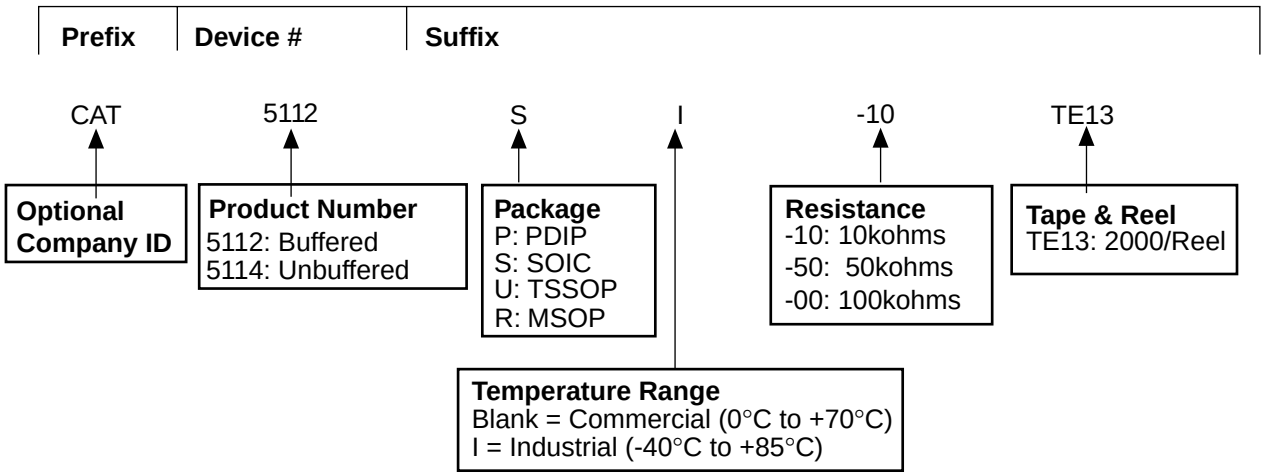

Notes:
(1) The device used in the above example is a CAT5112 SI-10TE13 (SOIC, 10K Ohms, Industrial Temperature, Tape & Reel)

CATALYST

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CAT5113

100-Tap Digitally Programmable Potentiometer (DPP™)

FEATURES

- 100-position linear taper potentiometer
- Non-volatile NVRAM wiper storage
- Low power CMOS technology
- Single supply operation: 2.5V-6.0V
- Increment Up/Down serial interface
- Resistance values: 10kΩ , 50kΩ and 100kΩ
- Available in PDIP, SOIC, TSSOP and MSOP packages

APPLICATIONS

- Automated product calibration
- Remote control adjustments
- Offset, gain and zero control
- Tamper-proof calibrations
- Contrast, brightness and volume controls
- Motor controls and feedback systems
- Programmable analog functions

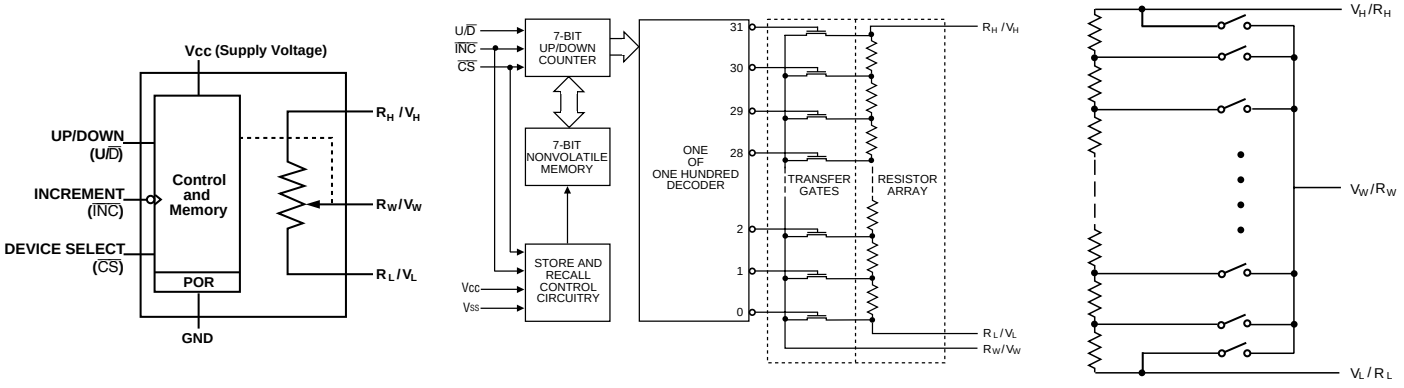
DESCRIPTION

The CAT5113 is a single digitally programmable potentiometer (DPP™) designed as a electronic replacement for mechanical potentiometers and trim pots. Ideal for automated adjustments on high volume production lines, they are also well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous or remote environment.

The CAT5113 contains a 100-tap series resistor array connected between two terminals R_H and R_L. An up/down counter and decoder that are controlled by three input pins, determines which tap is connected to the wiper, R_W. The wiper setting, stored in nonvolatile memory, is not lost when the device is powered down and is automatically reinstated when power is returned. The wiper can be adjusted to test new system values without effecting the stored setting. Wiper-control of the CAT5113 is accomplished with three input control pins, $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$. The $\overline{INC}$ input increments the wiper in the direction which is determined by the logic state of the U/$\overline{D}$ input. The $\overline{CS}$ input is used to select the device and also store the wiper position prior to power down.

The digitally programmable potentiometer can be used as a three-terminal resistive divider or as a two-terminal variable resistor. DPPs bring variability and programmability to a wide variety of applications including control, parameter adjustments, and signal processing.

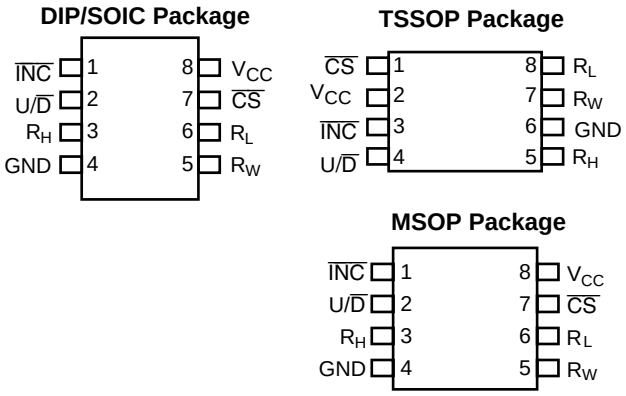
FUNCTIONAL DIAGRAM



GENERAL DETAILED ELECTRONIC POTENTIOMETER IMPLEMENTATION

Doc. No. 2009, Rev. J

PIN CONFIGURATION



PIN FUNCTIONS

Pin Name	Function
$\overline{INC}$	Increment Control
U/$\overline{D}$	Up/Down Control
R_H	Potentiometer High Terminal
GND	Ground
R_W	Potentiometer Wiper Terminal
R_L	Potentiometer Low Terminal
$\overline{CS}$	Chip Select
V_{CC}	Supply Voltage

PIN DESCRIPTIONS

$\overline{INC}$: Increment Control Input

The $\overline{INC}$ input moves the wiper in the up or down direction determined by the condition of the U/$\overline{D}$ input.

U/$\overline{D}$: Up/Down Control Input

The U/$\overline{D}$ input controls the direction of the wiper movement. When in a high state and $\overline{CS}$ is low, any high-to-low transition on $\overline{INC}$ will cause the wiper to move one increment toward the R_H terminal. When in a low state and $\overline{CS}$ is low, any high-to-low transition on $\overline{INC}$ will cause the wiper to move one increment towards the R_L terminal.

R_H: High End Potentiometer Terminal

R_H is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the R_L terminal. Voltage applied to the R_H terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND.

R_W: Wiper Potentiometer Terminal

R_W is the wiper terminal of the potentiometer. Its position on the resistor array is controlled by the control inputs, $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$. Voltage applied to the R_W terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND.

R_L: Low End Potentiometer Terminal

R_L is the low end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the R_H terminal. Voltage applied to the R_L terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND. R_L and R_H are electrically interchangeable.

$\overline{CS}$: Chip Select

The chip select input is used to activate the control input of the CAT5113 and is active low. When in a high state, activity on the $\overline{INC}$ and U/$\overline{D}$ inputs will not affect or change the position of the wiper.

DEVICE OPERATION

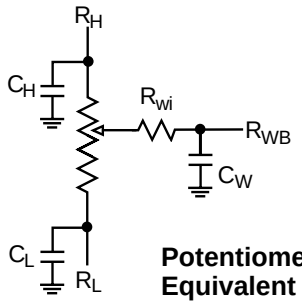
The CAT5113 operates like a digitally controlled potentiometer with R_H and R_L equivalent to the high and low terminals and R_W equivalent to the mechanical potentiometer's wiper. There are 100 available tap positions including the resistor end points, R_H and R_L. There are 99 resistor elements connected in series between the R_H and R_L terminals. The wiper terminal is connected to one of the 100 taps and controlled by three inputs, $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$. These inputs control a seven-bit up/down counter whose output is decoded to select the wiper position. The selected wiper position can be stored in nonvolatile memory using the $\overline{INC}$ and $\overline{CS}$ inputs.

With $\overline{CS}$ set LOW the CAT5113 is selected and will respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ wil increment or decrement the wiper (depending on the state of the U/$\overline{D}$ input and seven-bit counter). The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH. When the CAT5113 is powered-down, the last stored wiper counter position is maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is set to the value stored.

With $\overline{INC}$ set low, the CAT5113 may be de-selected and powered down without storing the current wiper position in nonvolatile memory. This allows the system to always power up to a preset value stored in nonvolatile memory.

OPERATION MODES

$\overline{INC}$	$\overline{CS}$	U/$\overline{D}$	Operation
High to Low	Low	High	Wiper toward H
High to Low	Low	Low	Wiper toward L
High	Low to High	X	Store Wiper Position
Low	Low to High	X	No Store, Return to Standby
X	High	X	Standby



Potentiometer Equivalent Circuit

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- V_{CC} to GND ..... –0.5V to +7V

Inputs
- $\overline{CS}$ to GND ..... –0.5V to V_{CC} +0.5V
- $\overline{INC}$ to GND ..... –0.5V to V_{CC} +0.5V
- U/$\overline{D}$ to GND ..... –0.5V to V_{CC} +0.5V
- H to GND ..... –0.5V to V_{CC} +0.5V
- L to GND ..... –0.5V to V_{CC} +0.5V
- W to GND ..... –0.5V to V_{CC} +0.5V

Operating Ambient Temperature
- Commercial ('C' or Blank suffix) ..... 0°C to +70°C
- Industrial ('I' suffix) ..... – 40°C to +85°C

Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Soldering (10 sec max) ..... +300°C

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Absolute Maximum Ratings are limited values applied individually while other parameters are within specified operating conditions, and functional operation at any of these conditions is NOT implied. Device performance and reliability may be impaired by exposure to absolute rating conditions for extended periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Test Method	Min	Typ	Max	Units
V_{ZAP}(1)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000			Volts
I_{LTH}(1)(2)	Latch-Up	JEDEC Standard 17	100			mA
T_{DR}	Data Retention	MIL-STD-883, Test Method 1008	100			Years
N_{END}	Endurance	MIL-STD-883, Test Method 1003	1,000,000			Stores

DC Electrical Characteristics: V_{CC} = +2.5V to +6.0V unless otherwise specified

Power Supply

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Operating Voltage Range		2.5	—	6.0	V
I_{CC1}	Supply Current (Increment)	V_{CC} = 6V, f = 1MHz, I_W=0	—	—	100	µA
		V_{CC} = 6V, f = 250kHz, I_W=0	—	—	50	
I_{CC2}	Supply Current (Write)	Programming, V_{CC} = 6V	—	—	1	mA
		V_{CC} = 3V	—	—	500	µA
ISB_1 (2)	Supply Current (Standby)	CS=V_{CC}-0.3V	—	—	1	µA
		U/D, INC=V_{CC}-0.3V or GND				

Logic Inputs

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	Input Leakage Current	V_{IN} = V_{CC}	—	—	10	µA
I_{IL}	Input Leakage Current	V_{IN} = 0V	—	—	–10	µA
V_{IH1}	TTL High Level Input Voltage	4.5V ≤ V_{CC} ≤ 5.5V	2	—	V_{CC}	V
V_{IL1}	TTL Low Level Input Voltage		0	—	0.8	V
V_{IH2}	CMOS High Level Input Voltage	2.5V ≤ V_{CC} ≤ 6V	V_{CC} x 0.7	—	V_{CC} + 0.3	V
V_{IL2}	CMOS Low Level Input Voltage		-0.3	—	V_{CC} x 0.2	V

NOTES: (1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} + 1V
(3) I_W=source or sink
(4) These parameters are periodically sampled and are not 100% tested.

Potentiometer Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{POT}	Potentiometer Resistance	-10 Device		10		kΩ
		-50 Device		50		
		-00 Device		100		
	Pot Resistance Tolerance				±15	%
V_{RH}	Voltage on R_H pin		0		V_{CC}	V
V_{RL}	Voltage on R_L pin		0		V_{CC}	V
	Resolution			1%		%
INL	Integral Linearity Error	$I_W \le 2\mu A$		0.5	1	LSB
DNL	Differential Linearity Error	$I_W \le 2\mu A$		0.25	0.5	LSB
R_{Wi}	Wiper Resistance	V_{CC} = 5V, I_W = 1mA			400	Ω
		V_{CC} = 2.5V, I_W = 1mA			1	kΩ
I_W	Wiper Current				1	mA
TC_{RPOT}	TC of Pot Resistance			300		ppm/°C
TC_{RATIO}	Ratiometric TC				20	ppm/°C
R_{ISO}	Isolation Resistance			TBD		Ω
V_N	Noise	100kHz / 1kHz		8/24		$nV/\sqrt{Hz}$
$C_H/C_L/C_W$	Potentiometer Capacitances			8/8/25		pF
fc	Frequency Response	Passive Attenuator, 10kΩ		1.7		MHz

AC CONDITIONS OF TEST

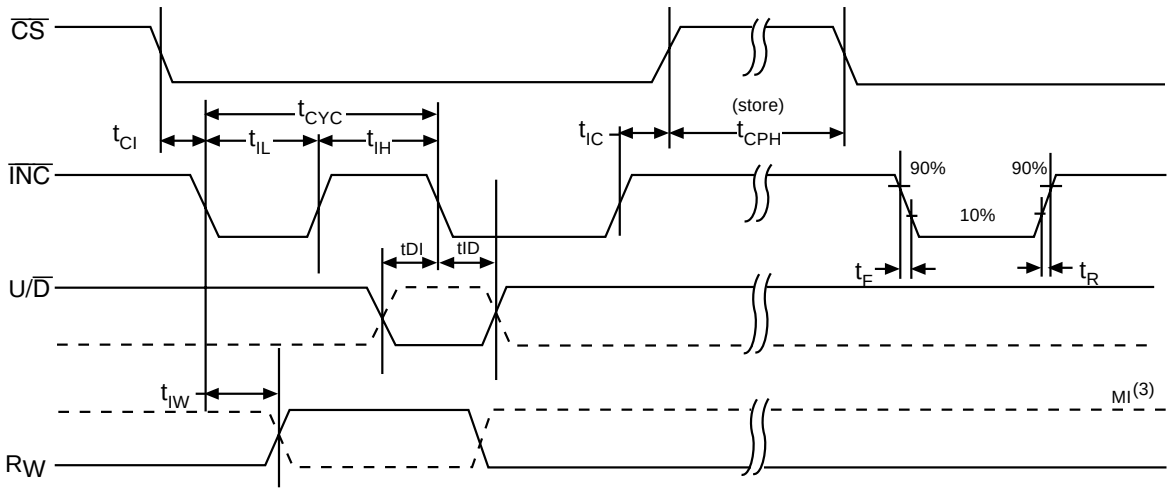
V_{CC} Range	$2.5V \le V_{CC} \le 6V$
Input Pulse Levels	$0.2V_{CC}$ to $0.7V_{CC}$
Input Rise and Fall Times	10ns
Input Reference Levels	$0.5V_{CC}$

AC OPERATING CHARACTERISTICS:

V_{CC} = +2.5V to +6.0V, $V_H = V_{CC}$, V_L = 0V, unless otherwise specified

Symbol	Parameter	Min	Typ(1)	Max	Units
t_{CI}	$\overline{CS}$ to INC Setup	100	—	—	ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	50	—	—	ns
t_{ID}	U/$\overline{D}$ to $\overline{INC}$ Hold	100	—	—	ns
t_{IL}	$\overline{INC}$ LOW Period	250	—	—	ns
t_{IH}	$\overline{INC}$ HIGH Period	250	—	—	ns
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1	—	—	µs
t_{CPH}	$\overline{CS}$ Deselect Time (NO STORE)	100	—	—	ns
t_{CPH}	$\overline{CS}$ Deselect Time (STORE)	10	—	—	ms
t_{IW}	$\overline{INC}$ to V_{OUT} Change	—	1	5	µs
t_{CYC}	$\overline{INC}$ Cycle Time	1	—	—	µs
t_R, t_F(2)	$\overline{INC}$ Input Rise and Fall Time	—	—	500	µs
t_{PU}(2)	Power-up to Wiper Stable	—	—	1	msec
t_{WR}	Store Cycle	—	5	10	ms

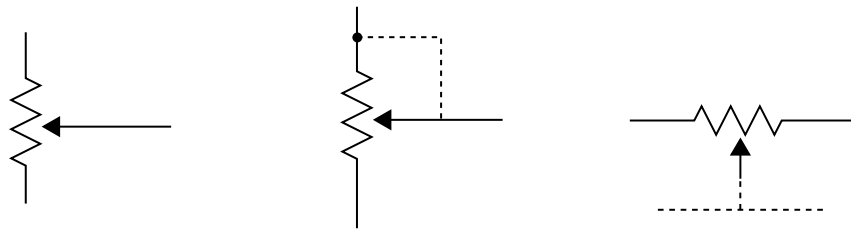
A. C. TIMING



(1) Typical values are for T_A=25˚C and nominal supply voltage.
(2) This parameter is periodically sampled and not 100% tested.
(3) MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

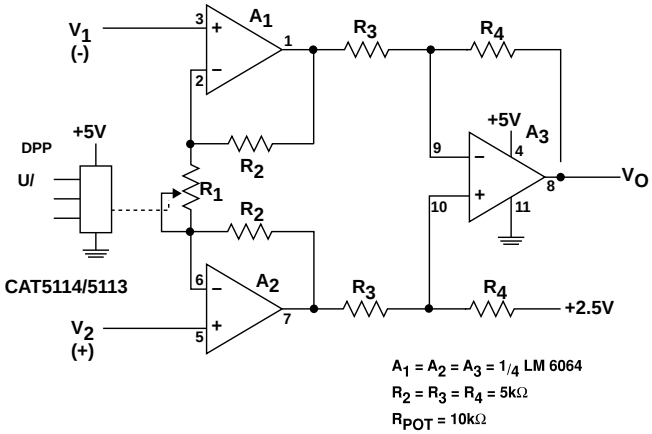
APPLICATIONS INFORMATION

Potentiometer Configurations

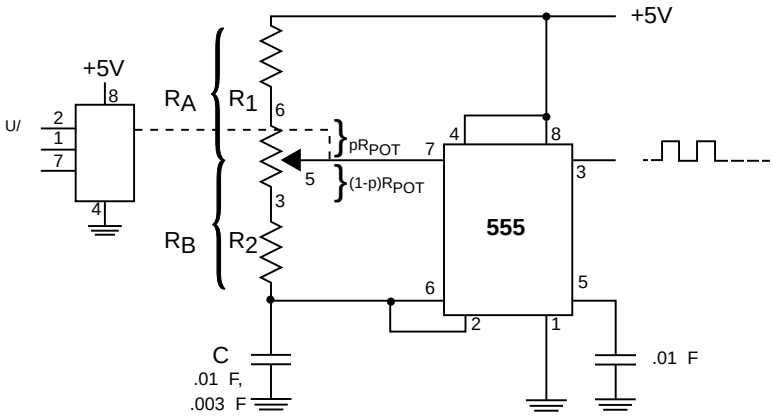


(a) resistive divider (b) variable resistance (c) two-port

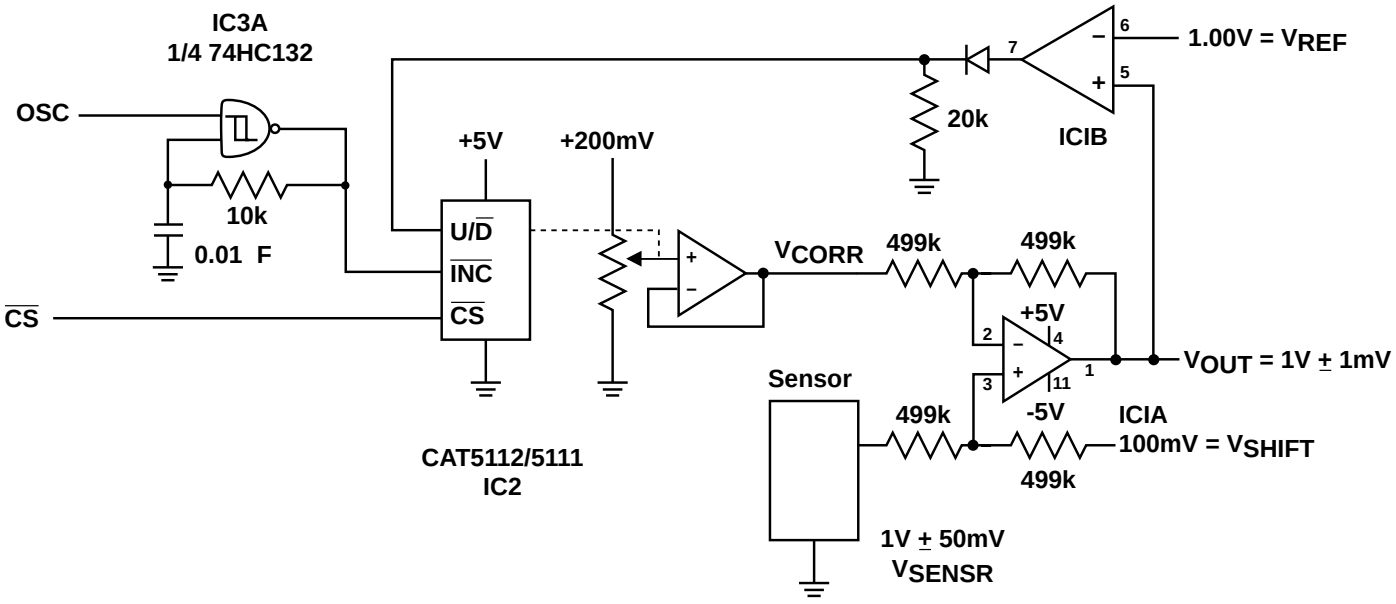
Applications



Programmable Instrumentation Amplifier

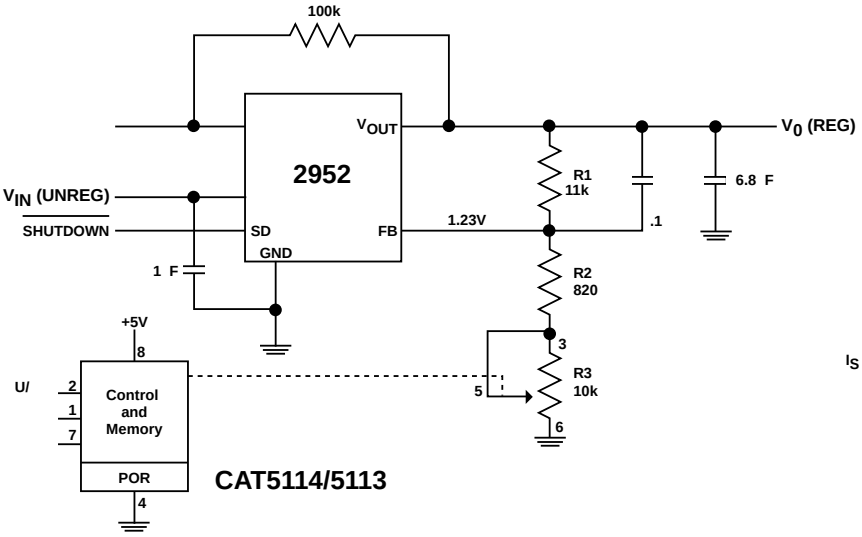


Programmable Sq. Wave Oscillator (555)

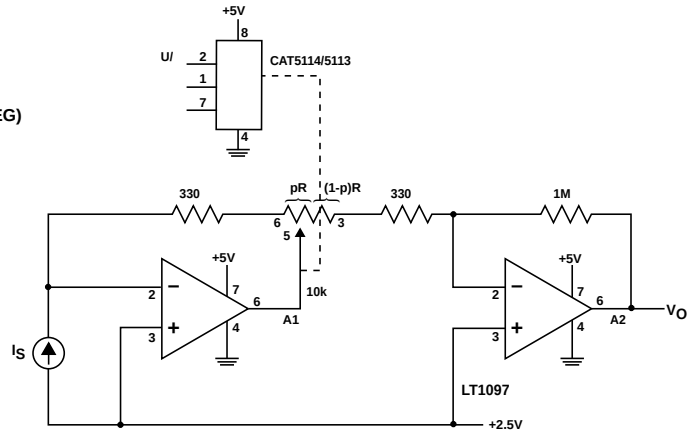


Sensor Auto Referencing Circuit

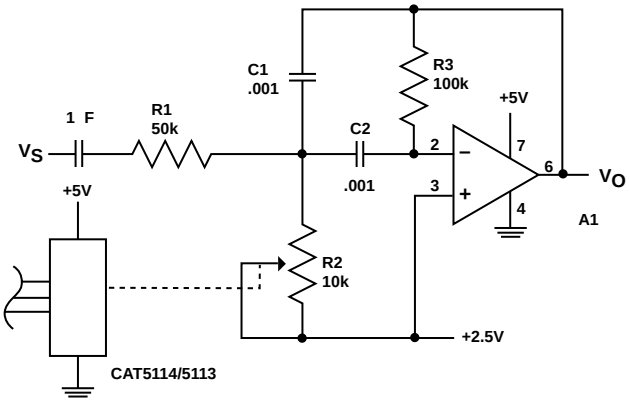
APPLICATIONS INFORMATION



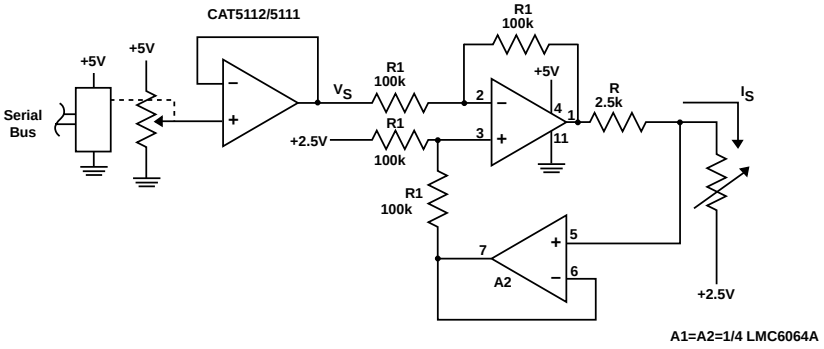
Programmable Voltage Regulator



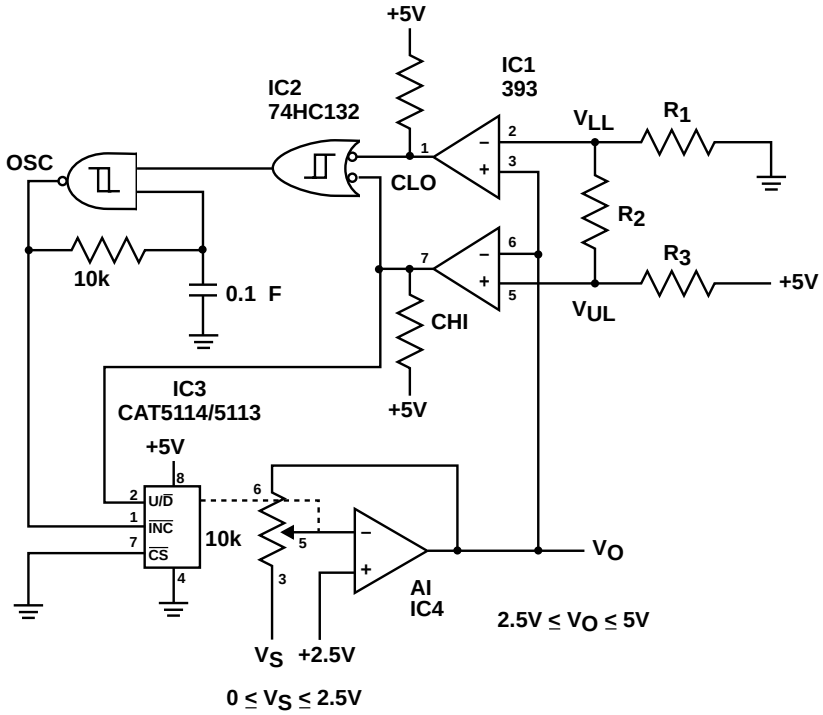
Programmable I to V convertor



Programmable Bandpass Filter

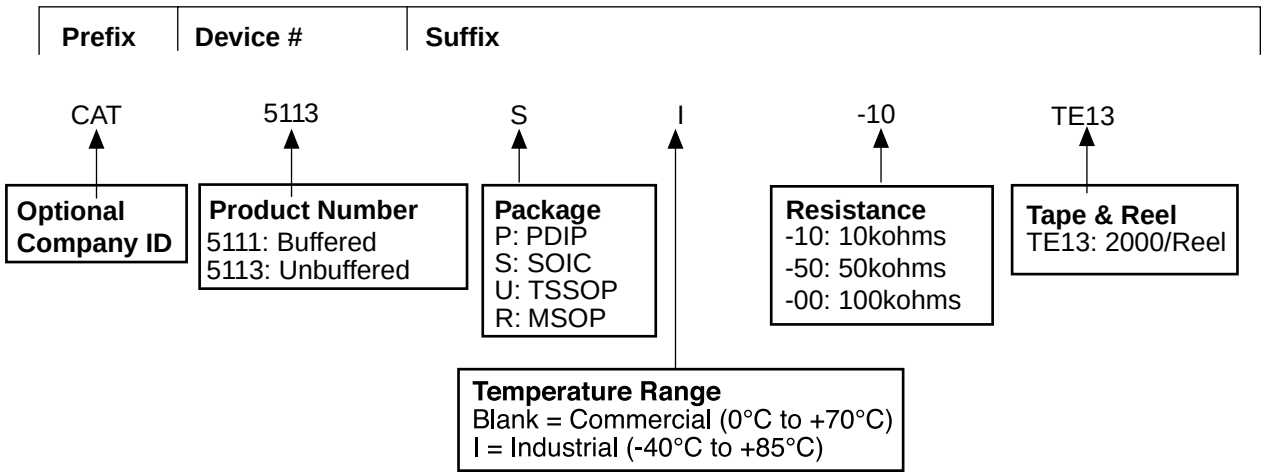


Programmable Current Source/Sink



Automatic Gain Control

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a CAT5113 SI-10TE13 (SOIC, 10K Ohms, Industrial Temperature, Tape & Reel)

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Publication #: 2009
Revison: J
Issue date: 04/18/02
Type: Final

CAT5114

32-Tap Digitally Programmable Potentiometer (DPP™)

FEATURES

- 32-position linear taper potentiometer
- Non-volatile NVRAM wiper storage
- Low power CMOS technology
- Single supply operation: 2.5V-6.0V
- Increment Up/Down serial interface
- Resistance values: 10kΩ, 50kΩ and 100kΩ
- Available in PDIP, SOIC, TSSOP and MSOP packages

APPLICATIONS

- Automated product calibration
- Remote control adjustments
- Offset, gain and zero control
- Tamper-proof calibrations
- Contrast, brightness and volume controls
- Motor controls and feedback systems
- Programmable analog functions

DESCRIPTION

The CAT5114 is a single digitally programmable potentiometer (DPP™) designed as a electronic replacement for mechanical potentiometers and trim pots. Ideal for automated adjustments on high volume production lines, they are also well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous or remote environment.

The CAT5114 contains a 32-tap series resistor array connected between two terminals R_H and R_L. An up/down counter and decoder that are controlled by three input pins, determines which tap is connected to the wiper, R_W. The wiper setting, stored in nonvolatile memory, is not lost when the device is powered down and is automatically reinstated when power is returned. The wiper can be adjusted to test new system values without effecting the stored setting. Wiper-control of the CAT5114 is accomplished with three input control pins, $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$. The $\overline{INC}$ input increments the wiper in the direction which is determined by the logic state of the U/$\overline{D}$ input. The $\overline{CS}$ input is used to select the device and also store the wiper position prior to power down.

The digitally programmable potentiometer can be used as a three-terminal resistive divider or as a two-terminal variable resistor. DPPs bring variability and programmability to a wide variety of applications including control, parameter adjustments, and signal processing.

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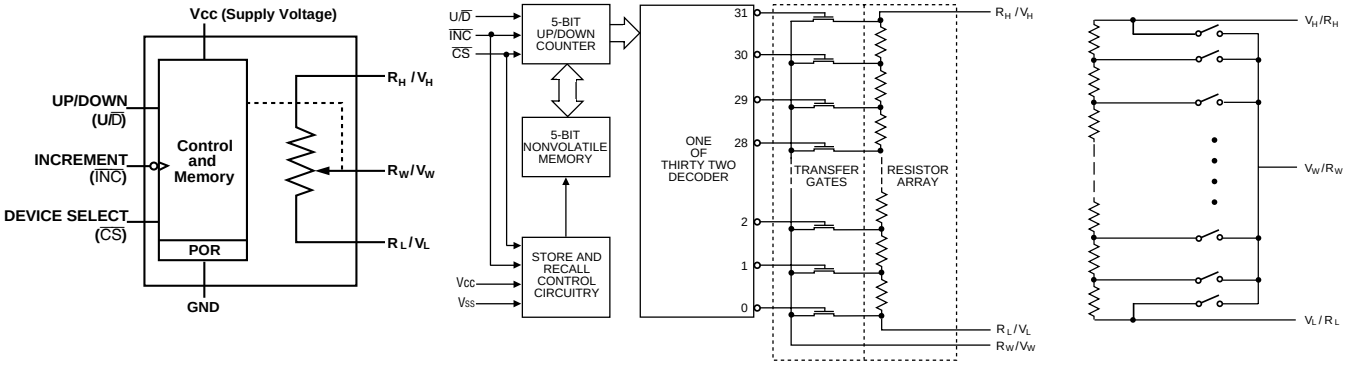
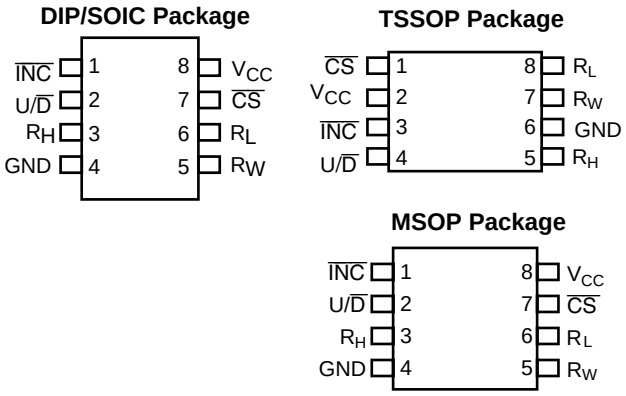


GENERAL DETAILED ELECTRONIC POTENTIOMETER IMPLEMENTATION

Doc. No. 2007, Rev. E

PIN CONFIGURATION



PIN FUNCTIONS

Pin Name	Function
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U/$\overline{D}$	Up/Down Control
R_H	Potentiometer High Terminal
GND	Ground
R_W	Potentiometer Wiper Terminal
R_L	Potentiometer Low Terminal
$\overline{CS}$	Chip Select
V_{CC}	Supply Voltage

PIN DESCRIPTIONS

$\overline{INC}$: Increment Control Input

The $\overline{INC}$ input moves the wiper in the up or down direction determined by the condition of the U/$\overline{D}$ input.

U/$\overline{D}$: Up/Down Control Input

The U/$\overline{D}$ input controls the direction of the wiper movement. When in a high state and $\overline{CS}$ is low, any high-to-low transition on $\overline{INC}$ will cause the wiper to move one increment toward the R_H terminal. When in a low state and $\overline{CS}$ is low, any high-to-low transition on $\overline{INC}$ will cause the wiper to move one increment towards the R_L terminal.

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R_H is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the R_L terminal. Voltage applied to the R_H terminal cannot exceed the supply voltage, V_{CC} or go below ground, GND.

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R_L: Low End Potentiometer Terminal

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DEVICE OPERATION

The CAT5114 operates like a digitally controlled potentiometer with R_H and R_L equivalent to the high and low terminals and R_W equivalent to the mechanical potentiometer's wiper. There are 32 available tap positions including the resistor end points, R_H and R_L. There are 31 resistor elements connected in series between the R_H and R_L terminals. The wiper terminal is connected to one of the 32 taps and controlled by three inputs, $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$. These inputs control a five-bit up/down counter whose output is decoded to select the wiper position. The selected wiper position can be stored in nonvolatile memory using the $\overline{INC}$ and $\overline{CS}$ inputs.

With $\overline{CS}$ set LOW the CAT5114 is selected and will respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ wil increment or decrement the wiper (depending on the state of the U/$\overline{D}$ input and five-bit counter). The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. The value of the counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH. When the CAT5114 is powered-down, the last stored wiper counter position is maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is set to the value stored.

With $\overline{INC}$ set low, the CAT5114 may be de-selected and powered down without storing the current wiper position in nonvolatile memory. This allows the system to always power up to a preset value stored in nonvolatile memory.

OPERATION MODES

$\overline{INC}$	$\overline{CS}$	U/$\overline{D}$	Operation
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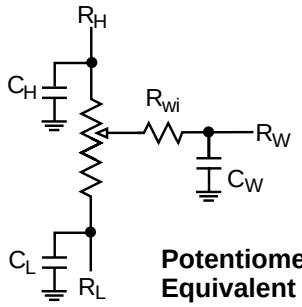
X	High	X	Standby



Potentiometer Equivalent Circuit

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- V_{CC} to GND ..... –0.5V to +7V

Inputs
- $\overline{CS}$ to GND ..... –0.5V to V_{CC} +0.5V
- $\overline{INC}$ to GND ..... –0.5V to V_{CC} +0.5V
- U/$\overline{D}$ to GND ..... –0.5V to V_{CC} +0.5V
- H to GND ..... –0.5V to V_{CC} +0.5V
- L to GND ..... –0.5V to V_{CC} +0.5V
- W to GND ..... –0.5V to V_{CC} +0.5V

Operating Ambient Temperature
- Commercial ('C' or Blank suffix) ..... 0°C to +70°C
- Industrial ('I' suffix) ..... – 40°C to +85°C

Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Soldering (10 sec max) ..... +300°C

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Absolute Maximum Ratings are limited values applied individually while other parameters are within specified operating conditions, and functional operation at any of these conditions is NOT implied. Device performance and reliability may be impaired by exposure to absolute rating conditions for extended periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Test Method	Min	Typ	Max	Units
V_{ZAP}(1)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000			Volts
I_{LTH}(1)(2)	Latch-Up	JEDEC Standard 17	100			mA
T_{DR}	Data Retention	MIL-STD-883, Test Method 1008	100			Years
N_{END}	Endurance	MIL-STD-883, Test Method 1003	1,000,000			Stores

DC Electrical Characteristics: V_{CC} = +2.5V to +6.0V unless otherwise specified

Power Supply

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Operating Voltage Range		2.5	—	6.0	V
I_{CC1}	Supply Current (Increment)	V_{CC} = 6V, f = 1MHz, I_W=0 V_{CC} = 6V, f = 250kHz, I_W=0	— —	— —	100 50	µA
I_{CC2}	Supply Current (Write)	Programming, V_{CC} = 6V V_{CC} = 3V	— —	— —	1 500	mA µA
ISB_1 (2)	Supply Current (Standby)	CS=V_{CC}-0.3V U/D, INC=V_{CC}-0.3V or GND	—	—	1	µA

Logic Inputs

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	Input Leakage Current	V_{IN} = V_{CC}	—	—	10	µA
I_{IL}	Input Leakage Current	V_{IN} = 0V	—	—	–10	µA
V_{IH1}	TTL High Level Input Voltage	4.5V ≤ V_{CC} ≤ 5.5V	2	—	V_{CC}	V
V_{IL1}	TTL Low Level Input Voltage		0	—	0.8	V
V_{IH2}	CMOS High Level Input Voltage	2.5V ≤ V_{CC} ≤ 6V	V_{CC} x 0.7	—	V_{CC} + 0.3	V
V_{IL2}	CMOS Low Level Input Voltage		-0.3	—	V_{CC} x 0.2	V

NOTES: (1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} + 1V
(3) I_W=source or sink
(4) These parameters are periodically sampled and are not 100% tested.

Potentiometer Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{POT}	Potentiometer Resistance	-10 Device		10		kΩ
		-50 Device		50		
		-00 Device		100		
	Pot Resistance Tolerance				±15	%
V_{RH}	Voltage on R_H pin		0		V_{CC}	V
V_{RL}	Voltage on R_L pin		0		V_{CC}	V
	Resolution			3.2		%
INL	Integral Linearity Error	$I_W \le 2\mu A$		0.5	1	LSB
DNL	Differential Linearity Error	$I_W \le 2\mu A$		0.25	0.5	LSB
R_{Wi}	Wiper Resistance	V_{CC} = 5V, I_W = 1mA			400	Ω
		V_{CC} = 2.5V, I_W = 1mA			1	kΩ
I_W	Wiper Current				1	mA
TC_{RPOT}	TC of Pot Resistance			300		ppm/°C
TC_{RATIO}	Ratiometric TC				20	ppm/°C
R_{ISO}	Isolation Resistance			TBD		Ω
V_N	Noise	100kHz / 1kHz		8/24		nV/√Hz
$C_H/C_L/C_W$	Potentiometer Capacitances			8/8/25		pF
fc	Frequency Response	Passive Attenuator, 10kΩ		1.7		MHz

AC CONDITIONS OF TEST

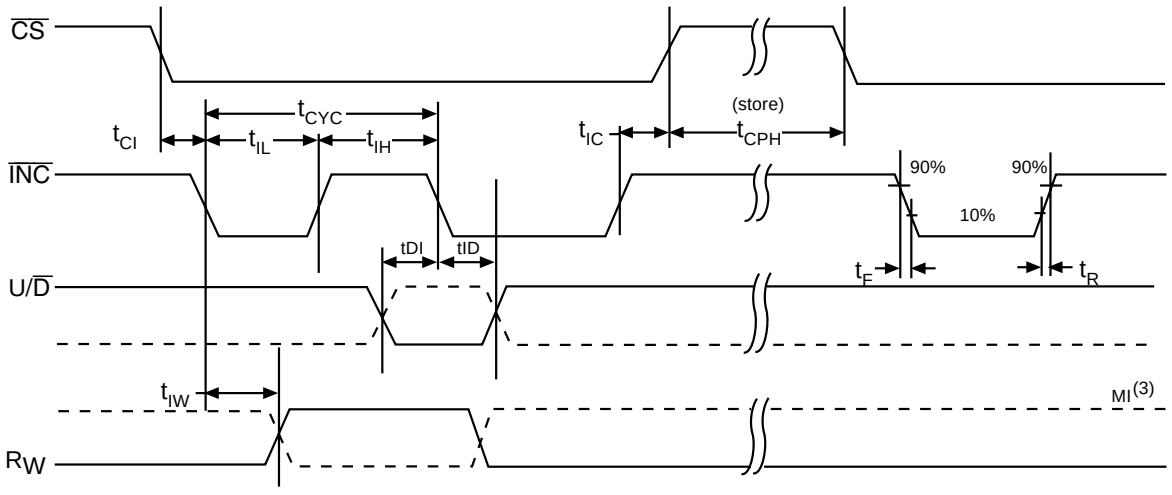
V_{CC} Range	$2.5V \le V_{CC} \le 6V$
Input Pulse Levels	$0.2V_{CC}$ to $0.7V_{CC}$
Input Rise and Fall Times	10ns
Input Reference Levels	$0.5V_{CC}$

AC OPERATING CHARACTERISTICS:

V_{CC} = +2.5V to +6.0V, $V_H = V_{CC}$, V_L = 0V, unless otherwise specified

Symbol	Parameter	Min	Typ(1)	Max	Units
t_{CI}	$\overline{CS}$ to INC Setup	100	—	—	ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	50	—	—	ns
t_{ID}	U/$\overline{D}$ to $\overline{INC}$ Hold	100	—	—	ns
t_{IL}	$\overline{INC}$ LOW Period	250	—	—	ns
t_{IH}	$\overline{INC}$ HIGH Period	250	—	—	ns
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1	—	—	µs
t_{CPH}	$\overline{CS}$ Deselect Time (NO STORE)	100	—	—	ns
t_{CPH}	$\overline{CS}$ Deselect Time (STORE)	10	—	—	ms
t_{IW}	$\overline{INC}$ to V_{OUT} Change	—	1	5	µs
t_{CYC}	$\overline{INC}$ Cycle Time	1	—	—	µs
$t_{R,}$ t_F(2)	$\overline{INC}$ Input Rise and Fall Time	—	—	500	µs
t_{PU}(2)	Power-up to Wiper Stable	—	—	1	msec
t_{WR}	Store Cycle	—	5	10	ms

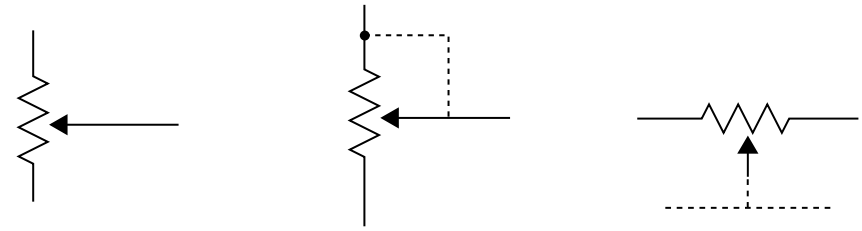
A. C. TIMING



(1) Typical values are for T_A=25°C and nominal supply voltage.
(2) This parameter is periodically sampled and not 100% tested.
(3) MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.

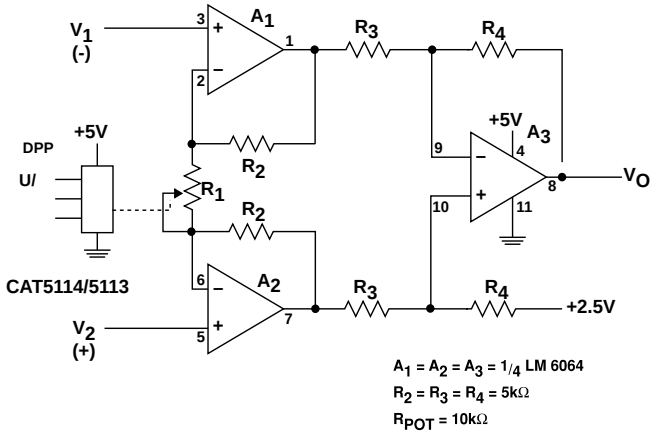
APPLICATIONS INFORMATION

Potentiometer Configurations

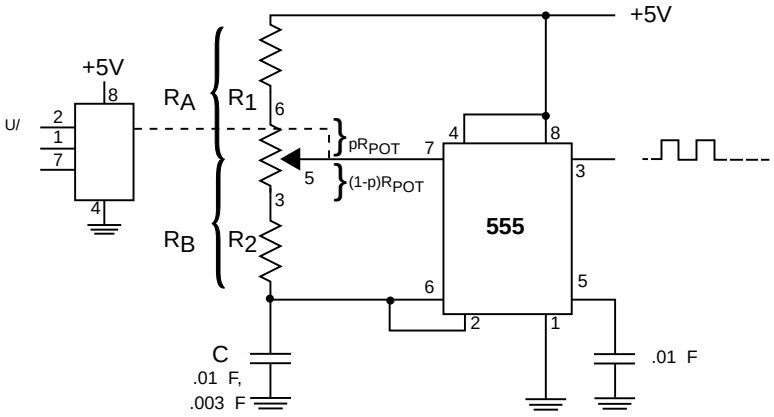


(a) resistive divider (b) variable resistance (c) two-port

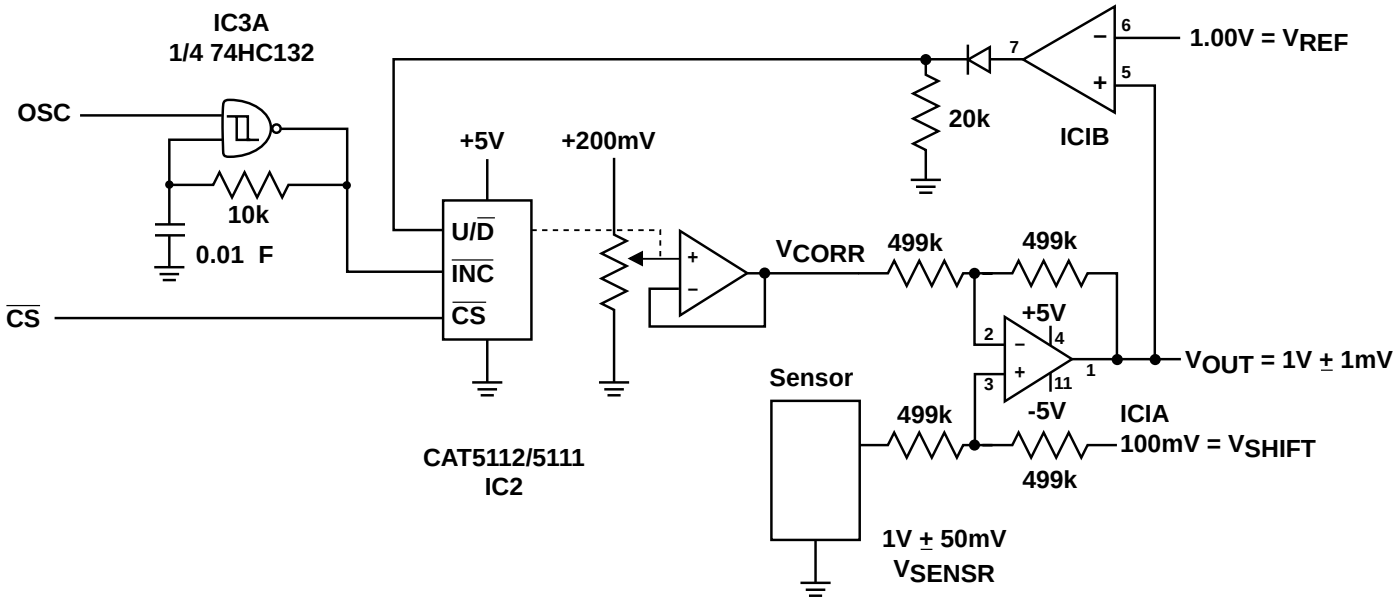
Applications



Programmable Instrumentation Amplifier

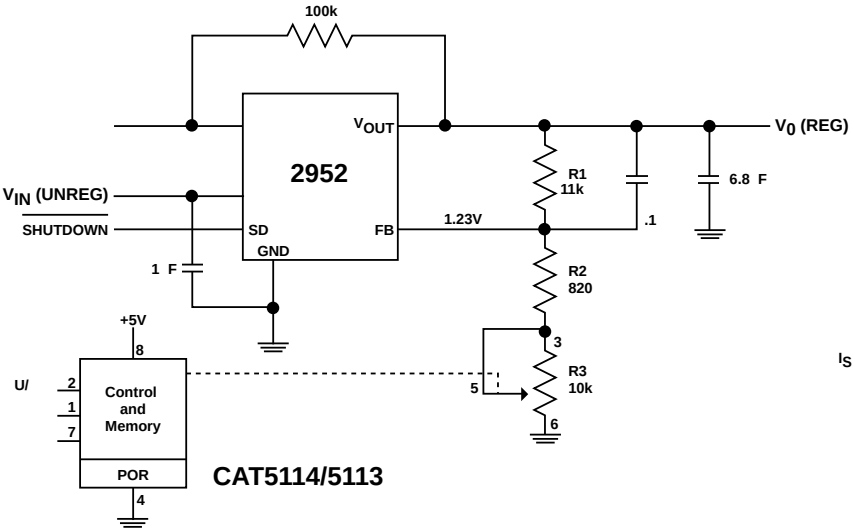


Programmable Sq. Wave Oscillator (555)

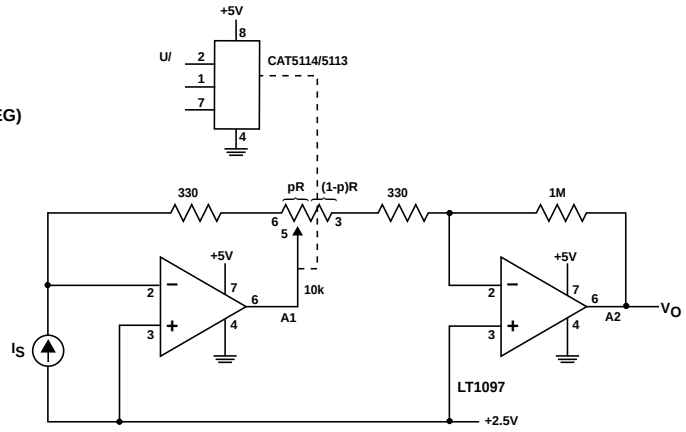


Sensor Auto Referencing Circuit

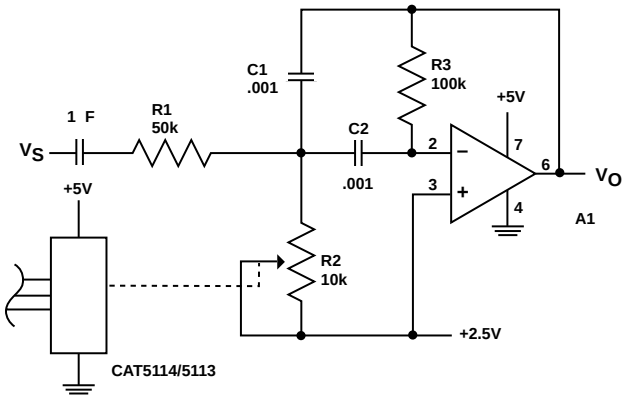
APPLICATIONS INFORMATION



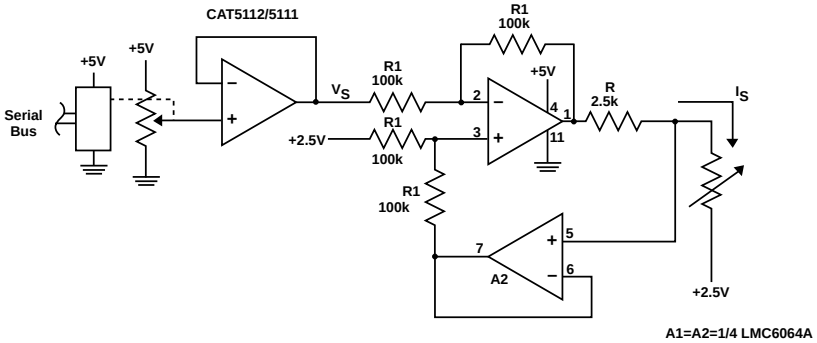
Programmable Voltage Regulator



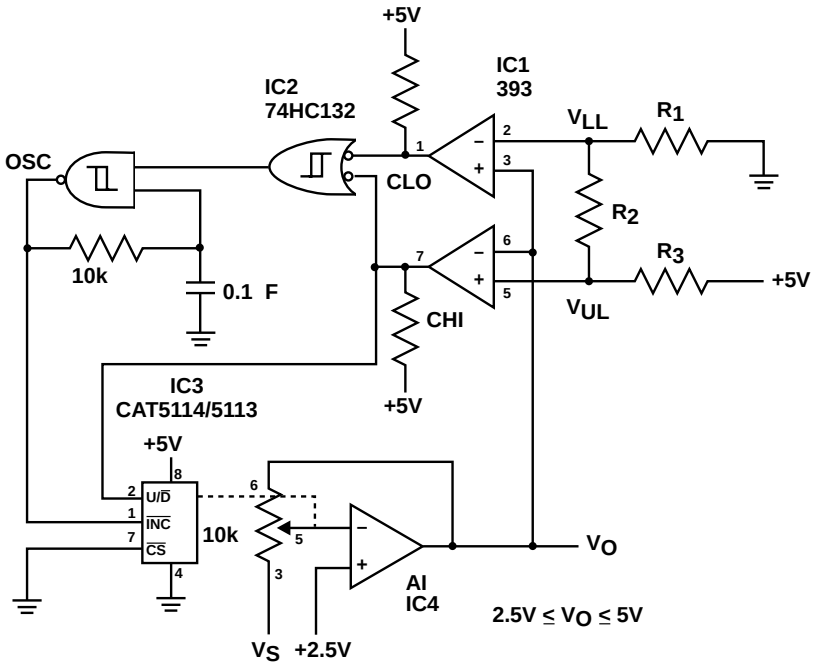
Programmable I to V convertor



Programmable Bandpass Filter

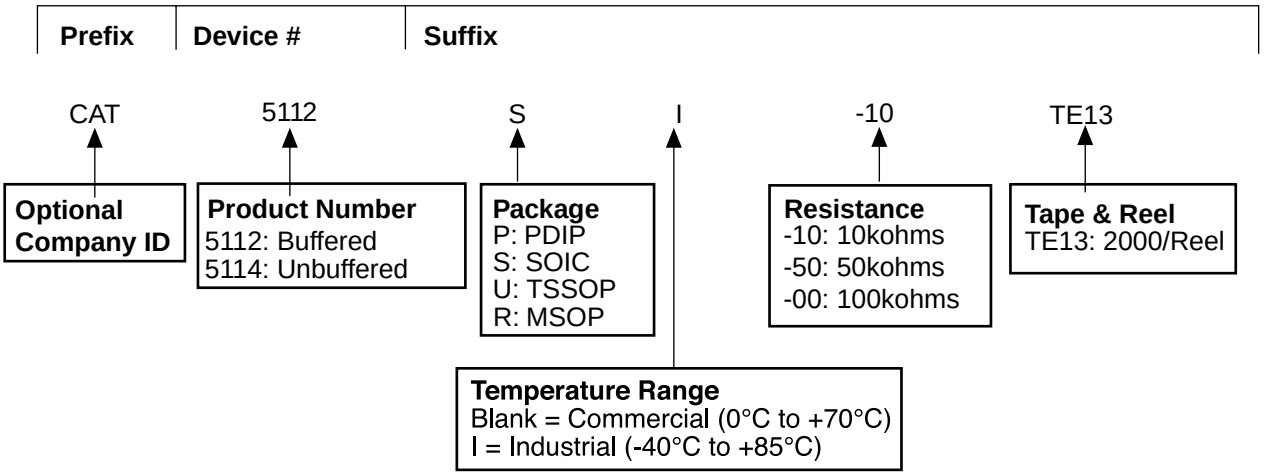


Programmable Current Source/Sink



Automatic Gain Control

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a CAT5114 SI-10TE13 (SOIC, 10K Ohms, Industrial Temperature, Tape & Reel)

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