AMI
AMERICAN MICROSYSTEMS, INC.

Library Characteristics

AMI8G 0.8 micron CMOS Gate Array

AMI's "AMI8Gx" series of 0.8µm gate arrays exploits a proprietary power grid and track routing architecture on a compact, channelless, sea-of-gates design to provide one of the highest performance, cost effective array products available today.

Features

- **Excellent performance:**
  - 260 MHz maximum toggle rate on clocked flip-flops ($T_J = 135°C$).
  - 185 ps delay (FO = 2) for a 2-input NAND gate.
- **Operating Temp ranges from -55 to 125°C:** Few competing products allow this range.
- **Clock tree generation:** ≤ 400 ps clock skew (fan out = 3500 at 80 MHz).
- **1 to 16 mA drive per single I/O cell:** Selectable I/O drive with controllable slew rate. Extra I/O cells allow combined I/O drive up to 96 mA without reducing pad count.
- **Automatic Test Program Generation:** Includes scan macros (NETSCAN™) for high fault coverage.
- **JTAG Boundary Scan macro support**
- **Full operating voltage range from 2.7V to 5.5V**
- **ESD protection > 2kV; latchup > 100 mA**
- **Cost driven architecture:**
  - Offers both two and three level metal interconnect to provide the lowest user cost for the number of gates and pads required.
  - Provides 6 extra power pads per corner to pre-serve more I/O cells for signal use.
  - Contains extra I/O cells to provide extra drive without wasting bond pads.
- **Extensive library for quick design:**
  - Complete primary cell and I/O library.
  - Synchronous single port RAM compilers with over 2000 compiled RAM sizes from 32 x 1 to 1K x 32-bits.
  - MG65C02, MG29C01, MG29C10, MG80C85, MG82Cxx, MGMC51 megacells.
  - Various datapath logic synthesizers (FIFOs, multipliers, adders, barrel shifters).
- **Wide range of packaging:** Full QFP and LCC line, DIPs and PGAs, individual die, (ball grid array package under study). Burn-in capability as needed.
- **3V, 5V, and combined 3V/5V operation:** Each individual pad cell can be driven independently by a 3V or 5V supply. 3V to 5V and 5V to 3V level shift is available in all I/O cells. Core can be either 3V for low power or 5V for high speed.
- **Power equals 3.2 µW/MHz/cell**

AMI8Gx Gate Array Family

Part Number	Raw Gates	Usable Gates[1]		Available I/O Cells	Available Bond Pads[2]
		Triple Metal	Double Metal		
AMI8G663	657,972	432,180	324,526	732	528
AMI8G392	392,616	259,920	194,256	564	424
AMI8G247	246,790	172,750	123,400	448	336
AMI8G201	200,740	140,500	100,400	404	304
AMI8G142	135,744	90,496	67,872	340	256
AMI8G93	90,720	58,320	44,064	276	208
AMI8G65	65,608	42,812	32,248	232	176
AMI8G55	54,000	35,000	26,500	212	160
AMI8G44	44,620	25,760	22,080	192	144
AMI8G34	34,000	22,400	16,800	168	128
AMI8G21	20,904	13,728	10,296	132	100
AMI8G15	15,048	9,768	7,392	112	84
AMI8G9	9,180	5,916	4,488	88	68
AMI8G5	5,304	3,432	2,652	68	52

Notes: 1. Exact usable gate count will vary depending on design interconnect and macro selection.
2. 24 optional fixed power pins (6 in each corner) are not included in this number.

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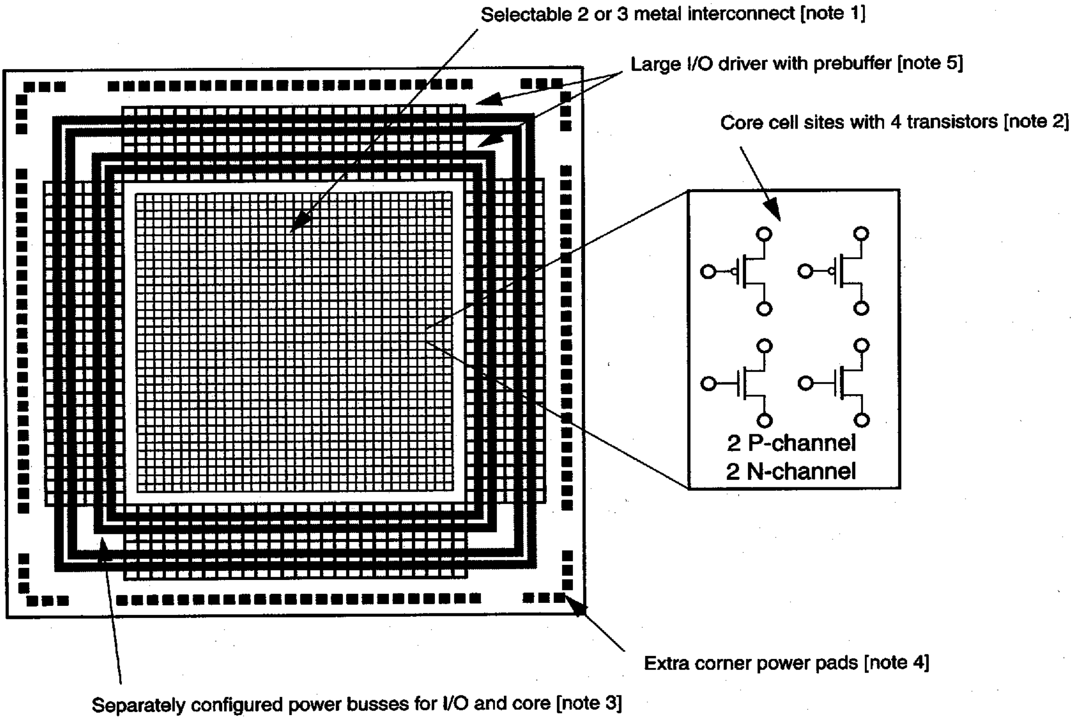
FIGURE 1: GATE ARRAY ARCHITECTURE



Architectural Overview

Some important elements of the AMI8Gx gate array family are:

- **[Note 1]** Drawn gate length of 0.8 micron; two or three level metal interconnect selectable.
- **[Note 2]** Two p-channel and two n-channel transistors per site (or cell). Sites are arrayed in a sea-of-gates structure that can allow interconnect routing over active sites. Also, p-channel transistors are sized larger than the stronger n-channel transistors in each cell to provide better matched rise and fall times.
- **[Note 3]** Four separate power busses for I/O cells to allow separate supplies for output buffers, input buffers, and mixed V_{DD} levels all on an individual I/O cell basis. Two separate power busses for core logic (not shown).
- **[Note 4]** 24 (six per corner) fixed power pads (not included in Bond Pad count in Table 1) available on each array for customer use.
- Each I/O cell can be configured as 5V V_{DD}, 3V V_{DD}, V_{SS}, or signal I/O.
- **[Note 5]** Each I/O cell has selectable drive from 1 mA to 16 mA. All I/O cell logic can be built in the I/O cell prebuffer. Level shifting (3V to 5V or 5V to 3V) may require the use of a few core gates.

Product Applications

The family's extended temperature and voltage operation range make it well suited for telecom, industrial, and military applications. The low cost structure also makes it ideal in computer and office automation ASIC requirements.

FPGA OR PAL CONVERSION: AMI can convert netlists from most FPGA and PAL devices to a more cost and performance effective AMI8Gx gate array design for volume production.

2ND SOURCE EXISTING PRODUCTS: Netlist conversion capabilities from AMI allow a competitive alternate supply with AMI8Gx for current high volume designs.

NEW DESIGN CAPTURE: AMI8Gx design is supported by many popular third party software platforms, as well as AMI's Enhanced Design Utilities™ (EDU) environment.

PROCESS UPGRADE: Designs done in AMI's 1.25µm and 1.0µm gate array families can easily be upgraded to the AMI8Gx family. The AMI ASIC Standard Library provides a common netlist design base.

ASIC Design Tools and Methodology

AMI8Gx and other AMI ASIC families are supported on popular third party products:

- Cadence™
- Mentor Graphics®
- Synopsys®
- Viewlogic®
- Intergraph®
- Verilog® simulation
- IKOS® simulation accelerator
  (AMI's sign-off simulator)

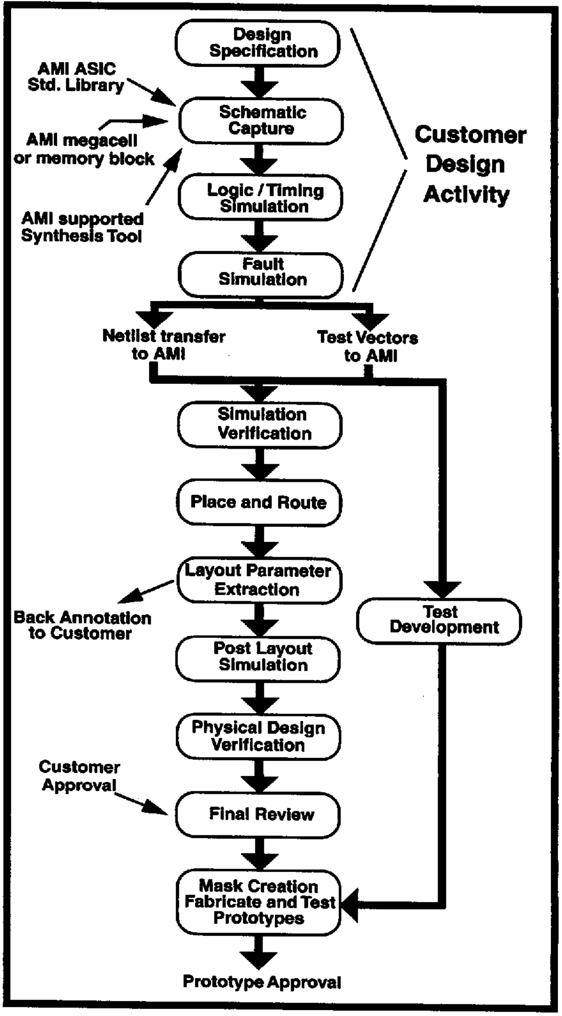
AMI has maintained critical proprietary software tools to ensure a tight, well coupled design to our silicon process. This methodology includes our expert-system design analysis tools, AMI's Enhanced Design Utilities (EDU), a software support methodology that covers the complete set of wafer processing possibilities, and a dedicated, experienced engineering staff that can assist at any level of the design process.

AMI Design Flow

AMI will supply an AMI8Gx design kit which includes a cell library containing symbols, simulation models and software for design verification, timing calculations, and netlist generation. For pre-layout timing simulations, capacitance values derived from statistical averages of known layouts are used. Once actual layout is completed by AMI, a post-layout interconnect capacitance table will be supplied for final validation of device timing.

Figure 2 shows a typical design flow for a new design.

FIGURE 2: ASIC DESIGN FLOW



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AMI Design Flow (cont.)

Working with an AMI design center, the customer is responsible for capturing and verifying the design using the AMI ASIC Standard Library. He is also responsible for creating the test vectors that will eventually serve as the logical part of the manufacturing test. Software aids such as logic synthesis, megacells, automatic test program generation, netlist rule checkers, etc. can greatly speed up this process. (A fault coverage check of the test vector set is optional and can be done as an additional service.)

When the design is received by the factory, the "Design Start Package" is reviewed by AMI engineers. This start package, which is completed by the customer, contains the device specification, netlist, critical timing paths, and test vectors. The design is pre-screened on the EDU and then resimulated on IKOS, AMI's sign-off simulator. The results are compared to the customer's simulation from the third-party CAE tool.

Once the design has passed the initial screening it is then ready for placement and routing. The layout proceeds by first placing memory and megacells, assigning priority to critical paths, and designing the distribution and buffering of clocks. Next, the layout is completed with automatic place-and-route on the balance of the circuit.

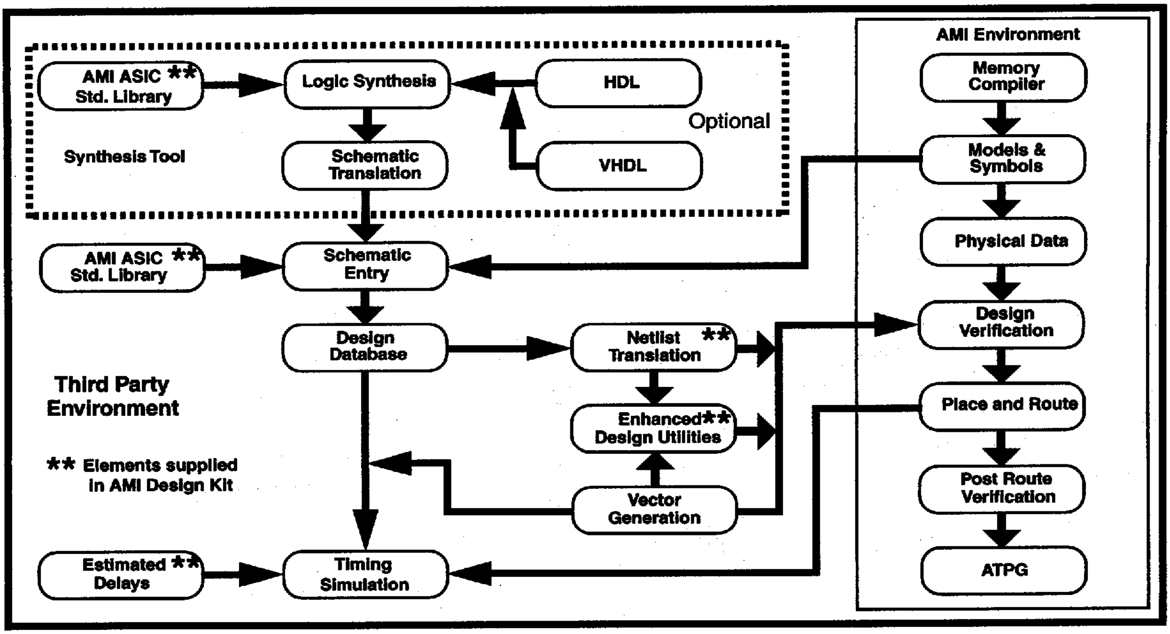
After layout has been completed the interconnect data is extracted from the physical layout to be fed back to the sign-off simulator for final circuit verification. This post layout interconnect data can be sent to the customer for final validation on his simulator. When the post-layout simulation has been completed and approved by the customer the design is then released for mask and wafer fabrication.

The test program is developed in parallel using internal automatic test program generation software. Prototypes can then be tested before they are shipped.

Figure 3 outlines a typical software environment when using third party tools. AMI uses EDIF to speed ports between various software products.

AMI's EDU's tools are intended to be used interactively at each stage of the design. EDU software is a set of design analysis tools that check both the design and test vectors for correctness and compatibility with in-house ASIC testers, and analyze the design for inefficiencies and possible flaws that could cause problems in manufacturing the device.

FIGURE 3: DESIGN ENVIRONMENT WITH THIRD PARTY SOFTWARE



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Memory Compiler Library

Memory Compiler	Size		Increment	Comments
	min.	max.		
SRAM (single-port, synchronous)	32 x 1	1K x 32	16-words, 1-bit	9 ns typical access time on 1K x 16

Note: Other SRAM and ROM compilers are available for standard cell or embedded array design approaches. Contact an AMI Design Center for details about these other product offerings.

The Design Library

AMI provides a robust collection of building blocks for the AMI8Gx gate array family. A broad range of primary cells is complemented with memory cell compilers and useful megacells. With such broad, US-based design talent, AMI can quickly design specific cells that customers need to add an edge in customization.

The AMI ASIC Standard Library

The AMI ASIC Standard Library contains a rich set of core and pad cells which allow great flexibility in building competitive devices for customer applications. The library is portable across all AMI's gate array and standard cell families.

Memory Compilers

The AMI8Gx family includes the memory compiler shown above. Each of the thousands of possible memory blocks created by this compiler is optimized precisely to the customers' parameters rather than built from a presized leaf cell that covers a range of sizes. This yields a better size and performance match for each application.

Upon supplying the cell specification to AMI, the customer can receive an accurate simulation timing specification overnight by facsimile and a full simulation model for any AMI supported software environment within five working days.

Megacells

American Microsystems, Inc. (AMI) provides a wide selection of Megacells for use in the development of ASICs; they ease the design of "systems on silicon." Chip designers today are faced with short time-to-market at the same time gate arrays and standard cells are allowing designs of up to several hundred thousand gates. Complex elements allow greater functionality without adversely affecting a design schedule. In fact they can accelerate time-to-market.

The Core Processor and Peripheral Megacells are designed to duplicate the function of industry standard parts and have a fixed function. The Datapath Megacells provide various logical and arithmetic functions and are produced using parameterized synthesizers which allow the creation of various megacell sizes and speeds.

Core Processors

Name	Function
MG29C01	4-bit microprocessor slice
MG29C10	Microprogram controller/sequencer
MG65C02	8-bit microprocessor
M320C25	DSP
M320C50	DSP
M8042	8-bit slave microcontroller
M8048	8-bit microcontroller
MGMC32	Core processor, 8032 compatible
MGMC32FB	Core processor, 8032FB compatible
MGMC32SD	Reduced function MGMC32

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Peripherals

Name	Function
MG1468C18	Real-time clock
M16C450	UART
MI6550A	UART with FIFO's
M6402	UART
M6845	CRT controller
M765A	Floppy disk controller
M8251A	Communication interface USART
M8253	Programmable interval timer
M82530	Serial communications controller
MG82C37A	Programmable DMA controller
MG82C50A	Asynchronous comm. element
MG82C54	Programmable interval timer
MG82C55A	Programmable peripheral interface
MG82C59A	Programmable interrupt controller
M8490	SCSI controller
M85C30	Serial communications controller
M8868A	UART
M91C36	Digital data separator
M91C360	Digital data separator
MFDC	Floppy disk controller
MGI2CSL	I^2C Serial bus slave transceiver
MI2C	I^2C Bus Interface

Datapath

Name	Function
MGAxxyyDv	Adder
MGAxxyyEv	Adder-subtractor
MGBxxyyAv	Barrel/arithmetic shifter
MGBxxBv	Barrel shifter
MGBxxyyCv	Arithmetic shifter
MGCxxAv	2-function comparator
MGCxxBv	6-function comparator
MGDxxAv	Decrementer
MGIxxAv	Incrementer
MGIxxBv	Incrementer/decrementer
MGMxxyyDv	Multiplier
MGMxxyyEv	Multiplier-accumulator
MGSxxyyAv	Subtractor

FIFOs

Name	Function
MGFxxyyC1	Latch-based asynchronous FIFO
MGFxxxxyyD	RAM-based synchronous FIFO
MGFxxxxyyE	RAM-based asynchronous FIFO

DC Specifications

Operating Specifications

Parameter		Minimum	Maximum	Units
V_{DD}, Supply voltage		2.7	5.5	Volts
Ambient temperature	- Military	-55	125	°C
	- Commercial	0	70	°C
CMOS Input Specifications (4.5V < V_{DD} < 5.5V; 0°C < T < 70°C)				
Vil	Low level input voltage		$0.3*V_{DD}$	Volts
Vih	High level input voltage	$0.7*V_{DD}$		Volts
Iil	Low level input current		-1.0	μA
Iih	High level input current		1.0	μA
Iil	Input pull-up current	-40	-105	μA
Iih	Input pull-down current	45	146	μA
Vt-	Schmitt negative threshold	$0.2*V_{DD}$		Volts
Vt+	Schmitt positive threshold		$0.8*V_{DD}$	Volts
Vh	Schmitt hysteresis	1.0		Volts
TTL Input Specifications (4.5V < V_{DD} < 5.5V; 0°C < T < 70°C)				
Vil	Low level input voltage		0.8	Volts
Vih	High level input voltage	2.0		Volts
Iil	Low level input current		-1.0	μA
Iih	High level input current		1.0	μA
Iil	Input pull-up current	-40	-105	μA
Iih	Input pull-down current	45	146	μA
Vt-	Schmitt negative threshold	0.7		Volts
Vt+	Schmitt positive threshold		2.1	Volts
Vh	Schmitt hysteresis	0.4		Volts

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Output Operating Specifications (4.5V < V_{DD} < 5.5V; 0°C < T < 70°C)

Parameter	Minimum	Maximum	Units
1.0 mA Driver			
Vol Low level output voltage		0.4	Volts
Voh High level output voltage	2.4		Volts
Iol Low level output current		1.0	mA
Ioh High level output current		-1.0	mA
2.0 mA Driver			
Vol Low level output voltage		0.4	Volts
Voh High level output voltage	2.4		Volts
Iol Low level output current		2.0	mA
Ioh High level output current		-2.0	mA
4.0 mA Driver			
Vol Low level output voltage		0.4	Volts
Voh High level output voltage	2.4		Volts
Iol Low level output current		4.0	mA
Ioh High level output current		-4.0	mA
8.0 mA Driver			
Vol Low level output voltage		0.4	Volts
Voh High level output voltage	2.4		Volts
Iol Low level output current		8.0	mA
Ioh High level output current		-8.0	mA
16.0 mA Driver			
Vol Low level output voltage		0.4	Volts
Voh High level output voltage	2.4		Volts
Iol Low level output current		16.0	mA
Ioh High level output current		-16.0	mA

Absolute Maximum Ratings

Parameter		Minimum	Maximum	Units
V_{DD}, Supply voltage		-0.3	6.0	Volts
Input pin voltage		-0.3	V_{DD}+0.3	Volts
Input pin current		-10.0	10.0	mA
Storage temperature	- Plastic packages	-55	125	°C
	- Ceramic packages	-65	150	°C
Lead temperature			300	°C for 10 sec.

Note that these specifications are to indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Further, operation at absolute maximum conditions for extended periods may adversely affect the long term reliability of the device.

Library Characteristics

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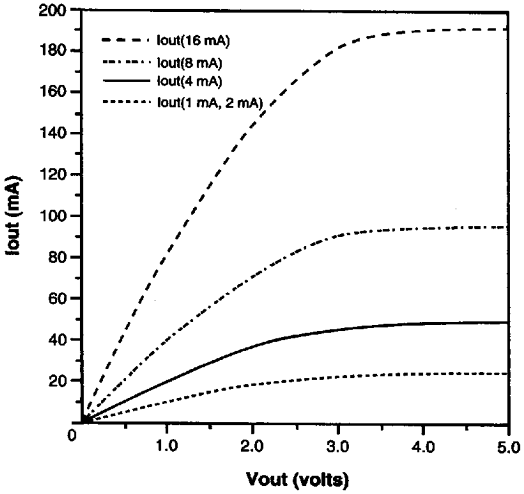
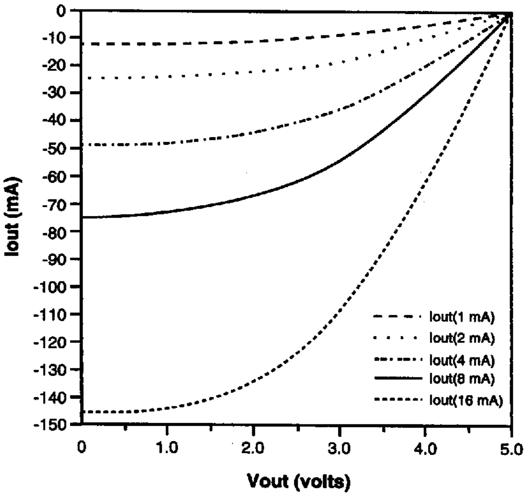
DC Characteristics
(V_{DD} = 5.0V, T = 25°C, Typical Process)

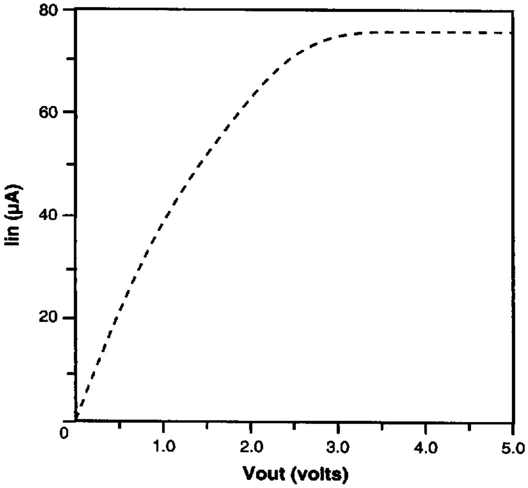
N-Channel Output Driver



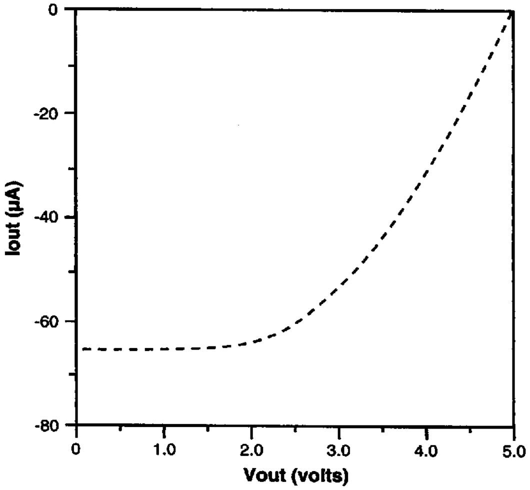
P-Channel Output Driver



N-Channel Pull-Down Device



P-Channel Pull-Up Device



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DC Derating Information

The DC Characteristics on page 2-9 can be derated to obtain values at other operating conditions using the formula:

$$I_{DC}*K_{PDC}*K_{VDC}*K_{TDC}$$

where I_{DC} is a value from the current curves on page 9. K_{PDC}, the DC process derating coefficient; K_{VDC}, the DC voltage derating coefficient; and K_{TDC}, the DC temperature derating coefficient, are described below. Due to the ESD protection structures, the N-channel driver has a different set of coefficients for K_{PDC} and K_{TDC}.

DC Variations with process (K_{PDC})

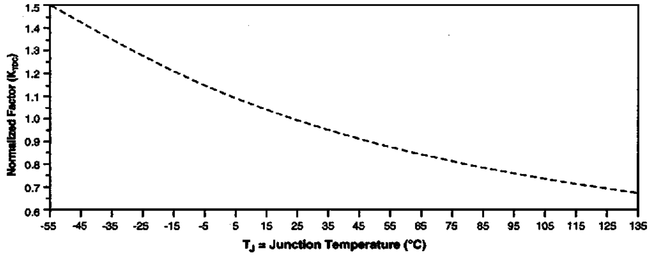
DC variations with process are given as fixed constants determined at the limits of acceptable manufacturing of the process. These are described below where WCS is the "Worst Case Speed" fabrication, TYP is the "Target" fabrication, and WCP is the "Worst Case Power" fabrication.

	N-Channel Output Driver (Vol = 0.4V)			N-Channel Pull-Down Device (Vol = 0.4V)			All P-Channel (Voh = 2.4V)		
Process	WCS	TYP	WCP	WCS	TYP	WCP	WCS	TYP	WCP
K_{PDC}	0.59	1.00	1.25	0.62	1.00	1.21	0.74	1.00	1.28

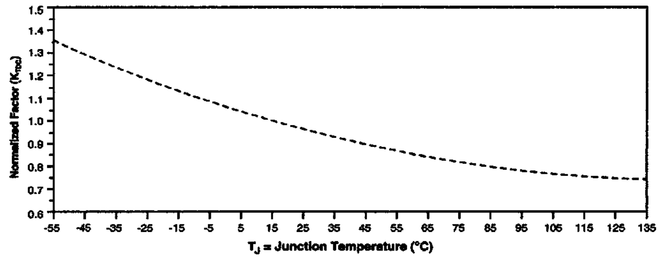
DC Variations with Voltage (K_{VDC})

	All N-Channel (Vol = 0.4V)			All P-Channel (Voh = 2.4V)		
V_{DD}	4.5	5.0	5.5	4.5	5.0	5.5
K_{VDC}	0.96	1.00	1.03	0.79	1.00	1.21

DC variations with temperature for the N-Channel output driver (K_{TDC})



DC variations with temperature for all other N-Channel and P-Channel devices



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Delay Derating Information

The propagation delays listed in the data sheets are for typical temperature, 25°C; typical supply voltage, 5.0V; and typical processing conditions. To calculate the delay at other conditions (including V_{DD} equals 3.0V) the following equation can be used:

$$T_{pdx} = T_{pdx}(typ)*K_P*K_V*K_T$$

where T_{pdx}(typ) is given in the data sheets. K_P, the process derating coefficient; K_T, the temperature derating coefficient; and K_V, the supply voltage derating coefficient, are described below.

Delay Variations with Temperature (K_T)

Delay varies linearly with temperature. The following formulas and common operating points can be used.

Temp	K_T
-55°C	0.79
-25°C	0.87
0°C	0.93
25°C	1.00
70°C	1.11
100°C	1.19
125°C	1.26

Temp. Range	K_T Formula
-55°C to 25°C	$K_T = 1.0 - (25-T_J°C)*2.58 \times 10^{-3}$
25°C to 140°C	$K_T = 1.0 + (T_J°C-25)*2.58 \times 10^{-3}$

Where T_J°C is the temperature at the silicon junction.

Delay Variations with Process (K_P)

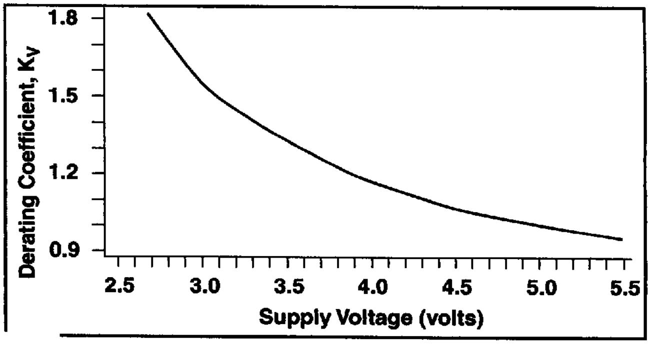
Delay variations with process are given as fixed constants determined at the limits of acceptable manufacturing of the process. These are described below.

Derating Coefficient (K_P)	Process Variation Point
1.36	Delay increase due to "Worst Case Speed" (WCS) fabrication
1.00	Typical delay; Fabrication target
0.74	Delay reduction due to "Worst Case Power" (WCP) fabrication

Delay Variations with Voltage (K_V)

Delay varies nonlinearly with voltage. Some common operating points and a characteristic curve are shown.

V_{DD}	K_V
2.7V	1.82
3.0V	1.59
3.3V	1.42
4.5V	1.08
4.75V	1.03
5.0V	1.00
5.25V	0.97
5.5V	0.94



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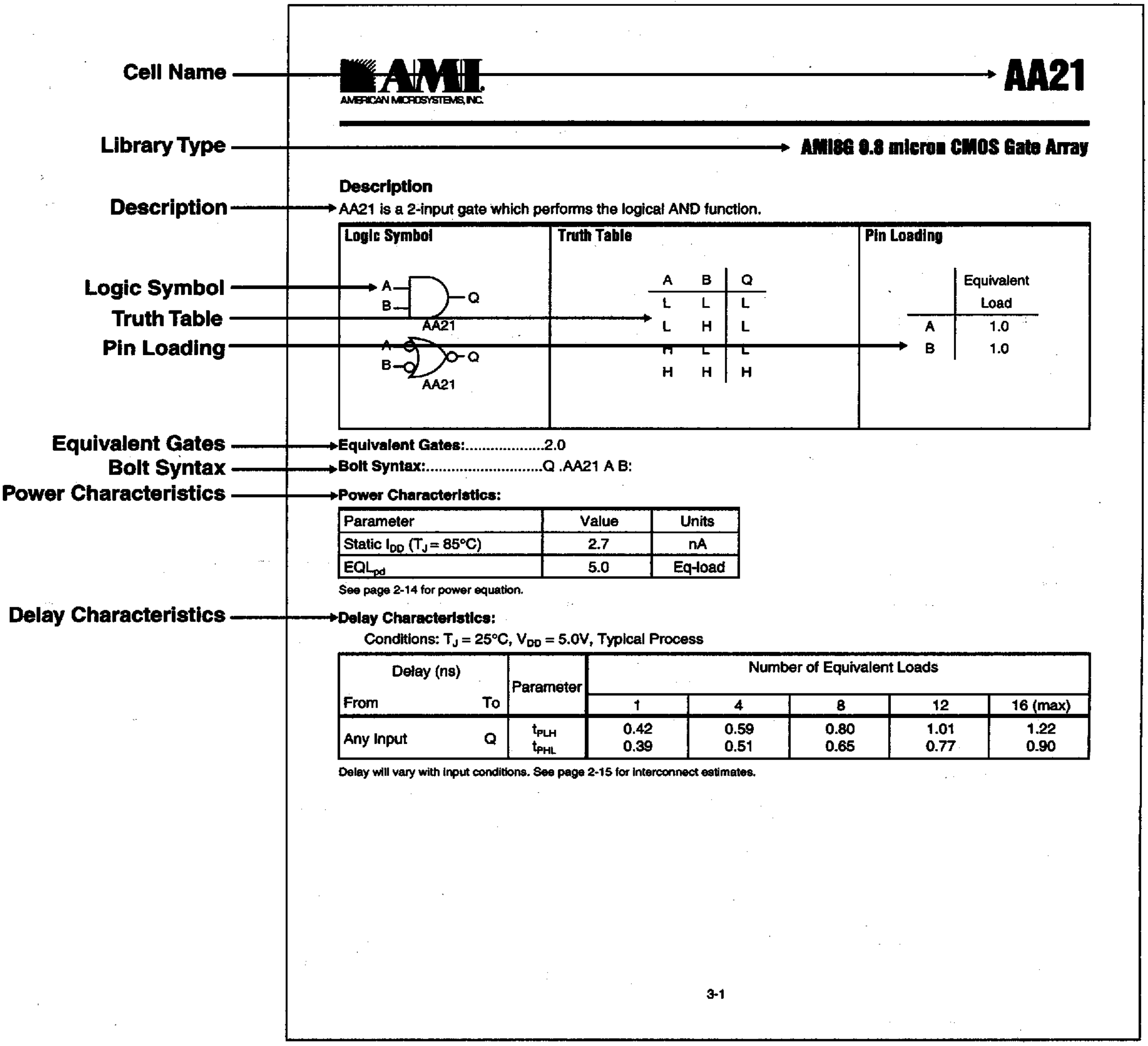
Interpreting the Data Sheet

The figure below shows a typical data sheet and points out the main features of the data sheet. Not shown is a schematic which accompanies some of the more complex cells.



AMI AMERICAN MICROSYSTEMS, INC.

AA21

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Description

AA21 is a 2-input gate which performs the logical AND function.

Logic Symbol

Truth Table

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0

Equivalent Gates:..................2.0

Bolt Syntax:...........................Q .AA21 A B:

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	2.7	nA
EQL_{pd}	5.0	Eq-load

See page 2-14 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.42 0.39	0.59 0.51	0.80 0.65	1.01 0.77	1.22 0.90

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

3-1

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A description of these features of the data sheet are as follows.

LIBRARY TYPE: Designates the feature size and library type such as standard cell or gate array.

CELL NAME: AMI's cell name.

DESCRIPTION: A brief sentence about the function of the cell.

LOGIC SYMBOL: Shows a picture of the symbol as it appears as an icon in the workstation design kits.

TRUTH TABLE: A boolean table showing the output logic levels as a function of the input logic levels.

Types of logic levels found in the logic tables are as follows:

H = High level steady state,
L = Low level steady state,
↑ = Transition from low level to high level,
↓ = Transition from high level to low level,
X = Any level including transitions,
NC = No change in output level for a given set of input levels,
IL = The output level is unknown for this set of illegal input levels,
Z = High impedance level,
UN = Undriven node or input,
Q(n) = The level of Q before an active transition on the affecting node, and
QN(n) = The level of QN before an active transition on the affecting node.

PIN LOADING: A table of cell input loads in units of equivalent loads (the input load normalized to the input load of an NA21, 2-input NAND gate).

EQUIVALENT GATES: Equivalent gates for the cell is defined as the cell area normalized to the area of the NA21.

BOLT SYNTAX: BOLT (Block Oriented Logic Translator) is an AMI proprietary netlist format. This line shows the BOLT syntax for the cell. One example of the use of BOLT is as a design interface from the workstation design kits to AMI.

POWER CHARACTERISTICS: Power for the cell can be described in three parts. The first part is the power dissipated due to the leakage current across the channels and through the formed diodes. The second part is due to the switching voltage across loads on the internal nodes of the cell. Finally, the third part is due to the switching voltage across a load that a cell is driving.

The power characteristics table provides the static leakage current for a junction temperature of 85°C, and the dissipative load for all the switching nodes in the cell in terms of equivalent loads.The load that a cell drives can be calculated by adding up input loads and adding to it the estimated load from the Load Estimation table on page 2-15. Below are equations for calculating the power dissipation.

Core Cells and Input Buffers

$$\text{POWER} = (\text{Static } I_{DD})\, V_{DD} + 0.05\text{E-}12(EQL_{pd})V_{DD}^2 f + 0.05\text{E-}12(EQL_l)V_{DD}^2 f$$

Output Buffers

$$\text{POWER} = (\text{Static } I_{DD})\, V_{DD} + 0.05\text{E-}12(EQL_{pd})V_{DD}^2 f + C_{ol}V_{DD}^2 f$$

where:

Static I_{DD} = static leakage current of the cell
V_{DD} = operating voltage
EQL_{pd} = load of the switching nodes in the cell
f = frequency of operation
C_{ol} = load in farads on the output buffer
EQL_l = load of the driven pins and interconnect

The frequency term of the power equation dominates, making the static current term insignificant. However, the term can be used to find the standby current.

AMI8G 0.8 micron CMOS Gate Array

DELAY CHARACTERISTICS: This table contains delay data for the various input to output paths in the cells. The table below explains each column in the delay characteristics. The traditional coefficients for a linear model have not been provided because AMI is now using a new equation to model the effects of loading on the input as well as on the output of a cell's path delay. The delay on the data sheets represents a typical load on the inputs of the cell. More accurate timing can be obtained using one of AMI's workstation kits. Contact your sales representative or the factory for details.

Explanation of Columns in the Delay Characteristics Table

Column Name	Explanation	
Delay (ns) From To	Names the two pins that identify the path for the delay	
Parameter	Mnemonic for the propagation delay or timing parameter whose value can be obtained from the values listed under the number of equivalent loads column.	
	t_{PLH}	Input to output propagation delay for a rising edge on the output
	t_{PHL}	Input to output propagation delay for a falling edge on the output
	t_{ZH}	High impedance to high level delay
	t_{ZL}	High impedance to low level delay
	t_{HZ}	High level to high impedance delay
	t_{LZ}	Low level to high impedance delay
	t_{su}	Input setup time with respect to clock
	t_h	Input hold time
	t_w	Input pulse width
Number of Equivalent Loads	The first row of values in this column contains five equivalent loads over the range of allowed loading for the cell (output buffer loading is in pico farads). The last value in the row on the right has the word "max" in parenthesis to indicate that this is the maximum load that the cell can drive[1]. The rest of the rows contain delay values for each of the parameters corresponding to given loads in the first row. To find the delay for a cell, add up the loads of all the inputs that the cell is driving, then add the estimated interconnect load from the Load Estimation table on page 2-15. Finally, look up the value for the desired parameter corresponding to the load on the cell. Interpolation may be used for values in between load columns. Again, more accurate delays can be achieved by obtaining an AMI workstation kit.	

Note: 1. Due to differing capabilities of logic simulators, the delay modeling implementation will vary and in some cases will still use the linear model. Consult the factory about modeling for some specific workstation kits and simulators. Loads beyond the maximum load are an extrapolation of the model and therefore their accuracy is not guaranteed.

AMI8G 0.8 micron CMOS Gate Array

Interconnect Load Estimation Table

Die Size	Fan Out (Equivalent Loads)							
	1	3	6	9	12	20	50	80
500	0.5	1.6	3.0	4.3	5.6	8.8	19.9	30.2
450	0.5	1.5	2.8	4.1	5.3	8.4	19.0	28.9
400	0.4	1.4	2.7	3.9	5.0	8.0	18.1	27.4
350	0.4	1.3	2.5	3.7	4.8	7.5	17.0	25.8
300	0.4	1.2	2.3	3.4	4.4	7.0	15.9	24.1
250	0.3	1.1	2.2	3.1	4.1	6.5	14.7	22.2
200	0.3	1.0	1.9	2.8	3.7	5.9	13.3	20.1
150	0.2	0.9	1.7	2.5	3.2	5.1	11.7	17.7
100	0.2	0.7	1.4	2.0	2.7	4.3	9.7	14.8

AMI8G 0.8 micron CMOS Gate Array

Packaging

The AMI8Gx gate array family can be packaged in a variety of popular packages.

New packages are in development which will extend the package offering. Some special packages or packaging requirements can be supplied if requested. More details on specific packages are available from an AMI sales representative.

Available Packages

( ) = Lead time required

	PQFP	TQFP	PLCC	PDIP	CQFP
AMI8G5	44,52,64,80,100	32,48,64,80,100	20,28,32,44,52	8,14,16,18,20,22, 24,28,40,48	40
AMI8G9	44,52,64,80,100,120	32,44,48,64, 80,100,176	20,28,32,44, 52,68,84	14,16,18,20,22, 24,28,40,48	40
AMI8G15	44,52,64,80, 100,120,128	32,44,48,64, 80,100,128,176	20,28,32,44,52	14,16,22,24, 28,40,48	40,64
AMI8G21	44,52,64,80,100, 120,128,144	44,64,80,100, 128,144,176	20,28,32,44, 52,68,84	22,24,28,40,48	40,64
AMI8G34	44,52,64,80,100, 120,128,144,160	44,64,80,100, 128,144,176	20,28,32,44, 52,68,84	22,24,28,40,48	40,44,(52),64,100,132
AMI8G44	44,52,64,80,100,120, 128,144,160,184,208	44,64,80,100, 128,144,176	28,32,44,52, 68,84	24,28,40,48	40,44,(52),64,100,132
AMI8G55	44,52,64,50,100,120, 128,144,160,184,208	44,64,80,100, 128,144,176	28,32,44,52, 68,84	24,28,40,48	44,(52),100,132,196
AMI8G65	44,52,64,80,100,120, 128,144,160,184,208,240	44,64,80,100, 128,144,176	28,32,44,52, 68,84	24,28,40	44,(52),100,132,196
AMI8G93	52,64,80,100,120,128, 144,160,184,208,240	44,64,80,100, 128,176,144	44,52,68,84	28,40	(52),132,144,196
AMI8G142	100,120,128,144,160, 184,208,240,256	128,144,176	44,52,68,84		132,144
AMI8G201	128,144,160,208,240,256	176	52,84		
AMI8G247	128,144,160,208,240,256	176			
AMI8G392	208,240				
			ENHANCED		
AMI8G5S	44,52,64,80,100,120	32,44,48,64,80,100	20,28,32,44,52,68,84	8,14,16,18,20, 22,24,28,40,48	40
AMI8G9S	44,52,64,80,100,120,128	32,44,48,64,80,100	20,28,32,44,52,68,84	14,16,20,22,24, 28,40,48	40,64
AMI8G11S	44,52,64,80,100,120,128	32,44,48,64,80,100	20,28,32,44,52,68,84	14,16,22,24, 28,40,48	40,64
AMI8G28S	44,52,64,80,100,120, 128,144,160	44,64,80,100, 128,144,176	20,28,32,44,52,68,84	22,24,28,40,48	40,44,(52),64,132
AMI8G34S	44,52,64,80,100,120, 128,144,160,184	44,64,80,100, 128,144,176	20,28,32,44,52,68,84	22,24,28,40,48	40,44,(52),64,100,132
AMI8G55S	44,52,64,80,100,120,128, 144,160,184, 208,240	44,64,80,100, 128,144,176	28,32,44,68,84	24,28,40,48	44,(52),100,132,196
AMI8G93S	44,52,64,80,100,120,128, 144,160,184, 208,240	44,64,80,100, 128,144,176	44,68,84	28,32,44,68,84	132,144,196

Library Characteristics

AMI8G 0.8 micron CMOS Gate Array

Available Packages

( ) = Lead time required

	JLDCC	CPGA	MQUAD	BGA	CLCC
AMI8G5	28	68,69,85			20,24,28,44,68
AMI8G9	28	68,69,85			20,24,28,44,68
AMI8G15	28,44,68,84	65,68,69,84,85,101,121,145		(169)	24,28,36,40, 44,48,52,68
AMI8G21	44,68,84	65,68,69,84,85,101,121,145		(121),(169),(208)	28,36,40,44,48, 58,68,84
AMI8G34	44,52,68,84	65,68,69,84,85,101,121,145,181		(121),(169),(208)	28,36,40,44,48, 58,68,84
AMI8G44	44,52,68,84	68,69,84,85,101,121,145,181	(144)	(121),(169),(208),(225)	36,40,44,48,52,68,84
AMI8G55	44,52,68,(84)	68,69,84,85,101,121,145,181	128,(144)	(121),(169),(208), (225),(256)	44,48,68,84
AMI8G65	44,52,68,84	68,69,84,85,101,145,181	128,(144)	(121),(169),(208), (225),(256)	44,48,68,84
AMI8G93	44,68,84	68,69,84,85,109,121, 132,145,181,208	128,(208)	(169),(225),(256),(313) (352),(388)	44,68,84
AMI8G142	68,84	68,69,84,109,121,132, 145,177,181,208	(208)	(169),(225),(256),(313) (352),(388)	68
AMI8G201	84	145,155,181,225		(169),(225),(256),(313) (352),(388)	
AMI8G247		145,155,225,257		(169),(225),(313) (352),(388)	
AMI8G392		476		(225),(313),(352),(388)	
			ENHANCED		
AMI8G5S	28	68,69,85			20,24,28,44,68
AMI8G9S	28	65,68,69,84,85,101,121,145			24,28,40,44,68
AMI8G11S	28,44,68,84	65,68,69,84,85,101,121,145		(169)	24,28,36,40,44, 48,52,68
AMI8G28S	44,52,68,84	68,69,84,85,101,121,145,181		(121),(169),(208)	28,36,40,44, 48,52,68
AMI8G34S	44,52,68,84	68,69,84,85,101,121,145,181		(121),(169),(208),(225)	28,36,40,44,48, 52,68,84
AMI8G55S	44,52,68,84	68,69,84,85,101,121,145,181	128,144	(121),(169),(208),(225)	44,48,68,84
AMI8G93S	44,68,84	68,69,84,109,121,132, 145,181,208	128,144	(169),(225),(256),(313), (352),(388)	44,68,84

PQFP = Plastic quad flatpack
TQFP = Thin quad flatpack (plastic)
MQUAD = Metal quad flatpack
CQFP = Ceramic qual flatpack
PLCC = Plastic leaded chip carrier - J lead

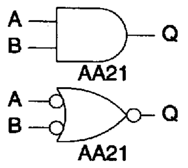
JLDCC = Ceramic leaded chip carrier - J lead
CLCC = Leadless chip carrier (ceramic)
PDIP = Plastic dual in-line package
CPGA = Ceramic pin grid array
BGA = Ball grid array

AA21

Description:

AA21 is a 2-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0

Equivalent Gates:...................2.0

Bolt Syntax:............................Q .AA21 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.7	nA
EQL_{pd}	5.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.42 0.39	0.59 0.51	0.80 0.65	1.01 0.77	1.22 0.90

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AA22

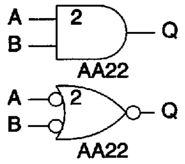
AMI
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

AA22 is a 2-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0

Equivalent Gates:...................2.0

Bolt Syntax:............................Q .AA22 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	6.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	7	14	21	28 (max)
Any Input	Q	t_{PLH}	0.46	0.64	0.82	1.00	1.18
		t_{PHL}	0.41	0.56	0.68	0.80	0.91

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

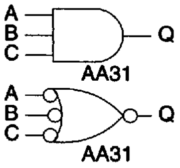
AA31

AMI8G 0.8 micron CMOS Gate Array

Description:

AA31 is a 3-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0

Equivalent Gates:....................2.0

Bolt Syntax:.............................Q .AA31 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	3.5	nA
EQL_{pd}	6.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.64 0.46	0.82 0.60	1.04 0.74	1.25 0.88	1.46 1.00

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AA32

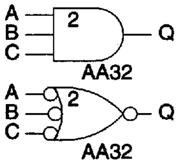
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

AA32 is a 3-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0

Equivalent Gates:...................3.0

Bolt Syntax:............................Q .AA32 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	4.4	nA
EQL_{pd}	9.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	7	14	21	28 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.72 0.50	0.91 0.65	1.11 0.79	1.30 0.91	1.48 1.03

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

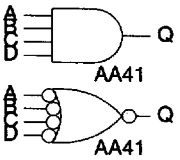
AA41

AMI8G 0.8 micron CMOS Gate Array

Description:

AA41 is a 4-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:....................3.0

Bolt Syntax:............................Q .AA41 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.4	nA
EQL_{pd}	8.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.88 0.52	1.08 0.66	1.31 0.82	1.52 0.95	1.73 1.09

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AA42

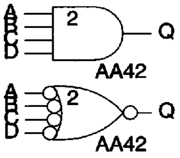
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

AA42 is a 4-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:....................3.0

Bolt Syntax:..............................Q .AA42 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	5.3	nA
EQL_{pd}	9.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	7	14	21	28 (max)
Any Input	Q	t_{PLH}	0.95	1.18	1.39	1.58	1.77
		t_{PHL}	0.53	0.70	0.85	0.97	1.09

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

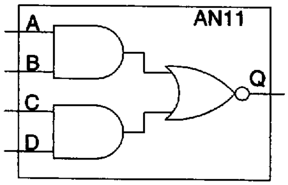
AN11

AMI8G 0.8 micron CMOS Gate Array

Description:

AN11 is an AND-NOR circuit consisting of two 2-input AND gates into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H
H	H	X	X	L
X	X	H	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:....................2.0

Bolt Syntax:.............................Q .AN11 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	1.8	nA
EQL_{pd}	5.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	5	7	9 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.60 0.33	0.79 0.44	0.99 0.54	1.18 0.65	1.37 0.75

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

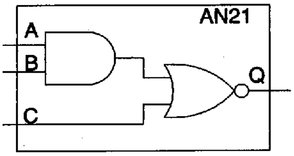
AN21

AMI8G 0.8 micron CMOS Gate Array

Description:

AN21 is an AND-NOR circuit consisting of one 2-input AND gate into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	Q
H	H	X	L
X	X	H	L
All other combinations			H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.6

Equivalent Gates:....................2.0

Bolt Syntax:.............................Q .AN21 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	1.8	nA
EQL_{pd}	5.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.40 0.24	0.55 0.31	0.70 0.38	0.85 0.44	1.00 0.51

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

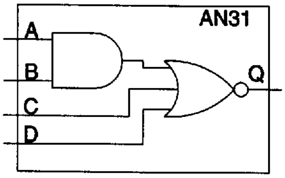
AN31

AMI8G 0.8 micron CMOS Gate Array

Description:

AN31 is an AND-NOR circuit consisting of a 2-input AND gate and two direct inputs into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	L	H
X	L	L	L	H
H	H	X	X	L
X	X	H	X	L
X	X	X	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:...................2.0

Bolt Syntax:............................Q .AN31 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.1	nA
EQL_{pd}	6.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	2	4	5	7 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.87 0.26	1.02 0.31	1.31 0.41	1.45 0.46	1.74 0.56

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

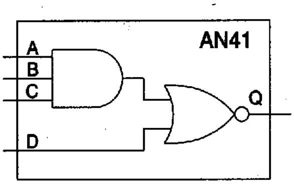
AN41

AMI8G 0.8 micron CMOS Gate Array

Description:

AN41 is an AND-NOR circuit consisting of one 3-input AND gate into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
H	H	H	X	L
X	X	X	H	L
All other combinations				H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.6
D	1.6

Equivalent Gates:....................3.0

Bolt Syntax:.............................Q .AN41 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	1.8	nA
EQL_{pd}	8.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	2	4	5	7 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.40 0.33	0.45 0.36	0.55 0.43	0.60 0.46	0.70 0.52

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMERICAN MICROSYSTEMS, INC.

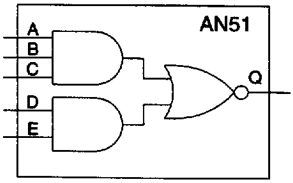
AN51

AMI8G 0.8 micron CMOS Gate Array

Description:

AN51 is an AND-NOR circuit consisting of one 3-input AND gate and one 2-input AND gate into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	H	X	X	L
X	X	X	H	H	L
All other combinations					H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Equivalent Gates:...................4.0

Bolt Syntax:............................Q .AN51 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	12.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.67 0.62	0.84 0.74	1.04 0.88	1.25 1.01	1.45 1.13

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

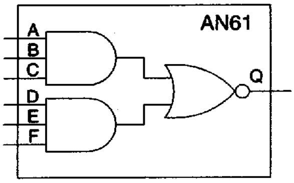
AN61

AMI8G 0.8 micron CMOS Gate Array

Description:

AN61 is an AND-NOR circuit consisting of two 3-input AND gates into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0

Equivalent Gates:....................5.0

Bolt Syntax:.............................Q .AN61 A B C D E F;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.8	nA
EQL_{pd}	15.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	7	14	21	28 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.78 0.74	0.95 0.87	1.13 0.99	1.31 1.11	1.49 1.22

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

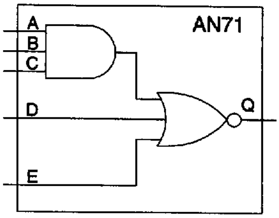
AN71

AMI8G 0.8 micron CMOS Gate Array

Description:

AN71 is an AND-NOR circuit consisting of one 3-input AND gate into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
All other combinations					H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.6
D	1.6
E	1.6

Equivalent Gates:....................4.0

Bolt Syntax:.............................Q .AN71 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	1.8	nA
EQL_{pd}	11.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	2	4	5	7 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.67 0.38	0.75 0.42	0.89 0.49	0.97 0.52	1.11 0.59

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

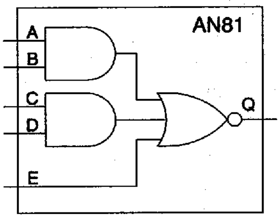
AN81

AMI8G 0.8 micron CMOS Gate Array

Description:

AN81 is an AND-NOR circuit consisting of two 2-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	X	X	X	L
X	X	H	H	X	L
X	X	X	X	H	L
All other combinations					H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Equivalent Gates: 5.0

Bolt Syntax: ....Q .AN81 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.8	nA
EQL_{pd}	15.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	7	14	21	28 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.85 0.64	1.04 0.79	1.23 0.92	1.42 1.04	1.60 1.15

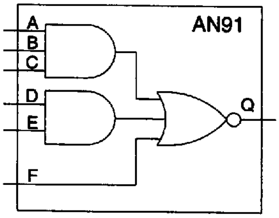
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AN91

Description:

AN91 is an AND-NOR circuit consisting of one 3-input AND gate and one 2-input AND gate into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	H	X	X	X	L
X	X	X	H	H	X	L
X	X	X	X	X	H	L
All other combinations						H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0

Equivalent Gates:....................5.0

Bolt Syntax:.............................Q .AN91 A B C D E F;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.8	nA
EQL_{pd}	15.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.78 0.56	0.96 0.69	1.17 0.83	1.38 0.96	1.59 1.08

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ANA1

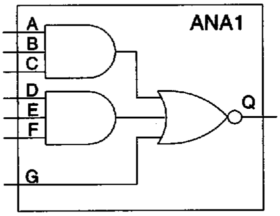
AMI
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

ANA1 is an AND-NOR circuit consisting of two 3-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
H	H	H	X	X	X	X	L
X	X	X	H	H	H	X	L
X	X	X	X	X	X	H	L
All other combinations							H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0
G	1.0

Equivalent Gates:....................6.0

Bolt Syntax:.............................Q .ANA1 A B C D E F G;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	10.6	nA
EQL_{pd}	19.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	7	14	21	28 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.86 0.80	1.06 0.95	1.25 1.08	1.43 1.19	1.61 1.30

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

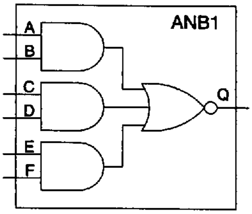
ANB1

AMI8G 0.8 micron CMOS Gate Array

Description:

ANB1 is an AND-NOR circuit consisting of three 2-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	X	X	X	X	L
X	X	H	H	X	X	L
X	X	X	X	H	H	L
All other combinations						H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0

Equivalent Gates:..................5.0

Bolt Syntax:............................Q .ANB1 A B C D E F;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	8.8	nA
EQL_{pd}	16.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
Any Input	Q	t_{PLH}	0.85	1.03	1.24	1.45	1.66
		t_{PHL}	0.70	0.83	0.98	1.11	1.24

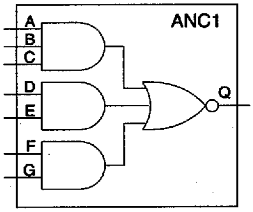
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI8G 0.8 micron CMOS Gate Array

Description:

ANC1 is an AND-NOR circuit consisting of one 3-input AND gate and two 2-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
H	H	H	X	X	X	X	L
X	X	X	H	H	X	X	L
X	X	X	X	X	H	H	L
All other combinations							H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0
G	1.0

Equivalent Gates:....................6.0

Bolt Syntax:............................Q .ANC1 A B C D E F G;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	10.6	nA
EQL_{pd}	19.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	7	14	21	28 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.87 0.64	1.06 0.78	1.26 0.91	1.44 1.03	1.62 1.14

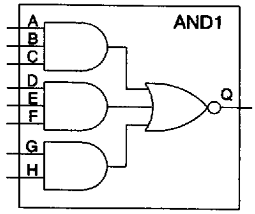
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AND1

Description:

AND1 is an AND-NOR circuit consisting of two 3-input AND gates and one 2-input AND gate into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
H	H	H	X	X	X	X	X	L
X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	H	H	L
All other combinations								H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0
G	1.0
H	1.0

Equivalent Gates:....................6.0

Bolt Syntax:.............................Q .AND1 A B C D E F G H;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	10.6	nA
EQL_{pd}	20.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.86 0.82	1.04 0.95	1.26 1.09	1.46 1.22	1.67 1.35

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ANE1

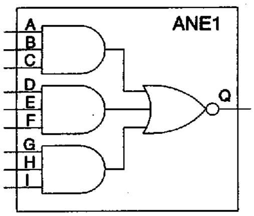
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

ANE1 is an AND-NOR circuit consisting of three 3-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Q
H	H	H	X	X	X	X	X	X	L
X	X	X	H	H	H	X	X	X	L
X	X	X	X	X	X	H	H	H	L
All other combinations									H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0
G	1.0
H	1.0
I	1.0

Equivalent Gates:....................7.0

Bolt Syntax:.............................Q .ANE1 A B C D E F G H I;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	12.4	nA
EQL_{pd}	22.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	7	14	21	28 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.96 0.81	1.15 0.94	1.35 1.07	1.53 1.19	1.71 1.30

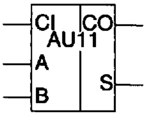
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AU11

Description:

AU11 is a combinational one-bit full adder.

Logic Symbol



Truth Table

CI	A	B	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

Pin Loading

	Equivalent Load
A	4.1
B	4.1
CI	3.1

Equivalent Gates:....................7.0

Bolt Syntax:..............................CO S .AU11 A B CI;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	7.1	nA
EQL_{pd}	23.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

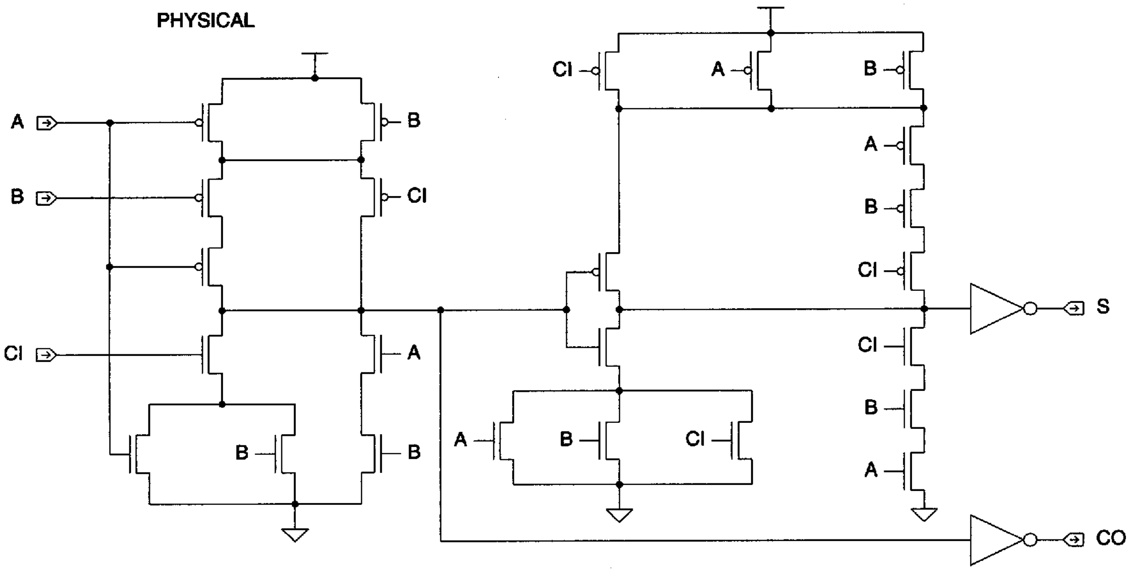
Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
A	S	t_{PLH} t_{PHL}	1.42 1.03	1.59 1.22	1.81 1.41	2.01 1.57	2.22 1.72
B	S	t_{PLH} t_{PHL}	1.43 1.10	1.64 1.26	1.82 1.42	2.03 1.57	2.24 1.71
CI	S	t_{PLH} t_{PHL}	1.21 1.08	1.40 1.24	1.60 1.41	1.81 1.56	2.02 1.69
A	CO	t_{PLH} t_{PHL}	0.70 0.95	0.88 1.14	1.10 1.34	1.31 1.51	1.52 1.67
B	CO	t_{PLH} t_{PHL}	0.69 0.97	0.87 1.16	1.09 1.36	1.30 1.53	1.51 1.69
CI	CO	t_{PLH} t_{PHL}	0.62 0.69	0.79 0.86	1.01 1.05	1.22 1.22	1.43 1.38

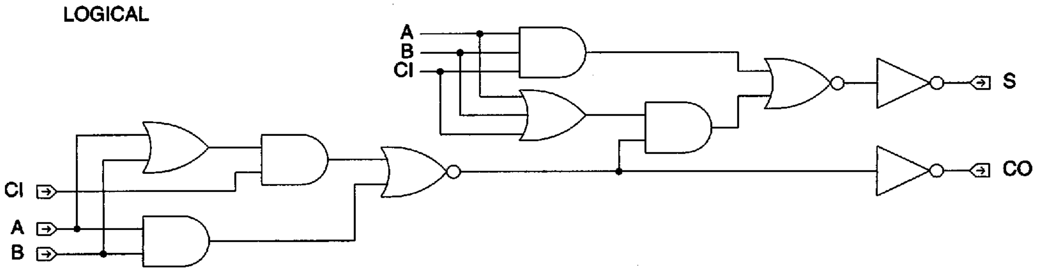
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

(continued on next page)

AMI8G 0.8 micron CMOS Gate Array

Logic Schematic





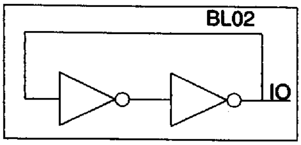
BL02

AMI8G 0.8 micron CMOS Gate Array

Description:

BL02 is a tri-state bus latch that stores the final binary level on the bus when left undriven.

Logic Symbol



Truth Table

N/A

Pin Loading

	Equivalent Load
IO	2.5

Equivalent Gates:....................4.0

Bolt Syntax:.............................IO .BL02;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	14.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Equivalent Load 1
IO	IO	t_{PLH}	0.34
		t_{PHL}	0.59

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

CVDD

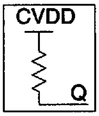
AMI8G 0.8 micron CMOS Gate Array

Description:

CVDD is the resistive tie-up to the core V_{DD} bus for all cell inputs.

Equivalent Gates:....................1.0

Bolt Syntax:.............................Q .CVDD;



CVSS

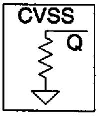
AMI8G 0.8 micron CMOS Gate Array

Description:

CVSS is the resistive tie-down to the core V_{SS} bus for all cell inputs.

Equivalent Gates:....................1.0

Bolt Syntax:..............................Q .CVSS;



DC24

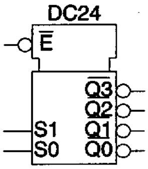
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DC24 is a two-to-four line decoder/demultiplexer with active low enable.

Logic Symbol



Truth Table

EN	S1	S0	Q0N	Q1N	Q2N	Q3N
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

Pin Loading

	Equivalent Load
S0	3.1
S1	3.1
EN	1.0

Equivalent Gates:..................8.0

Bolt Syntax:............................Q0N Q1N Q2N Q3N .DC24 EN S0 S1;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	13.3	nA
EQL_{pd}	27.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

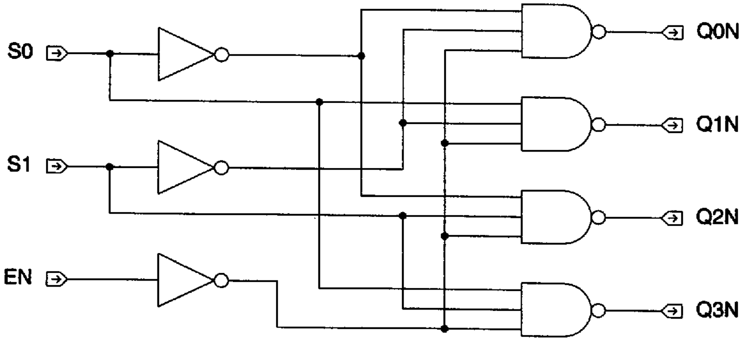
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	2	4	5	7 (max)
Sx	QN	t_{PLH} t_{PHL}	0.43 0.56	0.49 0.63	0.59 0.78	0.64 0.85	0.75 0.99
EN	QN	t_{PLH} t_{PHL}	0.59 0.71	0.64 0.79	0.75 0.94	0.80 1.01	0.91 1.15

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

(continued on next page)

Logic Schematic



DC38

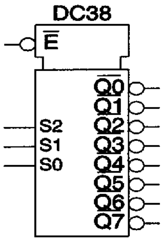
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DC38 is a three-to-eight line decoder/demultiplexer with active low enable.

Logic Symbol



Truth Table

Truth Table Appears On Next Page

Pin Loading

	Equivalent Load
S0	5.5
S1	5.2
S2	5.1
EN	1.0

Equivalent Gates:....................20.0

Bolt Syntax:.............................Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N .DC38 EN S0 S1 S2;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	31.8	nA
EQL_{pd}	58.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	2	3	5	6 (max)
Sx	QN	t_{PLH} t_{PHL}	0.61 0.86	0.66 0.95	0.72 1.04	0.82 1.22	0.87 1.31
EN	QN	t_{PLH} t_{PHL}	0.85 1.10	0.91 1.19	0.97 1.28	1.08 1.46	1.13 1.55

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

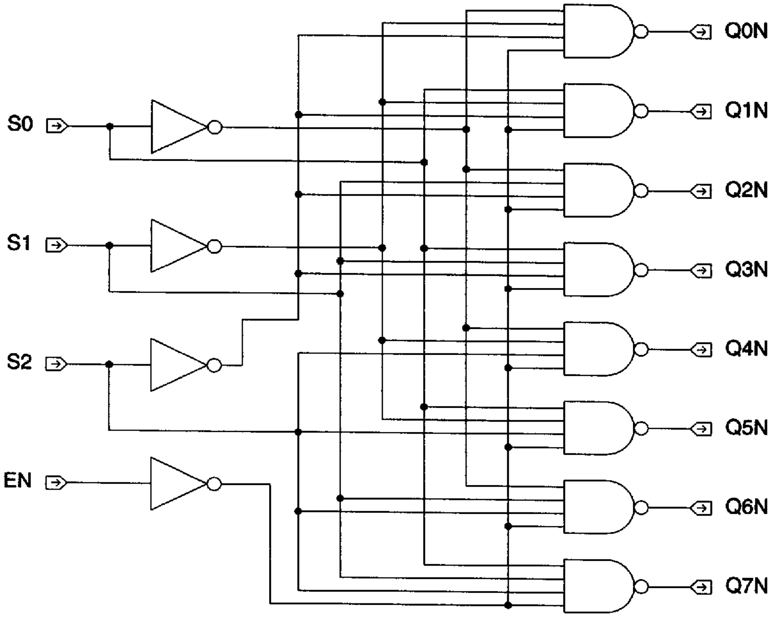
(continued on next page)

DC38

Truth Table

EN	S2	S1	S0	Q0N	Q1N	Q2N	Q3N	Q4N	Q5N	Q6N	Q7N
H	X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	L

Logic Schematic



DF081

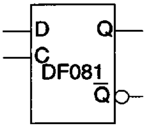
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF081 is a static, master-slave, D flip-flop without SET or RESET. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

D	C	Q	QN
H	↑	H	L
L	↑	L	H
X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.1

Equivalent Gates:....................6.0

Bolt Syntax:.............................Q QN .DF081 C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	6.2	nA
EQL_{pd}	21.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

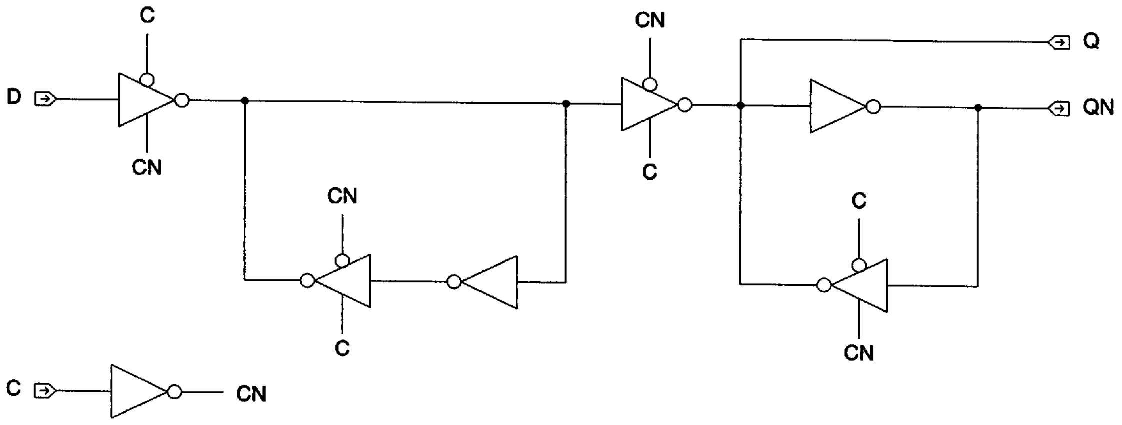
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.69 0.28	0.87 0.39	1.06 0.49	1.25 0.59	1.43 0.69
C	QN	t_{PLH} t_{PHL}	0.53 0.81	0.65 0.90	0.76 0.99	0.86 1.07	0.96 1.14
Min C Width	High	t_w	0.85				
Min C Width	Low	t_w	0.85				
Min D Setup		t_{su}	0.78				
Min D Hold		t_h	0.00				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

(continued on next page)

Logic Schematic



DF091

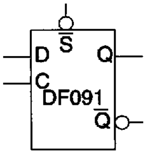
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF091 is a static, master-slave, D flip-flop. SET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.2
SN	2.0

Equivalent Gates:....................7.0

Bolt Syntax:.............................Q QN .DF091 C D SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.0	nA
EQL_{pd}	23.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.55 0.92	0.67 1.04	0.78 1.16	0.89 1.27	1.00 1.38
C	QN	t_{PLH} t_{PHL}	0.69 0.28	0.88 0.39	1.07 0.49	1.26 0.59	1.45 0.69
SN	Q	t_{PLH}	0.29	0.40	0.51	0.62	0.73
SN	QN	t_{PHL}	0.61	0.72	0.82	0.92	1.03

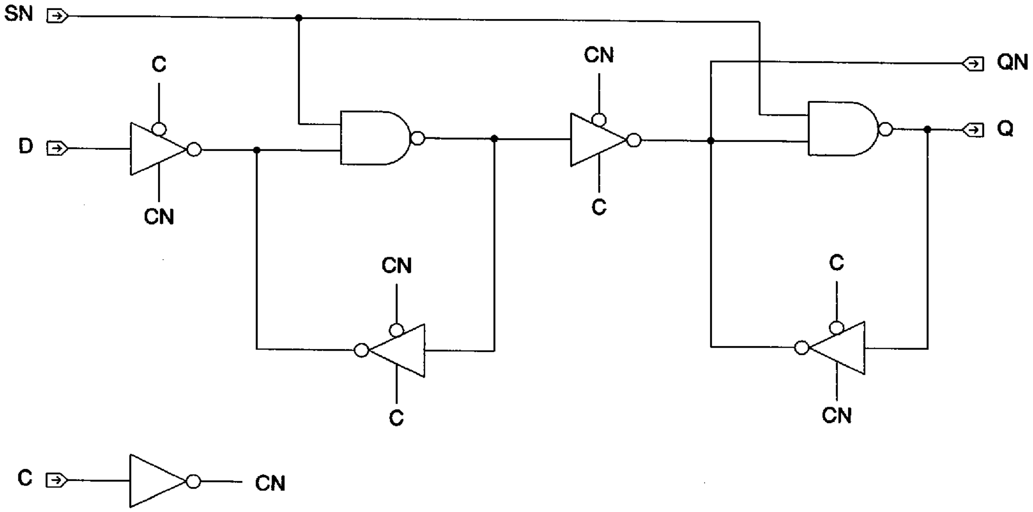
(continued on next page)

DF091

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	0.95				
Min C Width	Low	t_w	0.88				
Min SN Width	Low	t_w	0.63				
Min D Setup		t_{su}	0.85				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



DF0A1

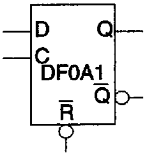
AMI
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF0A1 is a static, master-slave, D flip-flop. RESET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.2
RN	1.0

Equivalent Gates:.....................7.0

Bolt Syntax:.............................Q QN .DF0A1 C D RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	27.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.73 0.83	0.93 0.93	1.12 1.01	1.32 1.09	1.51 1.17
C	QN	t_{PLH} t_{PHL}	0.70 0.28	0.89 0.38	1.08 0.49	1.28 0.59	1.47 0.69
RN	Q	t_{PHL}	0.48	0.56	0.63	0.70	0.76
RN	QN	t_{PLH}	1.01	1.09	1.17	1.25	1.34

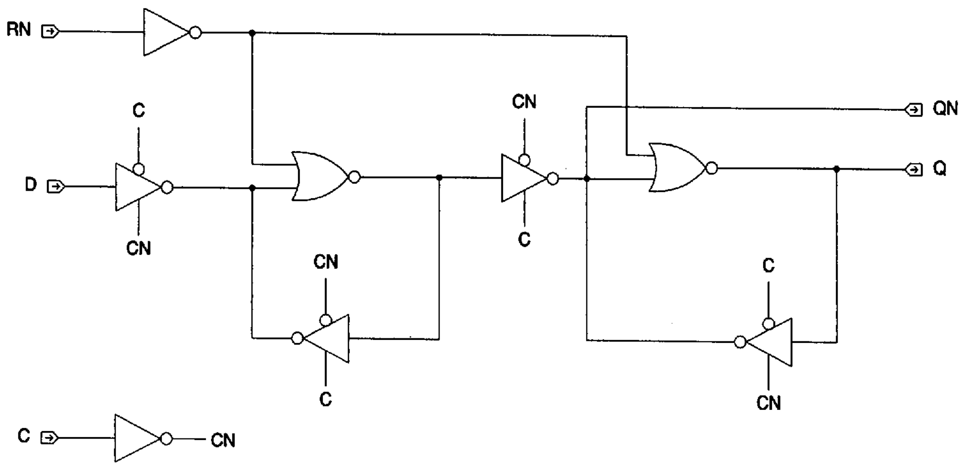
(continued on next page)

DF0A1

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	0.87				
Min C Width	Low	t_w	1.05				
Min RN Width	Low	t_w	1.01				
Min D Setup		t_{su}	0.79				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.67				
Min RN Hold		t_h	0.55				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Schematic Logic



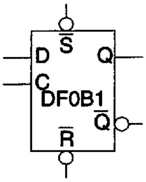
DF0B1

AMI8G 0.8 micron CMOS Gate Array

Description:

DF0B1 is a static, master-slave, D flip-flop. SET and RESET are asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

NC = No Change
IL = Illegal

Pin Loading

	Equivalent Load
D	1.0
C	3.2
SN	2.0
RN	2.1

Equivalent Gates:....................9.0

Bolt Syntax:..............................Q QN .DF0B1 C D RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.9	nA
EQL_{pd}	31.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.56 0.93	0.67 1.06	0.78 1.17	0.89 1.28	0.99 1.39
C	QN	t_{PLH} t_{PHL}	0.67 0.28	0.86 0.39	1.05 0.49	1.24 0.59	1.42 0.69
RN	Q	t_{PHL}	1.01	1.14	1.26	1.37	1.48
RN	QN	t_{PLH}	0.73	0.94	1.13	1.33	1.53
SN	Q	t_{PLH}	0.31	0.42	0.52	0.63	0.73
SN	QN	t_{PHL}	0.81	0.96	1.10	1.25	1.39

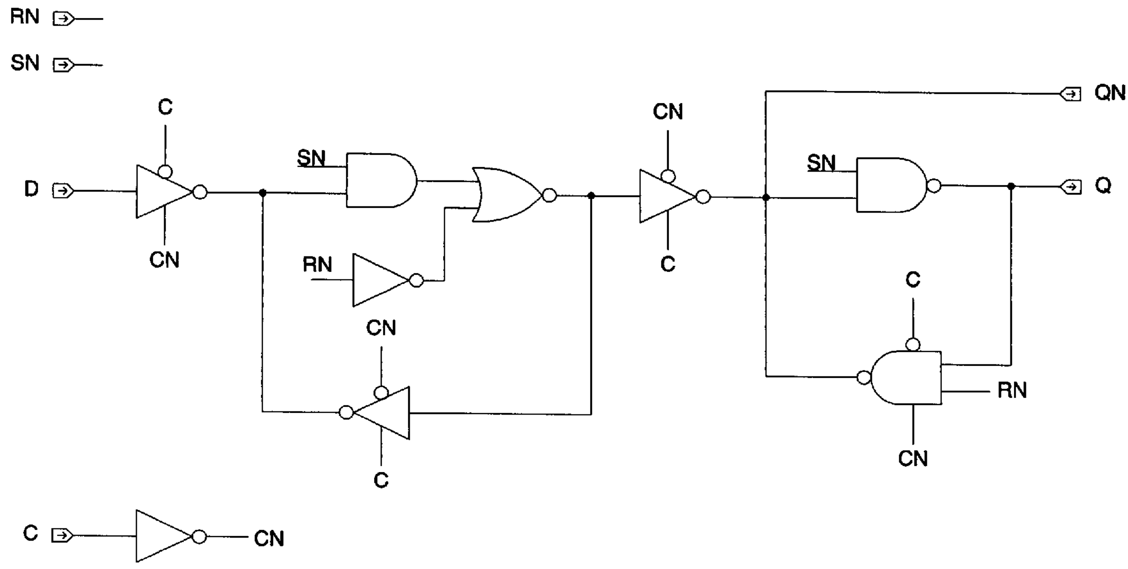
(continued on next page)

DF0B1

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	0.97				
Min C Width	Low	t_w	1.05				
Min RN Width	Low	t_w	0.97				
Min SN Width	Low	t_w	0.84				
Min D Setup		t_{su}	0.83				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.70				
Min RN Hold		t_h	0.56				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



DF101

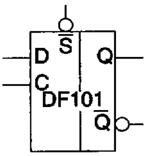
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF101 is a static, master-slave, D flip-flop. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.2
SN	2.0

Equivalent Gates:...................8.0

Bolt Syntax:............................Q QN .DF101 C D SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	9.7	nA
EQL_{pd}	28.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.55 0.86	0.73 1.03	0.95 1.21	1.16 1.37	1.37 1.52
C	QN	t_{PLH} t_{PHL}	1.38 0.82	1.56 0.95	1.77 1.10	1.97 1.23	2.18 1.36
SN	Q	t_{PLH}	0.98	1.15	1.37	1.57	1.78
SN	QN	t_{PHL}	0.46	0.59	0.73	0.87	0.99

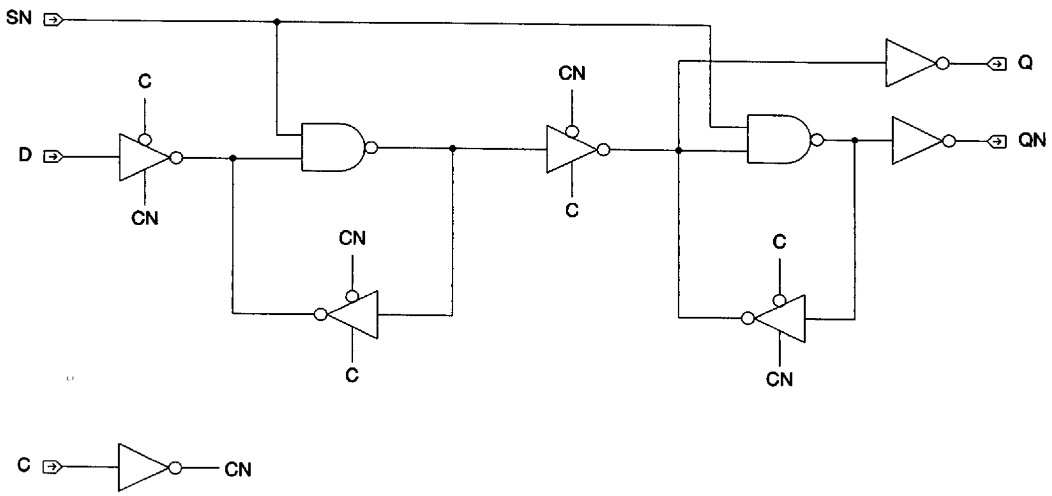
(continued on next page)

DF101

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min C Width	High	t_w	0.78				
Min C Width	Low	t_w	0.85				
Min SN Width		t_w	0.60				
Min D Setup		t_{su}	0.82				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.26				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



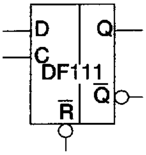
DF111

AMI8G 0.8 micron CMOS Gate Array

Description:

DF111 is a static, master-slave, D flip-flop. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.2
RN	1.0

Equivalent Gates:...................8.0

Bolt Syntax:............................Q QN .DF111 C D RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.9	nA
EQL_{pd}	32.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.54 0.87	0.72 1.04	0.94 1.23	1.15 1.38	1.36 1.53
C	QN	t_{PLH} t_{PHL}	1.19 0.97	1.35 1.13	1.56 1.29	1.76 1.43	1.97 1.57
RN	Q	t_{PHL}	1.28	1.45	1.62	1.78	1.92
RN	QN	t_{PLH}	0.68	0.84	1.05	1.26	1.46

(continued on next page)

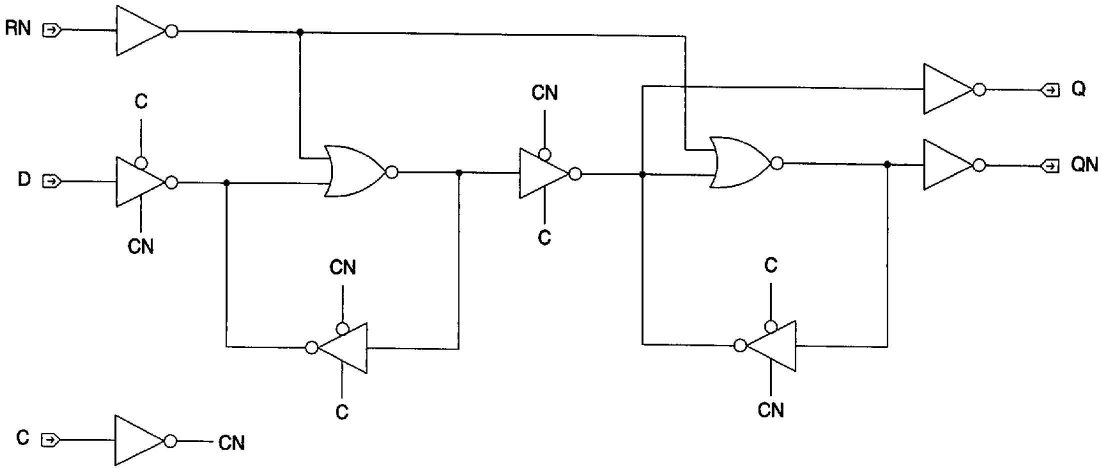
DF111

AMI8G 0.8 micron CMOS Gate Array

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min C Width	High	t_w	0.79				
Min C Width	Low	t_w	1.01				
Min RN Width		t_w	1.01				
Min D Setup		t_{su}	0.77				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.64				
Min RN Hold		t_h	0.56				

Delay will vary with input conditions. See page 2-15 for interconnect estimates

Logic Schematic



DF121

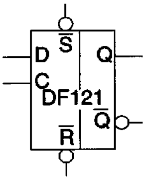
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF121 is a static, master-slave, D flip-flop. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

IL = Illegal NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.1
SN	2.0
RN	2.1

Equivalent Gates: 10.0

Bolt Syntax: ....Q QN .DF121 C D RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	10.6	nA
EQL_{pd}	35.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.55 0.84	0.72 1.01	0.94 1.18	1.15 1.34	1.36 1.48
C	QN	t_{PLH} t_{PHL}	1.37 0.82	1.55 0.95	1.76 1.09	1.97 1.22	2.18 1.35
SN	Q	t_{PLH}	1.23	1.42	1.65	1.86	2.07
SN	QN	t_{PHL}	0.47	0.60	0.75	0.88	1.01
RN	Q	t_{PHL}	0.90	1.08	1.26	1.42	1.56
RN	QN	t_{PLH}	1.46	1.63	1.84	2.05	2.26

(continued on next page)

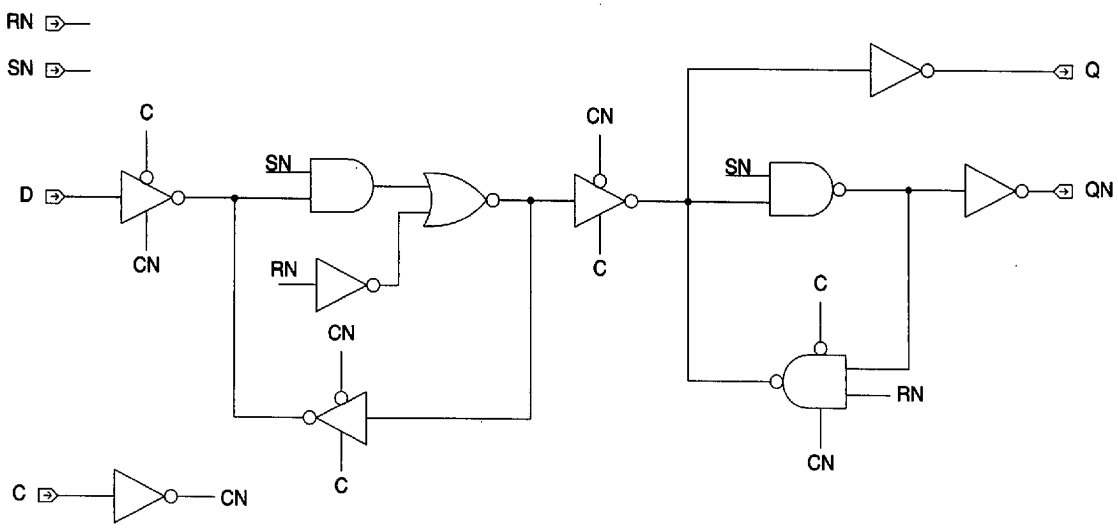
DF121

AMI8G 0.8 micron CMOS Gate Array

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min C Width	High	t_w	0.76				
Min C Width	Low	t_w	1.05				
Min RN Width	Low	t_w	0.96				
Min SN Width	Low	t_w	0.84				
Min D Setup		t_{su}	0.83				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.70				
Min RN Hold		t_h	0.56				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



DF281

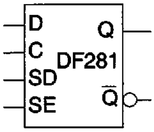
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF281 is a static, master-slave, multiplexed scan, D flip-flop without SET or RESET. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	Q	QN
↑	H	X	L	H	L
↑	L	X	L	L	H
↑	X	H	H	H	L
↑	X	L	H	L	H
L	X	X	X	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
C	3.1
D	1.0
SD	1.0
SE	2.1

Equivalent Gates:..................8.0

Bolt Syntax:............................Q QN .DF281 C D SD SE;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.0	nA
EQL_{pd}	29.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.53 0.80	0.64 0.90	0.75 0.99	0.85 1.06	0.95 1.14
C	QN	t_{PLH} t_{PHL}	0.69 0.29	0.87 0.39	1.06 0.49	1.24 0.59	1.43 0.70

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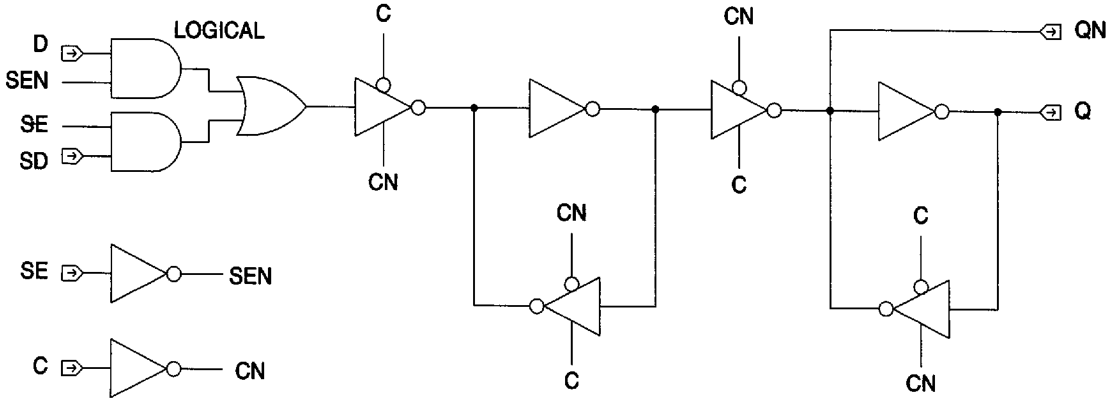
Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	3	5	7	9 (max)
Min C Width	High	t_w	0.59				
Min C Width	Low	t_w	1.03				
Min D Setup		t_{su}	1.17				
Min D Hold		t_h	0.00				
Min SD Setup		t_{su}	1.17				
Min SD Hold		t_h	0.00				
Min SE Setup		t_{su}	1.35				
Min SE Hold		t_h	0.00				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded

Logic Schematic



DF291

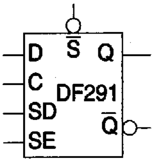
AMI
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF291 is a static, master-slave, multiplexed scan, D flip-flop. SET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	SN	Q	QN
↑	H	X	L	H	H	L
↑	L	X	L	H	L	H
↑	X	H	H	H	H	L
↑	X	L	H	H	L	H
X	X	X	X	L	H	L
L	X	X	X	H	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
C	3.1
D	1.0
SD	1.0
SE	2.1
SN	2.0

Equivalent Gates:..................11.0

Bolt Syntax:...........................Q QN .DF291 C D SD SE SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	9.7	nA
EQL_{pd}	32.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.58 0.95	0.69 1.08	0.80 1.19	0.90 1.30	1.01 1.41
C	QN	t_{PLH} t_{PHL}	0.69 0.29	0.87 0.40	1.06 0.50	1.25 0.60	1.43 0.71
SN	Q	t_{PLH}	0.30	0.41	0.51	0.62	0.72
SN	QN	t_{PHL}	0.63	0.74	0.84	0.94	1.05

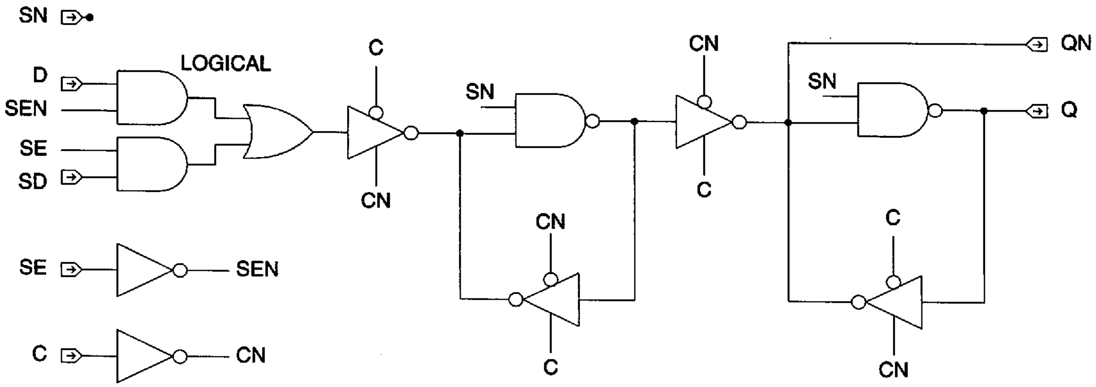
(continued on next page)

DF291

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	0.59				
Min C Width	Low	t_w	1.15				
Min SN Width	Low	t_w	0.64				
Min D Setup		t_{su}	1.45				
Min D Hold		t_h	0.00				
Min SD Setup		t_{su}	1.45				
Min SD Hold		t_h	0.00				
Min SE Setup		t_{su}	1.65				
Min SE Hold		t_h	0.00				
Min SN Setup		t_{su}	0.29				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded

Logic Schematic



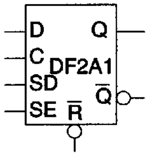
DF2A1

AMI8G 0.8 micron CMOS Gate Array

Description:

DF2A1 is a static, master-slave, multiplexed scan, D flip-flop. RESET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	Q	QN
↑	H	H	X	L	H	L
↑	L	H	X	L	L	H
↑	X	H	H	H	H	L
↑	X	H	L	H	L	H
X	X	L	X	X	L	H
L	X	H	X	X	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
C	3.1
D	1.0
RN	1.0
SD	1.0
SE	2.1

Equivalent Gates:..................11.0

Bolt Syntax:............................Q QN .DF2A1 C D RN SD SE;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.9	nA
EQL_{pd}	36.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.74 0.84	0.93 0.94	1.12 1.02	1.31 1.10	1.50 1.17
C	QN	t_{PLH} t_{PHL}	0.70 0.29	0.89 0.39	1.08 0.50	1.27 0.60	1.46 0.70
RN	Q	t_{PHL}	0.49	0.57	0.64	0.70	0.77
RN	QN	t_{PLH}	1.01	1.09	1.18	1.26	1.34

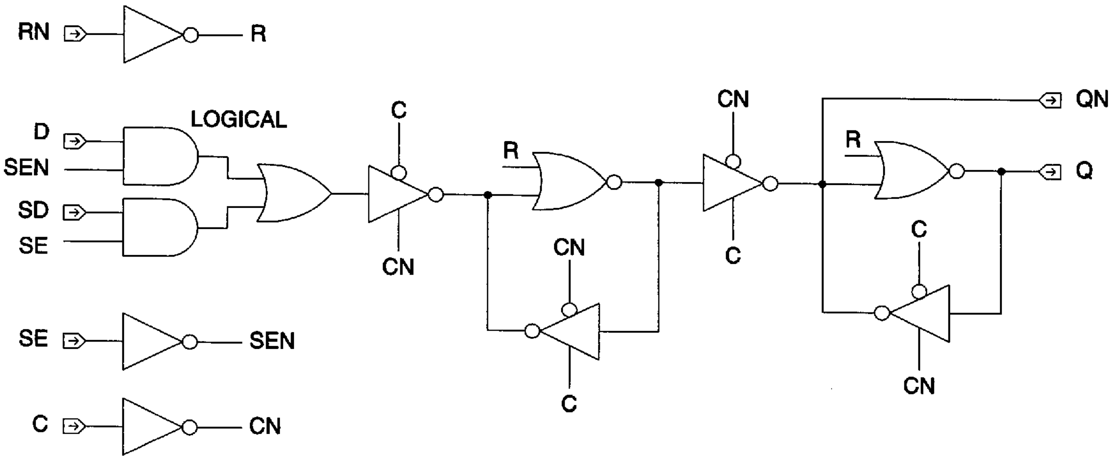
(continued on next page)

DF2A1

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	0.61				
Min C Width	Low	t_w	1.35				
Min RN Width	Low	t_w	1.04				
Min D Setup		t_{su}	1.27				
Min D Hold		t_h	0.00				
Min SD Setup		t_{su}	1.27				
Min SD Hold		t_h	0.00				
Min SE Setup		t_{su}	1.45				
Min SE Hold		t_h	0.00				
Min RN Setup		t_{su}	0.68				
Min RN Hold		t_h	0.56				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



DF2B1

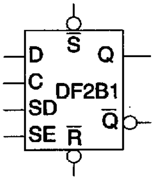
AMI
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF2B1 is a static, master-slave, multiplexed scan, D flip-flop. SET and RESET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	SN	Q	QN
↑	H	H	X	L	H	H	L
↑	L	H	X	L	H	L	H
↑	X	H	H	H	H	H	L
↑	X	H	L	H	H	L	H
X	X	L	X	X	H	L	H
X	X	H	X	X	L	H	L
X	X	L	X	X	L	IL	IL
L	X	H	X	X	H	NC	NC

NC = No Change IL = Illegal Condition

Pin Loading

	Equivalent Load
C	3.2
D	1.0
RN	2.0
SD	1.0
SE	2.1
SN	2.1

Equivalent Gates:..................12.0

Bolt Syntax:............................Q QN .DF2B1 C D RN SD SE SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	10.6	nA
EQL_{pd}	38.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.55 0.92	0.67 1.05	0.78 1.16	0.89 1.27	0.99 1.38
C	QN	t_{PLH} t_{PHL}	0.69 0.29	0.88 0.40	1.07 0.50	1.25 0.60	1.44 0.71
RN	Q	t_{PHL}	0.98	1.12	1.24	1.35	1.46
RN	QN	t_{PLH}	0.74	0.95	1.14	1.34	1.54
SN	Q	t_{PLH}	0.28	0.38	0.49	0.60	0.70
SN	QN	t_{PHL}	0.80	0.95	1.09	1.23	1.37

(continued on next page)

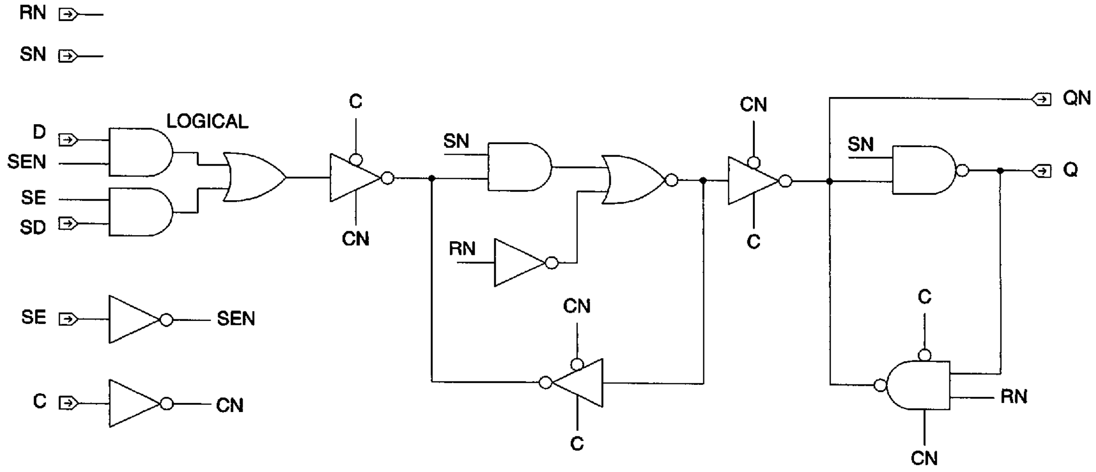
DF2B1

AMI8G 0.8 micron CMOS Gate Array

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	0.69				
Min C Width	Low	t_w	1.42				
Min RN Width	Low	t_w	0.98				
Min SN Width	Low	t_w	0.93				
Min D Setup		t_{su}	1.47				
Min D Hold		t_h	0.00				
Min SD Setup		t_{su}	1.47				
Min SD Hold		t_h	0.00				
Min SE Setup		t_{su}	1.67				
Min SE Hold		t_h	0.00				
Min RN Setup		t_{su}	0.74				
Min RN Hold		t_h	0.56				
Min SN Setup		t_{su}	0.31				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



DF401

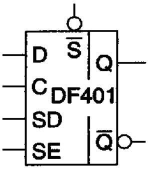
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF401 is a static, master-slave, multiplexed scan, D flip-flop. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	SN	Q	QN
↑	H	X	L	H	H	L
↑	L	X	L	H	L	H
↑	X	H	H	H	H	L
↑	X	L	H	H	L	H
X	X	X	X	L	H	L
L	X	X	X	H	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
C	3.1
D	1.0
SD	1.0
SE	2.1
SN	2.0

Equivalent Gates:..................12.0

Bolt Syntax:............................Q QN .DF401 C D SD SE SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	11.5	nA
EQL_{pd}	37.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

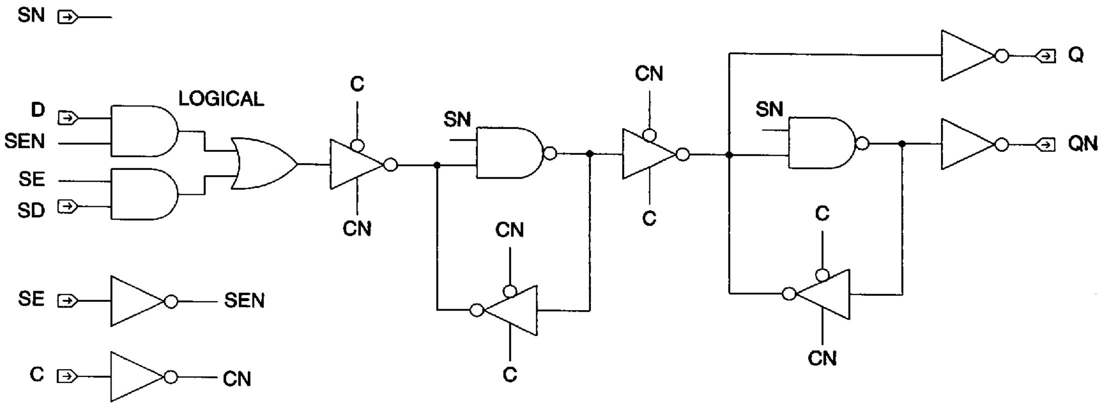
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.57 0.87	0.75 1.04	0.98 1.23	1.19 1.39	1.41 1.54
C	QN	t_{PLH} t_{PHL}	1.40 0.85	1.58 0.99	1.80 1.14	2.01 1.27	2.22 1.40
SN	Q	t_{PLH}	0.99	1.17	1.39	1.61	1.82
SN	QN	t_{PHL}	0.48	0.62	0.77	0.90	1.03

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min C Width	High	t_w	1.12				
Min C Width	Low	t_w	1.16				
Min SN Width	Low	t_w	0.72				
Min D Setup		t_{su}	1.49				
Min D Hold		t_h	0.00				
Min SD Setup		t_{su}	1.49				
Min SD Hold		t_h	0.00				
Min SE Setup		t_{su}	1.63				
Min SE Hold		t_h	0.00				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



Core Logic

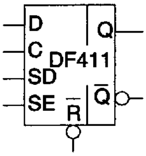
DF411

AMI8G 0.8 micron CMOS Gate Array

Description:

DF411 is a static, master-slave, multiplexed scan, D flip-flop. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	Q	QN
↑	H	H	X	L	H	L
↑	L	H	X	L	L	H
↑	X	H	H	H	H	L
↑	X	H	L	H	L	H
X	X	L	X	X	L	H
L	X	H	X	X	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
C	3.1
D	1.0
RN	1.0
SD	1.0
SE	2.1

Equivalent Gates:..................12.0

Bolt Syntax:............................Q QN .DF411 C D RN SD SE;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	10.6	nA
EQL_{pd}	40.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

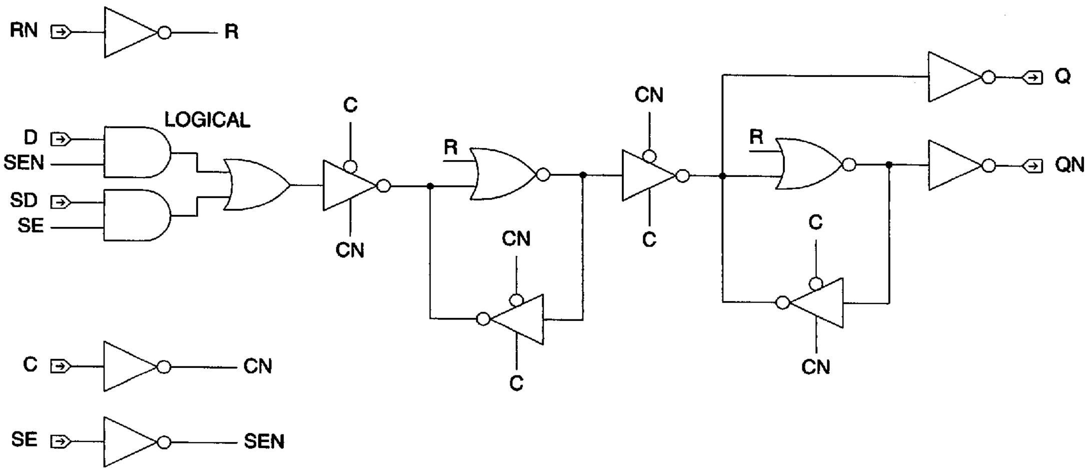
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.56 0.89	0.73 1.06	0.95 1.25	1.16 1.41	1.37 1.56
C	QN	t_{PLH} t_{PHL}	1.22 1.03	1.38 1.19	1.59 1.36	1.79 1.51	2.00 1.65
RN	Q	t_{PHL}	1.30	1.47	1.64	1.80	1.94
RN	QN	t_{PLH}	0.70	0.87	1.07	1.28	1.49

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min C Width	High	t_w	0.97				
Min C Width	Low	t_w	1.35				
Min RN Width	Low	t_w	1.03				
Min D Setup		t_{su}	1.27				
Min D Hold		t_h	0.00				
Min SD Setup		t_{su}	1.27				
Min SD Hold		t_h	0.00				
Min SE Setup		t_{su}	1.45				
Min SE Hold		t_h	0.00				
Min RN Setup		t_{su}	0.68				
Min RN Hold		t_h	0.56				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



DF421

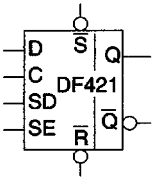
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF421 is a static, master-slave, multiplexed scan, D flip-flop. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	SN	Q	QN
↑	H	H	X	L	H	H	L
↑	L	H	X	L	H	L	H
↑	X	H	H	H	H	H	L
↑	X	H	L	H	H	L	H
X	X	L	X	X	H	L	H
X	X	H	X	X	L	H	L
X	X	L	X	X	L	IL	IL
L	X	H	X	X	H	NC	NC

NC = No Change IL = Illegal Condition

Pin Loading

	Equivalent Load
C	3.2
D	1.0
RN	2.0
SD	1.0
SE	2.1
SN	2.1

Equivalent Gates:..................12.0

Bolt Syntax:............................Q QN .DF421 C D RN SD SE SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	12.4	nA
EQL_{pd}	43.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.57 0.87	0.75 1.04	0.98 1.22	1.20 1.38	1.41 1.53
C	QN	t_{PLH} t_{PHL}	1.35 0.81	1.53 0.94	1.75 1.08	1.96 1.21	2.17 1.34
RN	Q	t_{PHL}	0.92	1.10	1.29	1.45	1.59
RN	QN	t_{PLH}	1.42	1.59	1.81	2.02	2.23
SN	Q	t_{PLH}	1.22	1.42	1.65	1.87	2.08
SN	QN	t_{PHL}	0.44	0.57	0.71	0.84	0.97

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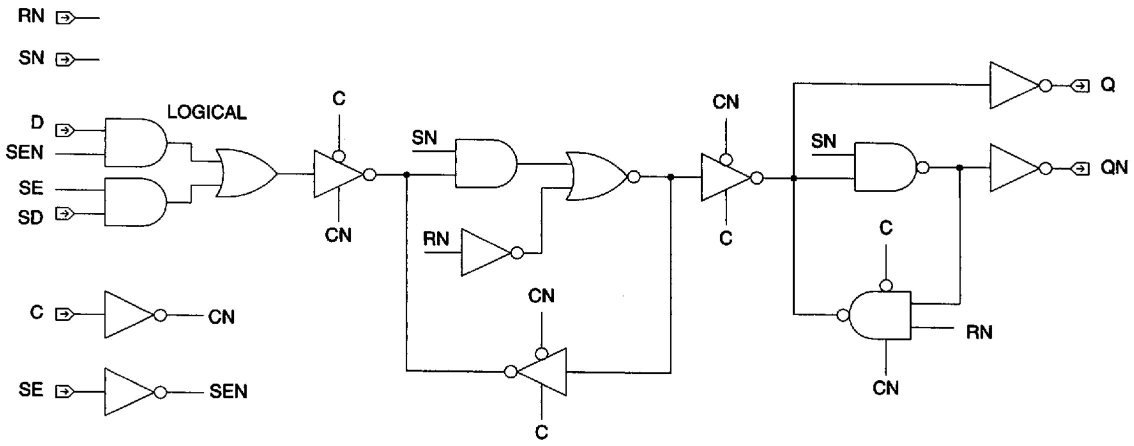
DF421

AMI8G 0.8 micron CMOS Gate Array

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
Min C Width	High	t_w	1.09				
Min C Width	Low	t_w	1.43				
Min RN Width	Low	t_w	0.98				
Min SN Width	Low	t_w	0.93				
Min D Setup		t_{su}	1.47				
Min D Hold		t_h	0.00				
Min SD Setup		t_{su}	1.47				
Min SD Hold		t_h	0.00				
Min SE Setup		t_{su}	1.67				
Min SE Hold		t_h	0.00				
Min RN Setup		t_{su}	0.74				
Min RN Hold		t_h	0.56				
Min SN Setup		t_{su}	0.31				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



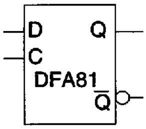
DFA81

AMI8G 0.8 micron CMOS Gate Array

Description:

DFA81 is a static, master-slave, D flip-flop without SET or RESET. Outputs are unbuffered and change state on the rising edge of the clock. Transmission gate equivalent of DF081.

Logic Symbol



Truth Table

D	C	Q	QN
H	↑	H	L
L	↑	L	H
X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.2

Equivalent Gates:..................6.0

Bolt Syntax:............................Q QN .DFA81 C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	18.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.71 0.59	0.82 0.66	0.93 0.73	1.03 0.80	1.14 0.87
C	QN	t_{PLH} t_{PHL}	0.51 0.56	0.63 0.66	0.74 0.75	0.85 0.83	0.96 0.91
Min C Width	High	t_w	0.50				
Min C Width	Low	t_w	0.62				
Min D Setup		t_{su}	0.54				
Min D Hold		t_h	0.00				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

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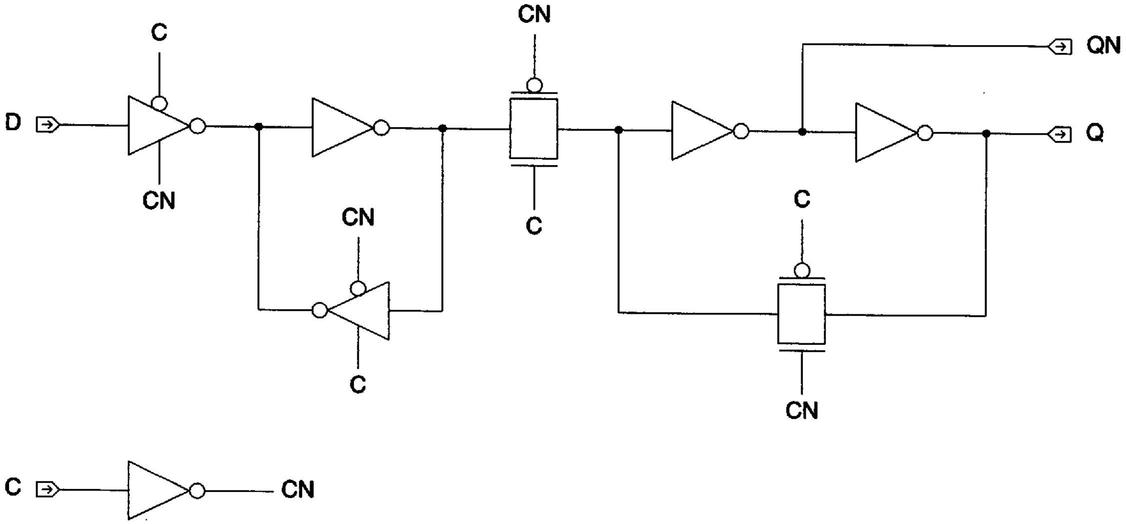
Logic Schematic



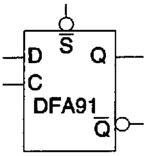
DFA91

AMI8G 0.8 micron CMOS Gate Array

Description:

DFA91 is a static, master-slave, D flip-flop. SET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock. Transmission gate equivalent of DF091.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.1
SN	2.0

Equivalent Gates:....................6.0

Bolt Syntax:.............................Q QN .DFA91 C D SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	21.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.70 0.67	0.81 0.78	0.91 0.88	1.01 0.98	1.11 1.09
C	QN	t_{PLH} t_{PHL}	0.48 0.51	0.61 0.61	0.72 0.69	0.83 0.77	0.94 0.85
SN	Q	t_{PLH}	0.39	0.50	0.61	0.72	0.83
SN	QN	t_{PHL}	0.64	0.74	0.83	0.91	0.99

(continued on next page)

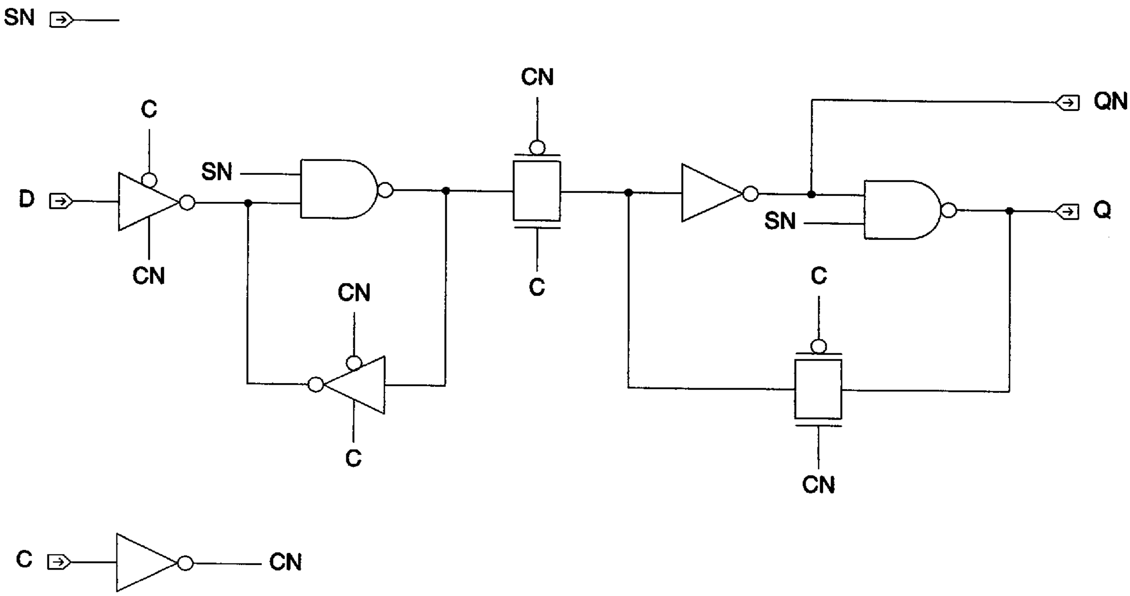
DFA91

AMI8G 0.8 micron CMOS Gate Array

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	0.72				
Min C Width	Low	t_w	0.69				
Min SN Width	Low	t_w	0.79				
Min D Setup		t_{su}	0.71				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.21				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



DFAA1

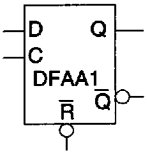
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DFAA1 is a static, master-slave, D flip-flop. RESET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock. Transmission gate equivalent of DF0A1.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.1
RN	2.1

Equivalent Gates:..................7.0

Bolt Syntax:............................Q QN .DFAA1 C D RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	21.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

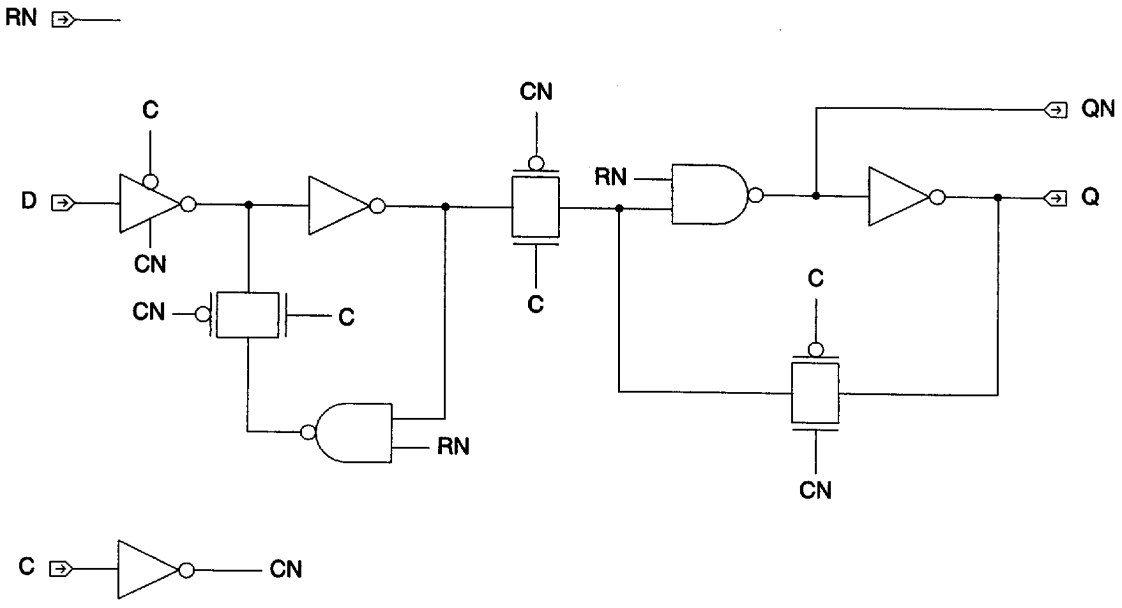
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.81 0.59	0.93 0.67	1.03 0.74	1.13 0.81	1.24 0.88
C	QN	t_{PLH} t_{PHL}	0.51 0.66	0.63 0.79	0.74 0.91	0.84 1.03	0.95 1.14
RN	Q	t_{PHL}	0.47	0.56	0.63	0.70	0.78
RN	QN	t_{PLH}	0.28	0.39	0.49	0.60	0.70

(continued on next page)

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	3	5	7	9 (max)
Min C Width	High	t_w	0.85				
Min C Width	Low	t_w	0.66				
Min RN Width	Low	t_w	0.46				
Min D Setup		t_{su}	0.58				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.19				
Min RN Hold		t_h	0.35				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Schematic Logic



DFAB1

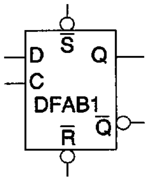
AMI
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DFAB1 is a static, master-slave, D flip-flop. SET and RESET are asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock. Transmission gate equivalent of DF0B1.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

NC = No Change
IL = Illegal

Pin Loading

	Equivalent Load
D	1.0
C	3.1
SN	2.0
RN	2.0

Equivalent Gates:..................7.0

Bolt Syntax:............................Q QN .DFAB1 C D RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	8.8	nA
EQL_{pd}	22.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.81 0.69	0.92 0.80	1.02 0.90	1.12 1.00	1.22 1.10
C	QN	t_{PLH} t_{PHL}	0.50 0.61	0.62 0.73	0.73 0.85	0.84 0.97	0.95 1.07
RN	Q	t_{PHL}	0.63	0.74	0.85	0.96	1.06
RN	QN	t_{PLH}	0.27	0.38	0.48	0.59	0.69
SN	Q	t_{PLH}	0.39	0.49	0.60	0.71	0.81
SN	QN	t_{PHL}	0.74	0.87	0.99	1.11	1.21

(continued on next page)

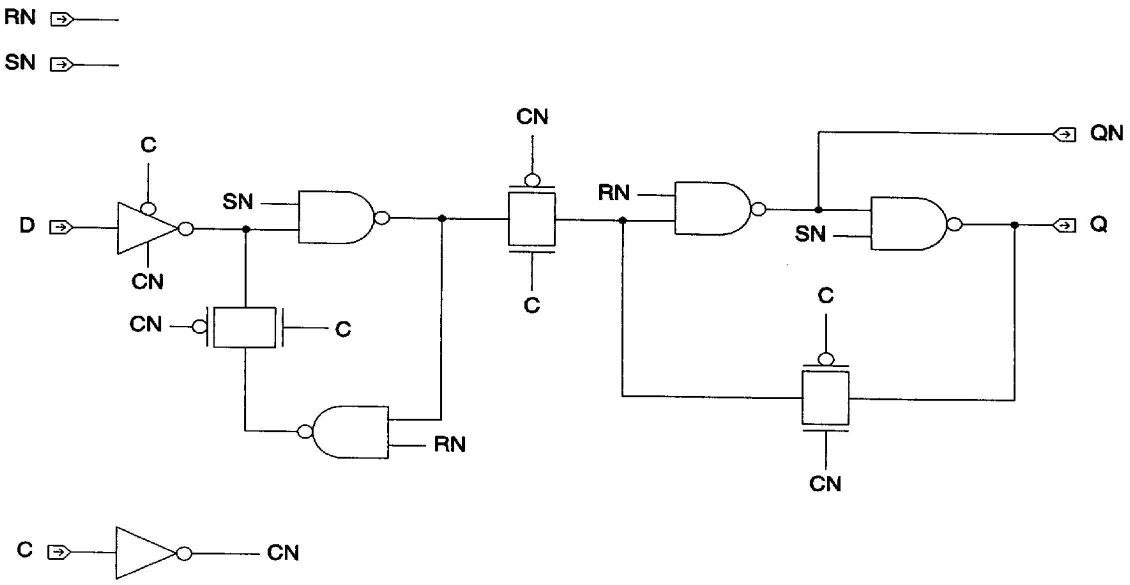
DFAB1

AMI8G 0.8 micron CMOS Gate Array

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	0.84				
Min C Width	Low	t_w	0.67				
Min RN Width	Low	t_w	0.46				
Min SN Width	Low	t_w	0.96				
Min D Setup		t_{su}	0.68				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.19				
Min RN Hold		t_h	0.35				
Min SN Setup		t_{su}	0.25				
Min SN Hold		t_h	0.24				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



DFB01

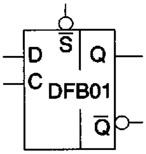
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DFB01 is a static, master-slave, D flip-flop. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock. Transmission gate equivalent of DF101.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.1
SN	2.0

Equivalent Gates:...................7.0

Bolt Syntax:............................Q QN .DFB01 C D SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	8.9	nA
EQL_{pd}	25.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.73 0.64	0.90 0.76	1.11 0.90	1.33 1.04	1.54 1.17
C	QN	t_{PLH} t_{PHL}	1.02 0.94	1.19 1.06	1.41 1.20	1.62 1.33	1.83 1.46
SN	Q	t_{PLH}	0.96	1.13	1.34	1.55	1.76
SN	QN	t_{PHL}	0.57	0.72	0.88	1.02	1.15

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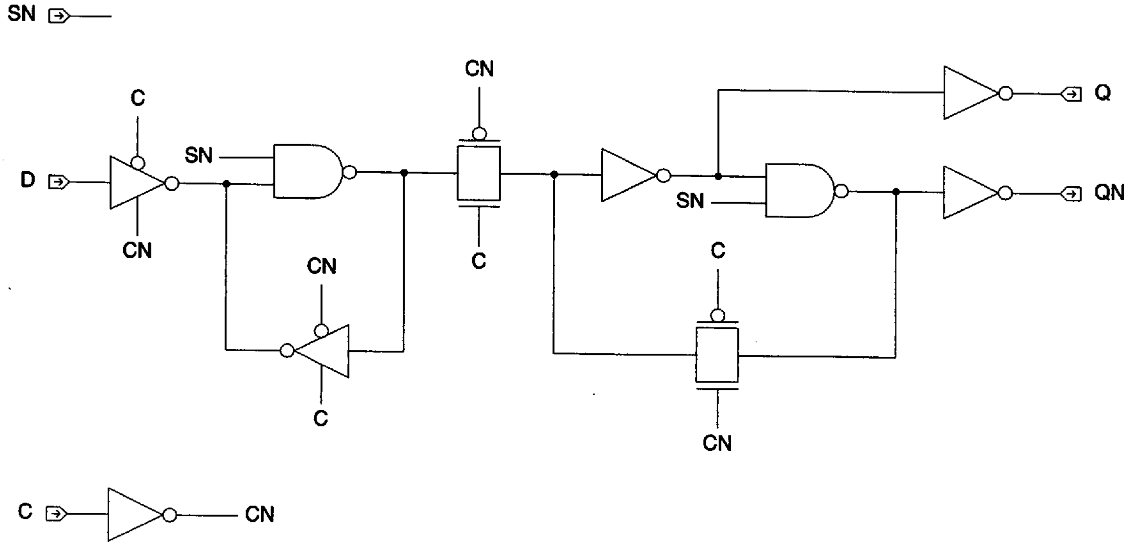
DFB01

AMI8G 0.8 micron CMOS Gate Array

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min C Width	High	t_w	0.67				
Min C Width	Low	t_w	0.69				
Min SN Width		t_w	0.79				
Min D Setup		t_{su}	0.71				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.21				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



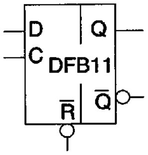
DFB11

AMI8G 0.8 micron CMOS Gate Array

Description:

DFB11 is a static, master-slave, D flip-flop. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock. Transmission gate equivalent of DF111

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.2
RN	2.1

Equivalent Gates:..................8.0

Bolt Syntax:............................Q QN .DFB11 C D RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.9	nA
EQL_{pd}	26.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.91 0.66	1.09 0.80	1.31 0.94	1.52 1.08	1.72 1.21
C	QN	t_{PLH} t_{PHL}	0.87 1.08	1.03 1.20	1.24 1.34	1.44 1.47	1.65 1.59
RN	Q	t_{PHL}	0.44	0.57	0.72	0.85	0.98
RN	QN	t_{PLH}	0.83	1.01	1.22	1.43	1.64

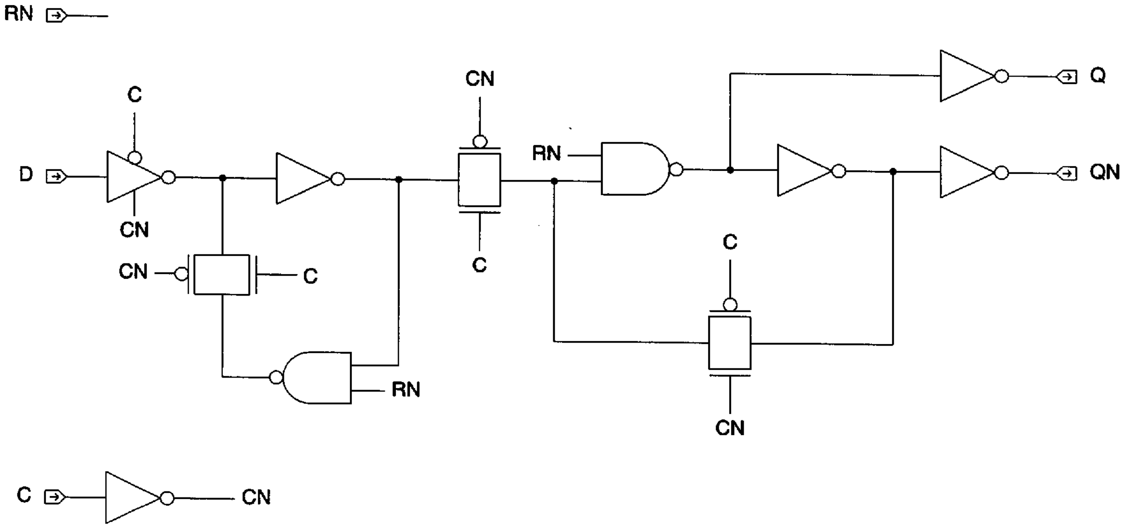
(continued on next page)

DFB11

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
Min C Width	High	t_w	0.84				
Min C Width	Low	t_w	0.66				
Min RN Width		t_w	0.46				
Min D Setup		t_{su}	0.58				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.19				
Min RN Hold		t_h	0.35				

Delay will vary with input conditions. See page 2-15 for interconnect estimates

Logic Schematic



DFB21

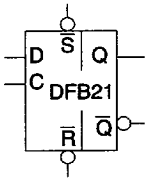
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DFB21 is a static, master-slave, D flip-flop. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock. Transmission gate equivalent of DF121.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

IL = Illegal NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.1
SN	2.0
RN	2.0

Equivalent Gates:...................10.0

Bolt Syntax:............................Q QN .DFB21 C D RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	10.6	nA
EQL_{pd}	27.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.86 0.65	1.03 0.78	1.25 0.92	1.46 1.05	1.67 1.18
C	QN	t_{PLH} t_{PHL}	1.03 1.07	1.20 1.20	1.41 1.34	1.62 1.47	1.83 1.59
SN	Q	t_{PLH}	1.08	1.25	1.46	1.67	1.88
SN	QN	t_{PHL}	0.55	0.70	0.86	1.00	1.13
RN	Q	t_{PHL}	0.43	0.55	0.70	0.83	0.96
RN	QN	t_{PLH}	1.04	1.23	1.45	1.67	1.87

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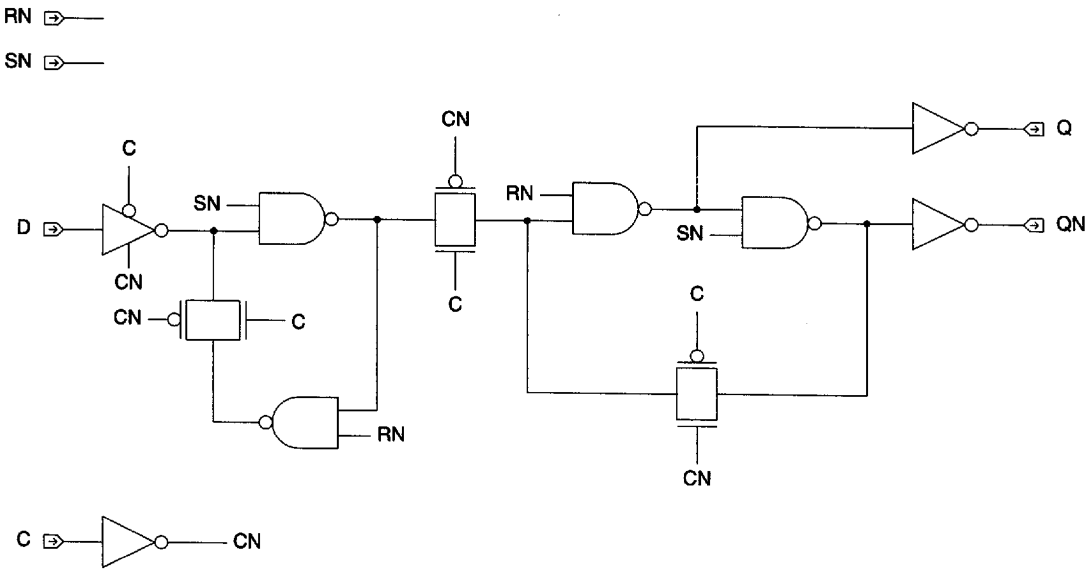
DFB21

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min C Width	High	t_w	0.79				
Min C Width	Low	t_w	0.67				
Min RN Width	Low	t_w	0.46				
Min SN Width	Low	t_w	0.96				
Min D Setup		t_{su}	0.68				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.19				
Min RN Hold		t_h	0.35				
Min SN Setup		t_{su}	0.25				
Min SN Hold		t_h	0.24				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



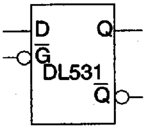
DL531

AMI8G 0.8 micron CMOS Gate Array

Description:

DL531 is a single-phase, unbuffered D latch with active low gate transparency and without SET or RESET.

Logic Symbol



Truth Table

GN	D	Q	QN
L	L	L	H
L	H	H	L
H	X	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	2.1

Equivalent Gates:..................3.0

Bolt Syntax:............................Q QN .DL531 D GN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	11.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	3	5	7	9 (max)
D	Q	t_{PLH} t_{PHL}	0.59 0.71	0.70 0.81	0.81 0.89	0.91 0.97	1.02 1.04
D	QN	t_{PLH} t_{PHL}	0.60 0.34	0.79 0.45	0.98 0.55	1.18 0.65	1.37 0.75
GN	Q	t_{PLH} t_{PHL}	0.75 0.58	0.86 0.67	0.96 0.76	1.07 0.84	1.17 0.91
GN	QN	t_{PLH} t_{PHL}	0.46 0.49	0.66 0.60	0.85 0.70	1.04 0.80	1.23 0.90
Min GN Width	Low	t_w	0.76				
Min D Setup		t_{su}	0.71				
Min D Hold		t_h	0.00				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

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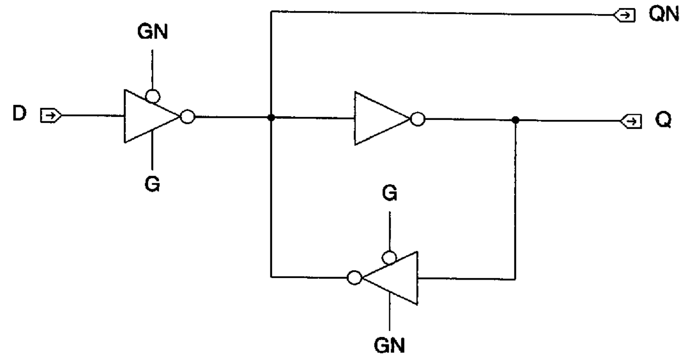
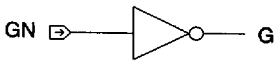
DL531

Logic Schematic





DL541

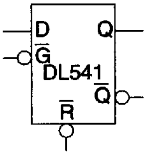
AMI
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DL541 is a single-phase, unbuffered D latch with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q	QN
H	L	L	L	H
H	H	L	H	L
H	X	H	NC	NC
L	X	X	L	H

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	2.1
RN	1.0

Equivalent Gates:....................5.0

Bolt Syntax:.............................Q QN .DL541 D GN RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	16.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
D	Q	t_{PLH} t_{PHL}	0.88 0.79	1.07 0.88	1.26 0.96	1.45 1.04	1.64 1.12
D	QN	t_{PLH} t_{PHL}	0.95 0.93	1.05 1.03	1.16 1.12	1.25 1.20	1.35 1.28
GN	Q	t_{PLH} t_{PHL}	1.05 0.66	1.24 0.75	1.43 0.83	1.62 0.91	1.81 0.98
GN	QN	t_{PLH} t_{PHL}	0.82 1.09	0.92 1.20	1.02 1.29	1.12 1.37	1.22 1.44
RN	Q	t_{PHL}	0.44	0.54	0.67	0.80	0.93
RN	QN	t_{PLH}	0.60	0.76	0.96	1.16	1.36

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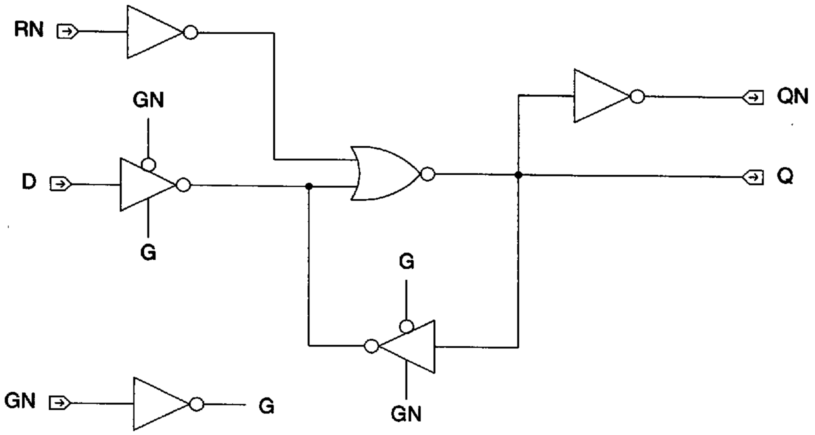
DL541

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	3	5	7	9 (max)
Min GN Width	Low	t_w	0.94				
Min RN Width	Low	t_w	1.00				
Min D Setup		t_{su}	0.88				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.60				
Min RN Hold		t_h	0.52				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



DL551

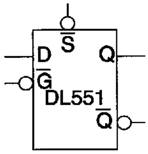
AMI
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DL551 is a single-phase, unbuffered D latch with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q	QN
L	X	X	H	L
H	H	X	NC	NC
H	L	L	L	H
H	L	H	H	L

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	2.1
SN	1.0

Equivalent Gates:...................4.0

Bolt Syntax:............................Q QN .DL551 D GN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	14.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
D	Q	t_{PLH} t_{PHL}	0.70 0.93	0.81 1.04	0.92 1.16	1.02 1.27	1.13 1.37
D	QN	t_{PLH} t_{PHL}	1.12 0.78	1.24 0.87	1.35 0.95	1.45 1.02	1.56 1.09
GN	Q	t_{PLH} t_{PHL}	0.85 0.79	0.96 0.91	1.07 1.02	1.17 1.13	1.28 1.24
GN	QN	t_{PLH} t_{PHL}	0.98 0.93	1.10 1.02	1.21 1.10	1.32 1.17	1.43 1.24
SN	Q	t_{PLH}	0.37	0.47	0.58	0.68	0.79
SN	QN	t_{PHL}	0.46	0.55	0.63	0.70	0.77

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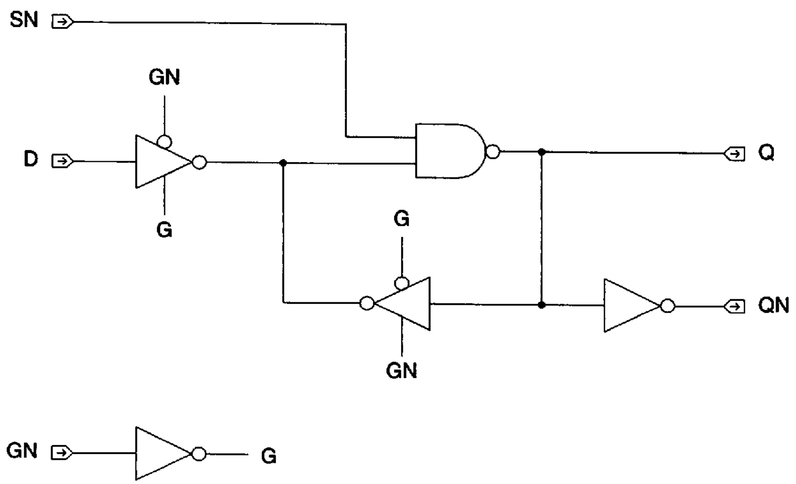
DL551

AMI8G 0.8 micron CMOS Gate Array

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min GN Width	Low	t_w	0.79				
Min SN Width	Low	t_w	0.64				
Min D Setup		t_{su}	0.93				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



DL561

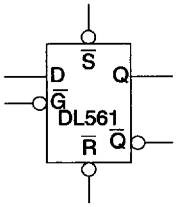
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DL561 is a single-phase, unbuffered D latch with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	X	H	NC	NC
H	H	L	L	L	H
H	H	H	L	H	L

NC = No Change IL = Illegal

Pin Loading

	Equivalent Load
D	1.0
GN	2.1
SN	1.0
RN	1.0

Equivalent Gates:..................5.0

Bolt Syntax:...........................Q QN .DL561 D GN RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	6.2	nA
EQL_{pd}	16.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	3	5	7	9 (max)
D	Q	t_{PLH} t_{PHL}	0.91 0.97	1.03 1.09	1.15 1.21	1.26 1.32	1.36 1.43
D	QN	t_{PLH} t_{PHL}	1.15 0.99	1.27 1.08	1.37 1.15	1.48 1.22	1.58 1.29
GN	Q	t_{PLH} t_{PHL}	1.02 0.83	1.14 0.95	1.26 1.07	1.37 1.18	1.48 1.29
GN	QN	t_{PLH} t_{PHL}	1.01 1.10	1.13 1.19	1.24 1.26	1.34 1.34	1.45 1.40
SN	Q	t_{PLH}	0.35	0.46	0.56	0.66	0.77
SN	QN	t_{PHL}	0.44	0.53	0.60	0.67	0.74
RN	Q	t_{PHL}	0.82	0.94	1.05	1.16	1.26
RN	QN	t_{PLH}	0.99	1.11	1.22	1.32	1.43

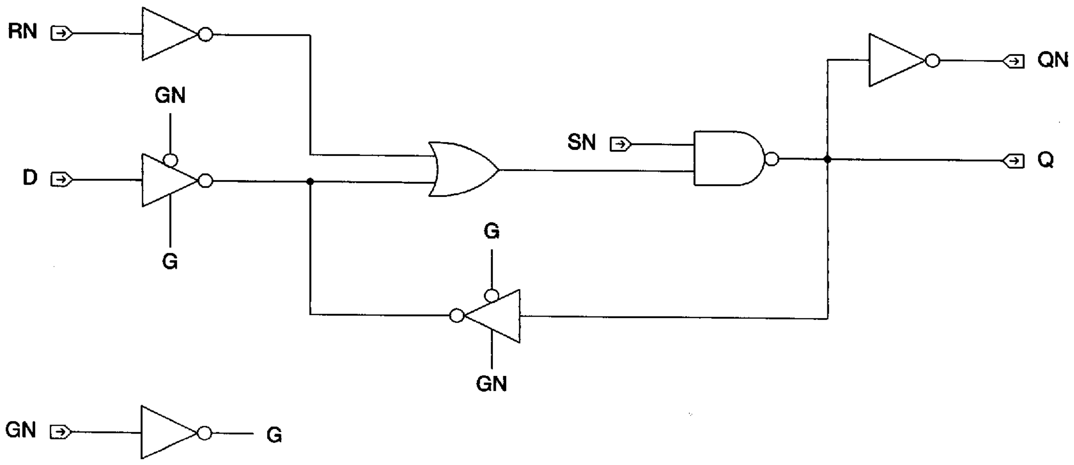
(continued on next page)

DL561

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min GN Width	Low	t_w	0.95				
Min RN Width	Low	t_w	0.40				
Min SN Width	Low	t_w	0.80				
Min D Setup		t_{su}	0.97				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.25				
Min SN Hold		t_h	0.33				
Min RN Setup		t_{su}	0.91				
Min RN Hold		t_h	0.20				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



DL641

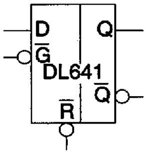
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DL641 is a single-phase, buffered D latch with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q	QN
H	L	L	L	H
H	H	L	H	L
H	X	H	NC	NC
L	X	X	L	H

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	2.0
RN	1.0

Equivalent Gates:....................6.0

Bolt Syntax:............................Q QN .DL641 D GN RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	21.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
D	Q	t_{PLH} t_{PHL}	1.26 1.15	1.42 1.26	1.62 1.39	1.82 1.52	2.02 1.65
D	QN	t_{PLH} t_{PHL}	1.00 1.05	1.17 1.22	1.38 1.41	1.59 1.56	1.79 1.71
GN	Q	t_{PLH} t_{PHL}	1.42 1.02	1.57 1.13	1.77 1.26	1.97 1.39	2.17 1.51
GN	QN	t_{PLH} t_{PHL}	0.87 1.20	1.04 1.37	1.25 1.56	1.46 1.72	1.66 1.86
RN	Q	t_{PHL}	0.79	0.91	1.04	1.16	1.29
RN	QN	t_{PLH}	0.65	0.82	1.03	1.24	1.44

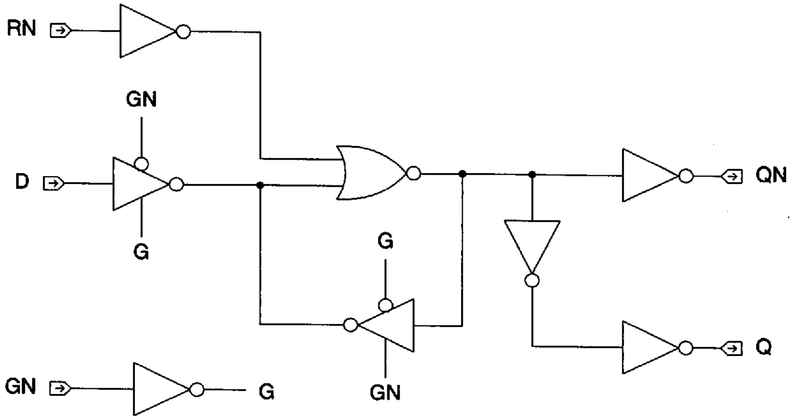
(continued on next page)

DL641

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
Min GN Width	High	t_w	0.30				
Min GN Width	Low	t_w	1.05				
Min RN Width	Low	t_w	0.97				
Min D Setup		t_{su}	0.91				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.73				
Min RN Hold		t_h	0.50				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



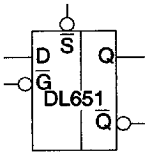
DL651

AMI8G 0.8 micron CMOS Gate Array

Description:

DL651 is a single-phase, buffered D latch with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q	QN
L	X	X	H	L
H	H	X	NC	NC
H	L	L	L	H
H	L	H	H	L

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	2.1
SN	1.0

Equivalent Gates:....................6.0

Bolt Syntax:............................Q QN .DL651 D GN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	18.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
D	Q	t_{PLH} t_{PHL}	1.02 1.31	1.18 1.42	1.39 1.55	1.59 1.68	1.80 1.81
D	QN	t_{PLH} t_{PHL}	1.16 0.83	1.34 0.97	1.56 1.12	1.77 1.26	1.98 1.39
GN	Q	t_{PLH} t_{PHL}	1.18 1.18	1.34 1.30	1.55 1.43	1.75 1.55	1.96 1.68
GN	QN	t_{PLH} t_{PHL}	1.03 0.99	1.21 1.13	1.43 1.28	1.64 1.42	1.85 1.55
SN	Q	t_{PLH}	0.70	0.86	1.07	1.27	1.48
SN	QN	t_{PHL}	0.51	0.65	0.81	0.94	1.07

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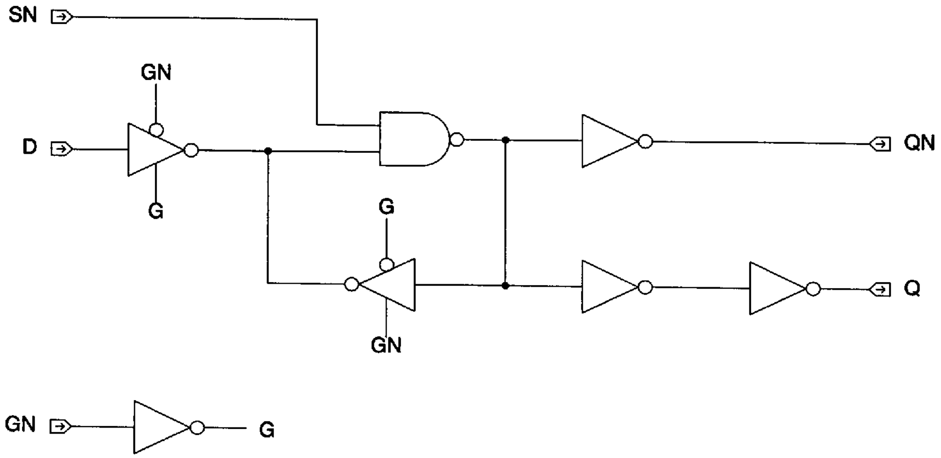
DL651

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min GN Width	High	t_w	0.27				
Min GN Width	Low	t_w	0.84				
Min SN Width	Low	t_w	0.69				
Min D Setup		t_{su}	0.88				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.32				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



DL661

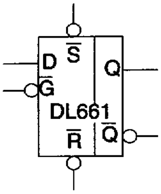
AMI
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DL661 is a single-phase, buffered D latch with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	X	H	NC	NC
H	H	L	L	L	H
H	H	H	L	H	L

IL = Illegal NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	2.0
SN	1.0
RN	1.0

Equivalent Gates:..................6.0

Bolt Syntax:............................Q QN .DL661 D GN RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.0	nA
EQL_{pd}	20.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

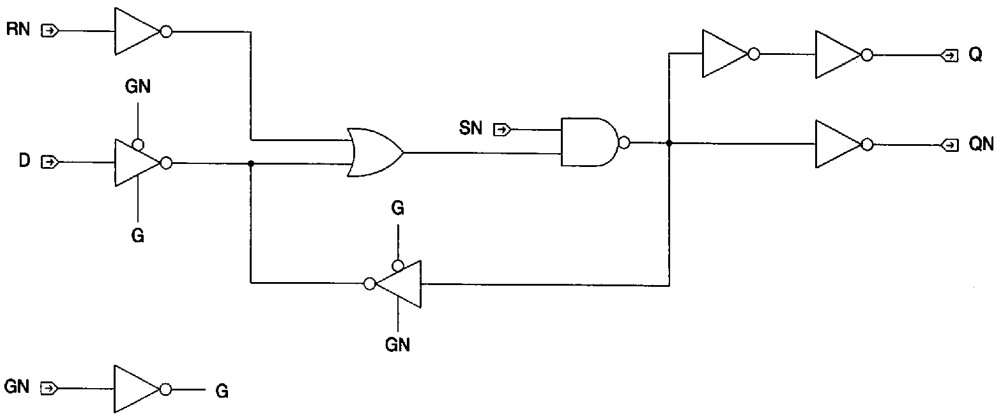
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
D	Q	t_{PLH} t_{PHL}	1.26 1.39	1.41 1.51	1.62 1.64	1.83 1.77	2.03 1.89
D	QN	t_{PLH} t_{PHL}	1.24 1.06	1.43 1.21	1.65 1.36	1.86 1.50	2.07 1.63
GN	Q	t_{PLH} t_{PHL}	1.37 1.26	1.52 1.37	1.73 1.50	1.94 1.63	2.14 1.76
GN	QN	t_{PLH} t_{PHL}	1.11 1.17	1.29 1.32	1.51 1.47	1.72 1.61	1.93 1.74
SN	Q	t_{PLH}	0.70	0.85	1.06	1.27	1.47
SN	QN	t_{PHL}	0.50	0.65	0.80	0.94	1.07
RN	Q	t_{PHL}	1.23	1.35	1.48	1.61	1.73
RN	QN	t_{PLH}	1.08	1.27	1.49	1.70	1.91

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
Min GN Width	High	t_w	0.28				
Min GN Width	Low	t_w	1.03				
Min RN Width	Low	t_w	0.60				
Min SN Width	Low	t_w	0.87				
Min D Setup		t_{su}	0.97				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.31				
Min SN Hold		t_h	0.33				
Min RN Setup		t_{su}	0.98				
Min RN Hold		t_h	0.19				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



DLZ01

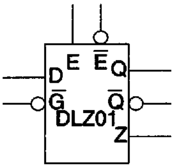
AMI
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DLZ01 is a single-phase, unbuffered D latch with active low gate transparency and with a dual-enable tri-state output.

Logic Symbol



Truth Table

D	GN	E	EN	Q	QN	Z
L	L	H	X	L	H	L
H	L	X	L	H	L	H
L	L	L	X	L	H	Z
H	L	X	H	H	L	Z
X	H	H	L	NC	NC	NC
X	H	L	H	NC	NC	Z

Z = High Impedance NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	2.1
E	0.5
EN	0.6
Z	1.3

Equivalent Gates:....................4.0

Bolt Syntax:............................Q QN Z .DLZ01 D E EN GN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.4	nA
EQL_{pd}	14.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
D	Q	t_{PLH} t_{PHL}	0.68 0.84	0.80 0.95	0.91 1.04	1.01 1.13	1.12 1.21
D	QN	t_{PLH} t_{PHL}	0.72 0.40	0.91 0.51	1.11 0.61	1.30 0.71	1.49 0.81
D	Z	t_{PLH} t_{PHL}	0.79 0.86	0.99 0.99	1.18 1.11	1.37 1.22	1.56 1.32
GN	Q	t_{PLH} t_{PHL}	0.84 0.71	0.95 0.81	1.06 0.91	1.17 0.99	1.27 1.08
GN	QN	t_{PLH} t_{PHL}	0.58 0.55	0.78 0.65	0.97 0.75	1.17 0.85	1.36 0.95
GN	Z	t_{PLH} t_{PHL}	0.94 0.73	1.14 0.86	1.33 0.97	1.52 1.08	1.71 1.19

(continued on next page)

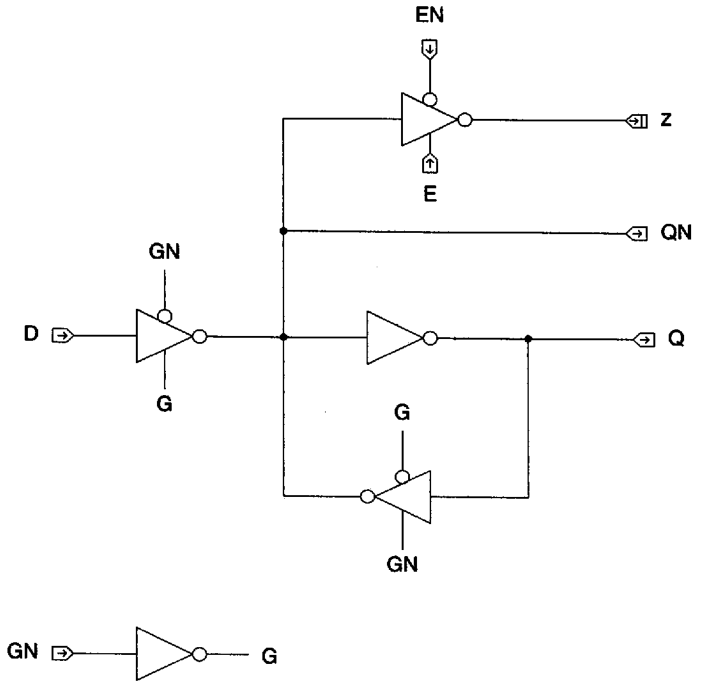
DLZ01

AMI8G 0.8 micron CMOS Gate Array

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	3	5	7	9 (max)
E	Z	t_{PLZ} t_{PZL}	0.09 0.20	0.31	0.41	0.52	0.62
EN	Z	t_{PHZ} t_{PZH}	0.11 0.32	0.51	0.70	0.89	1.08
Min GN Width	Low	t_w	0.85				
Min D Setup		t_{su}	0.84				
Min D Hold		t_h	0.00				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



DLZ11

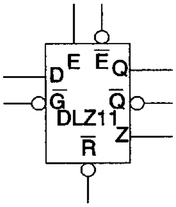
AMI
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

DLZ11 is a single-phase, unbuffered D latch with active low gate transparency and with a dual-enable tri-state output. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	E	EN	Q	QN	Z
H	L	L	H	X	L	H	L
H	H	L	X	L	H	L	H
H	L	L	L	X	L	H	Z
H	H	L	X	H	H	L	Z
H	X	H	H	L	NC	NC	NC
H	X	H	L	H	NC	NC	Z
L	X	X	H	X	L	H	L
L	X	X	L	X	L	H	Z

Z = High Impedance NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	2.0
RN	1.0
E	0.4
EN	0.6
Z	1.3

Equivalent Gates:....................5.0

Bolt Syntax:.............................Q QN Z .DLZ11 D E EN GN RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	17.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	3	5	7	9 (max)
D	Q	t_{PLH} t_{PHL}	0.95 0.90	1.07 1.01	1.19 1.10	1.30 1.19	1.41 1.27
D	QN	t_{PLH} t_{PHL}	0.78 0.60	0.97 0.74	1.16 0.88	1.35 1.02	1.54 1.16
GN	Q	t_{PLH} t_{PHL}	1.05 0.76	1.18 0.96	1.30 0.96	1.41 1.05	1.52 1.13
GN	QN	t_{PLH} t_{PHL}	0.63 0.70	0.83 0.84	1.02 0.98	1.21 1.12	1.41 1.26
RN	Q	t_{PHL}	0.71	0.81	0.90	0.98	1.06
RN	QN	t_{PLH}	0.53	0.65	0.76	0.87	0.97

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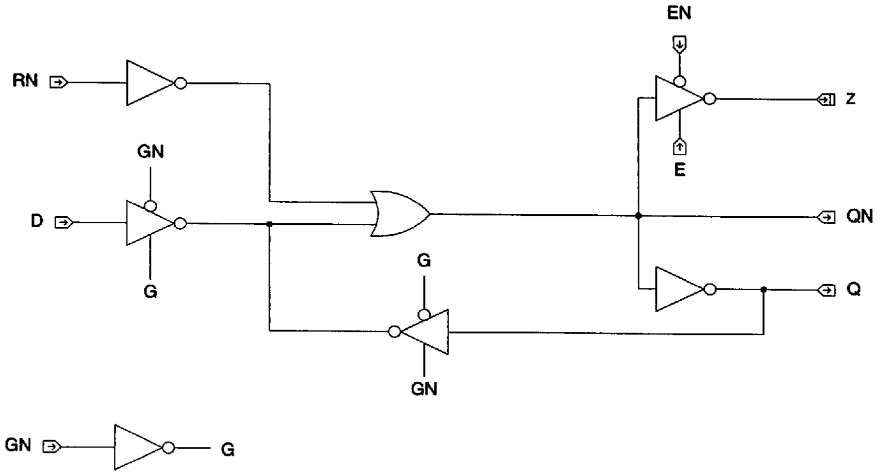
DLZ11

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	3	5	7	9 (max)
RN	Z	t_{PHL} t_{PLH}	0.72 1.10	0.84 1.30	0.95 1.49	1.06 1.68	1.16 1.87
D	Z	t_{PLH} t_{PHL}	1.04 0.91	1.24 1.05	1.43 1.17	1.62 1.28	1.81 1.38
GN	Z	t_{PLH} t_{PHL}	1.15 0.78	1.34 0.91	1.54 1.03	1.73 1.14	1.92 1.24
E	Z	t_{PLZ} t_{PZL}	0.09 0.20	0.31	0.41	0.52	0.62
EN	Z	t_{PHZ} t_{PZH}	0.11 0.32	0.52	0.71	0.90	1.09
Min GN Width	Low	t_w	1.08				
Min RN Width	Low	t_w	0.70				
Min D Setup		t_{su}	0.95				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.93				
Min RN Hold		t_h	0.20				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



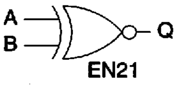
EN21

AMI8G 0.8 micron CMOS Gate Array

Description:

EN21 is a 2-input gate which performs the logical exclusive NOR (XNOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	H

Pin Loading

	Equivalent Load
A	2.0
B	2.0

Equivalent Gates:..................3.0

Bolt Syntax:............................Q .EN21 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	7.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

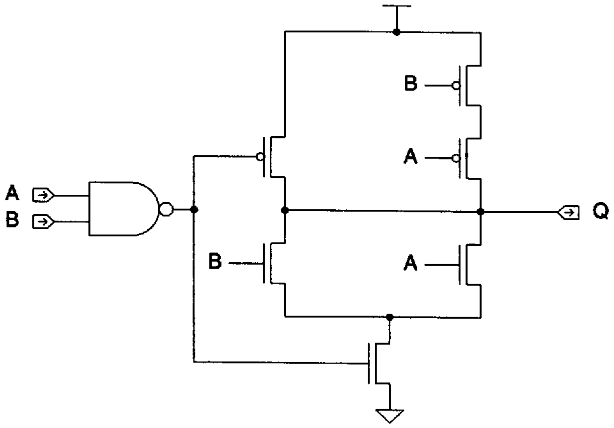
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.51 0.48	0.62 0.58	0.77 0.69	0.96 0.79	1.16 0.89

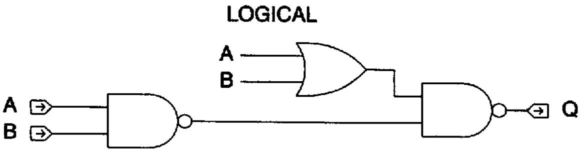
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

(continued on next page)

EN21

Logic Schematic





E021

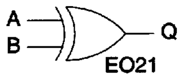
AMI AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

EO21 is a 2-input gate which performs the logical exclusive OR (XOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	L

Pin Loading

	Equivalent Load
A	2.0
B	2.1

Equivalent Gates:...................3.0

Bolt Syntax:.............................Q .EO21 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	1.8	nA
EQL_{pd}	8.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

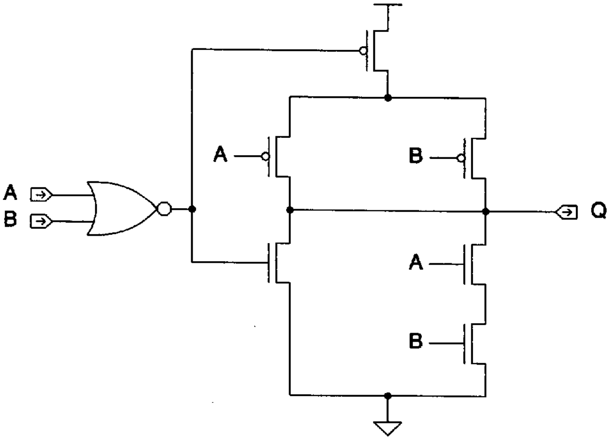
Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.61 0.58	0.80 0.66	0.99 0.74	1.18 0.81	1.37 0.88

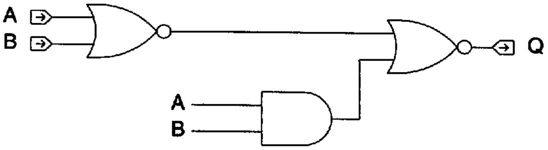
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

(continued on next page)

Logic Schematic



LOGICAL



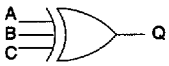
E031

AMI8G 0.8 micron CMOS Gate Array

Description:

EO31 is a 3-input gate which performs the logical exclusive OR (XOR) function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

Pin Loading

	Equivalent Load
A	2.1
B	2.0
C	2.0

Equivalent Gates:....................6.0

Bolt Syntax:.............................Q .EO31 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.6	nA
EQL_{pd}	18.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

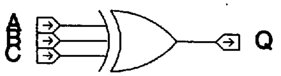
Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	3	5	7	9 (max)
Any Input	Q	t_{PLH} t_{PHL}	1.35 1.26	1.54 1.34	1.72 1.42	1.91 1.49	2.10 1.56

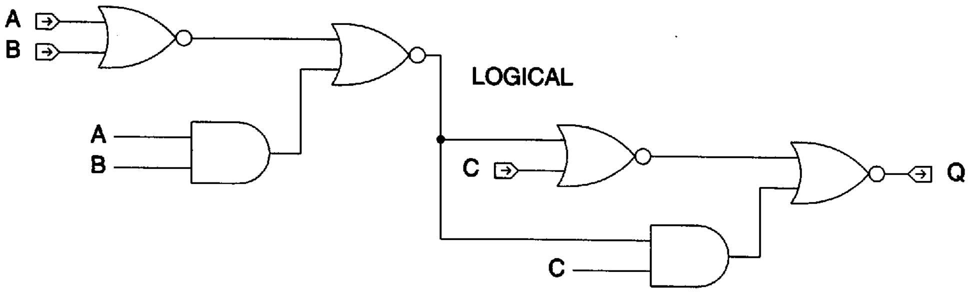
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

(continued on next page)

E031

Logic Schematic





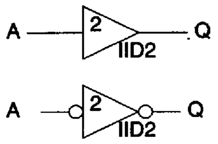
IID2

AMI8G 0.8 micron CMOS Gate Array

Description:

IID2 is a non-inverting clock driver with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	1.0

Equivalent Gates:..................2.0

Bolt Syntax:............................Q .IID2 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.7	nA
EQL_{pd}	4.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	7	14	21	28 (max)
A	Q	t_{PLH}	0.31	0.47	0.65	0.83	1.01
		t_{PHL}	0.34	0.48	0.60	0.71	0.82

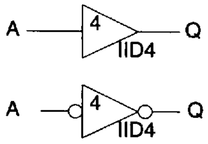
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

IID4

Description:

IID4 is a non-inverting clock driver with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	2.0

Equivalent Gates:...................3.0

Bolt Syntax:............................Q .IID4 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	11.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	14	27	40	53 (max)
A	Q	t_{PLH} t_{PHL}	0.31 0.35	0.48 0.49	0.65 0.60	0.82 0.70	0.99 0.81

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

IID6

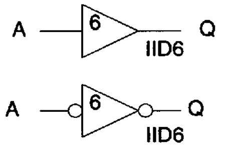
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

IID6 is a non-inverting clock driver with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	2.0

Equivalent Gates:..................4.0

Bolt Syntax:............................Q .IID6 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	16.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	20	39	59	78 (max)
A	Q	t_{PLH} t_{PHL}	0.35 0.41	0.53 0.56	0.70 0.67	0.87 0.78	1.03 0.89

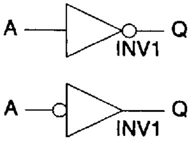
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

INV1

Description:

INV1 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Equivalent Load
A	1.0

Equivalent Gates:...................1.0

Bolt Syntax:............................Q .INV1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.9	nA
EQL_{pd}	1.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
A	Q	t_{PLH} t_{PHL}	0.18 0.12	0.34 0.23	0.55 0.36	0.75 0.49	0.96 0.61

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

INV2

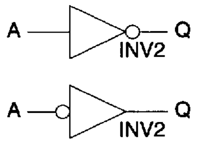
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

INV2 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Equivalent Load
A	2.1

Equivalent Gates:...................1.0

Bolt Syntax:............................Q .INV2 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	1.8	nA
EQL_{pd}	2.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

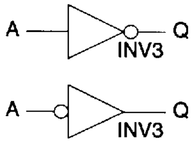
Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	7	14	21	28 (max)
A	Q	t_{PLH} t_{PHL}	0.14 0.10	0.31 0.21	0.49 0.32	0.68 0.43	0.87 0.54

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

INV3 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Equivalent Load
A	3.0

Equivalent Gates:....................2.0

Bolt Syntax:.............................Q .INV3 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.7	nA
EQL_{pd}	2.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
A	Q	t_{PLH} t_{PHL}	0.12 0.08	0.30 0.21	0.48 0.32	0.65 0.42	0.82 0.52

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

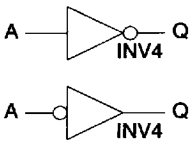
INV4

AMI8G 0.8 micron CMOS Gate Array

Description:

INV4 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Equivalent Load
A	4.1

Equivalent Gates:...................2.0

Bolt Syntax:............................Q .INV4 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	3.5	nA
EQL_{pd}	2.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	14	27	40	53 (max)
A	Q	t_{PLH} t_{PHL}	0.11 0.07	0.29 0.20	0.46 0.30	0.62 0.40	0.79 0.50

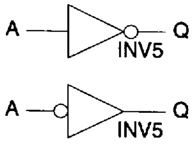
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

INV5

Description:

INV5 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Equivalent Load
A	5.1

Equivalent Gates:....................3.0

Bolt Syntax:............................Q .INV5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	4.4	nA
EQL_{pd}	4.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	17	33	50	66 (max)
A	Q	t_{PLH}	0.11	0.29	0.45	0.63	0.79
		t_{PHL}	0.07	0.20	0.30	0.40	0.50

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

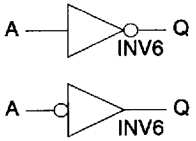
INV6

AMI8G 0.8 micron CMOS Gate Array

Description:

INV6 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Equivalent Load
A	6.1

Equivalent Gates:....................3.0

Bolt Syntax:............................Q .INV6 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	5.3	nA
EQL_{pd}	4.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	20	39	59	78 (max)
A	Q	t_{PLH} t_{PHL}	0.10 0.06	0.28 0.19	0.44 0.29	0.61 0.39	0.77 0.49

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

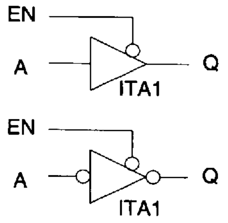
AMI
AMERICAN MICROSYSTEMS, INC.

ITA1

Description:

ITA1 is a non-inverting internal tri-state buffer with active low enable.

Logic Symbol



Truth Table

EN	A	Q
H	X	Z
L	L	L
L	H	H

Z = High Impedance

Pin Loading

	Equivalent Load
A	1.0
EN	1.6
Q	1.3

Equivalent Gates:...................2.0

Bolt Syntax:............................Q .ITA1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.7	nA
EQL_{pd}	6.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	3	5	7	9 (max)
A	Q	t_{PLH}	0.53	0.73	0.93	1.12	1.31
		t_{PHL}	0.43	0.54	0.65	0.75	0.86
EN	Q	t_{HZ}	0.11				
		t_{LZ}	0.17				
		t_{ZH}	0.25	0.44	0.63	0.83	1.02
		t_{ZL}	0.29	0.40	0.51	0.61	0.72

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ITA2

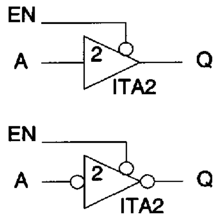
AMI
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

ITA2 is a non-inverting internal tri-state buffer with active low enable.

Logic Symbol



Truth Table

EN	A	Q
H	X	Z
L	L	L
L	H	H

Z = High Impedance

Pin Loading

	Equivalent Load
A	1.0
EN	2.7
Q	4.0

Equivalent Gates:....................4.0

Bolt Syntax:.............................QN .ITA2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.4	nA
EQL_{pd}	15.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	Delay (ns) To	Parameter	Number of Equivalent Loads 1	6	11	17	22 (max)
A	Q	t_{PLH}	0.55	0.72	0.88	1.07	1.23
		t_{PHL}	0.53	0.63	0.73	0.84	0.92
EN	Q	t_{HZ}	0.11				
		t_{LZ}	0.25				
		t_{ZH}	0.18	0.34	0.50	0.68	0.84
		t_{ZL}	0.30	0.41	0.51	0.61	0.70

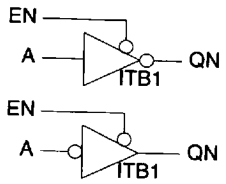
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ITB1

Description:

ITB1 is an inverting internal tri-state buffer with active low enable.

Logic Symbol



Truth Table

EN	A	QN
H	X	Z
L	L	H
L	H	L

Z = High Impedance

Pin Loading

	Equivalent Load
A	1.0
EN	1.6
QN	1.3

Equivalent Gates:....................2.0

Bolt Syntax:.............................QN .ITB1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	4.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
A	QN	t_{LH} t_{PHL}	0.39 0.23	0.59 0.34	0.78 0.44	0.97 0.54	1.16 0.64
EN	QN	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	0.11 0.17 0.25 0.29	 0.43 0.40	 0.63 0.50	 0.82 0.60	 1.01 0.70

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

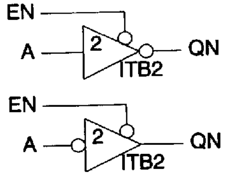
ITB2

AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:
ITB2 is an inverting internal tri-state buffer with active low enable.

Logic Symbol



Truth Table

EN	A	QN
H	X	Z
L	L	H
L	H	L

Z = High Impedance

Pin Loading

	Equivalent Load
A	3.2
EN	2.7
QN	4.0

Equivalent Gates:....................4.0
Bolt Syntax:............................QN .ITB2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	10.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	6	11	17	22 (max)
A	QN	t_{PLH}	0.32	0.49	0.65	0.84	1.00
		t_{PHL}	0.20	0.30	0.39	0.49	0.57
EN	QN	t_{HZ}	0.11				
		t_{LZ}	0.25				
		t_{ZH}	0.18	0.34	0.50	0.69	0.84
		t_{ZL}	0.30	0.40	0.50	0.60	0.69

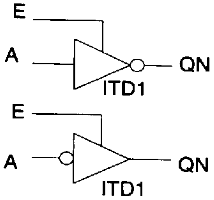
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ITD1

Description:

ITD1 is an inverting internal tri-state buffer with active high enable.

Logic Symbol



Truth Table

E	A	QN
L	X	Z
H	L	H
H	H	L

Z = High Impedance

Pin Loading

	Equivalent Load
A	1.0
E	1.5
QN	1.3

Equivalent Gates:....................2.0

Bolt Syntax:............................QN .ITD1 A E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	4.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	5	7	9 (max)
A	QN	t_{PLH}	0.40	0.59	0.78	0.97	1.16
		t_{PHL}	0.22	0.33	0.43	0.54	0.64
E	QN	t_{HZ}	0.26				
		t_{LZ}	0.09				
		t_{ZH}	0.33	0.52	0.71	0.90	1.09
		t_{ZL}	0.15	0.26	0.36	0.46	0.56

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ITD2

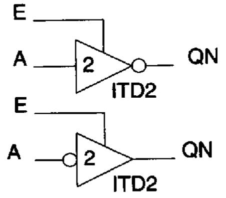
AMI
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

ITD2 is an inverting internal tri-state buffer with active high enable.

Logic Symbol



Truth Table

E	A	QN
L	X	Z
H	L	H
H	H	L

Z = High Impedance

Pin Loading

	Equivalent Load
A	3.2
E	2.5
QN	4.0

Equivalent Gates:....................4.0

Bolt Syntax:............................QN .ITD2 A E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	11.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	6	11	17	22 (max)
A	QN	t_{PLH}	0.34	0.51	0.67	0.86	1.02
		t_{PHL}	0.18	0.28	0.36	0.47	0.55
E	QN	t_{HZ}	0.42				
		t_{LZ}	0.09				
		t_{ZH}	0.32	0.48	0.64	0.83	0.99
		t_{ZL}	0.10	0.21	0.29	0.39	0.48

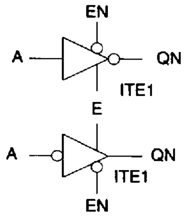
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ITE1

Description:

ITE1 is a two-phase inverting internal tri-state buffer.

Logic Symbol



Truth Table

EN	E	A	QN
H	L	X	Z
L	H	L	H
L	H	H	L
L	L	X	IL
H	H	X	IL

IL = Illegal

Pin Loading

	Equivalent Load
A	1.0
E	0.4
EN	0.5
QN	1.3

Equivalent Gates:....................1.0

Bolt Syntax:.............................QN .ITE1 A E EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	0.9	nA
EQL_{pd}	2.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	3	5	7	9 (max)
A	QN	t_{PLH} t_{PHL}	0.40 0.22	0.59 0.33	0.78 0.43	0.97 0.53	1.16 0.64
EN	QN	t_{HZ} t_{ZH}	0.11 0.33	0.52	0.71	0.90	1.09
E	QN	t_{LZ} t_{ZL}	0.09 0.20	0.31	0.41	0.52	0.62

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ITE2

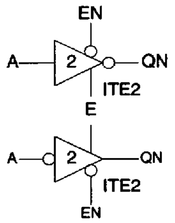
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

ITE2 is a two-phase inverting internal tri-state buffer.

Logic Symbol



Truth Table

EN	E	A	QN
H	L	X	Z
L	H	L	H
L	H	H	L
L	L	X	IL
H	H	X	IL

IL = Illegal

Pin Loading

	Equivalent Load
A	2.1
E	0.9
EN	1.1
QN	2.3

Equivalent Gates:..................2.0

Bolt Syntax:............................QN .ITE2 A E EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	4.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	6	11	17	22 (max)
A	QN	t_{PLH} t_{PHL}	0.34 0.20	0.59 0.33	0.83 0.46	1.11 0.61	1.35 0.74
EN	QN	t_{HZ} t_{ZH}	0.11 0.27	0.51	0.75	1.04	1.27
E	QN	t_{LZ} t_{ZL}	0.09 0.17	0.31	0.44	0.59	0.72

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

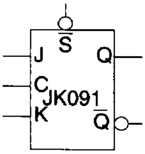
JK091

AMI8G 0.8 micron CMOS Gate Array

Description:

JK091 is a static, master-slave, JK flip-flop. SET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	J	K	C	Q(n+1)	QN(n+1)
L	X	X	X	H	L
H	L	L	↑	NC	NC
H	L	H	↑	L	H
H	H	L	↑	H	L
H	H	H	↑	QN(n)	Q(n)

NC = No Change

Pin Loading

	Equivalent Load
J	1.0
K	1.0
C	3.1
SN	2.0

Equivalent Gates:...................11.0

Bolt Syntax:............................Q QN .JK091 C J K SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	11.5	nA
EQL_{pd}	34.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.70 1.15	0.82 1.29	0.94 1.41	1.05 1.53	1.15 1.65
C	QN	t_{PLH} t_{PHL}	0.88 0.38	1.07 0.49	1.26 0.59	1.45 0.69	1.64 0.79
SN	Q	t_{PLH}	0.28	0.39	0.49	0.60	0.70
SN	QN	t_{PHL}	0.72	0.83	0.93	1.03	1.14

(continued on next page)

JK091

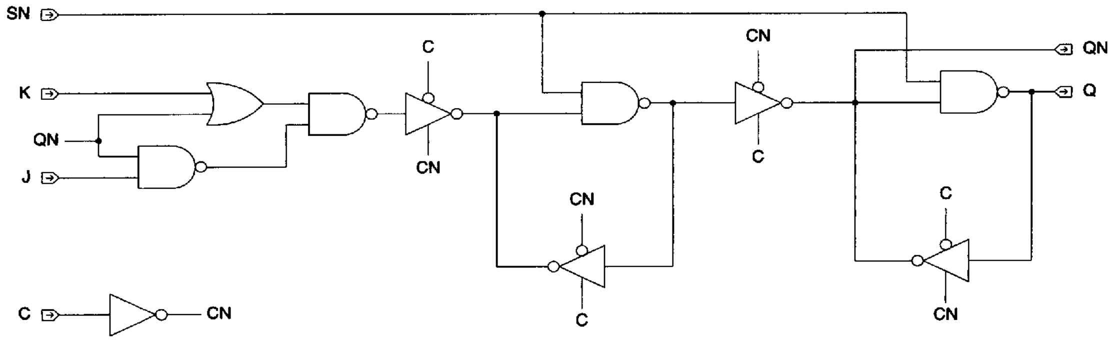
AMI
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	1.17				
Min C Width	Low	t_w	0.86				
Min SN Width	Low	t_w	0.63				
Min J Setup		t_{su}	1.45				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.15				
Min K Hold		t_h	0.00				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



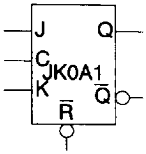
JK0A1

AMI8G 0.8 micron CMOS Gate Array

Description:

JK0A1 is a static, master-slave, JK flip-flop. RESET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	J	K	C	Q(n+1)	QN(n+1)
L	X	X	X	L	H
H	L	L	↑	NC	NC
H	L	H	↑	L	H
H	H	L	↑	H	L
H	H	H	↑	QN(n)	Q(n)

NC = No Change

Pin Loading

	Equivalent Load
J	1.0
K	1.0
C	3.1
RN	1.0

Equivalent Gates:..................11.0

Bolt Syntax:...........................Q QN .JK0A1 C J K RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	10.6	nA
EQL_{pd}	38.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.90 1.04	1.10 1.16	1.30 1.25	1.49 1.34	1.68 1.43
C	QN	t_{PLH} t_{PHL}	0.91 0.38	1.10 0.48	1.30 0.59	1.49 0.69	1.68 0.79
RN	Q	t_{PHL}	0.49	1.16	0.64	0.70	0.77
RN	QN	t_{PLH}	1.31	1.51	1.71	1.88	2.08

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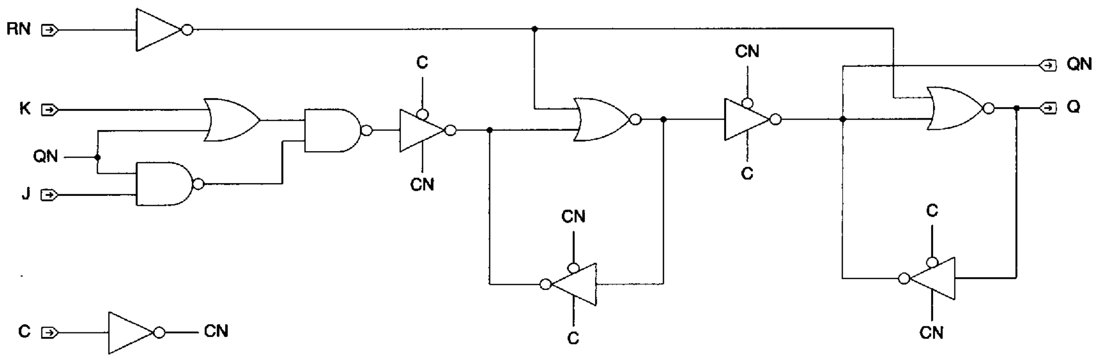
AMI8G 0.8 micron CMOS Gate Array

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	1.06				
Min C Width	Low	t_w	0.62				
Min RN Width	Low	t_w	1.02				
Min J Setup		t_{su}	1.37				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.22				
Min K Hold		t_h	0.00				
Min RN Setup		t_{su}	0.67				
Min RN Hold		t_h	0.56				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic

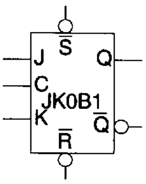


JK0B1

Description:

JK0B1 is a static, master-slave, JK flip-flop. SET and RESET are asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)	QN(n+1)
L	L	X	X	X	IL	IL
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	L	L	↑	NC	NC
H	H	L	H	↑	L	H
H	H	H	L	↑	H	L
H	H	H	H	↑	QN(n)	Q(n)

IL = Illegal NC = No Change

Pin Loading

	Equivalent Load
J	1.0
K	1.0
C	3.1
SN	2.0
RN	2.1

Equivalent Gates:....................12.0

Bolt Syntax:.............................Q QN .JK0B1 C J K RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	12.4	nA
EQL_{pd}	41.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.73 1.18	0.86 1.32	0.97 1.45	1.09 1.57	1.20 1.68
C	QN	t_{PLH} t_{PHL}	0.88 0.39	1.07 0.49	1.26 0.59	1.45 0.69	1.64 0.79
RN	Q	t_{PHL}	1.32	1.46	1.60	1.69	1.81
RN	QN	t_{PLH}	1.00	1.20	1.41	1.58	1.78
SN	Q	t_{PLH}	0.32	0.43	0.54	0.65	0.75
SN	QN	t_{PHL}	0.98	1.13	1.27	1.42	1.56

(continued on next page)

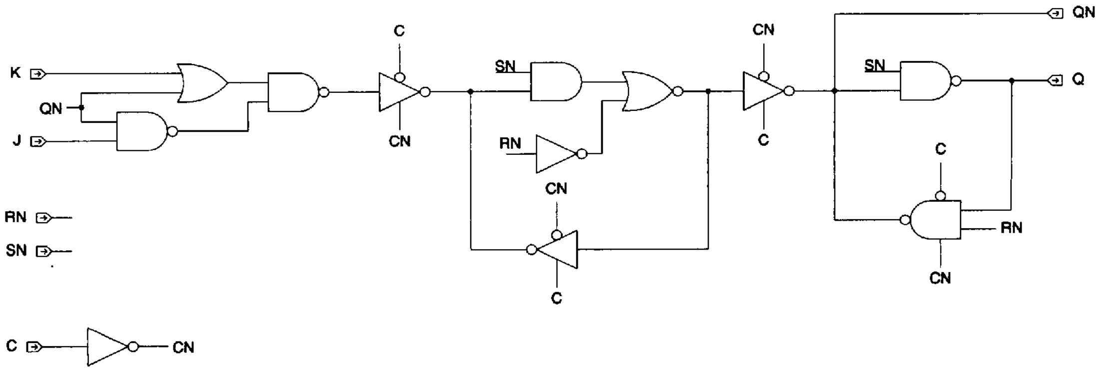
JK0B1

AMI8G 0.8 micron CMOS Gate Array

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	1.21				
Min C Width	Low	t_w	1.05				
Min RN Width	Low	t_w	0.96				
Min SN Width	Low	t_w	0.85				
Min J Setup		t_{su}	1.43				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.24				
Min K Hold		t_h	0.00				
Min RN Setup		t_{su}	0.71				
Min RN Hold		t_h	0.56				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



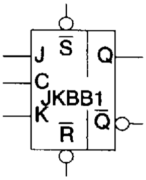
JKBB1

AMI8G 0.8 micron CMOS Gate Array

Description:

JKBB1 is a static, master-slave, JK flip-flop. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)	QN(n+1)
L	L	X	X	X	IL	IL
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	L	L	↑	NC	NC
H	H	L	H	↑	L	H
H	H	H	L	↑	H	L
H	H	H	H	↑	QN(n)	Q(n)

IL = Illegal NC = No Change

Pin Loading

	Equivalent Load
J	1.0
K	1.0
C	3.1
SN	2.0
RN	2.1

Equivalent Gates:..................12.0

Bolt Syntax:............................Q QN .JKBB1 C J K RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	14.2	nA
EQL_{pd}	46.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.71 1.05	0.90 1.24	1.13 1.44	1.34 1.62	1.55 1.78
C	QN	t_{PLH} t_{PHL}	1.63 0.99	1.81 1.12	2.02 1.27	2.23 1.40	2.44 1.53
RN	Q	t_{PHL}	1.16	1.37	1.58	1.72	1.88
RN	QN	t_{PLH}	1.77	1.94	2.16	2.33	2.54
SN	Q	t_{PLH}	1.46	1.67	1.91	2.13	2.34
SN	QN	t_{PHL}	0.48	0.61	0.76	0.89	1.02

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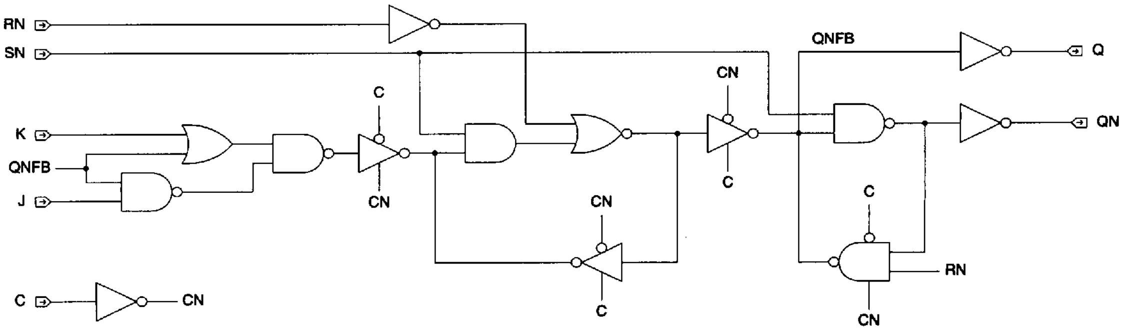
AMI8G 0.8 micron CMOS Gate Array

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min C Width	High	t_w	1.35				
Min C Width	Low	t_w	1.05				
Min RN Width	Low	t_w	1.74				
Min SN Width	Low	t_w	1.07				
Min J Setup		t_{su}	1.42				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.24				
Min K Hold		t_h	0.00				
Min RN Setup		t_{su}	0.71				
Min RN Hold		t_h	0.55				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



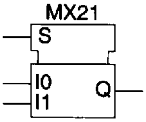
MX21

AMI8G 0.8 micron CMOS Gate Array

Description:

MX21 is a two-to-one digital multiplexer.

Logic Symbol



Truth Table

S	I0	I1	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

Pin Loading

	Equivalent Load
I0	1.0
I1	1.0
S	2.2

Equivalent Gates:....................3.0

Bolt Syntax:.............................Q .MX21 I0 I1 S;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	10.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Ix Input	Q	t_{PLH} t_{PHL}	0.54 0.59	0.72 0.75	0.94 0.93	1.15 1.09	1.36 1.24
S	Q	t_{PLH} t_{PHL}	0.73 0.80	0.91 0.96	1.12 1.12	1.34 1.27	1.55 1.41

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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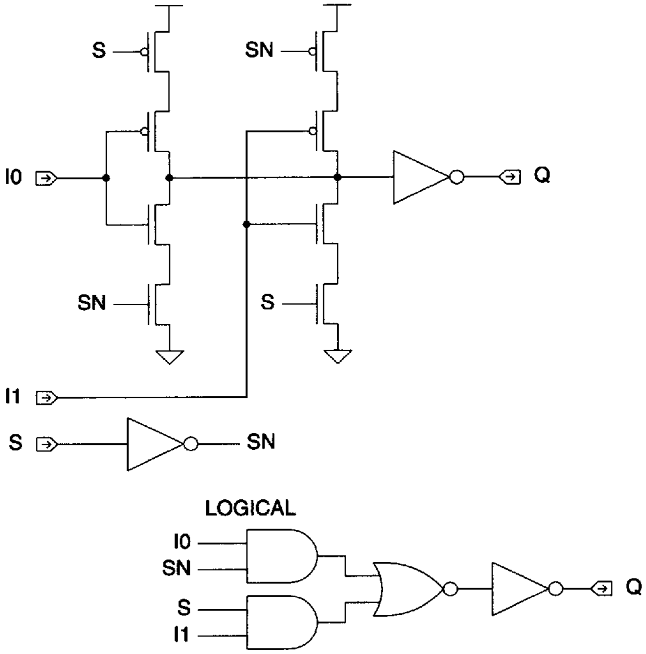
Logic Schematic



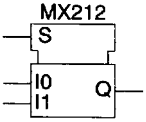
MX212

AMI8G 0.8 micron CMOS Gate Array

Description:

MX212 is a two-to-one digital multiplexer.

Logic Symbol



Truth Table

S	I0	I1	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

Pin Loading

	Equivalent Load
I0	1.0
I1	1.0
S	2.1

Equivalent Gates:....................4.0

Bolt Syntax:............................Q .MX212 I0 I1 S;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	13.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
Any Ix Input	Q	t_{PLH} t_{PHL}	0.64 0.75	0.78 0.90	0.91 1.03	1.04 1.14	1.17 1.25
S	Q	t_{PLH} t_{PHL}	0.82 0.96	0.96 1.10	1.09 1.23	1.22 1.34	1.35 1.44

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

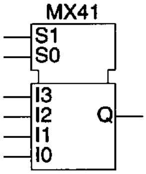
MX41

AMI8G 0.8 micron CMOS Gate Array

Description:

MX41 is a four-to-one digital multiplexer.

Logic Symbol



Truth Table

I0	I1	I2	I3	S1	S0	Q
L	X	X	X	L	L	L
H	X	X	X	L	L	H
X	L	X	X	L	H	L
X	H	X	X	L	H	H
X	X	L	X	H	L	L
X	X	H	X	H	L	H
X	X	X	L	H	H	L
X	X	X	H	H	H	H

Pin Loading

	Equivalent Load
I0	1.0
I1	1.0
I2	1.0
I3	1.0
S0	3.2
S1	3.2

Equivalent Gates:...................8.0

Bolt Syntax:............................Q .MX41 I0 I1 I2 I3 S0 S1;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	6.2	nA
EQL_{pd}	27.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Ix Input	Q	t_{PLH} t_{PHL}	1.13 0.92	1.33 1.20	1.55 1.47	1.77 1.70	1.98 1.90
Any Sx Input	Q	t_{PLH} t_{PHL}	1.16 1.33	1.35 1.58	1.58 1.83	1.79 2.04	2.00 2.23

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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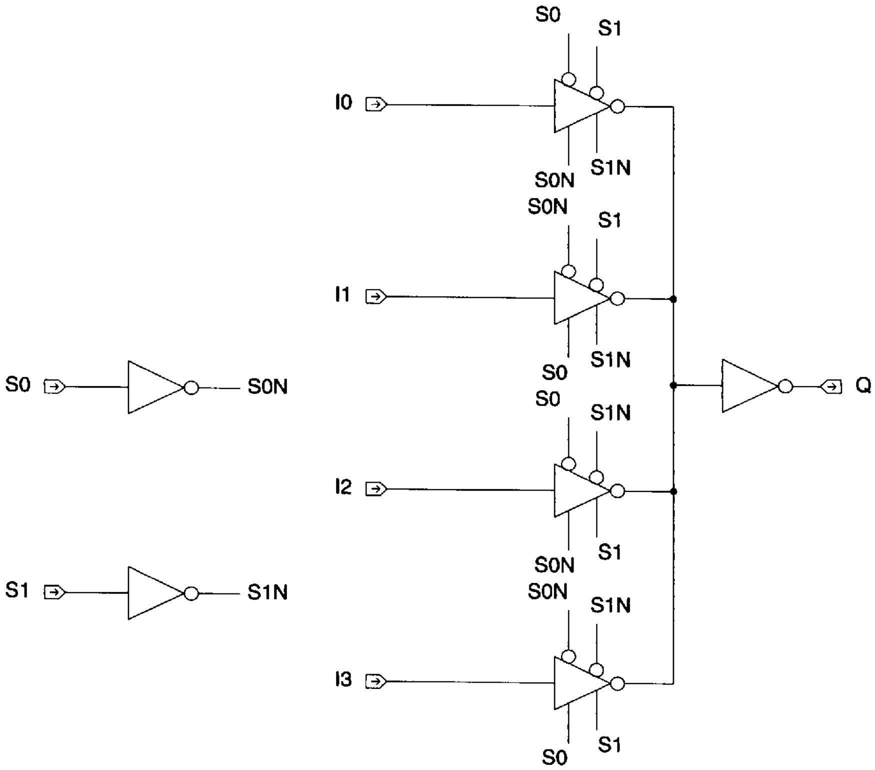
Logic Schematic



MX81

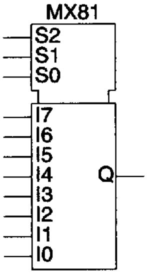
AMI
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

MX81 is an eight-to-one digital multiplexer.

Logic Symbol



Truth Table

S2	S1	S0	Q
L	L	L	I0
L	L	H	I1
L	H	L	I2
L	H	H	I3
H	L	L	I4
H	L	H	I5
H	H	L	I6
H	H	H	I7

Pin Loading

	Equivalent Load
I0	1.0
I1	1.0
I2	1.0
I3	1.0
I4	1.0
I5	1.0
I6	1.0
I7	1.0
S0	5.4
S1	3.1
S2	2.1

Equivalent Gates:...................20.0

Bolt Syntax:............................Q .MX81 I0 I1 I2 I3 I4 I5 I6 I7 S0 S1 S2;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	15.9	nA
EQL_{pd}	58.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
Any Ix Input	Q	t_{PLH} t_{PHL}	1.46 1.41	1.63 1.58	1.84 1.75	2.04 1.90	2.25 2.04
Any Sx Input	Q	t_{PLH} t_{PHL}	1.44 1.48	1.61 1.65	1.82 1.82	2.03 1.97	2.23 2.11

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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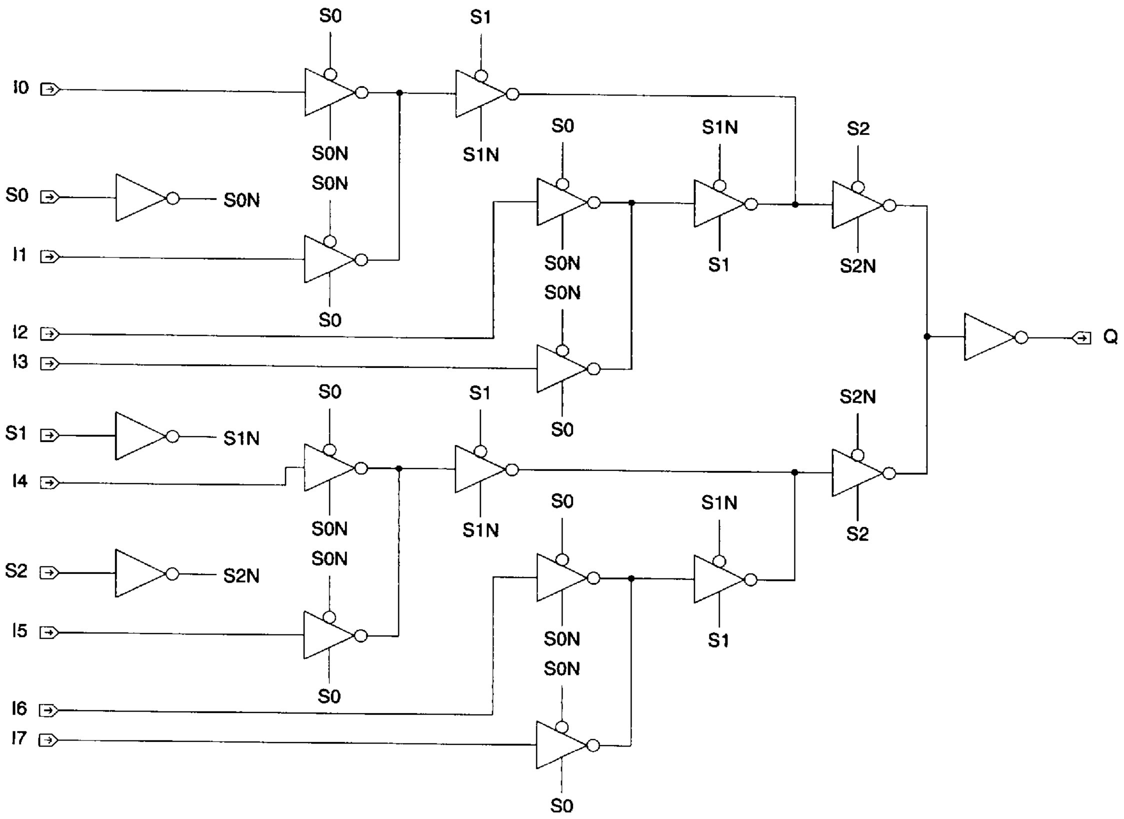
MX81

AMI8G 0.8 micron CMOS Gate Array

Logic Schematic



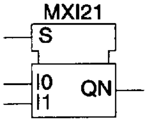
MXI21

AMI8G 0.8 micron CMOS Gate Array

Description:

MXI21 is an inverting two-to-one digital multiplexer.

Logic Symbol



Truth Table

S	I0	I1	QN
L	L	X	H
L	H	X	L
H	X	L	H
H	X	H	L

Pin Loading

	Equivalent Load
I0	1.0
I1	1.0
S	2.1

Equivalent Gates:...................4.0

Bolt Syntax:............................QN .MXI21 I0 I1 S;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	13.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	7	14	21	28 (max)
Any Ix Input	QN	t_{PLH} t_{PHL}	0.82 0.72	0.90 0.79	1.01 0.87	1.11 0.94	1.21 1.01
S	QN	t_{PLH} t_{PHL}	1.02 0.90	1.10 0.97	1.21 1.05	1.31 1.13	1.41 1.19

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

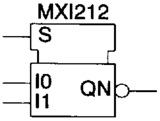
MXI212

AMI8G 0.8 micron CMOS Gate Array

Description:

MXI212 is an inverting two-to-one digital multiplexer.

Logic Symbol



Truth Table

S	I0	I1	QN
L	L	X	H
L	H	X	L
H	X	L	H
H	X	H	L

Pin Loading

	Equivalent Load
I0	1.0
I1	1.0
S	2.1

Equivalent Gates:...................6.0

Bolt Syntax:............................QN .MXI212 I0 I1 S;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	27.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	14	27	40	53 (max)
Any Ix Input	QN	t_{PLH} t_{PHL}	0.94 0.85	1.03 0.94	1.12 1.02	1.21 1.09	1.30 1.16
S	QN	t_{PLH} t_{PHL}	1.13 1.03	1.22 1.12	1.31 1.20	1.40 1.27	1.49 1.34

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

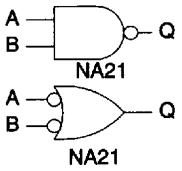
NA21

AMI8G 0.8 micron CMOS Gate Array

Description:

NA21 is a 2-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	H
H	L	H
H	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0

Equivalent Gates: 1.0

Bolt Syntax: ....Q .NA21 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	1.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

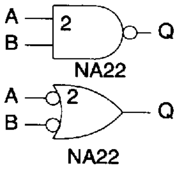
Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	3	5	7	9 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.22 0.19	0.33 0.29	0.43 0.39	0.54 0.49	0.64 0.59

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

NA22 is a 2-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	H
H	L	H
H	H	L

Pin Loading

	Equivalent Load
A	2.0
B	2.0

Equivalent Gates:...................2.0

Bolt Syntax:............................Q .NA22 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	3.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.19 0.16	0.27 0.24	0.38 0.34	0.48 0.45	0.58 0.55

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

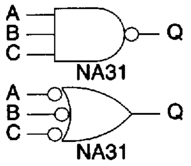
NA31

AMI8G 0.8 micron CMOS Gate Array

Description:

NA31 is a 3-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0

Equivalent Gates:....................2.0

Bolt Syntax:.............................Q .NA31 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.7	nA
EQL_{pd}	3.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	2	4	5	7 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.29 0.33	0.35 0.40	0.46 0.55	0.51 0.62	0.61 0.76

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

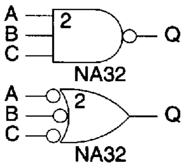
NA32

AMI8G 0.8 micron CMOS Gate Array

Description:

NA32 is a 3-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

Pin Loading

	Equivalent Load
A	2.0
B	2.0
C	2.0

Equivalent Gates:....................3.0

Bolt Syntax:............................Q .NA32 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	5.3	nA
EQL_{pd}	5.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	6	9	11 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.25 0.27	0.30 0.34	0.38 0.45	0.46 0.55	0.52 0.62

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

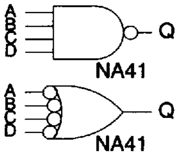
NA41

AMI8G 0.8 micron CMOS Gate Array

Description:

NA41 is a 4-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:...................2.0

Bolt Syntax:............................Q .NA41 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	4.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	2	3	5	6 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.32 0.46	0.38 0.55	0.43 0.64	0.54 0.82	0.60 0.91

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

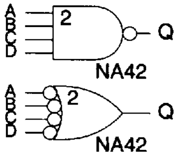
NA42

AMI8G 0.8 micron CMOS Gate Array

Description:

NA42 is a 4-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

Pin Loading

	Equivalent Load
A	2.0
B	2.0
C	2.0
D	2.0

Equivalent Gates:....................4.0

Bolt Syntax:.........................Q .NA42 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	8.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.29 0.41	0.35 0.50	0.40 0.59	0.46 0.68	0.51 0.77

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

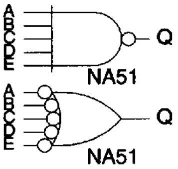
NA51

AMI8G 0.8 micron CMOS Gate Array

Description:

NA51 is a 5-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Equivalent Gates: 3.0

Bolt Syntax: .... Q .NA51 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.4	nA
EQL_{pd}	5.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	Delay (ns) To	Parameter	Number of Equivalent Loads 1	2	3	4	6 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.37 0.68	0.43 0.79	0.49 0.90	0.55 1.01	0.66 1.22

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

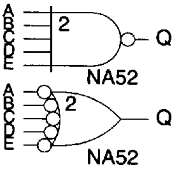
NA52

AMI8G 0.8 micron CMOS Gate Array

Description:

NA52 is a 5-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Equivalent Gates:...................4.0

Bolt Syntax:............................Q .NA52 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	7.1	nA
EQL_{pd}	11.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	2	4	6	8 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.74 1.24	0.77 1.27	0.82 1.32	0.88 1.36	0.93 1.40

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

NA61

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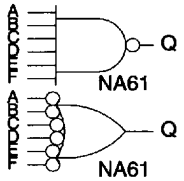
AMI8G 0.8 micron CMOS Gate Array

Description:

NA61 is a 6-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
X	X	X	X	L	X	H
X	X	X	X	X	L	H
H	H	H	H	H	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0

Equivalent Gates:...................5.0

Bolt Syntax:.............................Q .NA61 A B C D E F;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	8.0	nA
EQL_{pd}	17.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.74 1.04	0.82 1.12	0.93 1.22	1.03 1.30	1.13 1.38

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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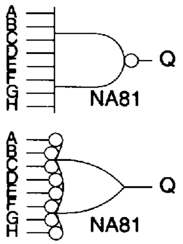
NA81

AMI8G 0.8 micron CMOS Gate Array

Description:

NA81 is an 8-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0
G	1.0
H	1.0

Equivalent Gates:...................6.0

Bolt Syntax:............................Q .NA81 A B C D E F G H;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	9.7	nA
EQL_{pd}	16.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.76 1.15	0.84 1.24	0.95 1.33	1.05 1.42	1.15 1.50

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

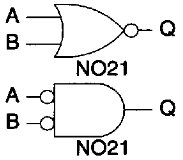
N021

AMI8G 0.8 micron CMOS Gate Array

Description:

NO21 is a 2-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0

Equivalent Gates:...................1.0

Bolt Syntax:............................Q .NO21 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.9	nA
EQL_{pd}	2.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	3	5	7	9 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.32 0.16	0.52 0.23	0.71 0.29	0.91 0.36	1.10 0.42

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

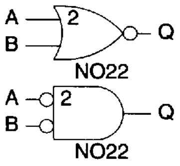
N022

AMI8G 0.8 micron CMOS Gate Array

Description:

NO22 is a 2-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	L

Pin Loading

	Equivalent Load
A	2.0
B	2.0

Equivalent Gates:..................2.0

Bolt Syntax:............................Q .NO22 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	4.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	Delay (ns) To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.27 0.13	0.42 0.19	0.62 0.26	0.81 0.32	1.01 0.39

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

N031

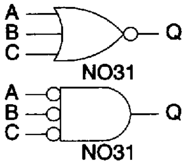
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

NO31 is a 3-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0

Equivalent Gates:..................2.0

Bolt Syntax:............................Q .NO31 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	1.1	nA
EQL_{pd}	4.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	2	4	5	7 (max)
Any Input	Q	t_{PLH}	0.62	0.77	1.07	1.21	1.50
		t_{PHL}	0.18	0.22	0.29	0.33	0.40

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI
AMERICAN MICROSYSTEMS, INC.

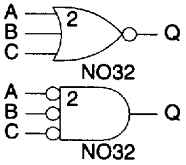
N032

AMI8G 0.8 micron CMOS Gate Array

Description:

NO32 is a 3-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

Pin Loading

	Equivalent Load
A	2.0
B	2.0
C	2.0

Equivalent Gates: 3.0

Bolt Syntax:............................ Q .NO32 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.1	nA
EQL_{pd}	7.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	Delay (ns) To	Parameter	Number of Equivalent Loads 1	3	6	9	11 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.50 0.14	0.65 0.18	0.88 0.24	1.10 0.29	1.24 0.33

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

N041

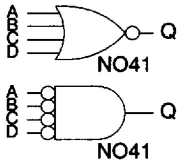
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

NO41 is a 4-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:..................2.0

Bolt Syntax:............................Q .NO41 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.4	nA
EQL_{pd}	5.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	2	3	5	6 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.96 0.19	1.15 0.23	1.35 0.26	1.73 0.34	1.91 0.37

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

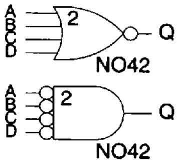
N042

AMI8G 0.8 micron CMOS Gate Array

Description:

NO42 is a 4-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:...................4.0

Bolt Syntax:............................Q .NO42 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	5.3	nA
EQL_{pd}	11.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	3	5	7	9 (max)
Any Input	Q	t_{PLH}	0.81	0.87	0.93	0.99	1.04
		t_{PHL}	0.52	0.57	0.61	0.65	0.69

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

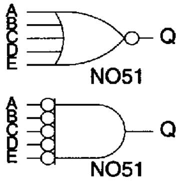
N051

AMI8G 0.8 micron CMOS Gate Array

Description:

NO51 is a 5-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	L	L	H
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Equivalent Gates:....................3.0

Bolt Syntax:.............................Q .NO51 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	8.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	2	3	4	6 (max)
Any Input	Q	t_{PLH} t_{PHL}	1.43 0.20	1.67 0.24	1.91 0.28	2.15 0.31	2.63 0.38

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

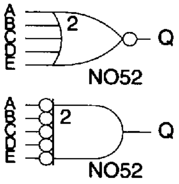
N052

AMI8G 0.8 micron CMOS Gate Array

Description:

NO52 is a 5-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	L	L	H
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Equivalent Gates:....................5.0

Bolt Syntax:............................Q .NO52 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	5.3	nA
EQL_{pd}	14.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	2	4	6	8 (max)
Any Input	Q	t_{PLH} t_{PHL}	1.20 0.58	1.23 0.60	1.29 0.65	1.35 0.69	1.41 0.73

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

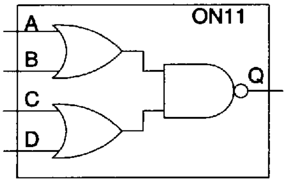
ON11

AMI8G 0.8 micron CMOS Gate Array

Description:

ON11 is an OR-NAND circuit consisting of two 2-input OR gates into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	L	H
All other combinations				L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:...................2.0

Bolt Syntax:............................Q .ON11 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	5.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.58 0.37	0.78 0.49	0.98 0.59	1.17 0.70	1.37 0.81

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

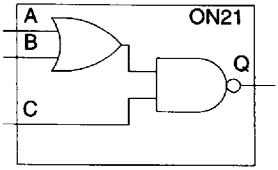
ON21

AMI8G 0.8 micron CMOS Gate Array

Description:

ON21 is an OR-NAND circuit consisting of one 2-input OR gate into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	Q
L	L	X	H
X	X	L	H
All other combinations			L

Pin Loading

	Equivalent Load
A	1.0
B	1.6
C	1.0

Equivalent Gates:...................2.0

Bolt Syntax:............................Q .ON21 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	2.7	nA
EQL_{pd}	4.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.26 0.28	0.40 0.41	0.54 0.54	0.68 0.67	0.82 0.79

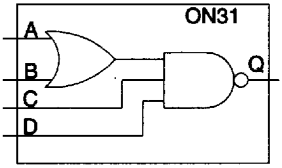
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI8G 0.8 micron CMOS Gate Array

Description:

ON31 is an OR-NAND circuit consisting of a 2-input OR gate and two direct inputs into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	X	H
X	X	X	L	H
All other combinations				L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:....................2.0

Bolt Syntax:.............................Q .ON31 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	2.7	nA
EQL_{pd}	4.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	2	4	5	7 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.40 0.43	0.50 0.51	0.69 0.65	0.79 0.72	0.98 0.86

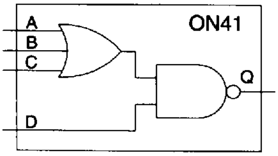
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ON41

Description:

ON41 is an OR-NAND circuit consisting of one 3-input OR gate into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	X	H
X	X	X	L	H
All other combinations				L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:...................3.0

Bolt Syntax:............................Q .ON41 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	3.5	nA
EQL_{pd}	10.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	2	4	5	7 (max)
Any Input	Q	t_{PLH} t_{PHL}	1.05 0.59	1.16 0.69	1.26 0.80	1.37 0.90	1.47 1.00

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ON51

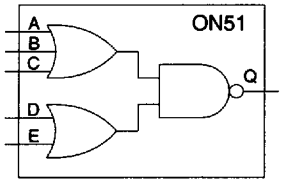
AMI
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

ON51 is an OR-NAND circuit consisting of one 3-input OR gate and one 2-input OR gate into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	X	X	H
X	X	X	L	L	H
All other combinations					L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Equivalent Gates:...................4.0

Bolt Syntax:............................Q .ON51 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	3.5	nA
EQL_{pd}	13.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	1.05 0.66	1.20 0.79	1.41 0.94	1.61 1.07	1.81 1.20

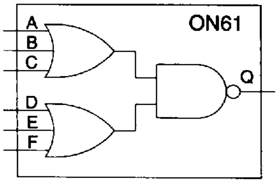
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ON61

Description:

ON61 is an OR-NAND circuit consisting of two 3-input OR gates into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	L	X	X	X	H
X	X	X	L	L	L	H
All other combinations						L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0

Equivalent Gates:....................5.0

Bolt Syntax:..............................Q .ON61 A B C D E F;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.4	nA
EQL_{pd}	17.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	7	14	21	28 (max)
Any Input	Q	t_{PLH} t_{PHL}	1.09 0.73	1.26 0.89	1.43 1.04	1.61 1.16	1.78 1.29

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

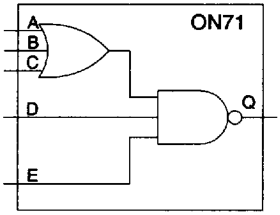
ON71

AMI8G 0.8 micron CMOS Gate Array

Description:

ON71 is an OR-NAND circuit consisting of one 3-input OR gate into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
All other combinations					L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Equivalent Gates: 4.0

Bolt Syntax: .... Q .ON71 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	4.4	nA
EQL_{pd}	11.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	2	4	5	7 (max)
Any Input	Q	t_{PLH} t_{PHL}	1.09 0.68	1.14 0.75	1.25 0.90	1.30 0.97	1.40 1.11

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

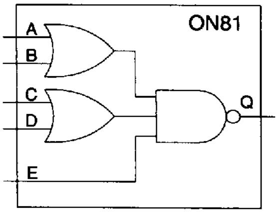
ON81

AMI8G 0.8 micron CMOS Gate Array

Description:

ON81 is an OR-NAND circuit consisting of two 2-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	X	X	X	H
X	X	L	L	X	H
X	X	X	X	L	H
All other combinations					L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Equivalent Gates:...................5.0

Bolt Syntax:............................Q .ON81 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.4	nA
EQL_{pd}	17.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.65 0.87	0.81 0.99	1.02 1.11	1.23 1.21	1.43 1.30

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

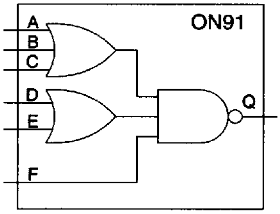
ON91

AMI8G 0.8 micron CMOS Gate Array

Description:

ON91 is an OR-NAND circuit consisting of one 3-input OR gate and one 2-input OR gate into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	L	X	X	X	H
X	X	X	L	L	X	H
X	X	X	X	X	L	H
All other combinations						L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.1
E	1.0
F	1.0

Equivalent Gates:..................6.0

Bolt Syntax:............................Q .ON91 A B C D E F;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	4.4	nA
EQL_{pd}	19.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.65 0.79	0.81 0.91	1.02 1.03	1.23 1.13	1.43 1.22

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

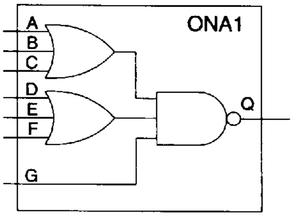
ONA1

AMI8G 0.8 micron CMOS Gate Array

Description:

ONA1 is an OR-NAND circuit consisting of two 3-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	L	L	X	X	X	X	H
X	X	X	L	L	L	X	H
X	X	X	X	X	X	L	H
All other combinations							L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0
G	1.0

Equivalent Gates:....................6.0

Bolt Syntax:.............................Q .ONA1 A B C D E F G;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	21.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	2	4	5	7 (max)
Any Input	Q	t_{PLH} t_{PHL}	1.04 0.85	1.07 0.92	1.13 1.07	1.15 1.14	1.20 1.28

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

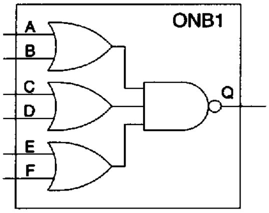
ONB1

AMI8G 0.8 micron CMOS Gate Array

Description:

ONB1 is an OR-NAND circuit consisting of three 2-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	X	X	X	X	H
X	X	L	L	X	X	H
X	X	X	X	L	L	H
All other combinations						L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0

Equivalent Gates:...................6.0

Bolt Syntax:.............................Q .ONB1 A B C D E F;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	8.0	nA
EQL_{pd}	20.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	Delay (ns) To	Parameter	Number of Equivalent Loads 1	2	4	5	7 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.73 0.69	0.79 0.76	0.90 0.90	0.95 0.97	1.05 1.11

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

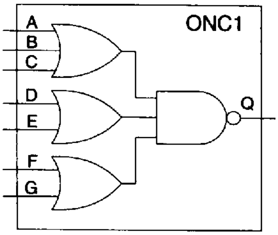
ONC1

AMI8G 0.8 micron CMOS Gate Array

Description:

ONC1 is an OR-NAND circuit consisting of one 3-input OR gate and two 2-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	L	L	X	X	X	X	H
X	X	X	L	L	X	X	H
X	X	X	X	X	L	L	H
All other combinations							L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0
G	1.0

Equivalent Gates:....................6.0

Bolt Syntax:.............................Q .ONC1 A B C D E F G;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	5.3	nA
EQL_{pd}	20.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	7	14	21	28 (max)
Any Input	Q	t_{PLH} t_{PHL}	1.07 1.07	1.24 1.27	1.42 1.44	1.59 1.58	1.77 1.72

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OND1

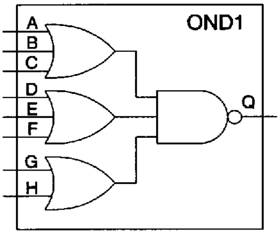
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

OND1 is an OR-NAND circuit consisting of two 3-input OR gates and one 2-input OR gate into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
L	L	L	X	X	X	X	X	H
X	X	X	L	L	L	X	X	H
X	X	X	X	X	X	L	L	H
All other combinations								L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0
G	1.0
H	1.0

Equivalent Gates:..................6.0

Bolt Syntax:.............................Q .OND1 A B C D E F G H;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	4.4	nA
EQL_{pd}	21.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	1.08 0.90	1.24 1.07	1.44 1.24	1.64 1.40	1.85 1.54

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

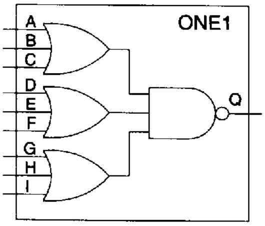
ONE1

AMI8G 0.8 micron CMOS Gate Array

Description:

ONE1 is an OR-NAND circuit consisting of three 3-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Q
L	L	L	X	X	X	X	X	X	H
X	X	X	L	L	L	X	X	X	H
X	X	X	X	X	X	L	L	L	H
All other combinations									L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0
G	1.0
H	1.0
I	1.0

Equivalent Gates:..................7.0

Bolt Syntax:............................Q .ONE1 A B C D E F G H I;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	27.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	7	14	21	28 (max)
Any Input	Q	t_{PLH} t_{PHL}	1.23 1.19	1.39 1.38	1.57 1.55	1.75 1.70	1.93 1.84

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OR21

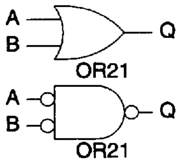
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

OR21 is a 2-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0

Equivalent Gates:....................2.0

Bolt Syntax:.............................Q .OR21 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	1.8	nA
EQL_{pd}	4.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.34 0.49	0.50 0.62	0.71 0.77	0.92 0.91	1.12 1.04

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMERICAN MICROSYSTEMS, INC.

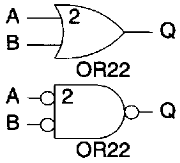
OR22

AMI8G 0.8 micron CMOS Gate Array

Description:

OR22 is a 2-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0

Equivalent Gates:....................2.0

Bolt Syntax:............................Q .OR22 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.7	nA
EQL_{pd}	5.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	7	14	21	28 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.35 0.56	0.51 0.72	0.70 0.87	0.88 1.00	1.05 1.12

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

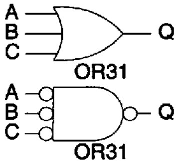
OR31

AMI8G 0.8 micron CMOS Gate Array

Description:

OR31 is a 3-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0

Equivalent Gates:...................2.0

Bolt Syntax:..............................Q .OR31 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	1.8	nA
EQL_{pd}	6.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.39 0.81	0.55 0.98	0.77 1.16	0.98 1.32	1.19 1.47

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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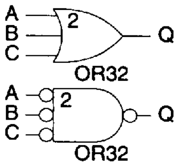
OR32

AMI8G 0.8 micron CMOS Gate Array

Description:

OR32 is a 3-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0

Equivalent Gates:...................3.0

Bolt Syntax:...........................Q .OR32 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.7	nA
EQL_{pd}	9.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	7	14	21	28 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.40 0.95	0.58 1.14	0.76 1.31	0.95 1.46	1.13 1.60

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

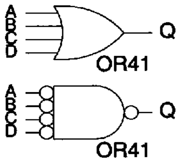
OR41

AMI8G 0.8 micron CMOS Gate Array

Description:

OR41 is a 4-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	L
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:...................3.0

Bolt Syntax:............................Q .OR41 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	3.5	nA
EQL_{pd}	8.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.35 0.56	0.51 0.74	0.72 0.95	0.93 1.16	1.13 1.36

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

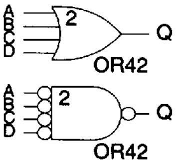
OR42

AMI8G 0.8 micron CMOS Gate Array

Description:

OR42 is a 4-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	L
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:....................4.0

Bolt Syntax:...............................Q .OR42 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	12.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	7	14	21	28 (max)
Any Input	Q	t_{PLH}	0.36	0.53	0.71	0.89	1.06
		t_{PHL}	0.64	0.85	1.05	1.23	1.42

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

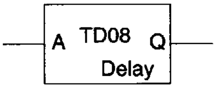
TD08

AMI8G 0.8 micron CMOS Gate Array

Description:

TD08 is a non-inverting time delay.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	1.0

Equivalent Gates:...................11.0

Bolt Syntax:............................Q .TD08 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	6.9	nA
EQL_{pd}	55.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	6	11	17	22 (max)
A	Q	t_{PLH}	10.04	10.25	10.41	10.58	10.72
		t_{PHL}	10.76	11.00	11.20	11.41	11.59

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI
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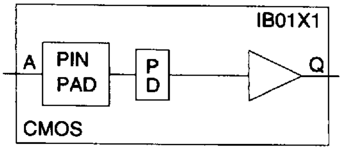
IB01X1

AMI8G 0.8 micron CMOS Gate Array

Description:

IB01X1 is a non-inverting, CMOS-level input buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	187.8

Bolt Syntax:............................Q .IB01X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	50.5	nA
EQL_{pd}	48.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	Delay (ns) To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
A	Q	t_{PLH} t_{PHL}	0.71 0.91	0.89 1.09	1.03 1.23	1.17 1.37	1.31 1.50

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

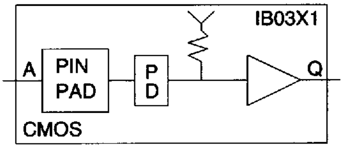
IB03X1

AMI8G 0.8 micron CMOS Gate Array

Description:

IB03X1 is a non-inverting, CMOS-level input buffer pad with pull-up.

Logic Symbol



Truth Table

A	Q
L	L
H	H
UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	187.8

Bolt Syntax:............................Q .IB03X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	51.0	nA
EQL_{pd}	58.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	11	21	31	41 (max)
A	Q	t_{PLH} t_{PHL}	0.71 0.90	0.89 1.09	1.03 1.23	1.17 1.37	1.31 1.50

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

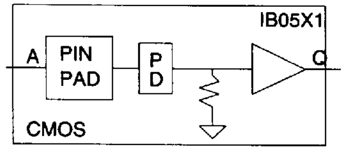
IB05X1

AMI8G 0.8 micron CMOS Gate Array

Description:

IB05X1 is a non-inverting, CMOS-level input buffer pad with pull-down.

Logic Symbol



Truth Table

A	Q
L	L
H	H
UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	187.8

Bolt Syntax:............................Q .IB05X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	50.5	nA
EQL_{pd}	60.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	Delay (ns) To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
A	Q	t_{PLH} t_{PHL}	0.71 0.91	0.89 1.09	1.03 1.23	1.17 1.37	1.31 1.50

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

IB07X1

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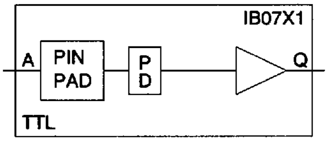
AMI8G 0.8 micron CMOS Gate Array

Description:

IB07X1 is a non-inverting, TTL-level input buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	187.8

Bolt Syntax:............................Q .IB07X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	49.9	nA
EQL_{pd}	49.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	11	21	31	41 (max)
A	Q	t_{PLH} t_{PHL}	0.83 1.18	1.01 1.40	1.01 1.40	1.28 1.73	1.42 1.88

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

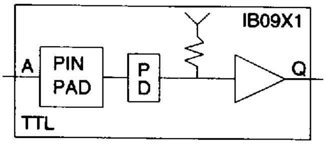
IB09X1

AMI8G 0.8 micron CMOS Gate Array

Description:

IB09X1 is a non-inverting, TTL-level input buffer pad with pull-up.

Logic Symbol



Truth Table

A	Q
L	L
H	H
UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	187.8

Bolt Syntax:............................Q .IB09X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	50.4	nA
EQL_{pd}	59.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
A	Q	t_{PLH} t_{PHL}	0.84 1.18	1.01 1.41	1.15 1.58	1.29 1.73	1.29 1.88

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

IB0BX1

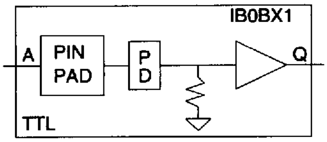
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

IB0BX1 is a non-inverting, TTL-level input buffer pad with pull-down.

Logic Symbol



Truth Table

A	Q
L	L
H	H
UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	187.8

Bolt Syntax: ....Q .IB0BX1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	49.9	nA
EQL_{pd}	61.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	11	21	31	41 (max)
A	Q	t_{PLH}	0.84	1.01	1.15	1.29	1.43
		t_{PHL}	1.19	1.41	1.58	1.73	1.88

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

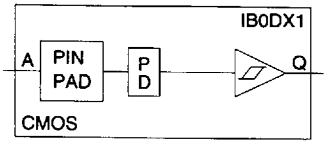
IB0DX1

AMI8G 0.8 micron CMOS Gate Array

Description:

IB0DX1 is a non-inverting, CMOS-level Schmitt trigger input buffer pad with voltage hysteresis.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	217.4

Bolt Syntax:............................Q .IB0DX1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	50.4	nA
EQL_{pd}	51.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

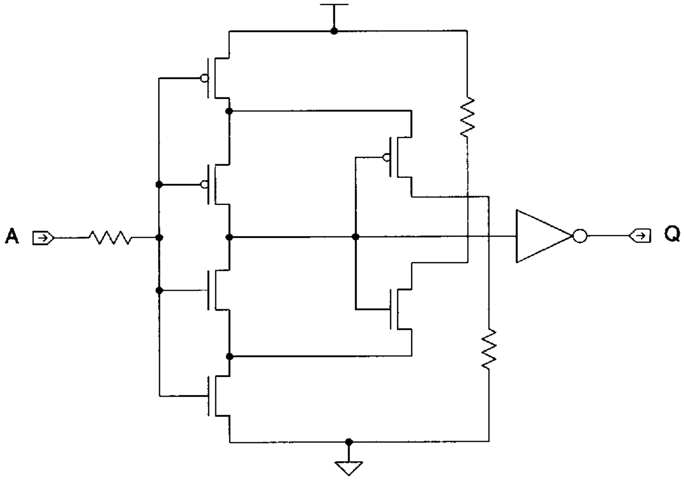
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
A	Q	t_{PLH} t_{PHL}	2.64 1.96	2.87 2.18	3.06 2.35	3.23 2.51	3.39 2.66

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

(continued on next page)

Logic Schematic



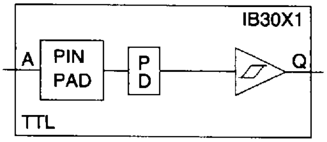
IB30X1

AMI8G 0.8 micron CMOS Gate Array

Description:

IB30X1 is a non-inverting, TTL-level Schmitt trigger input buffer pad with voltage hysteresis.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	217.4

Bolt Syntax:.............................Q .IB30X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	49.9	nA
EQL_{pd}	54.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	11	21	31	41 (max)
A	Q	t_{PLH} t_{PHL}	1.35 2.88	1.53 3.20	1.68 3.44	1.82 3.65	1.96 3.84

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

IBF1X5

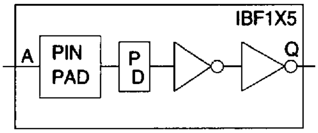
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

IBF1X5 is a non-inverting, CMOS-level input clock-driver pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	117.4

Bolt Syntax: ....Q .IBF1X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	51.6	nA
EQL_{pd}	185.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	Delay (ns) To	Parameter	Number of Equivalent Loads 1	86	172	257	343 (max)
A	Q	t_{PLH} t_{PHL}	1.18 1.23	1.37 1.40	1.53 1.54	1.68 1.66	1.84 1.79

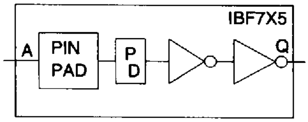
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

IBF7X5

Description:

IBF7X5 is a non-inverting, TTL-level input clock-driver pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	117.4

Bolt Syntax:............................Q .IBF7X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	49.9	nA
EQL_{pd}	189.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	86	172	257	343 (max)
A	Q	t_{PLH} t_{PHL}	1.37 1.24	1.54 1.42	1.70 1.58	1.85 1.72	2.00 1.84

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

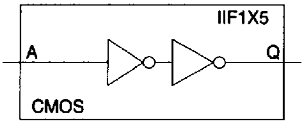
IIF1X5

AMI8G 0.8 micron CMOS Gate Array

Description:

IIF1X5 is a non-inverting, second ring, CMOS-level input clock-driver.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	5.7

Bolt Syntax: ....Q .IIF1X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	51.6	nA
EQL_{pd}	171.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	86	172	257	343 (max)
A	Q	t_{PLH}	0.69	0.87	1.03	1.19	1.34
		t_{PHL}	0.68	0.84	0.98	1.11	1.23

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI
AMERICAN MICROSYSTEMS, INC.

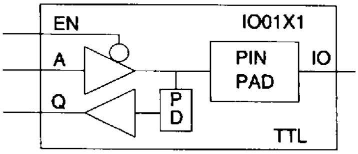
I001X1

AMI8G 0.8 micron CMOS Gate Array

Description:

IO01X1 is a 1 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.0
IO	199.4

Bolt Syntax:............................IO Q .IO01X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	53.7	nA
EQL_{pd}	269.0	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.70 1.00	0.85 1.21	0.98 1.38	1.11 1.53	1.24 1.67

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	25	35	50	75 (max)
A	IO	t_{PLH} t_{PHL}	3.01 4.59	4.21 6.35	5.41 8.11	7.20 10.76	10.19 15.18
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	0.95 0.60 3.15 4.62	 4.35 6.37	 5.55 8.14	 7.34 10.79	 10.33 15.20

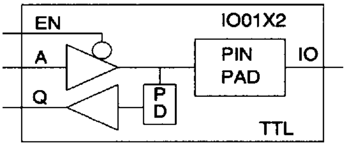
IO01X2

AMI8G 0.8 micron CMOS Gate Array

Description:

IO01X2 is a 2 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.0
IO	199.4

Bolt Syntax: ....IO Q .IO01X2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	53.7	nA
EQL_{pd}	271.6	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.69	0.85	0.98	1.11	1.25
		t_{PHL}	1.02	1.24	1.40	1.55	1.69

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	IO	t_{PLH}	1.99	4.09	5.58	7.08	10.06
		t_{PHL}	4.59	10.78	15.20	19.61	28.45
EN	IO	t_{HZ}	1.30				
		t_{LZ}	0.60				
		t_{ZH}	2.15	4.24	5.74	7.23	10.21
		t_{ZL}	4.60	10.79	15.21	19.62	28.46

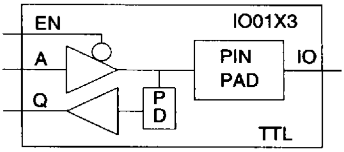
I001X3

AMI8G 0.8 micron CMOS Gate Array

Description:

IO01X3 is a 4 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	5.1
EN	4.4
IO	199.5

Bolt Syntax:............................IO Q .IO01X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	56.4	nA
EQL_{pd}	284.5	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.69 1.02	0.85 1.22	0.98 1.39	1.11 1.54	1.24 1.68

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH} t_{PHL}	1.35 2.65	2.43 5.75	3.92 10.16	6.91 19.01	9.89 27.83
EN	IO	t_{HZ}	1.39				
		t_{LZ}	0.61				
		t_{ZH}	1.58	2.65	4.15	7.13	10.12
		t_{ZL}	2.64	5.75	10.17	19.02	27.84

IO01X5

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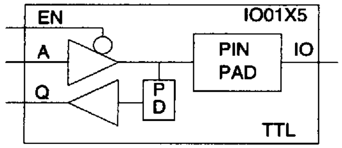
AMI8G 0.8 micron CMOS Gate Array

Description:

IO01X5 is an 8 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	9.5
EN	6.5
IO	199.9

Bolt Syntax:............................IO Q .IO01X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	61.8	nA
EQL_{pd}	313.3	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.70 1.02	0.85 1.23	0.98 1.40	1.11 1.55	1.25 1.69

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH} t_{PHL}	1.08 1.87	1.70 3.46	2.48 5.68	3.98 10.12	5.47 14.52
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.72 0.68 1.43 1.85	 2.06 3.47	 2.83 5.70	 4.34 10.14	 5.83 14.54

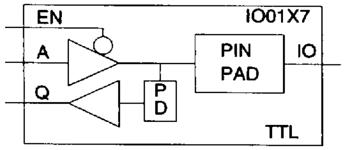
IO01X7

AMI8G 0.8 micron CMOS Gate Array

Description:

IO01X7 is a 16 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	13.6
EN	9.8
IO	200.1

Bolt Syntax:............................IO Q .IO01X7 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	68.3	nA
EQL_{pd}	348.8	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.68	0.83	0.97	1.10	1.23
		t_{PHL}	1.00	1.20	1.36	1.51	1.64

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

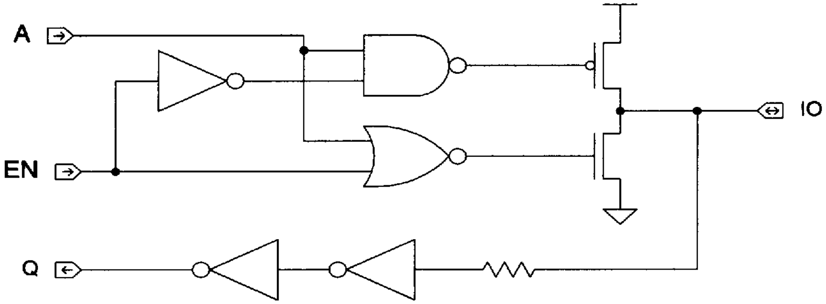
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.00	1.47	2.02	3.05	4.05
		t_{PHL}	1.38	2.22	3.36	5.59	7.80
EN	IO	t_{HZ}	1.79				
		t_{LZ}	0.98				
		t_{ZH}	1.25	1.73	2.29	3.31	4.32
		t_{ZL}	1.34	2.22	3.38	5.61	7.83

(continued on next page)

AMI8G 0.8 micron CMOS Gate Array

Logic Schematic



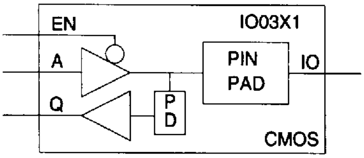
IO03X1

AMI8G 0.8 micron CMOS Gate Array

Description:

IO03X1 is a 1 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.0
IO	199.4

Bolt Syntax:.............................IO Q .IO03X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.2	nA
EQL_{pd}	267.8	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.72 0.91	0.89 1.08	1.02 1.22	1.16 1.35	1.29 1.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	25	35	50	75 (max)
A	IO	t_{PLH} t_{PHL}	5.08 3.19	7.28 4.30	9.47 5.41	12.75 7.07	18.23 9.84
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	0.95 0.60 5.23 3.22	7.42 4.39	9.61 5.44	12.89 7.10	18.37 9.87

IO03X2

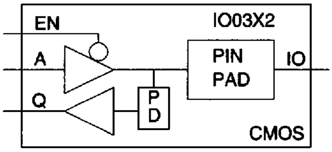
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

IO03X2 is a 2 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.0
IO	199.4

Bolt Syntax:...........................IO Q .IO03X2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	54.2	nA
EQL_{pd}	270.4	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.72 0.91	0.89 1.08	1.02 1.22	1.16 1.35	1.29 1.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	IO	t_{PLH} t_{PHL}	3.05 3.21	6.88 7.09	9.62 9.86	12.35 12.63	17.82 18.17
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.30 0.60 3.20 3.22	7.04 7.10	9.77 9.87	12.50 12.64	17.97 18.18

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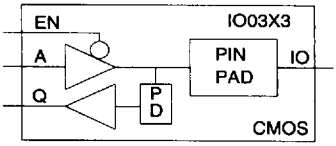
IO03X3

AMI8G 0.8 micron CMOS Gate Array

Description:

IO03X3 is a 4 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	5.1
EN	4.3
IO	199.5

Bolt Syntax:.............................IO Q .IO03X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	56.9	nA
EQL_{pd}	283.3	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.72 0.91	0.89 1.09	1.03 1.23	1.16 1.35	1.29 1.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

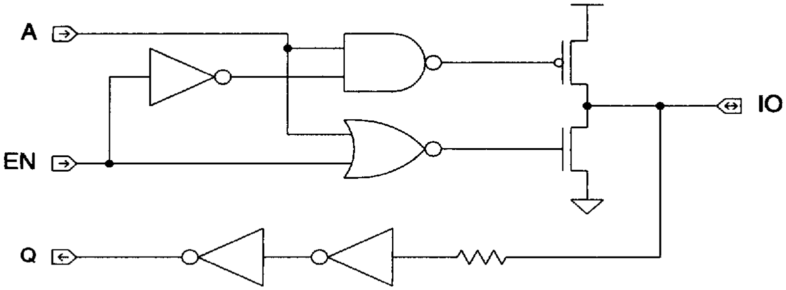
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH} t_{PHL}	1.91 1.95	3.84 3.90	6.58 6.66	12.05 12.20	17.51 17.74
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.40 0.59 2.13 1.94	 4.07 3.90	 6.80 6.67	 12.27 12.21	 17.74 17.75

(continued on next page)

AMI8G 0.8 micron CMOS Gate Array

Logic Schematic



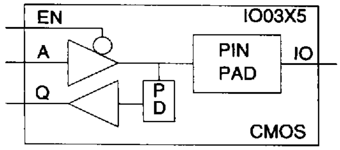
IO03X5

AMI8G 0.8 micron CMOS Gate Array

Description:

IO03X5 is an 8 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	9.5
EN	6.5
IO	200.0

Bolt Syntax:..............................IO Q .IO03X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	62.4	nA
EQL_{pd}	312.6	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.75	0.92	1.06	1.20	1.33
		t_{PHL}	0.94	1.12	1.26	1.39	1.52

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.42	2.45	3.83	6.58	9.31
		t_{PHL}	1.49	2.52	3.92	6.69	9.46
EN	IO	t_{HZ}	1.73				
		t_{LZ}	0.68				
		t_{ZH}	1.80	2.83	4.22	6.96	9.69
		t_{ZL}	1.48	2.52	3.93	6.71	9.48

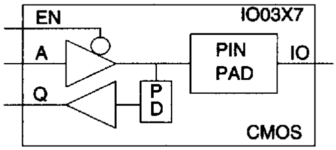
I003X7

AMI8G 0.8 micron CMOS Gate Array

Description:

IO03X7 is a 16 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	13.6
EN	9.8
IO	200.1

Bolt Syntax:............................IO Q .IO03X7 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	68.9	nA
EQL_{pd}	347.8	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.72	0.89	1.03	1.18	1.32
		t_{PHL}	0.95	1.12	1.26	1.39	1.52

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

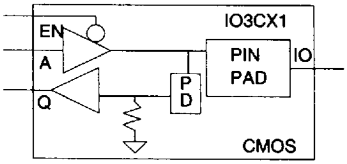
Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.26	2.00	2.96	4.80	6.62
		t_{PHL}	1.16	1.72	2.46	3.86	5.25
EN	IO	t_{HZ}	1.79				
		t_{LZ}	0.98				
		t_{ZH}	1.51	2.27	3.22	5.07	6.89
		t_{ZL}	1.12	1.72	2.47	3.89	5.28

IO3CX1

Description:

IO3CX1 is a 1 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.1
IO	199.4

Bolt Syntax: ....IO Q .IO3CX1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.2	nA
EQL_{pd}	280.5	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.72 0.91	0.89 1.08	1.02 1.22	1.16 1.35	1.29 1.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	25	35	50	75 (max)
A	IO	t_{PLH} t_{PHL}	5.16 3.19	7.36 4.29	9.56 5.39	12.85 7.03	18.35 9.78
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	0.96 0.60 5.30 3.22	 7.50 4.33	 9.69 5.43	 12.99 7.09	 18.49 9.85

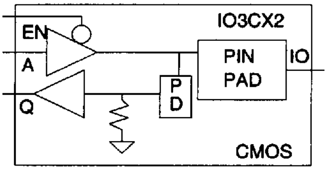
IO3CX2

AMI8G 0.8 micron CMOS Gate Array

Description:

IO3CX2 is a 2 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.9
EN	3.1
IO	199.4

Bolt Syntax:............................IO Q .IO3CX2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.2	nA
EQL_{pd}	283.1	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.72 0.91	0.89 1.08	1.02 1.22	1.16 1.35	1.29 1.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	IO	t_{PLH} t_{PHL}	3.08 3.21	6.93 7.07	9.67 9.82	12.41 12.58	17.89 18.08
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.31 0.60 3.23 3.22	 7.08 7.09	 9.82 9.85	 12.56 12.61	 18.03 18.14

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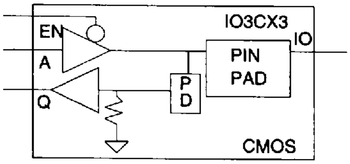
IO3CX3

AMI8G 0.8 micron CMOS Gate Array

Description:

IO3CX3 is a 4 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	5.1
EN	4.4
IO	199.5

Bolt Syntax: ....IO Q .IO3CX3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	56.9	nA
EQL_{pd}	298.2	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.72 0.91	0.89 1.09	1.03 1.22	1.16 1.35	1.29 1.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

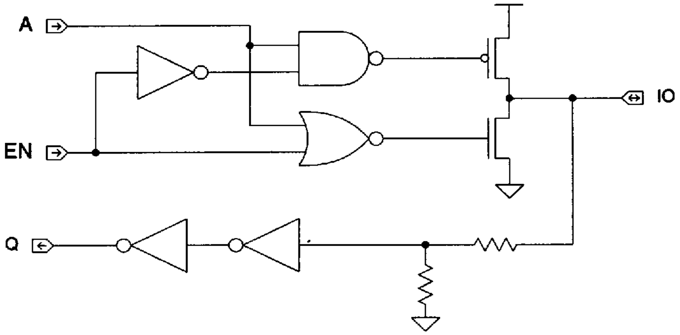
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH} t_{PHL}	1.93 1.96	3.87 3.89	6.61 6.65	12.09 12.18	17.55 17.70
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.40 0.59 2.16 1.94	 4.09 3.90	 6.83 6.67	 12.31 12.20	 17.78 17.73

(continued on next page)

AMI8G 0.8 micron CMOS Gate Array

Logic Schematic

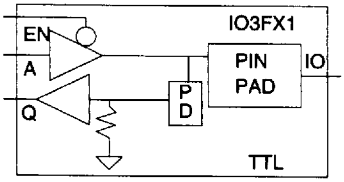


IO3FX1

Description:

IO3FX1 is a 1 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.9
EN	3.1
IO	199.4

Bolt Syntax:............................IO Q .IO3FX1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	53.7	nA
EQL_{pd}	282.7	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.70 1.02	0.85 1.23	0.99 1.40	1.12 1.55	1.25 1.69

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	IO	t_{PLH} t_{PHL}	3.06 4.58	4.26 6.34	5.45 8.09	7.25 10.73	10.25 15.12
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	0.96 0.60 3.19 4.62	 4.39 6.38	 5.59 8.14	 7.39 10.78	 10.39 15.19

IO3FX2

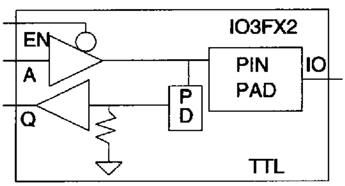
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

IO3FX2 is a 2 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.9
EN	3.1
IO	199.4

Bolt Syntax:............................IO Q .IO3FX2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	53.7	nA
EQL_{pd}	285.3	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.70 1.03	0.86 1.24	0.99 1.41	1.12 1.56	1.25 1.70

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	IO	t_{PLH} t_{PHL}	2.02 4.61	4.12 10.76	5.61 15.16	7.11 19.55	10.10 28.36
EN	IO	t_{HZ} t_{LZ} t_{ZH} $t_{Z'}$	1.30 0.60 2.17 4.62	 4.27 10.78	 5.76 15.19	 7.26 19.59	 10.25 28.41

AMI
AMERICAN MICROSYSTEMS, INC.

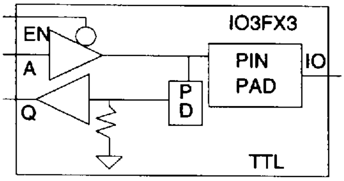
IO3FX3

AMI8G 0.8 micron CMOS Gate Array

Description:

IO3FX3 is a 4 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	5.1
EN	4.5
IO	199.5

Bolt Syntax:............................IO Q .IO3FX3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	56.4	nA
EQL_{pd}	298.2	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.70 1.04	0.86 1.25	0.99 1.42	1.12 1.56	1.25 1.70

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

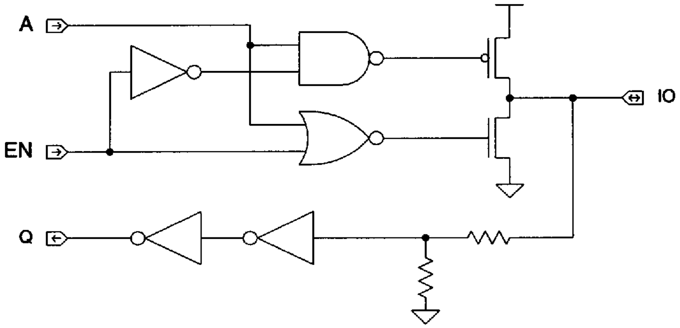
Output Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH} t_{PHL}	1.38 2.66	2.46 5.75	3.96 10.15	6.94 18.98	9.93 27.78
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.40 0.63 1.60 2.65	2.68 5.75	4.18 10.17	7.17 19.00	10.15 27.81

(continued on next page)

Logic Schematic



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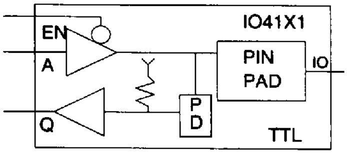
IO41X1

AMI8G 0.8 micron CMOS Gate Array

Description:

IO41X1 is a 1 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.0
IO	199.4

Bolt Syntax:............................IO Q .IO41X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.2	nA
EQL_{pd}	279.6	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.70	0.85	0.98	1.11	1.24
		t_{PHL}	1.00	1.21	1.38	1.53	1.67

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	IO	t_{PLH}	3.00	4.18	5.37	7.14	10.10
		t_{PHL}	4.61	6.37	8.14	10.80	15.24
EN	IO	t_{HZ}	0.96				
		t_{LZ}	0.60				
		t_{ZH}	3.15	4.34	5.52	7.31	10.28
		t_{ZL}	4.64	6.40	8.17	10.83	15.26

IO41X2

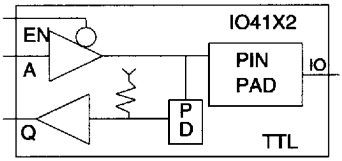
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

IO41X2 is a 2 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.0
IO	199.4

Bolt Syntax:............................IO Q .IO41X2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.2	nA
EQL_{pd}	282.2	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.69 1.02	0.85 1.23	0.98 1.40	1.11 1.55	1.25 1.69

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	IO	t_{PLH} t_{PHL}	1.99 4.62	4.07 10.82	5.56 15.25	7.04 19.67	10.00 28.53
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.30 0.60 2.15 4.62	 4.24 10.83	 5.73 15.26	 7.22 19.69	 10.19 28.55

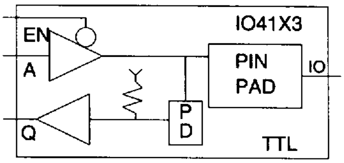
IO41X3

AMI8G 0.8 micron CMOS Gate Array

Description:

IO41X3 is a 4 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	5.1
EN	4.4
IO	199.5

Bolt Syntax:............................IO Q .IO41X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	56.9	nA
EQL_{pd}	295.1	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.69 1.02	0.85 1.22	0.98 1.39	1.11 1.54	1.24 1.68

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

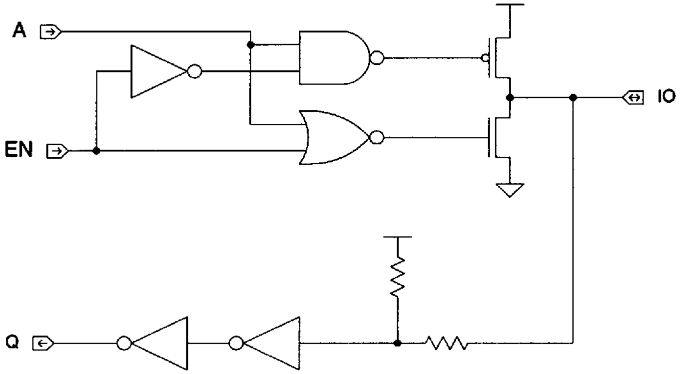
Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH} t_{PHL}	1.36 2.67	2.43 5.77	3.92 10.18	6.89 19.03	9.86 27.88
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.40 0.61 1.58 2.65	 2.65 5.77	 4.15 10.19	 7.13 19.04	 10.11 27.89

(continued on next page)

Logic Schematic



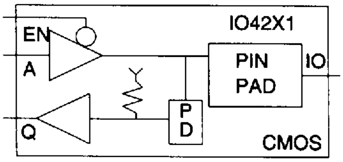
IO42X1

AMI8G 0.8 micron CMOS Gate Array

Description:

IO42X1 is a 1 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.1
IO	199.4

Bolt Syntax:............................IO Q .IO42X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.7	nA
EQL_{pd}	278.6	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.72 0.91	0.89 1.08	1.02 1.22	1.16 1.35	1.29 1.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	IO	t_{PLH} t_{PHL}	5.07 3.21	7.24 4.32	9.42 5.43	12.68 7.10	18.11 9.87
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	0.96 0.60 5.22 3.24	7.39 4.35	9.57 5.46	12.84 7.13	18.29 9.90

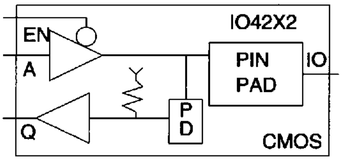
IO42X2

AMI8G 0.8 micron CMOS Gate Array

Description:

IO42X2 is a 2 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.1
IO	199.4

Bolt Syntax:............................IO Q .IO42X2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.7	nA
EQL_{pd}	281.2	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	Delay (ns) To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.72 0.91	0.89 1.08	1.02 1.22	1.16 1.35	1.29 1.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	Delay (ns) To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	IO	t_{PLH} t_{PHL}	3.05 3.23	6.87 7.12	9.59 9.89	12.31 12.66	17.75 18.21
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.31 0.60 3.20 3.24	 7.03 7.13	 9.76 9.90	 12.48 12.67	 17.94 18.22

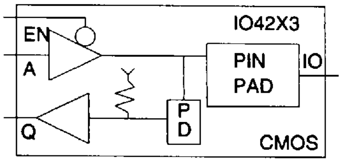
IO42X3

AMI8G 0.8 micron CMOS Gate Array

Description:

IO42X3 is a 4 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	5.1
EN	4.3
IO	199.5

Bolt Syntax:............................IO Q .IO42X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	57.5	nA
EQL_{pd}	294.0	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.72	0.89	1.03	1.16	1.29
		t_{PHL}	0.91	1.08	1.22	1.35	1.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

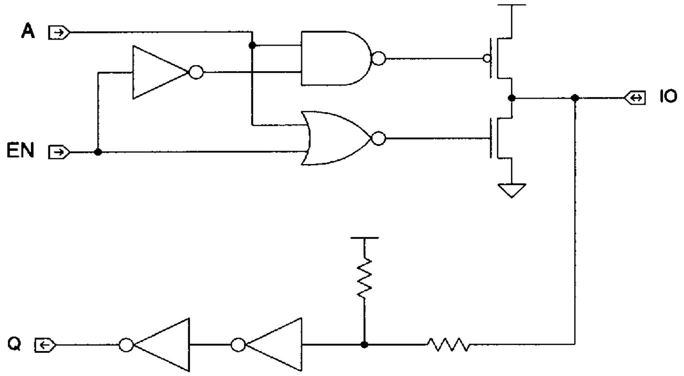
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.91	3.84	6.57	12.02	17.48
		t_{PHL}	1.96	3.91	6.68	12.22	17.76
EN	IO	t_{HZ}	1.40				
		t_{LZ}	0.59				
		t_{ZH}	2.14	4.07	6.80	12.26	17.72
		t_{ZL}	1.95	3.91	6.68	12.23	17.77

(continued on next page)

AMI8G 0.8 micron CMOS Gate Array

Logic Schematic



AMI
AMERICAN MICROSYSTEMS, INC.

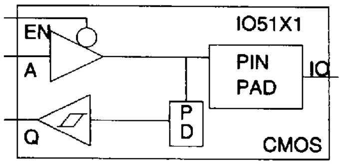
I051X1

AMI8G 0.8 micron CMOS Gate Array

Description:

IO51X1 is a 1 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and CMOS Schmitt trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.1
IO	199.4

Bolt Syntax: ....IO Q .IO51X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.1	nA
EQL_{pd}	274.6	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	2.60	2.82	3.00	3.16	3.31
		t_{PHL}	1.93	2.15	2.32	2.47	2.61

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	IO	t_{PLH}	5.09	7.28	9.47	12.75	18.23
		t_{PHL}	3.20	4.31	5.41	7.08	9.85
EN	IO	t_{HZ}	0.95				
		t_{LZ}	0.60				
		t_{ZH}	5.23	7.42	9.61	12.90	18.37
		t_{ZL}	3.23	4.33	5.44	7.10	9.87

IO51X2

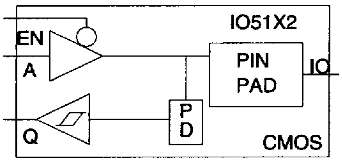
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

IO51X2 is a 2 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and CMOS Schmitt trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.1
IO	199.4

Bolt Syntax:............................IO Q .IO51X2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	54.1	nA
EQL_{pd}	277.2	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	Delay (ns) To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	2.60 1.94	2.83 2.14	3.01 2.31	3.17 2.47	3.32 2.61

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	Delay (ns) To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	IO	t_{PLH} t_{PHL}	3.05 3.22	6.88 7.09	9.62 9.86	12.36 12.63	17.82 18.17
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.30 0.60 3.21 3.23	 7.04 7.10	 9.77 9.87	 12.51 12.64	 17.98 18.18

AMI
AMERICAN MICROSYSTEMS, INC.

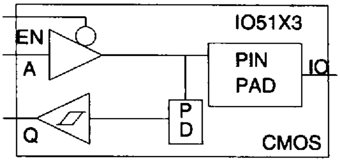
IO51X3

AMI8G 0.8 micron CMOS Gate Array

Description:

IO51X3 is a 4 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and CMOS Schmitt trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	5.1
EN	4.2
IO	199.5

Bolt Syntax:............................IO Q .IO51X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	56.9	nA
EQL_{pd}	290.0	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	2.64 1.97	2.87 2.19	3.05 2.35	3.21 2.50	3.35 2.65

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

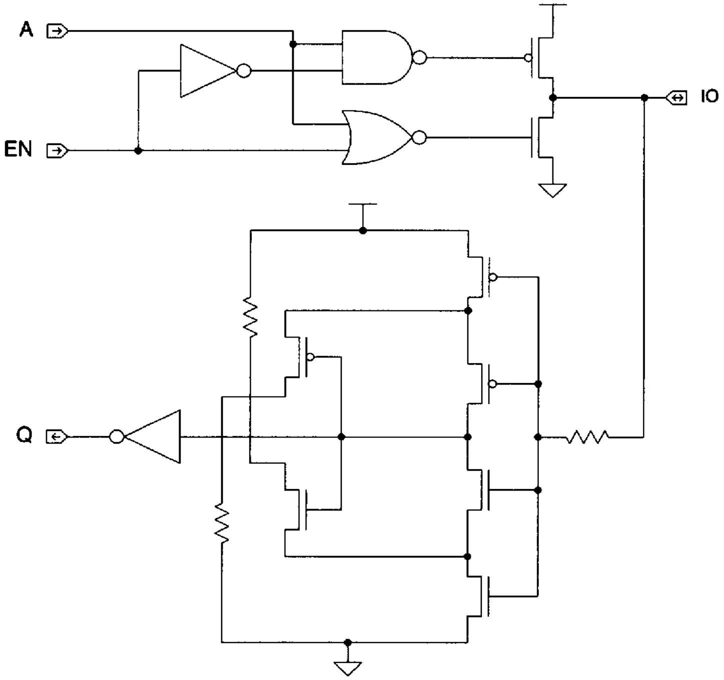
Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH} t_{PHL}	1.91 1.96	3.84 3.90	6.58 6.66	12.05 12.20	17.51 17.74
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.40 0.58 2.13 1.94	4.07 3.89	6.80 6.67	12.27 12.21	17.74 17.75

(continued on next page)

AMI8G 0.8 micron CMOS Gate Array

Logic Schematic



AMI
AMERICAN MICROSYSTEMS, INC.

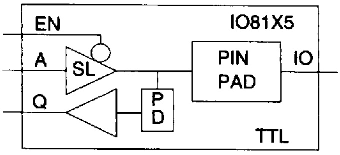
I081X5

AMI8G 0.8 micron CMOS Gate Array

Description:

IO81X5 is an 8 mA, non-inverting, TTL-level, bidirectional buffer pad with an active low enabled tri-state and controlled slew rate output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	9.9
EN	6.9
IO	199.7

Bolt Syntax:.............................IO Q .IO81X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	63.6	nA
EQL_{pd}	318.9	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.75 1.07	0.90 1.28	1.04 1.44	1.17 1.59	1.30 1.73

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH} t_{PHL}	1.36 2.69	2.44 5.77	3.93 10.07	6.92 18.47	9.90 26.78
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.60 0.68 1.71 2.67	 2.78 5.76	 4.28 10.06	 7.26 18.46	 10.25 26.77

IO81X7

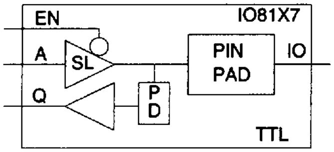
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

IO81X7 is a 16 mA, non-inverting, TTL-level, bidirectional buffer pad with an active low enabled tri-state and controlled slew rate output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	14.3
EN	8.7
IO	200.4

Bolt Syntax:............................IO Q .IO81X7 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	69.0	nA
EQL_{pd}	357.6	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.75	0.90	1.03	1.16	1.29
		t_{PHL}	1.05	1.25	1.41	1.56	1.70

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.09	1.69	2.46	3.96	5.45
		t_{PHL}	1.75	3.31	5.51	9.86	14.16
EN	IO	t_{HZ}	1.86				
		t_{LZ}	1.02				
		t_{ZH}	1.55	2.17	2.95	4.45	5.94
		t_{ZL}	1.70	3.29	5.50	9.86	14.17

AMERICAN MICROSYSTEMS, INC.

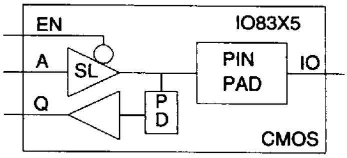
IO83X5

AMI8G 0.8 micron CMOS Gate Array

Description:

IO83X5 is an 8 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state and controlled slew rate output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	10.1
EN	6.7
IO	199.7

Bolt Syntax:............................IO Q .IO83X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	64.1	nA
EQL_{pd}	318.2	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.78	0.95	1.09	1.22	1.35
		t_{PHL}	0.98	1.15	1.29	1.42	1.54

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	50	100	200	300 (max)
A	IO	t_{PLH}	1.92	3.86	6.60	12.07	17.53
		t_{PHL}	1.98	3.93	6.70	12.24	17.78
EN	IO	t_{HZ}	1.60				
		t_{LZ}	0.68				
		t_{ZH}	2.27	4.20	6.94	12.41	17.87
		t_{ZL}	1.96	3.92	6.69	12.23	17.77

IO83X7

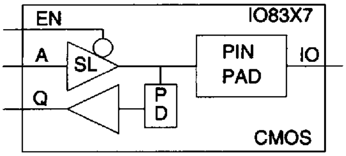
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

IO83X7 is a 16 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state and controlled slew rate output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	14.2
EN	8.7
IO	200.4

Bolt Syntax: ....IO Q .IO83X7 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	69.6	nA
EQL_{pd}	356.7	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.78	0.95	1.09	1.22	1.35
		t_{PHL}	0.98	1.14	1.28	1.41	1.54

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	50	100	200	300 (max)
A	IO	t_{PLH}	1.42	2.43	3.82	6.56	9.29
		t_{PHL}	1.38	2.36	3.74	6.51	9.28
EN	IO	t_{HZ}	1.86				
		t_{LZ}	1.02				
		t_{ZH}	1.89	2.92	4.30	7.04	9.78
		t_{ZL}	1.33	2.34	3.74	6.52	9.29

AMI
AMERICAN MICROSYSTEMS, INC.

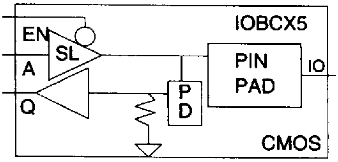
IOBCX5

AMI8G 0.8 micron CMOS Gate Array

Description:

IOBCX5 is an 8 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state, controlled slew rate output, and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	10.3
EN	7.1
IO	199.7

Bolt Syntax: ....IO Q .IOBCX5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	64.1	nA
EQL_{pd}	331.0	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process .

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.79 0.98	0.95 1.15	1.09 1.29	1.22 1.42	1.35 1.55

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH} t_{PHL}	1.94 1.99	3.87 3.93	6.62 6.69	12.09 12.22	17.56 17.74
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.60 0.68 2.28 1.96	4.22 3.92	6.96 6.69	12.43 12.22	17.90 17.75

IOBFX5

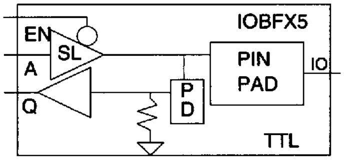
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

IOBFX5 is an 8 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state, controlled slew rate output, and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	10.0
EN	7.3
IO	199.7

Bolt Syntax:.............................IO Q .IOBFX5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	63.6	nA
EQL_{pd}	331.9	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.76 1.08	0.91 1.29	1.04 1.45	1.17 1.60	1.31 1.74

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

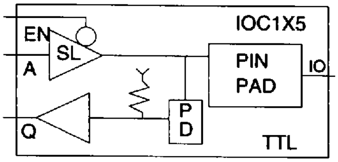
Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	50	100	200	300 (max)
A	IO	t_{PLH}	1.37	2.45	3.94	6.93	9.92
		t_{PHL}	2.70	5.78	10.07	18.45	26.72
EN	IO	t_{HZ}	1.60				
		t_{LZ}	0.68				
		t_{ZH}	1.72	2.79	4.29	7.28	10.26
		t_{ZL}	2.68	5.76	10.06	18.45	26.73

IOC1X5

Description:

IOC1X5 is an 8 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state, controlled slew rate output, and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	9.9
EN	6.9
IO	199.7

Bolt Syntax:............................IO Q .IOC1X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	64.1	nA
EQL_{pd}	329.8	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.76 1.08	0.91 1.29	1.04 1.45	1.17 1.60	1.31 1.74

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH} t_{PHL}	1.36 2.70	2.43 5.79	3.93 10.09	6.90 18.50	9.88 26.81
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.60 0.68 1.70 2.68	2.78 5.77	4.27 10.08	7.25 18.49	10.23 26.81

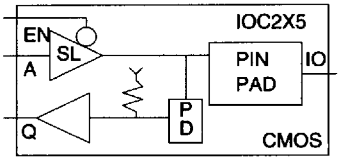
IOC2X5

AMI8G 0.8 micron CMOS Gate Array

Description:

IOC2X5 is an 8 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state, controlled slew rate output, and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	10.1
EN	6.8
IO	199.7

Bolt Syntax: ....IO Q .IOC2X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	64.6	nA
EQL_{pd}	328.7	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	0.78 0.98	0.95 1.15	1.08 1.28	1.21 1.41	1.35 1.54

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH} t_{PHL}	1.92 1.99	3.85 3.94	6.59 6.71	12.04 12.25	17.50 17.80
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.60 0.68 2.27 1.97	 4.20 3.92	 6.93 6.70	 12.39 12.24	 17.85 17.79

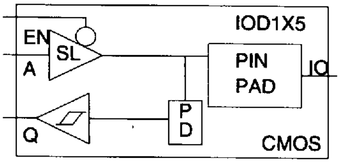
IOD1X5

AMI8G 0.8 micron CMOS Gate Array

Description:

IOD1X5 is an 8 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state, controlled slew rate output, and CMOS Schmitt trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	10.1
EN	6.9
IO	199.7

Bolt Syntax:............................IO Q .IOD1X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	64.0	nA
EQL_{pd}	325.5	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH} t_{PHL}	2.76 2.06	2.99 2.27	3.17 2.44	3.33 2.59	3.48 2.73

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH} t_{PHL}	1.93 1.98	3.86 3.93	6.60 6.70	12.07 12.24	17.53 17.78
EN	IO	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.61 0.68 2.27 1.96	4.20 3.92	6.94 6.69	12.41 12.23	17.87 17.77

OB01X1

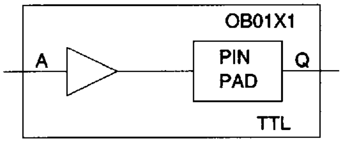
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB01X1 is a 1 mA, non-inverting, TTL-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	1.3

Bolt Syntax: ....Q .OB01X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	47.4	nA
EQL_{pd}	260.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	25	35	50	75 (max)
A	Q	t_{PLH}	3.10	4.30	5.49	7.29	10.28
		t_{PHL}	4.56	6.32	8.07	10.76	15.15

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

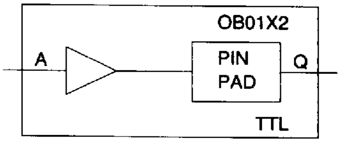
OB01X2

AMI8G 0.8 micron CMOS Gate Array

Description:

OB01X2 is a 2 mA, non-inverting, TTL-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	2.3

Bolt Syntax:............................Q .OB01X2 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	48.5	nA
EQL_{pd}	264.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	50	75	100	150 (max)
A	Q	t_{PLH}	1.75	3.84	5.33	6.82	9.81
		t_{PHL}	4.40	10.56	14.99	19.39	28.25

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB01X3

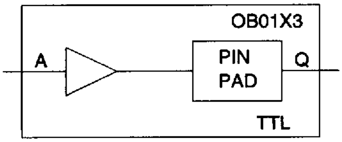
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB01X3 is a 4 mA, non-inverting, TTL-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	3.4

Bolt Syntax:............................Q .OB01X3 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	49.5	nA
EQL_{pd}	271.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH} t_{PHL}	1.24 2.58	2.29 5.66	3.78 10.11	6.77 18.92	9.75 27.76

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

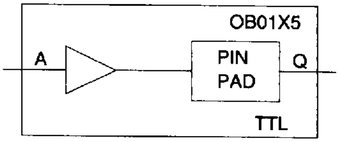
OB01X5

AMI8G 0.8 micron CMOS Gate Array

Description:

OB01X5 is an 8 mA, non-inverting, TTL-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	5.9

Bolt Syntax:............................Q .OB01X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	51.5	nA
EQL_{pd}	291.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	50	100	200	300 (max)
A	Q	t_{PLH} t_{PHL}	1.03 1.72	1.61 3.29	2.37 5.51	3.87 9.96	5.36 14.35

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB01X7

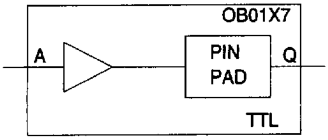
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB01X7 is a 16 mA, non-inverting, TTL-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	7.8

Bolt Syntax:............................Q .OB01X7 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	53.5	nA
EQL_{pd}	288.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH} t_{PHL}	1.04 1.37	1.48 2.21	2.02 3.35	3.04 5.58	4.03 7.78

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

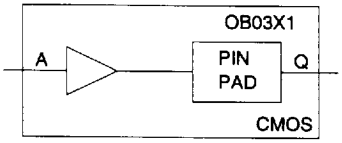
OB03X1

AMI8G 0.8 micron CMOS Gate Array

Description:

OB03X1 is a 1 mA, non-inverting, CMOS-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	1.3

Bolt Syntax:............................Q .OB03X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	47.4	nA
EQL_{pd}	260.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	25	35	50	75 (max)
A	Q	t_{PLH} t_{PHL}	5.17 3.17	7.35 4.28	9.55 5.39	12.84 7.05	18.31 9.81

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

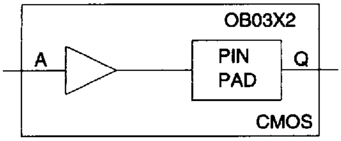
OB03X2

AMI8G 0.8 micron CMOS Gate Array

Description:

OB03X2 is a 2 mA, non-inverting, CMOS-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	2.9

Bolt Syntax:............................Q .OB03X2 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	48.5	nA
EQL_{pd}	263.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	Q	t_{PLH} t_{PHL}	2.78 3.00	6.60 6.87	9.34 9.66	12.06 12.42	17.54 17.96

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMERICAN MICROSYSTEMS, INC.

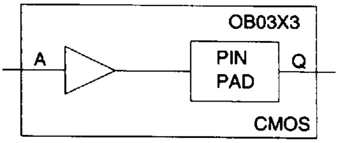
OB03X3

AMI8G 0.8 micron CMOS Gate Array

Description:

OB03X3 is a 4 mA, non-inverting, CMOS-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	3.4

Bolt Syntax:............................Q .OB03X3 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	49.5	nA
EQL_{pd}	271.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	50	100	200	300 (max)
A	Q	t_{PLH}	1.76	3.68	6.42	11.89	17.35
		t_{PHL}	1.87	3.80	6.57	12.12	17.66

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

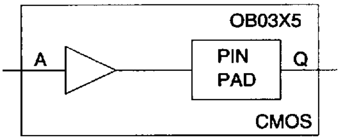
OB03X5

AMI8G 0.8 micron CMOS Gate Array

Description:

OB03X5 is an 8 mA, non-inverting, CMOS-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	5.9

Bolt Syntax:............................Q .OB03X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	51.5	nA
EQL_{pd}	291.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH} t_{PHL}	1.35 1.36	2.35 2.36	3.73 3.75	6.47 6.52	9.21 9.30

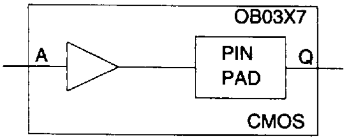
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB03X7

Description:

OB03X7 is a 16 mA, non-inverting, CMOS-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	7.8

Bolt Syntax:............................Q .OB03X7 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	53.5	nA
EQL_{pd}	288.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	Delay (ns) To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH} t_{PHL}	1.30 1.14	2.01 1.70	2.95 2.44	4.79 3.84	6.62 5.23

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

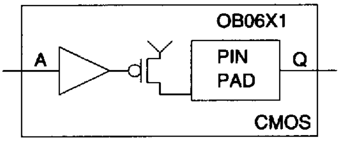
OB06X1

AMI8G 0.8 micron CMOS Gate Array

Description:

OB06X1 is a 1 mA, inverting, CMOS-level, P-channel, open-drain (pull-up) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Equivalent Load
A	1.3
Q	217.5

Bolt Syntax:............................Q .OB06X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	48.5	nA
EQL_{pd}	258.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	Q	t_{PLH} t_{HZ}	3.89 0.80	5.49	7.08	9.44	13.40

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

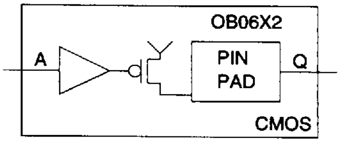
OB06X2

AMI8G 0.8 micron CMOS Gate Array

Description:

OB06X2 is a 2 mA, inverting, CMOS-level, P-channel, open-drain (pull-up) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Equivalent Load
A	1.3
Q	217.6

Bolt Syntax:............................Q .OB06X2 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	49.5	nA
EQL_{pd}	263.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	Q	t_{PLH} t_{HZ}	2.33 0.85	5.12	7.09	9.05	13.01

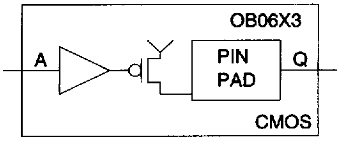
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB06X3 is a 4 mA, inverting, CMOS-level, P-channel, open-drain (pull-up) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Equivalent Load
A	1.2
Q	217.7

Bolt Syntax:............................Q .OB06X3 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	50.5	nA
EQL_{pd}	270.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	50	100	200	300 (max)
A	Q	t_{PLH} t_{HZ}	1.64 1.06	3.04	5.02	8.99	12.93

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

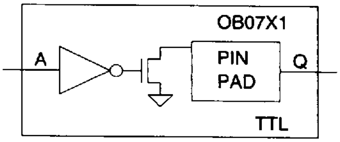
OB07X1

AMI8G 0.8 micron CMOS Gate Array

Description:

OB07X1 is a 1 mA, non-inverting, TTL-level, N-channel, open-drain (pull-down) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	Z

Pin Loading

	Equivalent Load
A	1.3
Q	217.4

Bolt Syntax:............................Q .OB07X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	47.4	nA
EQL_{pd}	254.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	Q	t_{PHL} t_{LZ}	4.31 0.54	6.09	7.84	10.46	14.86

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB07X2

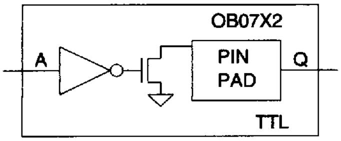
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB07X2 is a 2 mA, non-inverting, TTL-level, N-channel, open-drain (pull-down) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	Z

Pin Loading

	Equivalent Load
A	2.3
Q	217.4

Bolt Syntax:............................Q .OB07X2 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	48.5	nA
EQL_{pd}	256.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	50	75	100	150 (max)
A	Q	t_{PHL} t_{LZ}	4.23 0.38	10.34	14.76	19.17	27.97

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

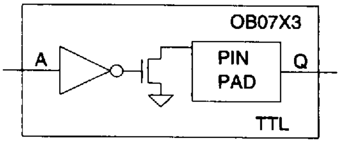
OB07X3

AMI8G 0.8 micron CMOS Gate Array

Description:

OB07X3 is a 4 mA, non-inverting,TTL-level, N-channel, open-drain (pull-down) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	Z

Pin Loading

	Equivalent Load
A	3.4
Q	217.4

Bolt Syntax:.............................Q .OB07X3 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	49.5	nA
EQL_{pd}	258.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	50	100	200	300 (max)
A	Q	t_{PHL} t_{LZ}	2.25 0.42	5.35	9.79	18.60	27.45

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB09X1

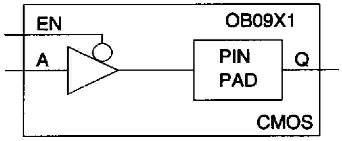
AMI
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB09X1 is a 1 mA, non-inverting, CMOS-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Equivalent Load
A	2.7
EN	2.8
Q	217.5

Bolt Syntax:..........................Q .OB09X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	50.1	nA
EQL_{pd}	265.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	Q	t_{PLH}	5.07	7.25	9.45	12.73	18.21
		t_{PHL}	3.21	4.32	5.12	7.07	9.83
EN	Q	t_{HZ}	0.96				
		t_{LZ}	0.59				
		t_{ZH}	5.22	7.39	9.58	12.87	18.35
		t_{ZL}	3.24	4.34	5.44	7.09	9.86

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI
AMERICAN MICROSYSTEMS, INC.

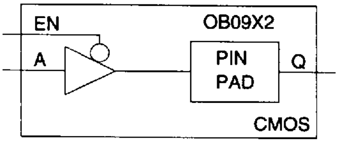
OB09X2

AMI8G 0.8 micron CMOS Gate Array

Description:

OB09X2 is a 2 mA, non-inverting, CMOS-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Equivalent Load
A	2.7
EN	2.8
Q	217.5

Bolt Syntax:.............................Q .OB09X2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	50.2	nA
EQL_{pd}	268.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	Q	t_{PLH}	3.04	6.86	9.61	12.36	17.82
		t_{PHL}	3.20	7.08	9.85	12.63	18.17
EN	Q	t_{HZ}	1.30				
		t_{LZ}	0.59				
		t_{ZH}	3.19	7.03	9.77	12.51	17.97
		t_{ZL}	3.20	7.93	9.86	12.65	18.18

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

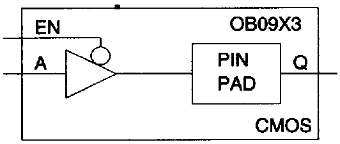
OB09X3

AMI8G 0.8 micron CMOS Gate Array

Description:

OB09X3 is a 4 mA, non-inverting, CMOS-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Equivalent Load
A	4.8
EN	3.9
Q	217.8

Bolt Syntax:............................Q .OB09X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	52.9	nA
EQL_{pd}	280.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	50	100	200	300 (max)
A	Q	t_{PLH}	1.90	3.84	6.58	12.05	17.52
		t_{PHL}	1.95	3.89	6.66	12.19	17.75
EN	Q	t_{HZ}	1.40				
		t_{LZ}	0.58				
		t_{ZH}	2.13	4.06	6.81	12.27	17.75
		t_{ZL}	1.93	3.89	6.67	12.20	17.76

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI
AMERICAN MICROSYSTEMS, INC.

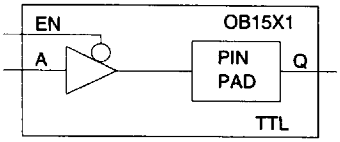
OB15X1

AMI8G 0.8 micron CMOS Gate Array

Description:

OB15X1 is a 1 mA, non-inverting, TTL-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Equivalent Load
A	2.7
EN	2.8
Q	217.5

Bolt Syntax:............................Q .OB15X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	50.2	nA
EQL_{pd}	265.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	25	35	50	75 (max)
A	Q	t_{PLH} t_{PHL}	3.00 4.61	4.19 6.34	5.39 8.12	7.18 10.74	10.17 15.15
EN	Q	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	0.96 0.59 3.14 4.63	 4.34 6.37	 5.53 8.14	 7.32 10.77	 10.31 15.17

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB15X2

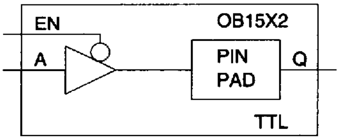
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB15X2 is a 2 mA, non-inverting, TTL-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Equivalent Load
A	2.7
EN	2.8
Q	217.6

Bolt Syntax:............................Q .OB15X2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	50.2	nA
EQL_{pd}	268.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	Q	t_{PLH} t_{PHL}	1.98 4.57	4.08 10.77	5.57 15.19	7.07 19.59	10.05 28.44
EN	Q	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.30 0.59 2.13 4.58	4.23 10.78	5.73 15.19	7.22 19.60	10.20 28.45

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

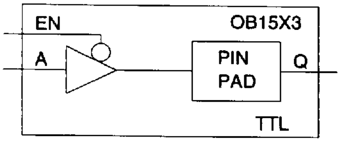
OB15X3

AMI8G 0.8 micron CMOS Gate Array

Description:

OB15X3 is a 4 mA, non-inverting, TTL-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Equivalent Load
A	4.8
EN	3.9
Q	217.7

Bolt Syntax:............................Q .OB15X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	52.9	nA
EQL_{pd}	280.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH} t_{PHL}	1.35 2.65	2.43 5.74	3.92 10.16	6.91 19.02	9.89 27.83
EN	Q	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.40 0.58 1.57 2.63	2.65 5.74	4.15 10.17	7.13 19.03	10.11 27.84

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB81X5

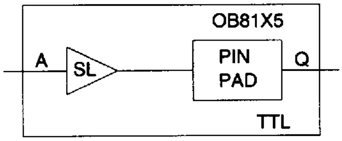
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB81X5 is an 8 mA, non-inverting, TTL-level, output buffer pad with controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	8.1

Bolt Syntax:............................Q .OB81X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	54.9	nA
EQL_{pd}	301.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	Delay (ns) To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH} t_{PHL}	1.24 2.59	2.30 5.57	3.79 9.70	6.78 17.77	9.76 25.76

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

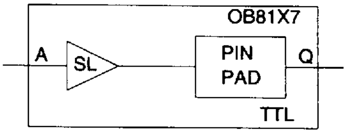
OB81X7

AMI8G 0.8 micron CMOS Gate Array

Description:

OB81X7 is a 16 mA, non-inverting, TTL-level, output buffer pad with controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	10.9

Bolt Syntax:............................Q .OB81X7 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	58.0	nA
EQL_{pd}	304.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH} t_{PHL}	1.01 1.69	1.57 3.23	2.33 5.40	3.82 9.62	5.31 13.73

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB83X5

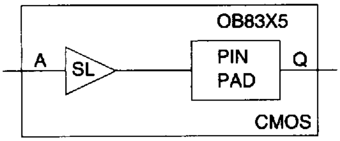
AMI
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB83X5 is an 8 mA, non-inverting, CMOS-level, output buffer pad with controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	8.1

Bolt Syntax: ....Q .OB83X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.9	nA
EQL_{pd}	301.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	Delay (ns) To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH} t_{PHL}	1.79 1.89	3.71 3.84	6.44 6.61	11.88 12.14	17.30 17.69

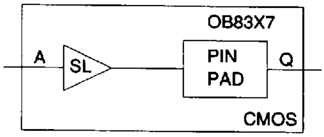
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB83X7

Description:

OB83X7 is a 16 mA, non-inverting, CMOS-level, output buffer pad with controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	10.9

Bolt Syntax:............................Q .OB83X7 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	58.0	nA
EQL_{pd}	304.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH} t_{PHL}	1.31 1.31	2.30 2.30	3.67 3.60	6.41 6.45	9.14 9.21

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB86X5

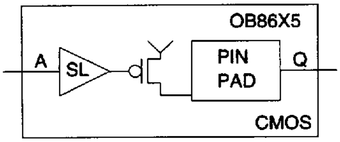
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB86X5 is an 8 mA, inverting, CMOS-level, output buffer pad with a P-channel open-drain (pull-up) and controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Equivalent Load
A	1.2
Q	217.8

Bolt Syntax:............................Q .OB86X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	53.9	nA
EQL_{pd}	289.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH} t_{PHZ}	1.70 1.25	2.91	4.63	8.03	11.43

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

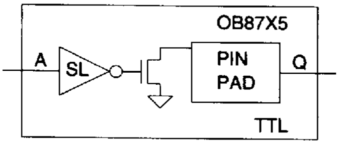
OB87X5

AMI8G 0.8 micron CMOS Gate Array

Description:

OB87X5 is an 8 mA, non-inverting, TTL-level, output buffer pad with N-channel open-drain (pull-down) and controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	L
H	Z

Pin Loading

	Equivalent Load
A	6.1
Q	217.4

Bolt Syntax:............................Q .OB87X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	51.5	nA
EQL_{pd}	275.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PHL}	2.25	5.23	9.34	17.38	25.28
		t_{PLZ}	0.42				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB89X5

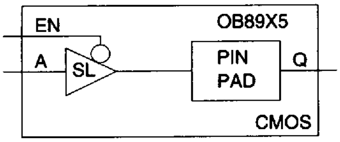
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB89X5 is an 8 mA, non-inverting, CMOS-level, tri-state output buffer pad with active low enable and controlled slew rate output.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Equivalent Load
A	9.5
EN	6.3
Q	217.8

Bolt Syntax:............................Q .OB89X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	60.1	nA
EQL_{pd}	318.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	50	100	200	300 (max)
A	Q	t_{PLH}	1.92	3.85	6.59	12.06	17.50
		t_{PHL}	1.99	3.92	6.69	12.23	17.77
EN	Q	t_{HZ}	1.60				
		t_{LZ}	0.68				
		t_{ZH}	2.27	4.20	6.93	12.40	17.86
		t_{ZL}	1.96	3.91	6.68	12.22	17.76

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI
AMERICAN MICROSYSTEMS, INC.

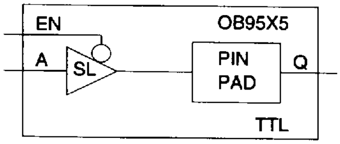
OB95X5

AMI8G 0.8 micron CMOS Gate Array

Description:

OB95X5 is an 8 mA, non-inverting, TTL-level, tri-state output buffer pad with active low enable and controlled slew rate output.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Equivalent Load
A	9.5
EN	6.3
Q	217.8

Bolt Syntax: ....Q .OB95X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	60.1	nA
EQL_{pd}	318.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	50	100	200	300 (max)
A	Q	t_{PLH}	1.36	2.43	3.93	6.92	9.90
		t_{PHL}	2.68	5.75	10.04	18.45	26.74
EN	Q	t_{HZ}	1.60				
		t_{LZ}	0.68				
		t_{ZH}	1.70	2.78	4.27	7.26	10.24
		t_{ZL}	2.66	5.74	10.03	18.44	26.73

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

PORA

AMI8G 0.8 micron CMOS Gate Array

Description:

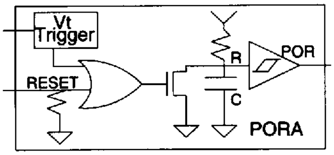
PORA is a power-on-reset circuit for 5V operation.

When power is applied, the POR output is asserted low for at least 400 nanoseconds after the logic circuits become operational. The active high RESET input also drives the POR signal to its active low state.

For proper operation, user-designed external circuitry must limit the slew rate of V_{DD} power to a maximum of one volt per microsecond. This ensures that the reset pulse will be properly output when V_{DD} falls to zero and immediately returns to its valid range.

PORA will work at V_{DD} voltages down to 3.0V. For operation with V_{DD} voltage below 4.5V, user-designed external circuitry must limit maximum V_{DD} slew rate to 0.5V per microsecond.

Logic Symbol



Truth Table

RESET	POR
L	H
H	L

Pin Loading

	Equivalent Load
RESET	0.9

Bolt Syntax: ....POR .PORA RESET;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	103.0	nA
EQL_{pd}	670.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	11	21	31	41 (max)
RESET	POR	t_{PLH} t_{PHL}	978.2 5.49	978.4 5.76	978.6 5.97	978.8 6.17	979.0 6.35

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

PORB

AMI8G 0.8 micron CMOS Gate Array

Description:

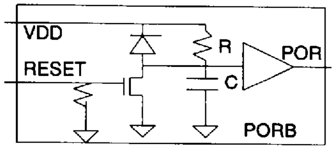
PORB is a power-on-reset circuit for 3V operation.

The POR output is active low. The active high RESET input can also drive the POR line low.

PORB is designed for rapidly rising V_{DD} power associated with battery-operated equipment. For proper operation, V_{DD} slew rate must be faster than 7.5V per microsecond.

The POR output will remain low at least 50 ns after V_{DD} reaches a valid 3V level.

Logic Symbol



Truth Table

RESET	POR
L	H
H	L

Pin Loading

	Equivalent Load
RESET	TBD

Bolt Syntax:............................POR .PORB RESET;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	TBD	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	4	8	12	16 (max)
RESET	POR	t_{PLH}	1356.9	1357.0	1357.2	1357.3	1357.4
		t_{PHL}	5.54	5.62	5.73	5.82	5.90

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

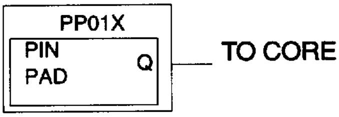
PP01X

AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

Description:

PP01X is a V_{SS} power supply pin for output buffers, input buffers, and core cells combined. The PP01X is intended for circumstances where output and core busses are to be tied together. It should not be used in conjunction with PPP1X or PPC1X.

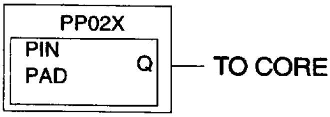


PP02X

AMI8G 0.8 micron CMOS Gate Array

Description:

PP02X is a V_{DD} power supply pin for output buffers, input buffers, and core cells combined. One PP02X must be used for each power (V_{DD}) pin.

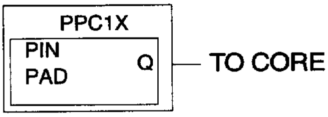


PPC1X

AMI8G 0.8 micron CMOS Gate Array

Description:

PPC1X is a V_{SS} power supply pin for core cells and input buffers only. One PPC1X must be used for each ground (V_{SS}) pin for the core cells and input buffers.

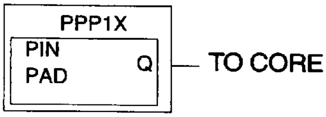


PPP1X

AMI8G 0.8 micron CMOS Gate Array

Description:

PPP1X is a V_{SS} power supply pin for output buffers only. One PPP1X must be used for each ground (V_{SS}) pin.



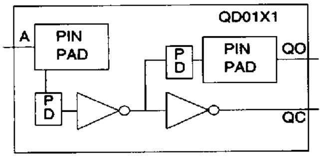
QD01X1

AMI8G 0.8 micron CMOS Gate Array

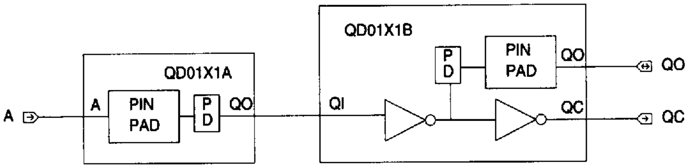
Description:

QD01X1 is a 3.58 MHz (1MHz - 10 MHz) crystal oscillator, where QC is the clock to the chip logic and QO is the oscillator feedback. This cell is made up of two pad cells and requires the use of two package pins. The Logic Schematic below shows how to connect the two pad cells.

Logic Symbol



Logic Schematic



Truth Table

A	QC	QO
L	L	H
H	H	L

Pin Loading

	Equivalent Load
A	107.1
QO	107.1

Bolt Syntax:............................A QO .QD01X1A ;

....QC QO .QD01X1B QI;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	23.3	nA
EQL_{pd}	125.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
QO	QC	t_{PLH} t_{PHL}	1.00 1.05	1.15 1.21	1.28 1.34	1.41 1.46	1.54 1.59

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

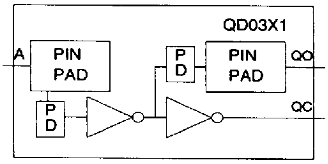
QD03X1

AMI8G 0.8 micron CMOS Gate Array

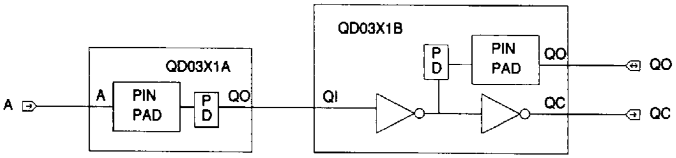
Description:

QD03X1 is a 20 MHz (10 MHz - 32 MHz) crystal oscillator, where QC is the clock to the chip logic and QO is the oscillator feedback. This cell is made up of two pad cells and requires the use of two package pins. The Logic Schematic below shows how to connect the two pad cells.

Logic Symbol



Logic Schematic



Truth Table

A	QC	QO
L	L	H
H	H	L

Pin Loading

	Equivalent Load
A	107.1
QO	107.1

Bolt Syntax:............................A QO .QD03X1A ;

....QC QO .QD03X1B QI;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	23.3	nA
EQL_{pd}	125.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
QO	QC	t_{PLH} t_{PHL}	1.00 1.05	1.15 1.21	1.28 1.34	1.41 1.46	1.54 1.59

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

QD06X1

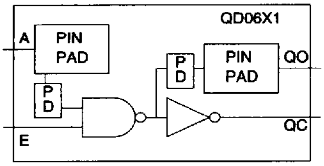
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

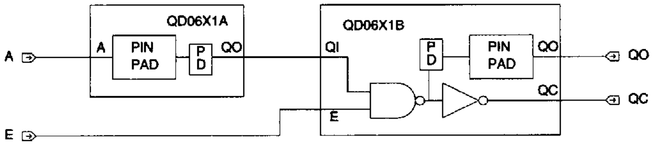
Description:

QD06X1 is a 33 MHz enabled crystal oscillator, where QC is the clock to the chip logic and QO is the oscillator feedback. This cell is made up of two pad cells and requires the use of two package pins. The Logic Schematic below shows how to connect the two pad cells.

Logic Symbol



Logic Schematic



Truth Table

A	QC	QO
L	L	H
H	H	L

Pin Loading

	Equivalent Load
A	107.1
E	2.0
QO	107.1

Bolt Syntax:............................A QO .QD06X1A E;

....QC QO .QD06X1B QI;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	23.3	nA
EQL_{pd}	125.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Number of Equivalent Loads				
From	To		1	11	21	31	41 (max)
QO	QC	t_{PLH} t_{PHL}	1.00 1.05	1.15 1.21	1.28 1.34	1.41 1.46	1.54 1.59

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

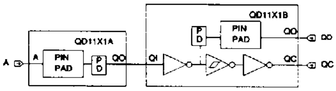
QD11X1

AMI8G 0.8 micron CMOS Gate Array

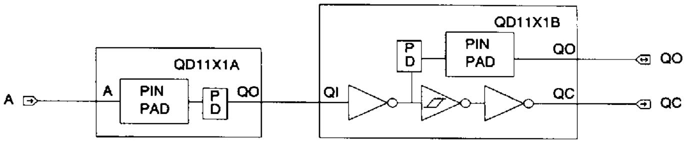
Description:

QD11X1 is a 32kHz (32kHz - 1MHz) crystal oscillator with Schmitt trigger. QC is the clock to the chip logic and QO is the oscillator feedback. This cell is made up of two pad cells and requires the use of two package pins. The Logic Schematic below shows how to connect the two pad cells.

Logic Symbol



Logic Schematic



Truth Table

A	QC	QO
L	H	H
H	L	L

Pin Loading

	Equivalent Load
A	107.1
QO	107.1

Bolt Syntax:............................A QO .QD11X1A ;

....QC QO .QD11X1B QI;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	23.3	nA
EQL_{pd}	125.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	Delay (ns) To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
QO	QC	t_{PLH} t_{PHL}	2.28 1.58	2.49 1.77	2.65 1.93	2.80 2.07	2.94 2.21

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

QD13X1

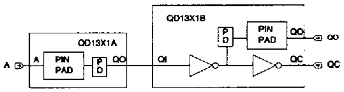
AMI
AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

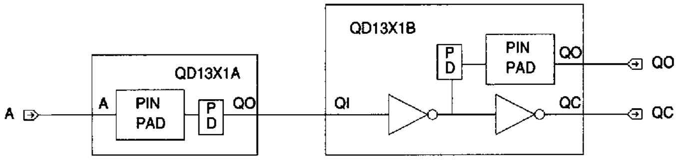
Description:

QD13X1 is a 33-36 MHz third-overtone crystal oscillator, where QC is the clock to the chip logic and QO is the oscillator feedback. This cell is made up of two pad cells and requires the use of two package pins. The Logic Schematic below shows how to connect the two pad cells.

Logic Symbol



Logic Schematic



Truth Table

A	QC	QO
L	L	H
H	H	L

Pin Loading

	Equivalent Load
A	107.1
QO	107.1

Bolt Syntax:............................A QO .QD13X1A ;

....QC QO .QD13X1B QI;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} ($T_J = 85°C$)	23.3	nA
EQL_{pd}	125.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: $T_J = 25°C$, $V_{DD} = 5.0V$, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
QO	QC	t_{PLH} t_{PHL}	1.04 1.23	1.20 1.20	1.34 1.52	1.48 1.64	1.62 1.76

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Megacell Overview

Digital Soft Megacells

Overview

American Microsystems, Inc. (AMI) provides a wide selection of Megacells for use in the development of ASICs; they ease the design of "systems on silicon". Chip designers today are faced with short time-to-market at the same time gate arrays and standard cells are allowing designs of up to several hundred thousand gates. Complex elements allow greater functionality without adversely affecting a design schedule. In fact they can accelerate time-to-market.

Megacells also provide industry standard functions that have been proven in silicon. Reducing design time, board space, system costs, and power requirements while increasing reliability and performance, AMI Megacells enable the ASIC designer to develop chips that take on the characteristics of systems.

The terms megacell, megamacro, megafunction, macrocell, core and other trademarked terms are prevalent in the industry today. These terms are often interchangeable, and some have specific meaning to various companies. They refer to complex blocks of logic that implement a digital function. Often the function is compatible to a standard product like an 8051. Other times the function is more generic; a configurable PCI controller, for example. Sometimes there is associated physical data, sometimes not. "Core" often refers to a complex function that has hand-packed physical data and an associated standard physical interface. It cannot be modified by the end user.

At AMI we refer to all complex functions as Megacells. These are broken down into Cores (8051 and 6502 code compatibles etc.), peripherals (UARTs, SCSI controllers, timers, RTCs etc.), datapath (multipliers, adders, shifters etc.), and FIFOs.

AMI offers a selection of soft Megacells that duplicate the function of industry standard parts (core processors and peripherals), and Megacells developed by using parameterized logic synthesizers (Datapath and FIFOs).

AMI's strategy is to make all megacells soft. This works well except for certain FIFOs that require the use of RAM (a hard cell). Some megacells are defined using VHDL while others are netlist based. There is no associated physical data with AMI's megacells. The physical mask layout will be different for each instance depending on other functions being used, the place-and-route tools, and process technology. Because our Megacells are soft, they are technology independent and many can be customized to meet your particular needs.

Why Megacells

Using megacells in designing ASICs has several advantages. Megacells help decrease design time and cost by providing large building blocks that are the equivalent of standard products and functions. The power consumption of a soft megacell can be greatly reduced in comparison to the HMOS standard product that it replaces. Also, because several functions can be put on a single die, printed circuit board space and capacitance can be saved and the power requirements to get signals on and off ICs are minimized.

Reliability and system costs improve because of decreased part and pin counts. Also, because the megacell is typically implemented in a process technology smaller than the original standard product, performance can be several times that of the standard product.

Core Processors and Peripherals

The Core Processor and Peripheral megacells are designed to duplicate the function of industry standard parts. The datasheets for these megacells are intended to give a short overview, to define cell pinout and to outline any functional differences between AMI's megacell and the industry standard part. Detailed functional information can be found in any standard device datasheet.

Core Processors

MEGACELL	FUNCTION
MG29C01	4-Bit microprocessor slice
MG29C10	Microprogram controller/sequencer
M320C25	DSP processor
M320C50	DSP processor
MG65C02	8-Bit microprocessor
M8042	8-Bit slave microcontroller
M8048	8-Bit microcontroller
MG80C85	8-Bit microprocessor
MGMC32	Core processor, 8032 compatible
MGMC32FB	Core processor, 8032FB compatible
MGMC32SD	Reduced function MGMC32

Megacell Overview

Digital Soft Megacells

Peripherals

MEGACELL	FUNCTION
MG1468C18	Real-time clock
M16C450	UART
M6402	UART
M6845	CRT controller
M765A	Floppy disk controller
M8251A	Communication interface USART
M8253	Programmable interval timer
M82530	Serial communications controller
MG82C37A	Programmable DMA controller
MG82C50A	Asynchronous comm. element
MG82C54	Programmable interval timer
MG82C55A	Programmable peripheral interface
MG82C59A	Programmable interrupt controller
M8490	SCSI controller
M85C30	Serial communications controller
M8868A	UART
M91C36	Digital data separator
M91C360	Digital data separator
MFDC	Floppy disk controller
MGI2CSL	I^2C Serial bus slave transceiver
MI2C	I^2C Bus interface

Datapath, FIFOs

Most of these megacells are produced using parameterized synthesizers which allow the creation of various megacell sizes and speeds. They can be optimized for either minimum delay, minimum gate count or can be designed to meet a specified delay.

These synthesizers produce soft megacell schematics in the ASIC Standard Library and are available on various workstations. The datasheets contain a functional description, a pin description, and sample equivalent gate counts with sample delays.

Datapath

MEGACELL	FUNCTION
MGAxxyyDv	Adder
MGAxxyyEv	Adder-subtractor
MGBxxyyAv	Barrel/arithmetic shifter
MGBxxBv	Barrel shifter
MGBxxyyCv	Arithmetic shifter
MGCDxxAv	Decrement Counter
MGCUxxAv	Increment Counter
MGCxxAv	2-function comparator
MGCxxBv	6-function comparator
MGDxxAv	Decrementer
MGIxxAv	Incrementer
MGIxxBv	Incrementer/decrementer
MGMxxyyDv	Multiplier
MGMxxyyEv	Multiplier-accumulator
MGSxxyyAv	Subtractor

FIFOs

MEGACELL	FUNCTION
MGFxxyyC1	Latch-Based FIFO
MGFxxxxyyD	Synchronous FIFO
MGFxxxxyyE	Asynchronous FIFO

Soft Megacells

Soft Megacells provide extreme flexibility with regard to design changes, testability, fault grading, design checking, process selection, and whether the design is implemented as a Gate Array or Standard Cell. Also, to improve the robustness of the Megacell, AMI's Megacells are built with fully static logic and no internal tristates.

Since no physical entity is associated with the Megacell, its characteristics and functions can be changed or deleted. For example, to change the initial conditions of the MGMC32 output ports, it is only necessary to change the output port flip-flop in each port cell from a set type of flop to a reset type of flop.

By deleting unused functions, gate count can be minimized. For example, if a timer or UART is not being used, it can be deleted resulting in a lower gate count. Running the simulations, as one would do after any design change, validates correct implementation of the design change.

However, it is in design checking where the strengths of the soft Megacell approach become obvious. Electronic design has benefited from the recent introduction of software programs that check many aspects of the design, including set up and hold times for flip-flops, the possibility of asynchronous race conditions, and the fault coverage of the test vectors. The netlist implementation of the Megacell can be subjected to these checks along with the rest of the circuitry. Behavioral models, which are frequently used with hard Megacells, bypass these checks.

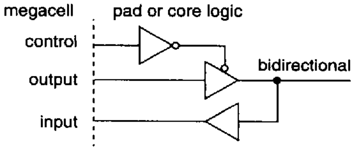
Since the soft megacell uses only components of the ASIC standard library, process dependencies in the design are minimized, if not completely removed. As a result, the design can be ported to new technologies as they become available. This means not only future cost savings, but extended voltage and temperature operation as well.

Bidirectional Pins

Many of AMI's Megacells are functional equivalents of standard products which have bidirectional pins. A bidirectional pin can be either an input or an output. To make our megacells easier to use and to reduce the possibility of excess current, AMI has split these single bidirectional pins into three pins: input, output and control.

If it is necessary to recombine these pins into a single bidirectional pin, the logic in the following figure can be used. If the bidirectional pin is to become a pin on the ASIC, this logic can come from a pad cell. Often the control pin controls a bank of bidirectional pins.

Split-Pins to Bidirectional-Pin Logic



Testing

Testability of Megacells in ASIC designs is important. Usually, additional logic is necessary to simplify testing. Providing either direct or multiplexed input and output pins for controlling and observing the Megacell can greatly simplify testing and system debugging. This dictates that designs are contained in packages having at least as many pins as the Megacell with the highest pin count.

If some pins on the ASIC will be multiplexed between their normal function and a megacell function a test-mode will be needed to apply the simulation patterns to the megacell. When enabled by this test mode, the megacell pins are connected to the pins of the ASIC. The supplied, or independent, simulation patterns can then be run to develop a test or to verify the functionality of the Megacell.

There are a number of ways to implement a test-mode. The simplest is to use an otherwise unused pin. Another approach is to use two or three ASIC pins and determine an unused condition in normal operation. This condition can then be used to enable the test-mode. Finally, in a bus oriented design, it may be possible to write to an unused register bit to signify test-mode.

Timing

Because AMI's Megacells are technology independent the electrical and timing characteristics of the design will depend on the process, layout, and implementation. When the Megacell is included in a design, delays can be estimated using the customer-preferred logic simulator and delay calculator. Post-layout simulations using actual capacitance numbers will provide even more accurate timing characteristics.

Datapath Megacells are designed to have delays that meet the user's timing requirements. These delays may change slightly when the Megacells are incorporated into the ASIC.

Our Core Processor and Peripheral Megacells have simple pin-to-pin relationships with all input changes expected on the cycle boundary. Some Megacell clocks expect signals that are in the return-to-one or return-to-zero format. Functional timing diagrams are available for Megacells that have more complex timing relationships.

Electrical Characteristics

AMI's Megacells do not have any direct external connections to the pins of an ASIC. All necessary connections should be made with pad buffers external to the Megacell. The selection of the pad buffer--if one is used--is up to the system designer, and that selection will establish the DC electrical characteristics of the final design.

All inputs to the Megacells are one to four logical loads. All outputs are buffered so that loading on a given pin will not affect the internal operation.

Ordering and Availability

To order a Megacell, complete the "ASIC Megacell Order-form", available from any AMI databook, and submit by fax (208-234-6659), email (megacells@poci.amis.com), or from AMI's internet homepage (http://www.amis.com). Current Megacell information can also be obtained at AMI's homepage.

Prices for Megacells are charged on a per-use basis. This charge is encountered each time the cell is used on a new design. A few Megacells also have an associated royalty. Contact Marketing for a price quote.

AMERICAN MICROSYSTEMS, INC.

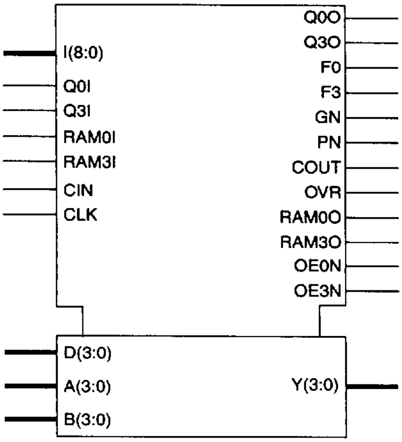
MG29C01
4-Bit Microprocessor

Features

- A high-performance, low-power CMOS megacell featuring functional compatibility with the industry standard 2901
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- 4-Bit cascadable bit-slice
- Eight function ALU including addition, two subtraction and five logic operations on two operands
- Microprogrammable with three groups of three bits each for ALU function, destination control and source operand
- Two address architecture provides independent access to two working registers
- Five source ports for data selection
- Four status flags including carry, zero, overflow and sign

LOGIC SYMBOL

MG29C01



Description

The MG29C01 is a high-performance 4-bit cascadable microprocessor.

The MG29C01 offers the designer a simple and methodical approach to designing bit-slice microprocessors, high-speed ALUs and boolean machines.

The MG29C01 consists of a fast ALU, a 16-word by 4-bit two port RAM and the required decoding, multiplexing and shifting circuits. The microinstruction word consists of nine bits divided into three groups. Bits 0-2 select the ALU source operads. Bits 3-5 select the ALU function and bits 6-8 select the destination register.

The ALU allows for several arithmetic functions which include: unsigned addition and subtraction, two's complement and one's complement addition and subtraction, and decrementing. The ALU also produces the status bits: overflow, carry-out, F0. Boolean functions offered include: AND, OR, XOR, XNOR, INVERT, PASS, ZERO, and MASK.

The MG29C01 also includes a 16-word by 4-bit register, a 4-bit Q register, and various sources for the ALU.

Soft Megacells

This soft megacell is in the ASIC Standard Library which is technology and process independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MG29C01
4-Bit Microprocessor

AMI AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
I(8:0)	Input	The nine instruction lines.
CIN	Input	Carry in to the ALU.
CLK	Input	The clock input.
D(3:0)	Input	Data inputs. These data may be selected as one of the ALU sources. D(0) is the LSB.
A(3:0)	Input	The address inputs to the register stack, used to select which register's contents are available through the A port. A(0) is the LSB.
B(3:0)	Input	The address inputs to the register stack used to select which registers contents are available through the B port. B(0) is the LSB.
Q0O, Q3O Q0I, Q3I	I/O	The input and output shift lines for the LSB and MSB of the Q register, allow for shift up and shift down operations. Q3 is the MSB. Q0O is valid when OE0N is low and Q3O is valid when OE3N is low.
F0	Output	Becomes active when all four ALU outputs are low.
F3	Output	The most significant ALU output bit.
GN, PN	Output	The generate and propagate outputs of the ALU, can be used to for carry look-ahead.
COUT	Output	Carry out of the ALU.
OVR	Output	Overflow. Indicates the result of an arithmetic two's complement operation has overflowed into the sign bit.
OE0N	Output	A low on this pin indicates Q0O and RAM0O are valid.
OE3N	Output	A low on this pin indicates Q3O and RAM3O are valid.
RAM0O, RAM3O RAM0I, RAM3I	I/O	The input and output shift lines for the LSB and MSB of the register stack, allow for shift up and shift down operations. RAM3 is the MSB. RAM0O is valid when OE0N is low and RAM3O is valid when OE3N is low.
Y(3:0)	Output	Data outputs. These outputs are connected to either ALU or A port of the register stack.

Megacells

Equivalent Gates

STANDARD CELL	GATE ARRAY
810	1000

AMERICAN MICROSYSTEMS, INC.

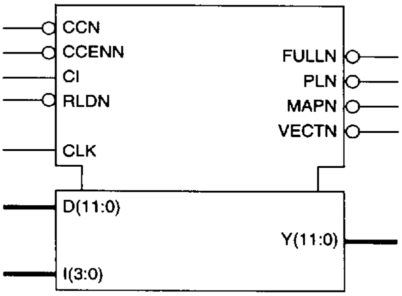
MG29C10
12-Bit Microprogram Controller

Features

- A high-performance, low-power CMOS megacell featuring functional compatibility with the industry standard 2910
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- 12-Bit internal elements can address up to 4069 words of microcode
- 16 sequence control instructions, most are conditional on state of internal loop counter and/or external conditional input
- 12-Bit down counter is pre-settable for repeating instructions or counting loop iterations internally
- Four microprogram address sources including 9-level stack, microprogram counter, branch address bus, and internal holding register
- Internal decoder function controls output enables for three branch address devices

LOGIC SYMBOL

MG29C10



Description

The MG29C10 is a high-performance 12-bit microprogram controller. It functions as an address sequencer for controlling the execution of microinstructions in microprogram memory.

It also controls conditional branching to any microinstruction within its 4096 word range. There are nine levels of subroutine nesting with return linkage and looping capability provided by a last-in, first-out stack.

The MG29C10 has four sources for providing the 12-bit address during each microinstruction. These four sources are as follows:

1. A direct external input.
2. A register/counter (R) which retains data loaded during an earlier microinstruction.
3. The last-in, first-out stack/file (F).
4. The address counter/register which usually increments the addresses.

The MG29C10 consists of six functional blocks: an instruction PLA, a multiplexer, a register/counter, a zero detector, a 9-word by 12-bit stack, a microprogram counter register, and an incrementer.

Soft Megacells

This soft megacell is in the ASIC Standard Library which is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MG29C10
12-Bit Microprogram Controller

AMI
AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
CCN	Input	Used as test input criterion. Active low.
CCENN	Input	Enables CCN. Active low.
CI	Input	Carry input to the low order of the microprogram counter.
RLDN	Input	Forces loading of register/counter regardless of instruction or condition. Active low.
CLK	Input	Master input clock.
D(11:0)	Input	Direct data input to register/counter and multiplexer. D(0) is the LSB.
I(3:0)	Input	Instruction inputs. I(0) is the LSB.
FULLN	Output	Goes low when the internal stack is full. Active low.
PLN	Output	Used to select #1 source (usually a pipeline register) as the direct input source.
MAPN	Output	Used to select #2 source (usually a mapping ROM or PLA) as the direct input source.
VECTN	Output	Used to select #3 source (usually an interrupt starting address) as the direct input source.
Y(11:0)	Output	Address to microprogram memory. Y(0) is the LSB.

Equivalent Gates

STANDARD CELL	GATE ARRAY
1,350	1,950

AMI
AMERICAN MICROSYSTEMS, INC.

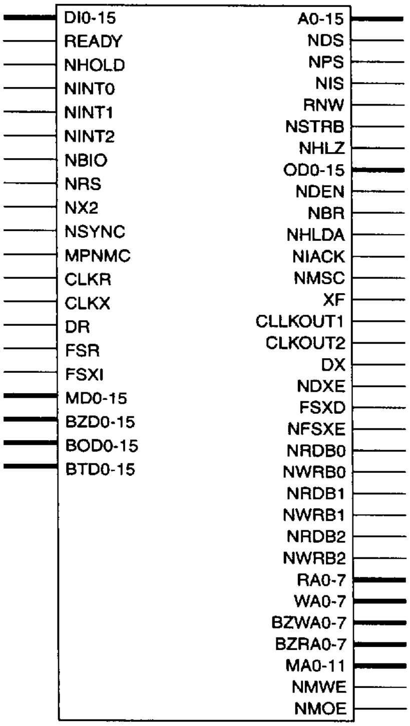
M320C25 DSP

Features

- AMI's implementation of 3Soft's MegaMacro®
- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- 32-bit ALU/accumulator
- 16 X 16 parallel multiplier
- 16-bit shifter
- Up to 64k words of program memory
- Up to 64k words of data memory
- 16-bit timer
- Serial port
- Equivalent gates: 17,000

LOGIC SYMBOL

M320C25



Description

The M320C25 is a digital signal processor with separate data and program memory, both of which may be up to 64k words. It has a 16-bit shifter, a 16 X 16 bit parallel multiplier and a 32-bit ALU/accumulator. Instructions are pipelined and it can perform single-cycle multiply/accumulate instructions. It contains a 16-bit timer, eight auxiliary registers, an eight-level hardware stack, sixteen input and sixteen output channels, and a serial port. It is fully compatible, including instructions execution times, with industry standard devices.

The M32C25 contains no RAM or ROM but provides functional interconnect signals for connecting to memory blocks. If internal program memory is required, a single port RAM (or ROM) block of up to 4k X 16 may be connected to the M320C25 (also the 256 X 16 internal data RAM block 0 may be configured as program memory). If internal data memory is required 1,2 or 3 blocks of dual-port RAM may be connected to the M320C25. Block 0 and 1 can be up to 256 X 16 and block 2 up to 32 X 16.

M320C50
DSP

AMERICAN MICROSYSTEMS, INC.

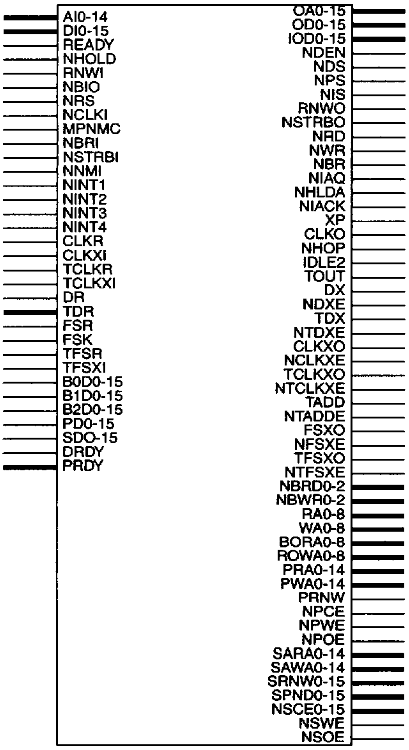
Digital Soft Megacells

Features

- AMI's implementation of 3Soft's MegaMacro®
- Functionally compatible with the industry standard
- 32-bit ALU/accumulator
- 16 X 16 parallel multiplier
- 16-bit shifter
- 16-bit parallel logic space
- Up to 64k words each of program and data memory
- 64K I/O space
- Interrupt controller
- Serial port and TDM serial port
- Equivalent gates: 40,000

LOGIC SYMBOL

M320C50



Description

The M320C50 is a digital signal processor with separate data and program memory. The program memory may be up to 64k words. The data memory may be up to 64k words, up to 32 words of which may be global access. It has 64k 16-bit I/O ports, sixteen of which are memory mapped. The central ALU has a 32-bit arithmetic logic unit, a 32-bit accumulator and accumulator buffer, a 16-bit scaling shifter, and a 16 X 16 parallel multiplier. A separate parallel logic unit can perform bit manipulations on any data memory location or control/status register. It has eight auxiliary registers, an eight level hardware stack, and a four stage instruction pipeline. The M320C50 contains no ROM or RAM but provides functional interconnect signals for connecting to memory blocks.

Peripherals are controlled through 28 memory-mapped registers and consists of: a timer, a serial port, a time-division-multiplexed serial port, a programmable wait-state generator, an interrupt controller, and the I/O ports.

The M320C50 is compatible, including instructions execution times, with industry standard devices.

AMERICAN MICROSYSTEMS, INC.

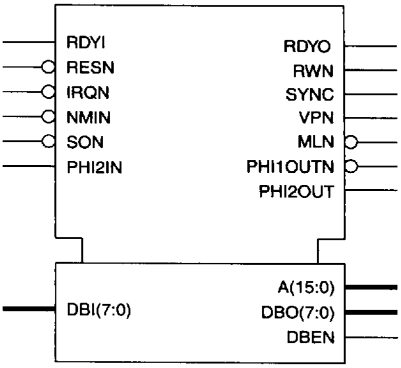
MG65C02
8-Bit Core Microprocessor

Features

- High-performance, schematic-based megacell
- Functional compatibility with the industry standard 6502
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- 8-Bit Microprocessor
- Fully Static Design
- 0-33 MHz Operation
- 64 kbytes Program Address Space
- Enhanced Instruction Set
- Supports Bit Manipulation
- 72 instructions and 212 opcodes
- 15 address modes
- Interrupt Capability

LOGIC SYMBOL

MG65C02



Description

The MG65C02 is an 8-bit microprocessor which is compatible with the industry standard W65C02S. It has been designed to be compatible with both the original NMOS 6502 and the newer CMOS variations from various vendors.

The MG65C02 runs all 6502 opcodes as well as the new Enhanced Instruction set which include the new bit manipulation opcodes - RMB, SMB, BBR, BBS, and WAI and STP instructions. The latest functions are also incorporated in the MG65C02 such as Bus Enable, Vector-Pull, and Memory Lock. It accesses 65 kbytes of addressable Memory. It is fully static allowing the external clock to stop in either state. Operation frequency follows a range of 0 MHz, for low power or standby modes, to more than 25 MHz for high speed applications.

Soft Megacells

The MG65C02 is designed as a soft megacell in the ASIC standard library, which allows it to be used with other logic and/or megacells. The soft megacell approach has advantages of design flexibility and portability, and a path for future cost reduction by process migration. It can be used in gate array or standard cell circuits. The core allows access to pins and functions not available in the industry standard 6502.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MG65C02
8-Bit Core Microprocessor

AMI
AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTION
A0-A15	O	Address to memory.
DBO0-DBO7	O	Data bus output. Valid when DBEN is high.
DBI0-DBI7	I	Data bus Input. Should be valid when DBEN is low.
DBEN	O	Data Bus Enable.
RDYI	I	Ready Input, active low. Stops the internal clock.
RDYO	O	Ready Output. The WAI instruction uses this pin to bring RDYI low.
RESN	I	Active low Reset.
IRQN	I	Active low Interrupt.
NMIN	I	Active low Non-maskable interrupt.
SON	I	Active low sets the overflow bit in the status word.
RWN	O	Read/Write. Active low for write.
SYNC	O	Synchronize. Active during opcode fetch cycle.
VPN	O	Vector Pull, active low. Low during interrupt vector access.
MLN	O	Memory Lock, active low. Low during Read-Modify-Write (RMW) portion of RMW instructions.
PHI2IN	I	Clock.
PHI1OUTN	O	Clock. Out of phase with C2IN.
PHI2OUT	O	Clock. In phase with PHI2IN. It also goes high with the STP instruction.

Equivalent Gates

STANDARD CELL	GATE ARRAY
2,950	3,850

AMI
AMERICAN MICROSYSTEMS, INC.

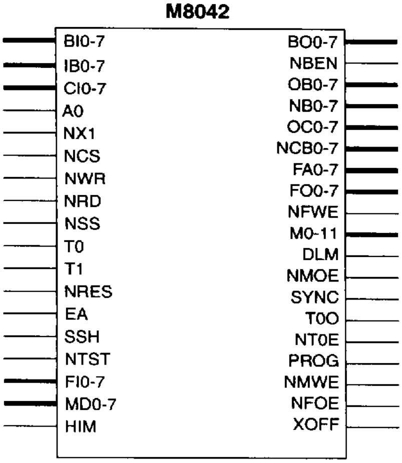
M8042
8-Bit Slave Microcontroller

Digital Soft Megacells

Features

- AMI's implementation of 3Soft's MegaMacro®
- Functionally compatible with the industry standard 8042
- Uses AMI's ASIC Standard Library for technology independence
- Up to 256 bytes of data memory
- Up to 4K bytes of program memory
- Memory down-load mode
- 8-bit timer/counter
- DMA, interrupt or polled operation supported
- Power saving modes
- Equivalent gates (does not include RAM or ROM): Standard Cell - 2,750; Gate Array - 3,500

LOGIC SYMBOL



Description

The M8042 is an 8-bit slave microcontroller. This microcode-free design is software compatible with industry standard discrete devices. It can address data RAM of up to 256 bytes and program RAM or ROM of up to 4K bytes. If program memory is implemented with RAM a special down-load mode is available to program the RAM. An 8-bit timer/counter and 18 I/O pins are available.

Data is transferred between the M8042 and a master CPU through separate input and output data bus buffers. Communication can be controlled by two DMA handshaking lines or by interrupts.

The M8042 has two power saving modes; soft power down mode and hard power down mode. In soft power down mode the clock to the ALU is stopped but the timer/counter and interrupts are still active. In hard power down mode the clock to the entire M8042 is stopped.

Signals are present that allow the end user to choose the appropriate memory block for each implementation. This allows memory size to be configured, and if necessary, the program memory block may be implemented as "down-loadable" RAM.

As no I/O cells are included in the design, all bidirectional lines (the Data Bus, the Port1 and Port2 buses) are split into input and output sections, and have associated control lines for enabling and disabling 3-state buffers where appropriate. There are individual enable lines for each of the Port1 and Port2 outputs. This allows implementation of the 'quasi-bidirectional' pins feature of the original device.

There is only one clock input (NX1), this is again due to the fact that there are no I/O cells in the design. The output of a suitable crystal oscillator I/O cell should be connected to this input. XOFF (which is high true) is used to disable the oscillator I/O cell in power saving mode.

This megacell requires the use of ROM and RAM which can be ordered from the AMI Memory group.

A per-use fee is associated with this megacell. Contact the factory for more information.

M8048
8-Bit Microcontroller

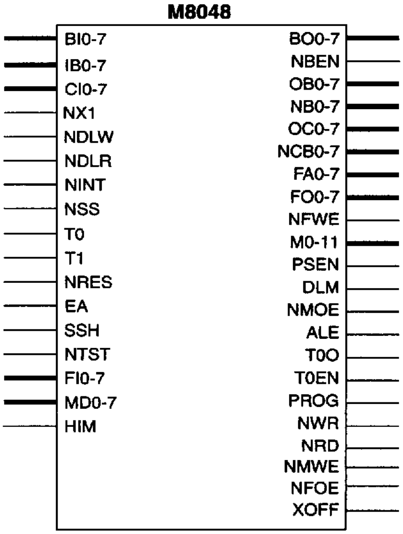
AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Features

- AMI's implementation of 3Soft's MegaMacro®
- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Up to 256 bytes of data memory
- Up to 4K bytes of RAM or ROM program memory
- Memory down-load mode
- 8-bit timer/counter
- Power saving modes
- Equivalent gates:
  Standard Cell - 2,770; Gate Array - 3,470

LOGIC SYMBOL



Description

The M8048 is an 8-bit microcontroller. This microcode-free design is software compatible (including instruction execution times) with industry standard discrete devices. It can address data RAM of up to 256 bytes and program RAM or ROM of up to 4k bytes. If program memory is implemented with RAM a special down-load mode is available to program the RAM. An 8-bit timer/counter and 27 I/O lines are available, and both internal and external interrupts are supported.

The M8048 has two power saving modes; soft power down mode and hard power down mode. In soft power down mode the clock to the ALU is stopped but the timer/counter and interrupts are still active. In hard power down mode the clock to the entire M8048 is stopped.

A per-use fee is associated with this megacell. Contact the factory for more information.

AMERICAN MICROSYSTEMS, INC.

MG80C85
8-Bit Microprocessor

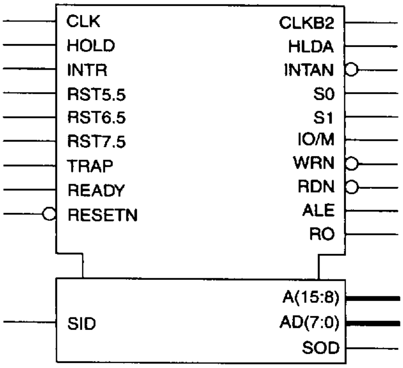
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell featuring functional compatibility with the industry standard 8085 and 8085A
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- Full support of extended instruction set, and standard 8080 and 8085/8085A instruction sets
- Runs over 10,000 CP/M® programs
- Direct addressing to 64 kbytes
- Four Interrupt inputs (one non-maskable)

LOGIC SYMBOL

MG80C85



Description

The MG80C85 is an 8-bit microprocessor which features complete functional compatibility with industry standard 8085s and 8085As, and includes support for the special extended instruction set. Its design incorporates an onboard system controller, clock generator, serial I/O port and direct addressing capability to 64K bytes of memory. The MG80C85 utilizes a multiplexed data bus, with 16-bit addresses split between an 8-bit address bus and an 8-bit data bus.

The MG80C85 is a macrocell building block for ASIC Logic design. Thus it can be used in conjunction with existing standard cell and gate array libraries to incorporate into original customer IC designs for lower overall system costs.

Soft Megacells

This soft megacell is in the ASIC Standard Library which is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MG80C85
8-Bit Microprocessor

AMI
AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
A(15:8)	O	High Address Bus. The most significant 8 bits of the memory address. A(15) is the MSB.
AD(7:0)	I/O	Low Address and Data Bus. The low order memory address bus multiplexed with the data bus.
ALE	O	Address Latch Enable. This signal occurs during the first clock state of a machine cycle.
CLK	O	Clock. The period of CLK is twice the period of the CLKBY2 input.
HLDA	O	Hold Acknowledge. Indicates that the CPU has received the HOLD request.
HOLD	I	Hold Request. Indicates another master is requesting the use of the address and data buses.
INTAN	O	Interrupt Acknowledge. This active low signal indicates that the interrupt request input (INTR) has been recognized and acknowledged.
INTR	I	Interrupt Request. When INTR goes HIGH, it will inhibit the Program Counter, generate an $\overline{\text{INTA}}$) signal, and sample the data bus for a RESTART or CALL instruction.
IO/$\overline{\text{M}}$	O	Machine Cycle Status. See S0 and S1 status bits for further details.
RDN, WRN	O	Read and Write Control. These active low signals indicate that selected memory or I/O device is to be read or written to. They are high impedance during HOLD, HALT and RESET modes.
READY	I	Ready. This signal is set to HIGH during read or write cycles to indicate that the selected memory or I/O device is ready to send or receive data.
RESETN	I	Reset In. This active low signal sets the Program Counter to zero, and resets the interrupt enable (INTE) and HLDA flip-flop.
RO	O	Reset Out. Indicates that the CPU is being reset.
RST7.5 RST6.5 RST5.5	I	Restart Interrupts. These inputs provide three maskable interrupts which invoke an automatic internal restart. RST7.5 is the highest relative priority, followed by RST6.5 and RST5.5. All three interrupts have a higher priority than INTR.
SO,S1, IO/$\overline{\text{M}}$	O	Status Outputs. These signals provide an indication of the machine status during any given cycle. The status may be latched by the falling edge of the ALE signal.
SID	I	Serial Input Data. Data on this pin is loaded into accumulator bit 7 during a RIM instruction.
SOD	O	Serial Output Data. This signal is set or reset by the SIM instruction.
TRAP	I	Trap Interrupt. The highest priority non-maskable restart interrupt.
CLKBY2	I	Clock by Two. This is the input clock source, used to drive the internal clock generator.

Equivalent Gates

STANDARD CELL	GATE ARRAY
TBD	TBD

AMERICAN MICROSYSTEMS, INC.

MGMC32 Family
8-Bit Core Microcontrollers

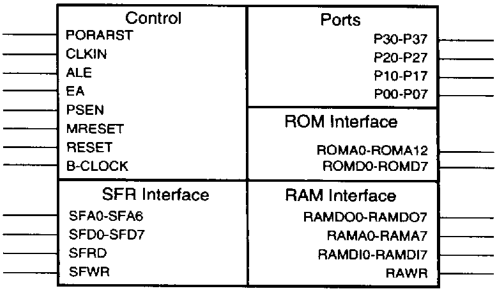
Digital Soft Megacells

Features

- Functionally compatible with the industry standard 8051 family
- Several configurations to choose from; including PCA and reduced-function options
- Schematic-based, uses the ASIC Standard Library for technology independence
- Fully Static Design
- Capable of high speed operation
- Low Standby Current At Full Supply Voltage
- 64 kilobytes of Data and Program Address Space
- Boolean Processor and serial port
- Access To Special Function Register Bus

LOGIC SYMBOL

MGMC32



Description

AMI's MGMC32 ASIC microcontroller family is a set of 8-bit microcontrollers that are functionally compatible with the industry standard 8052 and 8052FB. All members of the MGMC32 family are built around the same core processor and use the same instruction set. They differ only in the number and types of peripherals. None of these controllers contain ROM or RAM, the user should add any desired memory.

All controllers are supported by a multiple source, two level interrupt capability. The core processor supports up to 256 bytes of scratchpad RAM and up to 64K of ROM. The size of the internal ROM may be adjusted to meet a specific application.

MGMC32

The basic MGMC32 contains four 8-bit parallel ports, two external interrupt sources, three timer/counters, a serial port, and power management. It is compatible with the 8052.

MGMC32SD

The MGMC32SD removes the serial port.

MGMC32FB

This configuration adds a programmable-counter array, a watchdog timer, and an emulator port to the MGMC32. It is compatible with the industry standard 8052FB.

These configurations duplicate existing microcontrollers and will meet the requirements of most applications. However, the MGMC32 is not limited to just these configurations. The internal SFR bus has been made available to the designer. This allows the designer to place their own application into the SFR address space where it may be directly operated on by the 8051 instruction set.

Since the MGMC32 microcontrollers are ASIC soft Megacells in the ASIC Standard Library, they obtain their AC and DC characteristics from the process that they are manufactured in. This allows the end user to select both the strengths of the output buffers and type of input buffer desired for each pin. And by choosing the appropriate process, it is possible to obtain low voltage operation at supplies of 3 volts or less. The process also provides for the maximum processor speed. Since the design is fully static, the clock may be stopped at any time and in either state in order to minimize power.

MGMC32 Family
8-Bit Core Microcontrollers

AMI
AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTION
P30-P37	IO	Port 3
P20-P27	IO	Port 2
P10-P17	IO	Port 1
P00-P07	IO	Port 0
RESET	I	Reset. Resets to location 0 only.
PORARST	I	Initializes the Power On Reset.
MRESET	I	Master Reset.
EA	IO	External Address. IO used with some In Circuit Emulators.
ALE	IO	Address Latch Enable.Is an input for special modes during reset.
PSEN	IO	Program Store Enable. Enables external ROM fetch. Is an input for special modes during reset.
CLKIN	I	Clock input.
B-CLOCK	O	Buffered Clock. Runs at half the XTAL2I frequency. Can clock synchronous memories.
ROMA0-ROMA12	O	ROM Address Bus.
ROMD0-ROMD7	I	ROM Data Bus.
SFA0-SFA6	O	Special Function Register Address Bus.
SFD0-SFD7	IO	Special Function Data Bus.
SFRD	O	Special Function Write Strobe.
SFWR	O	Special Function Read Strobe.
RAMA0-RAMA7	O	Scratchpad RAM Address Bus.
RAMDO0-RAMDO7	O	Scratchpad RAM Data Out Bus.
RAMDI0-RAMDI7	I	Scratchpad RAM Data In Bus.
RAWR	O	Scratchpad RAM Write.
RARD	O	Scratchpad RAM Read.

Equivalent Gates (does not include ROM or RAM)

	STANDARD CELL	GATE ARRAY
MGMC32SD	7,370	9,200
MGMC32	8,800	11,000
MGMC32FB	11,720	14,750

AMERICAN MICROSYSTEMS, INC.

MG1468C18
Real-Time Clock

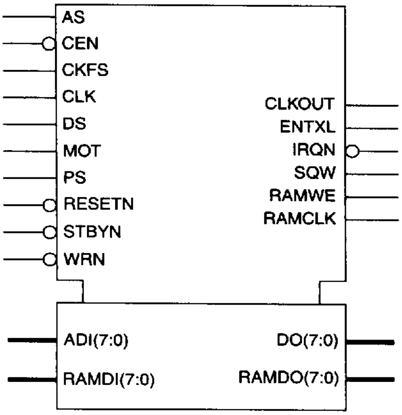
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell
- Functionally compatible with the industry standard 146818
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- 12- or 24-hour clock with a.m and p.m. mode
- Leap year and end-of-month recognition
- Programmable alarm

LOGIC SYMBOL

MG1468C18



Description

The MG1468C18 Real-Time Clock is a peripheral device which may be used with various processors/computers. It combines these features: a complete time-of-day clock with alarm and one hundred year calendar; and a programmable periodic interrupt and square wave generator.

The Real-Time Clock is designed for use as a battery powered element, including all the common backed-up functions such as RAM, time and calendar.

The megacell has been partitioned with battery backup application in mind. For purposes of electrical isolation the multiplexed address and data bus is split into input and output sides. The split avoids any possible conduction paths which result when the outputs of the tristate buffers in a portion of the chip, which could be without power, are connected to active or tristate outputs of powered circuits.

If not using battery backup, it is possible to configure the megacell to appear to the rest of the ASIC as if the data bus were bidirectional using ENTXL.

This megacell requires the use of an external 64-byte by 8-bit RAM with outputs always enabled. This RAM, in the correct process, can be ordered from the AMI Memory group.

Soft Megacells

This soft megacell is in the ASIC Standard Library which is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MG1468C18
Real-Time Clock

AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
ADI(7:0)	Input	Multiplexed bidirectional address and data bus. May be combined with the DO(7:0) bus using the ENTXL signal.
AS	Input	Address strobe. The falling edge of AS latches the address from the ADI bus.
CEN	Input	Chip enable, active low.
CKFS	Input	Selects the output frequency of CLKOUT. When CKFS=1, the frequency of CLKOUT will equal CLK. When CKFS=0. the frequency of CLKOUT will equal CLK/4.
CLK	Input	Time-base input for the time functions of the Real-TIme Clock.
CLKOUT	Output	Output at the time-base frequency divided by 1 or 4.
DO(7:0)	Output	Data output bus. May be combined with the ADI(7:0) bus using the ENTXL signal.
DS	Input	Data Strobe. The DS signal is used with the WRN signal to latch write data from the ADI bus and output data to the DO bus.
ENTXL	Output	Input/Output bus control. Used to create a multiplexed address/data bus external to the RTC. When ENTXL = 0, this external bus should be put in output mode, indicating a read cycle. If ENTXL = 1, the bus should be in a high-impedance state, allowing external drive.
IRQN	Output	Interrupt request, active low. Signifies an interrupt condition is present.
MOT	Input	Allows selection between Motorola (MOT=1) and Intel (MOT=0) bus timing.
PS	Input	Power sense. Used to control the Valid RAM and Time bit in register D.
RAMCLK	Output	RAM clock. An output from the megacell used to clock timed RAMs.
RAMDI(7:0)	Input	RAM data into the megacell.
RAMDO(7:0)	Output	RAM data coming out of the megacell.
RAMWE	Output	RAM write enable.
RESETN	Input	Megacell reset active low. Does not affect the clock, calendar or RAM functions.
STBYN	Input	Stand by, active low. Prevents access to the RTC.
SQW	Output	Square wave output from one of the 15 taps provided by the 22 internal-divider stages.
WRN	Input	Write enable, active low. Used with the DS pin to read and write data.

Equivalent Gates[1]

STANDARD CELL	GATE ARRAY
2,000	2,500

[1] Does not include RAM.

AMERICAN MICROSYSTEMS, INC.

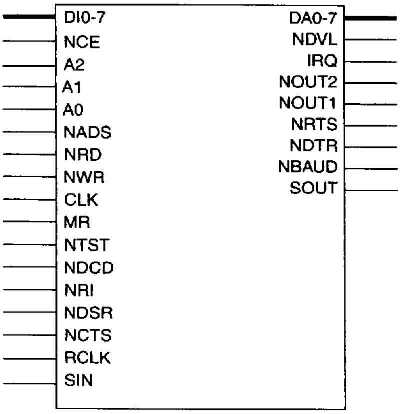
M16C450
UART

Features

- AMI's implementation of 3Soft's MegaMacro®
- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Programmable word length, stop bits and parity
- Programmable baud rate generator
- Interrupt generator
- Loop-back mode
- Scratch register
- Equivalent gates:
  Standard Cell - 1,700; Gate Array - 2,250

LOGIC SYMBOL

M16C450



Description

The M16C450 is a universal asynchronous receiver/transmitter (UART) which is fully programmable by an 8-bit CPU interface. It supports word lengths from five to eight bits, an optional parity bit and one or two stop bits. If enabled the parity can be odd, even or forced to a defined state. A 16-bit programmable baud rate generator and an 8-bit scratch register are included. Eight modem control lines and a diagnostic loop-back mode are provided.

An interrupt can be generated from any one of 10 sources.

Transmission is initiated by writing the data to be sent to the Transmitter Holding Register. The data will then be transferred to the Transmit Shift Register together with a start bit and parity and stop bits as determined by the Line Control Register. The bits to be transmitted are then clocked out of the transmit shift register by the transmit clock (NBAUD) which comes from the baud rate generator.

If enabled, an interrupt will be generated when the Transmitter Holding Register becomes empty.

Data is clocked into the receiver by the receive clock (RCLK). The receive clock should be 16 times the baud rate of the received data. A filter is used to remove spurious inputs which last for less than two periods of RCLK. When the complete word has been clocked into the receiver the data bits are transferred to the Receiver Buffer Register to be read by the CPU. The receiver also checks for a stop bit and for correct parity as determined by the Line Control Register.

If enabled, an interrupt will be generated when the data has been transferred to the Receiver Buffer Register. Interrupts can also be generated for incorrect parity or a missing stop bit (frame error).

The output modem control lines; NRTS, NDTR, NOUT1 and NOUT2 can be set or cleared by writing to the Modem Control Register. The current status of the input modem control line; NDCD, NRI, NDSR and NCTS can be read from the Modem Status Register. Bit 2 of this register will be set if the NRI modem status line has changed from low to high since the register was last read.

If enabled, an interrupt will be generated when NDSR, NCTS, NRI or NCD are asserted.

A per-use fee is associated with this megacell. Contact the factory for more information.

M6402
UART

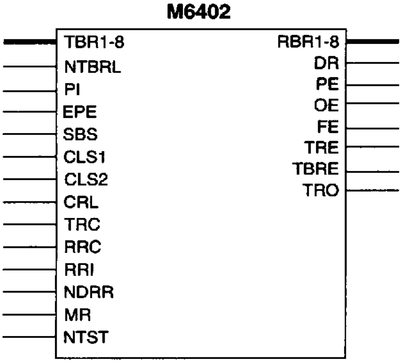
AMI
AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Features

- AMI's implementation of 3Soft's MegaMacro®
- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Programmable word length, stop bits and parity
- Double-buffered receiver and transmitter
- Overrun, parity and framing error detection
- Equivalent gates:
  Standard Cell - 580; Gate Array - 750

LOGIC SYMBOL



Description

The M6402 is a full–duplex universal asynchronous receiver/transmitter (UART). It supports word lengths from five to eight bits, an optional parity bit and one or two stop bits. It can detect overrun, parity and framing errors in the received character.

The M6402 differs from the M8868A in that the master reset clears the TRE output to "0" and does not initialize the receive buffer.

A per-use fee is associated with this megacell. Contact the factory for more information.

AMI
AMERICAN MICROSYSTEMS, INC.

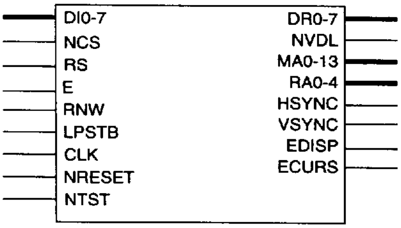
M6845
CRT Controller

Features

- AMI's implementation of 3Soft's MegaMacro®
- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Alphanumeric, semi-graphic and full-graphic capability
- Alphanumeric screen formats of up to 16K characters
- Programmable horizontal and vertical sync pulses
- Programmable cursor format and blink rate
- Light pen register
- Interlaced or non-interlaced scan modes
- Equivalent gates:
  Standard Cell - 2,100; Gate Array - 2,700

LOGIC SYMBOL

M6845



Description

The M6845 is a highly programmable controller designed to generate the timing and control signals necessary to meet a wide range of CRT (Cathode Ray Tube) based video controllers. It is programmed by an 8-bit CPU interface. It can address a character memory of up to 16K, which can represent one or more pages of characters. It can provide hardware scrolling through pages in multiple page setups. The position and width of the horizontal and vertical sync pulses are fully programmable, as is the size location and blink rate of the cursor.

The horizontal counter is clocked by the CLK input and counts from 0 up to the value stored in the Horizontal Total register. The counter output is used by the horizontal sync block to generate the HSYNC pulse, as defined by the Horizontal Sync. Position and Sync. Width registers, and by the display address generator block to produce the character memory address.

The raster counter is incremented by the horizontal counter and is used to count scan lines. The output is available on the row address lines (RA0-4).

The vertical counter is incremented by the raster counter and is used to count character lines. The output is used by the vertical sync block to generate the VSYNC pulse, as defined by the Vertical Sync. Position and Sync. Width registers, and by the display address generator block to produce the display memory address.

The frame counter is incremented by the vertical counter and is used to count display frames. The output is used by the cursor control block to blink the cursor at a rate determined by register 10.

By using both the display memory address and the row address an address space of 512K is available for use in graphic displays.

Addresses are provided during retrace to provide refresh for dynamic RAMs.

The light pen register will latch the display memory address when the LPSTB line goes high.

A per-use fee is associated with this megacell. Contact the factory for more information.

M765A
Floppy Disk Controller

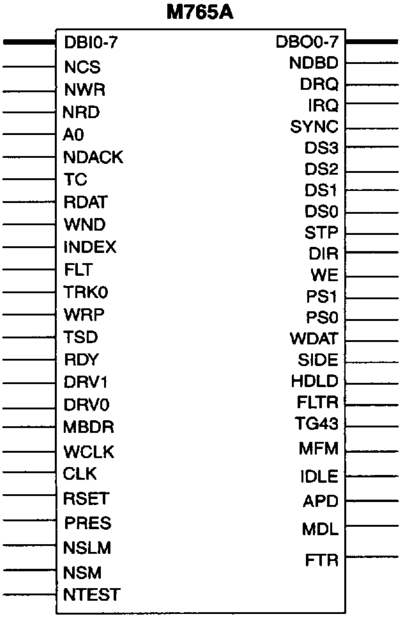
AMI
AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Features

- AMI's implementation of 3Soft's MegaMacro®
- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- IBM System 3740 format
- IBM System 34 format perpendicular recording format Data rates up to 1.25 Mbps
- Directly addresses 256 tracks
- 255 step recalibrate command
- Programmable write precompensation
- 16 byte FIFO
- Equivalent gates:
  Standard Cell - 7,100; Gate Array - 9,300

LOGIC SYMBOL



Description

The M765A is a floppy disk controller which also supports tape drives. This microcode-free design is compatible with industry standard discrete devices. It supports IBM System 3740 (FM), IBM System 34 (MFM), Perpendicular 500K BPS and Perpendicular 1M BPS formats. It supports 4 Mb floppy drives and is capable of data rates up to 1.25 Mbps. It provides drive select and motor signals, and supports drives with tunnel erase heads. It has programmable write precompensation and a 16 byte data FIFO. It can directly address 256 tracks and has the ability to access an unlimited number. The recalibrate command can step 255 tracks.

The M765A can be connected to a M91C360, or similar, data separator to form a complete floppy disk controller.

A per-use fee is associated with this megacell. Contact the factory for more information.

AMI
AMERICAN MICROSYSTEMS, INC.

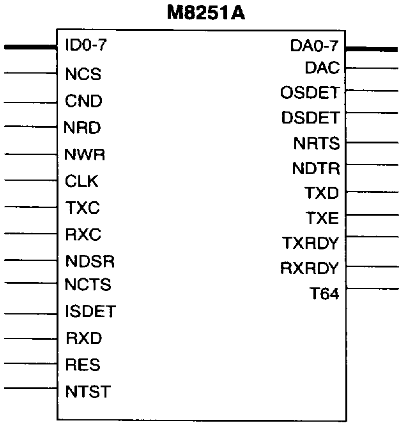
M8251A
Serial Communication Interface

Digital Soft Megacells

Features

- AMI's implementation of 3Soft's MegaMacro®
- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Synchronous and asynchronous operation
- Full duplex, double buffered transmitter and receiver
- Internal or external character synchronization
- 1X, 16X and 64X clock modes
- Framing, parity and overrun error detection
- Equivalent gates:
  Standard Cell - 1,500; Gate Array - 2,000

LOGIC SYMBOL



Description

The M8251A is a universal synchronous/asynchronous receiver/transmitter (USART) communications interface. It supports asynchronous communications with five to eight data bits, parity and one, one and a half, or two stop bits. It can provide automatic break detection. It supports synchronous communications with one or two SYNC characters, with internal or external SYNC detection. Both the transmit and receive data paths are double buffered. It has four modem control lines.

The M8251A is fully programmable by an 8-bit CPU interface.

The operating mode of the M8251A is programmed by writing to the mode control registers and SYNC registers, using the 8-bit CPU interface. Transmission can then begin by writing to the transmit buffer. Data is clocked out of the transmitter by the transmit clock (TXC), which can be 1, 16 or 64 times the baud rate. The data stream is clocked into the receiver by the receive clock (RXC), which can be 1, 16 or 64 times the baud rate. In synchronous mode character reception will not begin until the SYNC character, or characters, are detected. When each character has been received it is transferred to the receive buffer to be read by the CPU interface.

The M8251A has output signals to indicate when the transmit buffer is empty (TXRDY), when the receive buffer is full (RXRDY) and when the SYNC characters have been detected (OSDET, DSDET). Two input (NDSR, NCTS) and two output (NRTS, NDTR) modem control signals are also provided. A further input (ISDET) is provided for use with an external SYNC detector.

A per-use fee is associated with this megacell. Contact the factory for more information.

M8253
Programmable Interval Timer

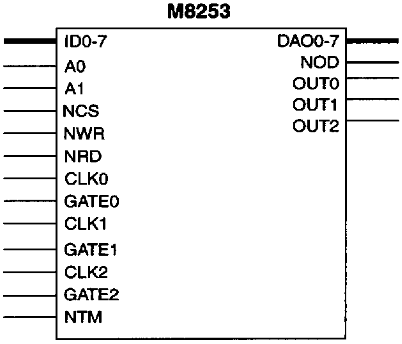
AMI
AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Features

- AMI's implementation of 3Soft's MegaMacro®
- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Three independent 16-bit counters
- Binary or BCD counting
- Six counter modes
- Equivalent gates:
  Standard Cell - 2,500; Gate Array - 3,250

LOGIC SYMBOL



Description

The M8253 contains three independent 16-bit timer/counters that can be programmed over a common 8-bit CPU interface. It can be used for timing external events, producing fixed delays or producing repetitive waveforms. The current value of each of the counters can be latched and read back over the CPU interface.

A per-use fee is associated with this megacell. Contact the factory for more information.

AMI
AMERICAN MICROSYSTEMS, INC.

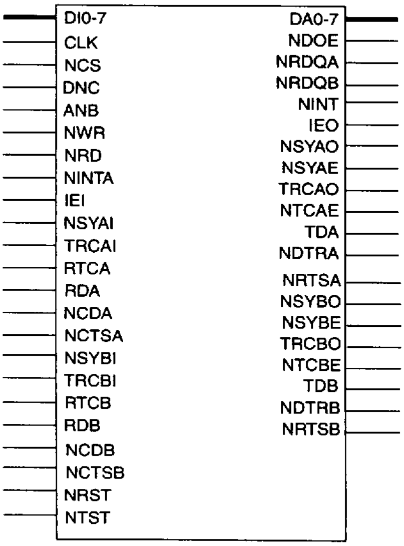
M82530
Serial Communications Controller

Features

- AMI's implementation of 3Soft's MegaMacro®
- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Asynchronous and synchronous modes
- MONOSYNC, BISYNC and SDLC supported
- SDLC loop-mode supported
- NRZ, NRZI and FM encoding/decoding
- Two independent full-duplex channels
- Digital phase-locked loop for each channel
- Baud rate generator for each channel
- Local loop-back and automatic echo modes
- Equivalent gates:
  Standard Cell - 9,400; Gate Array - 12,200

LOGIC SYMBOL

M82530



Description

The M82530 serial communications controller has two independent full-duplex channels which support asynchronous, bit synchronous (SDLC, HDLC and SDLC loop mode) and byte synchronous (MONOSYNC, BISYNC) communication modes. NRZ, NRZI and FM data encoding/decoding are supported. The M82530 includes a baud rate generator and a digital phase-locked loop for each channel. Two diagnostic modes: local loopback and automatic echo are available. The M82530 is fully programmable by an 8-bit system interface, which includes a six source interrupt controller. The interrupt controller has external signals that allow it to be daisy-chained with other interrupt controllers.

Each of the two identical channels in the M82530 contain a transmitter, a receiver, a baud rate generator, a digital phase-locked loop and a clock selector. The clock selector provides the clocks for the transmitter and the receiver blocks. The clocks can be programmed to come from one of two external clocks, from the baud rate generator, or derived from the receiver data stream by the phase-locked loop. In addition to the two serial communication channels there is a common 8-bit system interface and a six source interrupt controller.

The transmitter has a transmit shift register into which data to be transmitted is loaded. This data is loaded from the transmit buffer, sync characters and flags are loaded automatically from the sync registers. In SDLC mode a zero insertion block will insert zeros into long strings of ones. A CRC generator produces a CRC check word for appending to message blocks. The output data stream then passes to a data encoder block which can produce NRZ, NRZI or FM encoded formats. The final output selector allows the output to come from the receiver in diagnostic or loop modes.

The receiver input selector allows the received data stream to come from the transmitter in diagnostic modes or through a 1-bit delay, which is required in SDLC loop mode. The input stream then passes to a decoder to convert it into NRZ format. The data stream then goes into the receive data shift register. The receive data shift register can be extended to 16-bits for detecting 16-bit sync characters, and can automatically delete the extra zeros that were inserted into the data stream in SDLC mode. A CRC checker can be used in synchronous modes. The received data characters are transfered to the receive data FIFO and parity, frame or CRC errors are transfered to the receive error FIFO.

A per-use fee is associated with this megacell. Contact the factory for more information.

MG82C37A
Programmable DMA Controller

AMERICAN MICROSYSTEMS, INC.

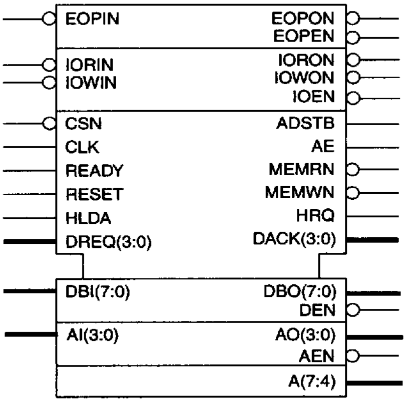
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell featuring functional compatibility with the industry standard 8237/8237A
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- Compatible with 8080/85, 8086/88, 80286/386 and 68000 µP families
- Four independent maskable DMA channels with autoinitialize capability
- Memory-to-memory transfer
- Fixed or rotating DMA request priority
- Independent polarity control for DREQ and DACK signals
- Address increment or decrement selection
- Cascadable to any number of channels

LOGIC SYMBOL

MG82C37A



Description

The MG82C37A is a high-performance, programmable Direct Memory Access (DMA) controller offering functional compatibility with the industry standard 8237/8237A. It features four channels, each independently programmable, and is cascadable to any number of channels. Each channel can be programmed to autoinitialize following DMA termination.

In addition, the MG82C37A supports both memory-to-memory transfer capability and memory block initialization, as well as a programmable transfer mode.

The MG82C37A is designed to improve system performance by allowing external devices to transfer data directly with system memory. High speed and very low-power consumption make it an ideal component for aerospace and defense applications. The low-power consumption also makes it an attractive addition in portable systems or systems with low-power standby modes.

The MG82C37A DMA controller is a state-driven address and control signal generator designed to accelerate data transfer in systems by moving data from an I/O device to memory, or memory to an I/O device. Data transfers are direct, rather than being stored enroute in a temporary register.

The MG82C37A also mediates memory-to-memory block transfers and will move data from a single location to a memory block. Temporary storage of data is required, but the transfer rate is significantly faster than CPU processes. The device provides operating modes to carry out both single byte and block transfers of data.

The organization of the MG82C37A is composed of three logic blocks, a series of internal registers and a counter section. The logic blocks include the Timing Control, Command Control and Priority Encoder circuits.

The Timing Control block generates internal timing signals from the clock input and produces external control signals.

Command Control decodes incoming instructions from the CPU, and the Priority Encoder block regulates DMA channel priority.

The internal registers hold internal states and instructions from the CPU. Addresses and word counts are computed in the counter section.

Soft Megacells

This soft megacell is in the ASIC Standard Library which is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

AMI
AMERICAN MICROSYSTEMS, INC.

MG82C37A
Programmable DMA Controller

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
AI(3:0)	I	Input address bus. During Idle Cycle, addresses which control register to be loaded or read.
AO(3:0)	O	Low output address bus. During active Cycle, lower 4 bits of the transfer address.
AEN	O	Control line used to determine when AO(3:0) and A(7:4) is valid. Active low.
A(7:4)	O	High Address Bus. During active Cycle, upper 4 bits of the transfer address.
ADSTB	O	Address Strobe. Controls latching of the upper address byte.
AE	O	Address Enable. Enables the higher order address byte onto the system address bus.
CLK	I	Clock Input. May be stopped for standby operation.
CSN	I	Chip Select, active low.
DACK(3:0)	O	DMA Acknowledge. Informs a peripheral that the requested DMA transfer has been granted.
DBI(7:0)	I	Data Bus input ports.
DBO(7:0)	O	Data Bus output ports.
DEN	O	Control line, active low. Used to determine when DBO(7:0) is valid.
DREQ(3:0)	I	DMA Request. DMA service is requested by activation of the channel from a specific device.
EOPIN	I	End of Process, active low. Force termination of DMA.
EOPON	O	Indicates when DMA is finished.
EOPEN	O	Control line used to determine when EOPON is valid. Active low.
HLDA	I	Hold Acknowledge. Indicates the CPU has released control of the system buses.
HRQ	O	Hold Request. Requests control of the system buses. HRQ is issued following a request for DMA service (DREQ) from a peripheral, and is acknowledged by the HLDA signal.
IORIN IORON	I O	I/O Read, active low. Idle Cycle: CPU input control signal for reading the Control Registers. Active Cycle: Output control signal to read data from a peripheral device during a DMA cycle.
IOWIN IOWON	I O	I/O Write, active low. Idle Cycle: CPU input control signal for loading the control registers. Active Cycle: Output control signal to load data to a peripheral device during a DMA cycle.
IOEN	O	Control line active low. Indicates when IORON, IOWON, MEMRN and MEMWN are valid.
MEMRN	O	Memory Read, active low. MG82C37A reads data from a selected memory address during a DMA Read or Memory-to-Memory transfer. Valid when IOEN is low.
MEMWN	O	Memory Write, active low. MG82C37A writes data to a selected memory address during a DMA Write or Memory-to-Memory transfer. Valid when IOEN is low.
READY	I	Extends the Memory Read and Write pulse widths to accommodate slow I/O peripherals.
RESET	I	Reset. Asynchronous signal clears internal registers and puts the MG82C37A in Idle Cycle.

Equivalent Gates

STANDARD CELL	GATE ARRAY
3,000	3,800

MG82C50A
Async. Communication Element

AMERICAN MICROSYSTEMS, INC.

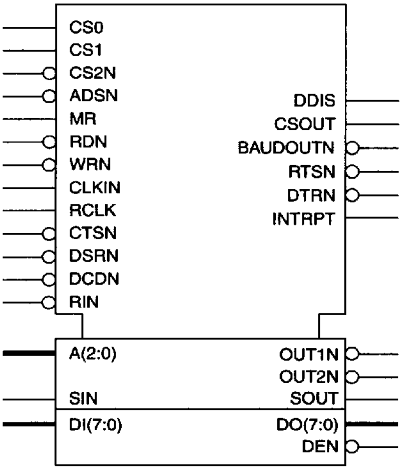
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell featuring functional compatibility with the industry standard 8250
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- Single megacell UART/BRG
- On chip baud rate generator 1 to 65535 Divisor generates the BAUDOUTN (16x) clock
- Prioritized interrupt mode
- Microprocessor bus oriented interface
- Modem interface
- Line break generation and detection
- Loopback mode
- Double buffered transmitter and receiver

LOGIC SYMBOL

MG82C50



Description

The MG82C50A Asynchronous Communications Element (ACE) is a high-performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single megacell. The device supports data rate from DC to 625K baud (0-10MHz clock). It is functionally compatible with the industry standard 8250.

The ACE receiver circuitry converts start, data, stop and parity bits into a parallel data word. The transmitter circuitry converts a parallel data word into serial form and appends the start, parity and stop bits. The word length is programmable to 5, 6, 7 or 8 data bits. Stop bit selection provides a choice of 1, 1.5 or 2 stop bits.

The Baud Rate Generator divides the clock frequency by a divisor programmable from 1 to 2^{16}-1 to provide standard RS-232C baud rates. The BAUDOUT programmable clock output provides a buffered oscillator or a 16x (16 times the data rate) baud rate clock for general purpose system use.

To meet the system requirements of a CPU interfacing to an asynchronous channel, the modem control signals RTSN, CTSN, DSRN, RIN, DCDN are provided.

Soft Megacells

This soft megacell is in the ASIC Standard Library which is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

AMI
AMERICAN MICROSYSTEMS, INC.

MG82C50A
Async. Communication Element

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
RDN	I	Read, active low. Causes the register selected by A(2:0) to be output to D(7:0).
WRN	I	Write, active low. Causes data from the data bus D(7:0) to be input to the MG82C50A.
DI(7:0) DO(7:0)	I O	Data Bus inputs and outputs, DI(0) and DO(0) are the LSBs.
DEN	O	Control line used to determine when DO(7:0) is valid. Active low.
A(2:0)	I	Register Select. Selects the internal registers during CPU bus operations. A(0) is the LSB.
CLKIN	I	Clock in. Clock connection for the internal Baud Rate Generator.
SOUT	O	Serial Data Output. Serial data output from the MG82C50A transmitter circuitry.
CTSN	I	Clear to Send, active low. Indicates that data on SOUT can be transmitted.
DSRN	I	Data Set Ready, active low. Indicates the modem is ready to exchange data.
DTRN	O	Data Terminal Ready, active low. Indicates to that the MG82C50A is ready to receive data.
RTSN	O	Request to Send, active low. Indicates data is ready to transmit. In half duplex operations, RTS is used to control the direction of the line.
BAUDOUTN	O	Baud out clock. Rate is the CLKIN frequency divided by the specified divisor in the BSR.
OUT1N,OUT2N	O	Outputs 1and 2, active low. Asserted by setting MCR(2,3) high. Inactive during loop mode.
RIN	I	Ring Indicator, active low. Indicates that a telephone ringing signal has been received by the modem or data set.
DCDN	I	Data Carrier Detect, active low. Indicates that the data carrier has been detected by the modem or data set.
MR	I	Master Reset. Forces the MG82C50A into an idle mode.
INTRPT	O	Interrupt Request. Goes active when an interrupt has occurred if enabled by the IER.
SIN	I	Serial Data Input. Serial data input from the communication line or modem to the MG82C50A receiver circuits. Disabled when operating in the loop mode.
CS0,CS1,CS2N	I	Chip Selects. Enables WRN and RDN. Latched by the ADSN input.
CSOUT	O	Chip Select Out. Indicates the megacell has been selected by active CS0, CS1 and CS2N.
DDIS	O	Driver Disable. Used to disable an external transceiver when the CPU is reading data.
ADSN	I	Address Strobe, active low. Latches A(2:0) and CS0, CS1 and CS2N inputs.
RCLK	I	Baud Rate Clock. This input is the 16x Baud Rate Clock for the receiver section of the MG82C50A. This input may be provided from the BAUDOUT output or an external clock.

Equivalent Gates

STANDARD CELL	GATE ARRRAY
2,000	2,500

MG82C54
Programmable Interval Timer

AMERICAN MICROSYSTEMS, INC.

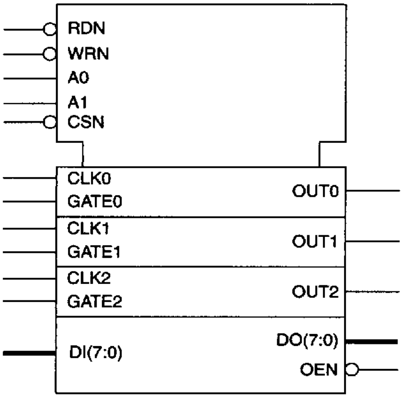
Digital Soft Megacells

Features

- A high-performance, low-power megacell featuring functional compatibility with the industry standard 8254
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- Available in several AMI process technologies
- Three independent 16-Bit counters
- Six programmable counter modes
- Status read-back command
- Binary or BCD counting

LOGIC SYMBOL

MG82C54



Description

The MG82C54 is a counter/timer megacell that includes complete functional compatibility with the industry standard 8254. Designed for fast operation, it has three independently programmable 16-bit counters and six programmable counter modes. Counting can be performed in both binary and BCD formats. Speed will depend on what AMI process technology is chosen.

The MG82C54 offers a very flexible, hardware solution to the generation of accurate time delays in microprocessor systems. A general purpose, multi-timing element, it can be used to implement event counters, elapsed time indicators, waveform generators plus a host of other functions.

Major functional blocks include read/write logic, control word register, and three programmable counters.

The read/write logic block generates internal control signals for the different functional blocks using address and control information obtained from the system. The active LOW signals, CSN, RDN and WRN are used to select the MG82C54 for operation, read a counter, and write to a counter (or the control word register) respectively. CSN must be LOW for RDN or WRN to be recognized.

The inputs A0 and A1are used to select the control word register, or one of the three counters that is to be written to or read from. A0 and A1 connect directly to the corresponding signals of the microprocessor address bus, while CS is derived from the address bus using either a linear select method, or an address decoder device.

The MG82C54 has a control word register which is a write only register. It is selected by the read/write logic block when A0 and A1=1. When CSN and WRN are LOW, data are written into the MG82C54 control word register. Control word data are interpreted as a number of different commands which are used to program the various device functions. For example, status information is available with the Read-Back Command.

The MG82C54 contains three identical, independent counter blocks. Each counter provides the same functions, but can be programmed to operate in different modes relative to each other. A typical counter contains the following functional elements: control logic, counter, output latches, count registers and status register.

The low-power consumption of the MG82C54 makes it ideally suited to portable systems or those with low-power standby modes.

Soft Megacells

This soft megacell is in the ASIC Standard Library which is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MG82C54
Programmable Interval Timer

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
A1,A0	I	Address. Used to select the Control Word Register (for read or write operations), or one of the three Counters. Normally connected to the system address bus.
CLK0	I	Clock input of counter 0.
CLK1	I	Clock input of counter 1.
CLK2	I	Clock input of counter 2.
CSN	I	Chip select, active low. Enables the MG82C54 to respond to RDN and WRN signals.
DI(7:0)	I	Input data bus.
DO(7:0)	O	Output data bus.
OEN	O	Output enable, active low. Output is low when valid output data is on DO bus.
GATE0	I	Gate input of counter 0.
GATE1	I	Gate input of counter 1.
GATE2	I	Gate input of counter 2.
OUT0	O	Output of counter 0.
OUT1	O	Output of counter 1.
OUT2	O	Output of counter 2.
RDN	I	Read Control, active low. Used to enable the MG82C54 for read operations by the CPU.
WRN	I	Write Control, active low. Used to enable the MG82C54 to be written to by the CPU.

Equivalent Gates

STANDARD CELL	GATE ARRAY
2,150	2,800

MG82C55A
Programmable Peripheral Interface

AMI AMERICAN MICROSYSTEMS, INC.

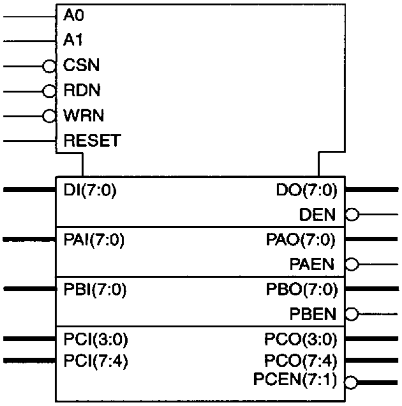
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell featuring functional compatibility with the industry standard 8255A
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- Supports 8086/8088 and 80186/188 microprocessors
- 24 programmable I/O pins
- Direct bit set/reset capability
- Bidirectional bus operation
- Enhanced control word read capability

LOGIC SYMBOL

MG82C55A



Description

The MG82C55A Programmable Peripheral Interface is a high speed, low power CMOS megacell offering functional compatibility with the industry standard 8255A. It is a general purpose I/O component which interfaces peripheral equipment to the microcomputer system bus usually without extra logic.

The MG82C55A has 24 I/O lines grouped as three 8-bit ports (A,B and C), in two control groups (A and B). Group A consists of port A and port C upper (7:4), while group B consists of port B and port C lower (3:0). Group A has three operating modes, (0,1,2) while group B has two (0,1). The operating modes are:

Mode 0: One 8-bit and one 4-bit uni-directional port, without handshaking.

Mode 1: One 8-bit uni-directional port with handshaking.

Mode 2: One 8-bit bi-directional port with handshaking.

For any modes other than mode 0, lines from port C are used as handshaking lines for ports A and B. Port A has latched inputs and latched outputs while ports B and C have unlatched inputs and latched outputs.

The system CPU has full access to the MG82C55A's control register which completely controls the megacell's configuration. When the control word register is read bit D7 will always be a logic ONE to indicate control word mode information.

Soft Megacells

This soft megacell is in the ASIC Standard Library which is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

AMERICAN MICROSYSTEMS, INC.

MG82C55A
Programmable Peripheral Interface

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
A1,A0	I	Address. These input signals, in conjunction with RDN and WRN, control the selection of one of the three ports or the control word registers.
CSN	I	Chip Select, active low. Enables the MG82C55A to respond to RDN and WRN signals. RDN and WRN are ignored otherwise.
DI(7:0) DO(7:0)	I O	Data Bus.
DEN	O	Control line, active low. Used to determine when DBO(7:0) is valid.
PAI(7:0) PAO(7:0)	I O	Port A. An 8-bit data output latch and an 8-bit data input buffer.
PAEN	O	Control line, active low. Used to determine when PAO(7:0) is valid.
PBI(7:0) PBO(7:0)	I O	Port B. An 8-bit data output latch and an 8-bit data input buffer.
PBEN	O	Control line, active low. Used to determine when PBO(7:0) is valid.
PCI(3:0) PCO(3:0)	I O	Port C, Pins (3:0). Lower nibble of an 8-bit data output latch and an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.
PCI(7:4) PCO(7:4)	I O	Port C, Pins(7:4). Upper nibble of Port C.
PCEN(7:1)	O	Control line, active low. Used to determine when PCO(7:0) is valid. PCEN(1) controls PCO(1:0).
RESET	I	Reset. A high on this input clears the control register and all ports are set to the input mode.
RDN	I	Read Control, active low. This input is low during CPU read operations.
WRN	I	Write Control, active low. This input is low during CPU write operations.

Megacells

Equivalent Gates

STANDARD CELL	GATE ARRAY
700	900

MG82C59A
Programmable Interrupt Controller

AMI AMERICAN MICROSYSTEMS, INC.

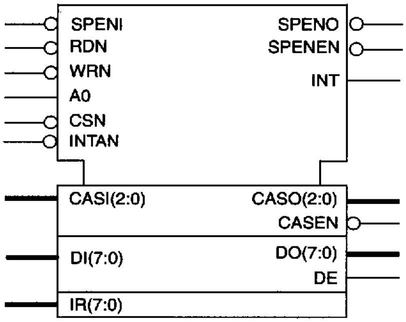
Digital Soft Megacells

Features

- A high-performance, low-power megacell featuring functional compatibility with the industry standard 8259/8259A
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- Eight level priority controller
- Expandable to 64 levels
- Programmable interrupt modes, with each interrupt maskable
- Edge- or level-triggered interrupt request inputs
- Polling operation

LOGIC SYMBOL

MG82C59A



Description

The MG82C59A is a high-performance, completely programmable interrupt controller. It can process eight interrupt request inputs, assigning a priority level to each one, and is cascadable up to 64 interrupt requests. Individual interrupting sources are maskable. Its two modes of operation (Call and Vector) allow it to be used with virtually all 8000 and 80000 type processors, as well as with 68000 family microprocessors.

Acting as an overall peripherals manager, its functions include:

- Accepting interrupt requests from assorted peripheral devices
- Determining which is the highest priority
- Establishing whether or not the new interrupt is of a higher priority than any interrupts which might be currently being serviced, and if so,
- Issuing an interrupt to the CPU
- Then providing the CPU with the interrupt service routine address of the interrupting peripheral

Each peripheral device usually has a specific interrupt service routine which is particular to its operational or functional requirements within the system. The MG82C59A can be programmed to hold a pointer to the service routine addresses associated with each of the peripheral devices under its control. Thus when a peripheral interrupt is passed through to the CPU, the MG82C59A can set the CPU Program Counter to the interrupt service routine required. These pointers (or vectors) are addresses in a vector table.

The MG82C59A is intended to run in one of two major operational modes, according to the type of CPU being used in the system. The CALL Mode is used for 8085 type microprocessor systems, while the VECTOR Mode is reserved for those systems using more sophisticated processors such as the 8088/86, 80286/386 or 68000 family.

In either mode, the MG82C59A can manage up to eight interrupt request levels individually, with a maximum capability of up to 64 interrupt request levels when cascaded with other MG82C59As. A selection of priority modes is also available such that interrupt requests can be processed in a number of different ways to meet the requirements of a variety of system configurations.

Priority modes can be changed or reconfigured dynamically at any time during system operation using the operation command words (OCWs), allowing the overall interrupt structure to be defined for a complete system. Note that the MG82C59A is programmed by the system software as an I/O peripheral.

The MG82C59A's high-performance and very low-power consumption makes it useful in portable systems and systems with low-power standby modes.

Soft Megacells

This soft megacell is in the ASIC Standard Library which is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MG82C59A
Programmable Interrupt Controller

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
A0	I	A0 Address Line. Acts in conjunction with the CSN, WRN and RDN signals. It is used to decipher various command words written by the CPU, and Status information read by the CPU. It is typically connected to the CPU - A0 address line.
CSN	I	Chip Select, active low. Used to enable RDN and WRN communication between the CPU and the MG82C59A. Note that INTAN functions are independent of CSN.
INTAN	I	Interrupt Acknowledge. Signal used to enable the MG82C59A interrupt vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
WRN	I	Write, active low. Used to enable the MG82C59A to accept command words from the CPU, when CSN is LOW.
RDN	I	Read, active low. Used to enable the MG82C59A to output status information onto the data bus for the CPU, when CS is LOW.
IR(7:0)	I	Interrupt Requests. Asynchronous input signals, an interrupt request is executed by raising an IR input, and holding it HIGH until it is acknowledged (Edge Triggered Mode), or just by a HIGH level on an IR input (Level Triggered Mode).
CASI(2:0) CASO(2:0)	I O	Cascade Lines. The CAS lines are used as a private bus by a MG82C59A master to control multiple MG82C59A slaves. The master uses only CASO(2:0). The slaves use CASI(2:0).
CASEN	O	Control line used to determine when CASO(2:0) is valid. Active low.
SPENI SPENO	I O	Slave Program/Enable Buffer. Dual function control signal. When in the Buffered Mode, SPENO is used to control buffer transceivers. When not in the Buffered Mode, SPENI is used to designate a master (SP = 1) or a slave (SP = 0).
SPENEN	O	Control line used to determine when SPENO is valid. Active low.
DI(7:0) DO(7:0)	I O	Data Bus. 8-Bit data bus for the transfer of control, status and interrupt vector information.
DE	O	Control line used to determine when DO(7:0) is valid. Active high.
INT	O	Interrupt. This signal goes HIGH when a valid interrupt request is asserted.

Equivalent Gates

STANDARD CELL	GATE ARRAY
1,450	2,000

M8490
SCSI Controller

AMI AMERICAN MICROSYSTEMS, INC.

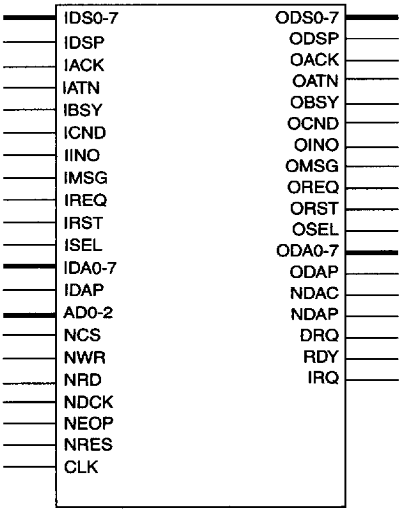
Digital Soft Megacells

Features

- AMI's implementation of 3Soft's MegaMacro®
- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Compatible with ANSI SCSI-II
- Initiator or target mode
- Provides arbitration and bus clear/free/settle delays
- Enhanced arbitration mode
- Generates 9 separate interrupts
- Compatible with 5380 SCSI controller
- Equivalent gates:
  Standard Cell - 1,200; Gate Array - 1,500

LOGIC SYMBOL

M8490



Description

The M8490 is a Small Computer Systems Interface (SCSI) controller. It can control 8-bit asynchronous communication over an ANSI SCSI-II bus. It has an 8-bit CPU interface through which the local processor can program it to act as initiator or target on the SCSI bus, and can control all phases of data transfers by writing to command registers within the M8490. It can generate up to 9 separate interrupts to signal to the local processor when commands have been completed or errors have occurred. Bus clear, free and settle delays, and optionally arbitration delays, can be generated automatically from an external clock. Signals are provided to allow data to be transferred to, and from, the M8490 by DMA.

The M8490 is 5380 compatible, applications currently using the 5380 controller should be able to use the M8490 with out software changes. The M8490 has additional features not found in the 5380 making it more attractive for new designs, these additional features are: CPU parity, programmable CPU and SCSI parity, loop back mode, enhanced arbitration and interrupt support.

The CPU interface block provides an 8-bit interface to the twelve internal registers that control the M8490. The registers control the operation of the SCSI bus controller, the DMA controller and the interrupt controller. The data transferred over the SCSI bus is also written and read by the CPU interface.

The DMA controller block provides an alternative means of writing data to the Output Data register, or reading data from the Input Data Register. When DMA is enabled the M8490 requests a DMA cycle by asserting DRQ high. When the request is acknowledged by asserting NDACK low then reads or writes will be directed to the IDS or ODS register respectively. A DMA transfer is terminated by asserting NEOP low during the last DMA transfer.

The interrupt controller can generate interrupts to signal the completion of a DMA transfer, the completion of arbitration, the selection of the M8490 or an error condition. The source of the interrupt can be found by reading the RPI register.

The SCSI controller block provides access to the SCSI bus. Internal timers are used to provide bus free, bus clear and bus settle delays, and to time the arbitration period.

A per-use fee is associated with this megacell. Contact the factory for more information.

AMERICAN MICROSYSTEMS, INC.

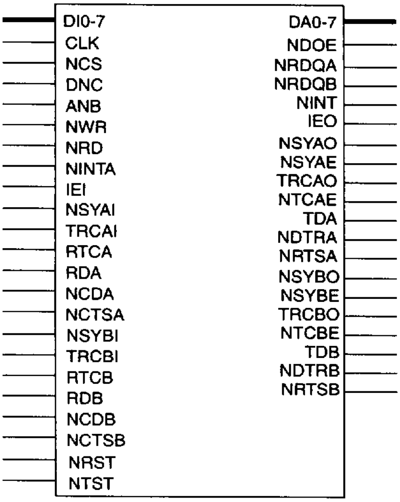
M85C30
Serial Communications Controller

Features

- AMI's implementation of 3Soft's MegaMacro®
- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Asynchronous and synchronous modes
- MONOSYNC, BISYNC and SDLC supported
- SDLC loop-mode supported
- NRZ, NRZI and FM encoding/decoding
- Two independent full-duplex channels
- Digital phase-locked loop for each channel
- Baud rate generator for each channel
- Local loop-back and automatic echo modes
- SDLC Frame counter and status FIFO
- Equivalent gates:
  Standard Cell - 12,700; Gate Array - 16,500

LOGIC SYMBOL

M85C30



Description

The M85C30 serial communications controller has two independent full-duplex channels which support asynchronous, bit synchronous (SDLC, HDLC and SDLC loop mode) and byte synchronous (MONOSYNC, BISYNC) communication modes. NRZ, NRZI and FM data encoding/decoding are supported.

It includes a baud rate generator and a digital phase-locked loop for each channel. Two diagnostic modes: local loopback and automatic echo are available. A character counter and a 10 X 19-bit frame status FIFO are available in SDLC mode.

The M85C30 is fully programmable by an 8-bit system interface, which includes a six source interrupt controller. The interrupt controller has external signals that allow it to be daisy-chained with other interrupt controllers.

A per-use fee is associated with this megacell. Contact the factory for more information.

M8868A
UART

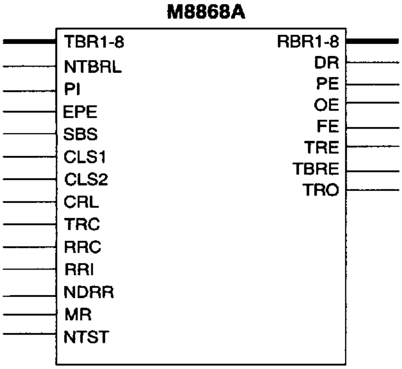
AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Features

- AMI's implementation of 3Soft's MegaMacro®
- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Programmable word length, stop bits and parity
- Double-buffered receiver and transmitter
- Overrun, parity and framing error detection
- Equivalent gates:
  Standard Cell - 600; Gate Array - 760

LOGIC SYMBOL



Description

The M8868A is a full-duplex universal asynchronous receiver/transmitter (UART). It supports word lengths from five to eight bits, an optional parity bit and one or two stop bits. It can detect overrun, parity and framing errors in the received character.

The M8868A differs from the M6402 in that the master reset sets the TRE output to "1" and clears the receive buffer.

A per-use fee is associated with this megacell. Contact the factory for more information.

AMI
AMERICAN MICROSYSTEMS, INC.

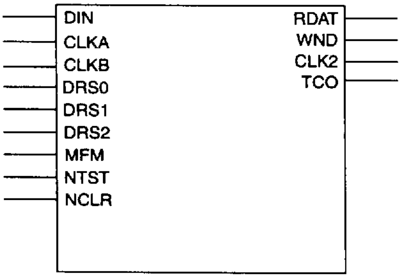
M91C36
Digital Data Separator

Features

- AMI's implementation of 3Soft's MegaMacro®
- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Data rates up to 1.25 Mbps
- 75% Jitter tolerance
- ±6.25% Frequency range
- Equivalent gates:
  Standard Cell - 800; Gate Array - 1,100

LOGIC SYMBOL

M91C36



Description

The M91C36 is a digital data separator for use with a floppy disk controller. It takes the "raw" FM or MFM data pulses from a disk drive and outputs a clock at the bit rate and data pulses synchronized to that clock. These signals can then go to a floppy disk controller, such as the MFDC, M765A or similar, for decoding. Three control lines, and the FM/MFM control line, together with a clock (typically 48 or 60 MHz) determine the data rate. This data rate can be up to 1.25 Mbps.

The M91C36 contains a clock selector block and a second order digital phase-locked loop which locks to the frequency and phase of the input data pulses.

The clock selector block produces an internal reference clock 16 times the cycle rate of the phase-locked loop (32 times the data rate). This internal reference clock determines the resolution to which the inputs and outputs are sampled, however the phase and frequency errors are calculated to a much higher resolution (12 bits and 8 bits respectively). This allows very high performance without using a very high clock speed.

The WND output is toggled at the end of every cycle of the phase-locked loop (twice per bit period). If a data pulse occurred at the DIN input during a cycle an active high pulse, lasting two periods of the internal reference clock and synchronized to WND, appears at the RDAT output.

Unlike an analogue data separator the performance of a digital data separator, such as the M91C36, is independent of the data rate. Its performance at 1.25 Mbps (with an internal clock of 40 MHz) is the same as its performance at 250 Kbps (with an internal clock of 8 MHz).

A per-use fee is associated with this megacell. Contact the factory for more information.

M91C360
Digital Data Separator

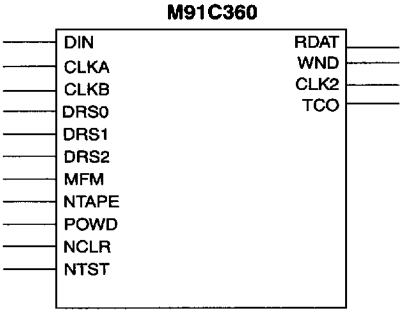
AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Features

- AMI's implementation of 3Soft's MegaMacro®
- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Data rates up to 1.25 Mbps
- Floppy disk or tape
- Power saving mode
- Equivalent gates:
  Standard Cell - 950; Gate Array - 1,250

LOGIC SYMBOL



Description

The M91C360 is a digital data separator for use with a floppy disk or tape controller. It takes the "raw" FM or MFM data pulses from a disk or tape drive and outputs a clock at the bit rate and data pulses synchronized to that clock. These signals can then go to a floppy disk controller, such as the MFDC, M765A or similar, for decoding.

Three control lines, and the FM/MFM control line, together with a clock (typically 48 or 60 MHz) determine the data rate. This data rate can be up to 1.25 Mbps.

The M91C360 can be configured for use with tape drives. This will increase the frequency range of the data separator at the cost of a slight reduction in jitter performance.

The M91C360 can be placed in a power-down mode which will stop the internal clock to reduce power when not in use.

The M91C360 contains a clock selector block and a second order digital phase-locked loop which locks to the frequency and phase of the input data pulses.

The clock selector block produces an internal reference clock 16 times the cycle rate of the phase-locked loop (32 times the data rate). This internal reference clock determines the resolution to which the inputs and outputs are sampled, however the phase and frequency errors are calculated to a much higher resolution (12 bits and 8 bits respectively). This allows very high performance without using a very high clock speed.

The WND output is toggled at the end of every cycle of the phase-locked loop (twice per bit period). If a data pulse occurred at the DIN input during a cycle an active high pulse, lasting two periods of the internal reference clock and synchronized to WND, appears at the RDAT output.

Unlike an analogue data separator the performance of a digital data separator, such as the M91C360, is independent of the data rate. Its performance at 1.25 Mbps (with an internal clock of 40 MHz) is the same as its performance at 250 Kbps (with an internal clock of 8 MHz).

A per-use fee is associated with this megacell. Contact the factory for more information.

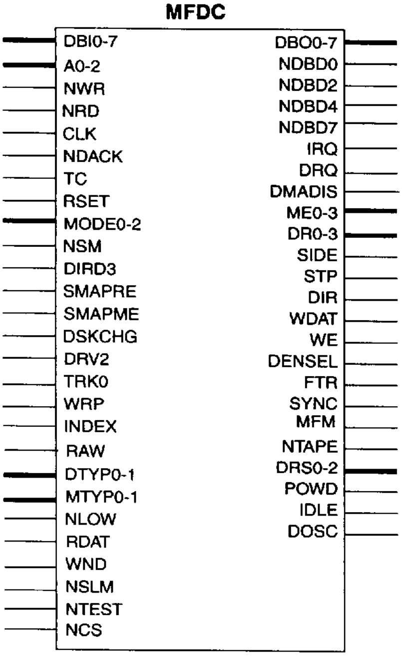
AMERICAN MICROSYSTEMS, INC.

MFDC
Floppy Disk Controller

Features

- AMI's implementation of 3Soft's MegaMacro®
- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- IBM System 3740 format
- IBM System 34 format
- Perpendicular recording format
- Data rates up to 1.25 Mbps
- Directly addresses 256 tracks
- 255 step recalibrate command
- Programmable write precompensation
- 16 byte FIFO
- Enhanced power-saving features
- Equivalent gates:
  Standard Cell - 8,100; Gate Array - 10,500

LOGIC SYMBOL



Description

The MFDC is a floppy disk controller which uses the M765A floppy disk controller core and includes the interface circuitry required in IBM PC compatible systems. It includes power saving features which are software compatible with the 82077SL. These include a clock disable signal, immediate auto-powerdown, low-latency awakening and a power-saving state for the write precompensator. The MFDC also contains multiplexers for swapping the default drive control outputs under software control.

The MFDC can be combined with the M91C360 digital data separator (or another data separator) to form a complete 82077SL compatible PC and PS/2™ floppy disk subsystem.

All references in this document to the 'core' or 'M765A' refer to the M765A Floppy Disk Controller that is incorporated in the MFDC net list.

PS/2™ is a trademark of IBM Corporation.

The MFDC uses the M765A core and provides additional interfacing logic for a PC compatible system. The additional blocks added to the M765A core are:

I/O BUFFERING. This block provides a PC compatible CPU interface and access to additional registers outside the M765Acore. The polarity of control signals can also be inverted by this block.

CLOCK GENERATOR. This block produces three clocks for the M765A core from the 24/30 MHz input clock to the MFDC. The frequency of the clocks to the M765A core are set by the data rate selected.

DRIVE MAPPING. This block controls the mapping of the logical drive numbers from the M765A core to the physical drive numbers coming from the MFDC.

WRITE PRECOMPENSATION. This block applies precompensation to the data stream coming from the M765A core. The amount of precompensation is determined by the delay period and data rate.

POWERDOWN CONTROLLER. This block can provide either direct or automatic powerdown which will stop internal clocks to save power.

A per-use fee is associated with this megacell. Contact the factory for more information.

MGI2CSL
I^{2}C Serial Bus Slave Transceiver

AMERICAN MICROSYSTEMS, INC.

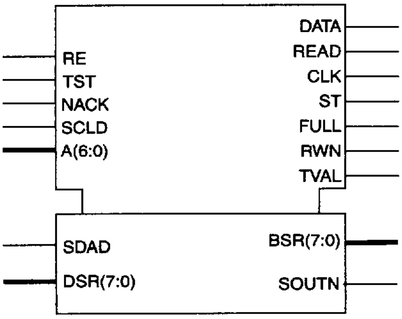
Digital Soft Megacells

Features

- Phillips licensed I^{2}C slave transceiver
- Supports normal (100kbit/s) and fast (400kbit/s) modes when used with appropriate pads
- Supports 7-bit addressing
- Schematic-based, uses the ASIC Standard Library for technology independence

LOGIC SYMBOL

MGI2CSL



Description

The MGI2CSL megacell implements an I^{2}C serial to 8-bit parallel bidirectional I/O port. The MGI2CSL is designed to provide I^{2}C bus handshaking and protocol support for a slave port. The seven bit port address is externally programmable from the A(6:0) bus. Port addresses are assigned by Phillips.

Received data is not latched. Received data is available on the BSR bus during the one clock cycle that FULL is HI. Data must be captured by the external logic during this time or it will be lost. FULL transitions on the falling edge of clock.

Because it is a minimal configuration it operates in slave mode only and does not support any of the following: clock stretching for slow peripherals, general call addressing, or ten-bit extended addressing. The MGI2CSL does support both normal (0 - 100kbit/s) and fast (0 - 400kbit/s) modes when used with appropriate pads. Contact the factory for pad selection and availability.

Phillips has represented to AMI that purchase of AMI's I^{2}C components conveys a license under the Phillips I^{2}C Patent Rights to use these components in an I^{2}C system. Provided that the system conforms to the I^{2}C Standard Specification as defined by Phillips.

Soft Megacells

This soft megacell is in the ASIC Standard Library which is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MGI2CSL

I²C Serial Bus Slave Transceiver

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
SCLD	I	Input from bus clock line.
SDAD	I	Input from bus data line.
RE	I	Reset, active high.
TST	I	Test mode, active high.
NACK	I	When high, suppresses transmission of acknowledge signal.
A(6:0)	I	Programs 7-bit address that the cell responds to. Address are assigned by Phillips.
DSR(7:0)	I	Parallel data input for serial out.
SOUTN	O	Serial data out to bus driver.
TVAL	O	Transmission valid. Goes high when port has received a valid address.
RWN	O	Status of read/write bit. Indicates whether master is reading or writing to this port. High indicates a read, a low indicates a write.
FULL	O	High indicates shift register full. BSR bus must be read before the next falling edge of CLK.
ST	O	High Indicates reception of start signal from bus or reset on RE.
CLK	O	Follows bus clock while transmission is valid.
READ	O	RWN delayed by one clock.
DATA	O	A high level indicates when in DATA mode. A low indicates ADDRESS mode.
BSR(7:0)	O	Parallel data out from serial in.

Equivalent Gates

STANDARD CELL	GATE ARRAY
210	250

MI2C
I^{2}C Bus Interface

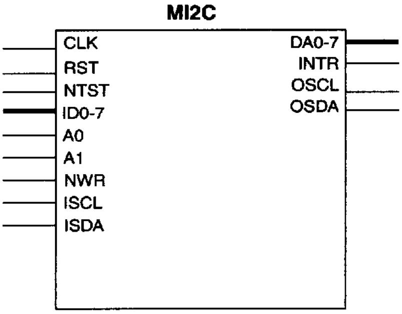
AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Features

- AMI's implementation of 3Soft's MegaMacro®
- Functionally compatible with the industry standard
- Uses AMI's ASIC Standard Library for technology independence
- Master or slave operation
- Multi-master systems supported
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Equivalent gates:
  Standard Cell - 1,200; Gate Array - 1,450

LOGIC SYMBOL



Description

The MI2C provides an interface between a microprocessor and an I^{2}C bus. It can operate in master or slave mode and performs arbitration in master mode to allow it to operate in multi-master systems. In slave mode it can interrupt the processor when it recognizes its own 7-bit address or the general call address. A clock divider is provided to allow operation from a wide range of input clock frequencies.

A per-use fee is associated with this megacell. Contact the factory for more information.

AMERICAN MICROSYSTEMS, INC.

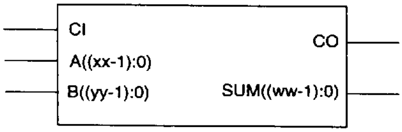
MGAxxyyDv
Adder

Features

- High-performance, Schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength for inputs A and B are user definable
- Selects multiple architectures for size and speed efficiency
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGAxxyyDv



Description

The MGAxxyyDv adder synthesizer builds xx-bit by yy-bit adders. Input operands are A and B with an input carry CI to produce the output SUM with a carry-out CO.

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead.

Inputs A and B and output SUM can be interpreted to be either in the two's complement or unsigned number format. The SUM output is the same format as the inputs; its size is the same as the largest of inputs A or B.

In the name, "xx" represents the A input size and "yy" represents the B input size. The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit by 20-bit adder optimized for minimum delay would be named MGA2420D2.

Functional Description

A	B	CI	SUM	CO
A	B	0	A + B	carry-out
A	B	1	A + B + 1	carry-out

Contact the factory for information on specific speeds and sizes or to have an Adder built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGAxxyyDv
Adder

AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
CI	Input	Carry in, active high.	1
A((xx-1):0)	Input	A Data inputs. A(0) is the LSB.	width > 0
B((yy-1):0)	Input	B Data inputs. B(0) is the LSB.	width > 0
CO	Output	Carry out, active high.	1
SUM((ww-1):0)	Output	SUM Data outputs. SUM(0) is the LSB.	width > 0

Sample Equivalent Gates

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGA0808D1	62	78	74	90
MGA0808D2	144	143	216	162
MGA1212D1	92	117	110	134
MGA1212D2	217	249	212	263

Sample Delays[1]

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGA0808D1	7.2 ns	5.9 ns	8.1 ns	5.27 ns
MGA0808D2	2.5 ns	2.15 ns	2.9 ns	2.17 ns
MGA1212D1	10.3 ns	8.39 ns	11.6 ns	7.54 ns
MGA1212D2	2.9 ns	2.43 ns	3.5 ns	2.37 ns

[1] These data are estimated and specified at 5.0V, Tj = 25°C and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage and temperature.

AMERICAN MICROSYSTEMS, INC.

MGAxxyyEv
Adder/Subtractor

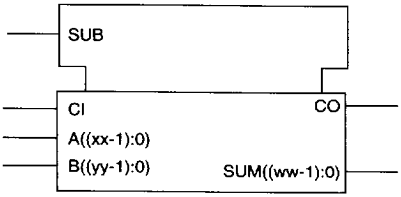
Digital Soft Megacells

Features

- High-performance, Schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength for inputs A and B are user definable
- Selects multiple architectures for size and speed efficiency
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGAxxyyEv



Description

The MGAxxyyEv adder/subtractor synthesizer builds xx-bit by yy-bit adder/subtractors. This megacell either adds (SUB=0) or subtracts (SUB=1) depending on the value of SUB. Input operands are A and B with an input carry CI and a subtract control line SUB. The outputs are SUM and carry-out CO.

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead.

Inputs A and B and output SUM can be interpreted to be either in the two's complement or unsigned number format. The SUM output is the same format as the inputs; its size is the same as the largest of inputs A or B.

In the name, "xx" represents the A input size and "yy" represents the B input size. The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit by 20-bit adder/subtractor optimized for minimum delay would be named MGS2420A2.

Functional Description

SUB	A	B	CI	SUM	CO
0	A	B	0	A + B	carry-out
0	A	B	1	A + B + 1	carry-out
1	A	B	0	A - B	carry-out
1	A	B	1	A - B - 1	carry-out

Contact the factory for information on specific speeds and sizes or to have an Adder/Subtractor built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology and process independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGAxxyyEv
Adder/Subtractor

AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
SUB	Input	Subtract control. Megacell subtracts when this input is high.	1
CI	Input	Carry in, active high.	1
A((xx-1):0)	Input	A Data inputs. A(0) is the LSB.	width > 0
B((yy-1):0)	Input	B Data inputs. B(0) is the LSB.	width > 0
CO	Output	Carry out, active high.	1
SUM((ww-1):0)	Output	SUM Data outputs. SUM(0) is the LSB.	width > 0

Sample Equivalent Gates

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGA0808E1	82	91	103	121
MGA0808E2	168	186	216	253
MGA1212E1	120	133	151	177
MGA1212E2	288	320	355	415

Sample Delays[1]

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGA0808E1	8.5 ns	7.0 ns	8.8 ns	6.2 ns
MGA0808E2	3.6 ns	3.0 ns	3.5 ns	2.5 ns
MGA1212E1	11.6 ns	9.5 ns	12.4 ns	8.7 ns
MGA1212E2	3.6 ns	3.0 ns	4.2 ns	2.9 ns

[1] These data are estimated and specified at 5.0V, Tj = 25°C and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage and temperature.

AMI
AMERICAN MICROSYSTEMS, INC.

MGBxxAv
Barrel/Arithmetic Shifter

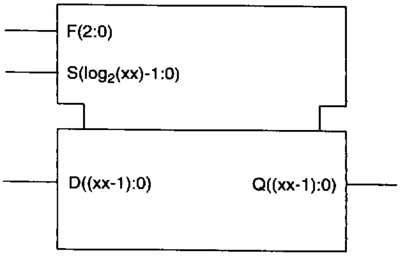
Digital Soft Megacells

Features

- Schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength is definable
- High-speed flash shift operations
- Logical and arithmetic shifts available

LOGIC SYMBOL

MGBxxAv



Description

The MGBxxAv barrel/arithmetic shifter synthesizer builds barrel/arithmetic shifters which provide various shift functions for a data word size of "xx" bits. The shifts are performed completely through combinational logic which allows for very fast operations. Commonly used logical and arithmetic shift functions are available.

The user has flexibility in specifying the word size. Within the name shown above, the "xx" represents the size of the data word. The size of the S bus is equal to log2(xx).

The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, an 8-bit shifter optimized for minimum gatecount would be named MGB08A1.

The S inputs select the number of bits to be shifted. For a right circular shift, the S inputs select the number of bits to be shifted. For a left circular shift, the two's compliment of the number of bits to be shifted is placed on the S inputs. In the case of an 8-bit shifter, for example, an input select value of two (010) operating on the input 00001100 will generate the output 00000011, a right shift of two bits. If S has the value of seven (111) the output would become 00011000, which would represent a right shift of seven or a left shift of one.

The type of shift function is controlled by the F inputs and are as described in the following table.

Shift Functions

F(2)	F(1)	F(0)	FUNCTION
0	0	0	Logic shift with zeros fill
0	0	1	Logic shift with ones fill
0	1	x	Arithmetic shift with sign extend
1	0	x	Logical shift with D0 fill
1	1	x	Left of Right circular shift

Sample Truth Tables(MGB04Av):

Logical shift with zeros fill, F(2:0) = 000

S(1:0)	Q(3)	Q(2)	Q(1)	Q(0)
00	D(3)	D(2)	D(1)	D(0)
01	0	D(3)	D(2)	D(1)
10	0	0	D(3)	D(2)
11	0	0	0	D(3)

Logical shift with ones fill, F(2:0) = 001

S(1:0)	Q(3)	Q(2)	Q(1)	Q(0)
00	D(3)	D(2)	D(1)	D(0)
01	1	D(3)	D(2)	D(1)
10	1	1	D(3)	D(2)
11	1	1	1	D(3)

Logical shift with D(0) fill, F(2:0) = 10x

S(1:0)	Q(3)	Q(2)	Q(1)	Q(0)
00	D(3)	D(2)	D(1)	D(0)
01	D(0)	D(3)	D(2)	D(1)
10	D(0)	D(0)	D(3)	D(2)
11	D(0)	D(0)	D(0)	D(3)

Arithmetic shift with sign extend, F(2:0) = 01x

S(1:0)	Q(3)	Q(2)	Q(1)	Q(0)
00	D(3)	D(2)	D(1)	D(0)
01	D(3)	D(3)	D(2)	D(1)
10	D(3)	D(3)	D(3)	D(2)
11	D(3)	D(3)	D(3)	D(3)

Left or Right circular shift, F(2:0) = 11x

S(1:0)	Q(3)	Q(2)	Q(1)	Q(0)
00	D(3)	D(2)	D(1)	D(0)
01	D(0)	D(3)	D(2)	D(1)
10	D(1)	D(0)	D(3)	D(2)
11	D(2)	D(1)	D(0)	D(3)

MGBxxAv
Barrel/Arithmetic Shifter

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Digital Soft Megacells

Pin Descriptions

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
F(2:0)	Input	Function inputs. These inputs determine the type of shift to be performed.	3
S($\log_2$(xx)-1:0)	Input	Shift inputs. Specifies the number of position to be shifted.	width = $\log_2$(xx)
D((xx-1):0)	Input	Data inputs. D(0) is the LSB.	width > 0
Q((xx-1):0)	Output	Data outputs. Q(0) is the LSB.	width > 0

Sample Equivalent Gates

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGB08A1	110	122	124	145
MGB08A2	133	148	156	183
MGB12A1	207	230	247	289
MGB12A2	250	278	304	356

Sample Delays[1]

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGB08A1	4.2 ns	3.4 ns	4.8 ns	3.4 ns
MGB08A2	3.6 ns	3.0 ns	4.0 ns	2.8 ns
MGB12A1	4.2 ns	3.4 ns	4.9 ns	3.4 ns
MGB12A2	3.5 ns	2.9 ns	3.9 ns	2.7 ns

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[1] These data are estimated and specified at 5.0V, Tj = 25°C and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage and temperature.

AMI
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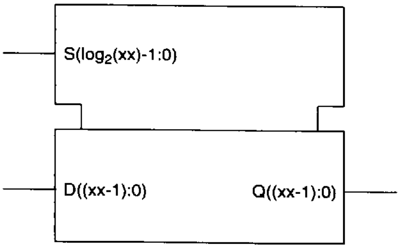
MGBxxBv
Barrel Shifter

Features

- High-performance, Schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength is definable
- High-speed flash barrel shift operations
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGBxxBv



Description

The MGBxxBv barrel shifter synthesizer builds barrel shifters which provide various shift functions for a data word size of "xx" bits. The shifts are performed completely through combinational logic which allows for very fast operations. Shifted data wraps around from the MSB to the LSB.

The S inputs select the number of bits to be shifted from the D inputs to the Q outputs. In the case of an 8-bit shifter, for example, an input select value of two (010) operating on the input 00001100 will generate the output 00110000, a left shift of two bits. If S has the value of seven (111), the output would become 00000110.

The user has flexibility in specifying the word size. Within the name shown above, the "xx" represents the size of the data word. The size of the S bus must be less than or equal to log2(xx). For example, if xx = 8, the size of the S bus must be equal to or less than 3. If not all shift combinations are needed, the size of the S bus can be reduced to save logic.

The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, an 8-bit shifter optimized for minimum gate count would be named MGB08B1.

Contact the factory for information on specific speeds and sizes or to have a Shifter built.

Sample Truth Table

S(1:0)	Q(3)	Q(2)	Q(1)	Q(0)
00	D(3)	D(2)	D(1)	D(0)
01	D(2)	D(1)	D(0)	D(3)
10	D(1)	D(0)	D(3)	D(2)
11	D(0)	D(3)	D(2)	D(1)

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGBxxBv Barrel Shifter

AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Descriptions

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
S($\log_2$(xx)-1:0)	Input	Shift inputs. Specifies the number of position to be shifted.	width $\leq \log_2$(xx)
D((xx-1):0)	Input	Data inputs. D(0) is the LSB.	width > 0
Q((xx-1):0)	Output	Data outputs. Q(0) is the LSB.	width > 0

Sample Equivalent Gates

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGB08B1	77	85	89	104
MGB08B2	80	89	126	147
MGB12B1	155	172	167	195
MGB12B2	200	222	248	290

Sample Delays[1]

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGB08B1	2.3 ns	1.9 ns	2.5 ns	1.8 ns
MGB08B2	2.3 ns	1.9 ns	2.4 ns	1.7 ns
MGB12B1	2.7 ns	2.2 ns	2.6 ns	1.8 ns
MGB12B2	2.8 ns	2.3 ns	3.0 ns	2.1 ns

1. These data are estimated and specified at 5.0V, Tj = 25°C and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage and temperature.

AMERICAN MICROSYSTEMS, INC.

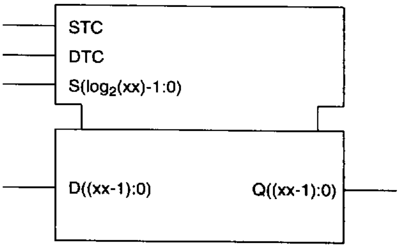
MGBxxyyCv
Arithmetic Shifter

Features

- High-performance, Schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength is definable
- High-speed flash arithmetic shift operations
- Two's complement or unsigned shift control and data
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGBxxyyCv



Description

The MGBxxyyCv arithmetic shifter synthesizer builds arithmetic shifters which provide various shift functions for a data word size of "xx" bits. The shifts are performed completely through combinational logic which allows for very fast operations.

The input data D is shifted left or right by the number of bits specified by the control input S. When the control signal STC is '0', S is interpreted as an unsigned positive number and the shifter performs only left shift operations.

When STC is '1', S is a two's complement number. If S is negative, a right shift is performed. If S is positive, a left shift is performed.

The input data D is interpreted as an unsigned number when DTC is '0' or a two's complement number when DTC is '1'. The type of D is only significant for right shift operations where zero padding is done on the MSBs for unsigned data and sign extension is done for two's complement data.

The user has flexibility in specifying the word size. Within the name shown above, the "xx" represents the size of the data word and "yy" represents the size of the S bus.The size of the S bus is equal to log2(xx).

The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example an 8-bit shifter optimized for minimum gate count would be named MGB0803C1.

Sample Truth Table (MGB0402Cv):

S(1:0)	STC	DTC	Q(3)	Q(2)	Q(1)	Q(0)
00	0	x	D(3)	D(2)	D(1)	D(0)
01	0	x	D(2)	D(1)	D(0)	0
10	0	x	D(1)	D(0)	0	0
11	0	x	D(0)	0	0	0
00	1	x	D(3)	D(2)	D(1)	D(0)
01	1	x	D(2)	D(1)	D(0)	0
10	1	0	0	0	D(3)	D(2)
11	1	0	0	D(3)	D(2)	D(1)
10	1	1	D(3)	D(3)	D(3)	D(2)
11	1	1	D(3)	D(3)	D(2)	D(1)

Contact the factory for information on specific speeds and sizes or to have a Shifter built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGBxxyyCv
Arithmetic Shifter

AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Descriptions

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
STC	Input	Determines whether S is interpreted as unsigned or two's complement.	1
DTC	Input	Determines whether D is interpreted as unsigned or two's complement.	1
S($\log_2$(xx)-1:0)	Input	Shift inputs. Specifies the number of position to be shifted.	width < $\log_2$(xx)
D((xx-1):0)	Input	Data inputs. D(0) is the LSB.	width > 0
Q((xx-1):0)	Output	Data outputs. Q(0) is the LSB.	width > 0

Sample Equivalent Gates

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGB0803C1	130	144	146	171
MGB0803C2	175	194	203	238
MGB1204C1	223	248	245	287
MGB1204C2	320	355	351	411

Sample Delays[1]

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGB0803C1	5.0 ns	4.1 ns	5.0 ns	3.5 ns
MGB0803C2	3.4 ns	2.8 ns	3.6 ns	2.5 ns
MGB1204C1	5.7 ns	4.7 ns	5.7 ns	4.0 ns
MGB1204C2	3.2 ns	2.6 ns	3.4 ns	2.4 ns

[1] These data are estimated and specified at 5.0V, Tj = 25°C and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage and temperature.

AMERICAN MICROSYSTEMS, INC.

MGCDxxAv
Decrement Counter

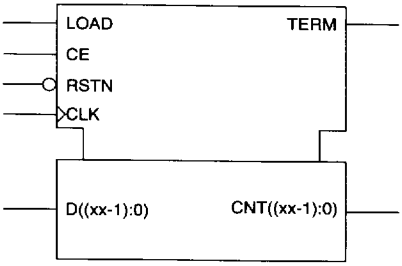
Digital Soft Megacells

Features

- High-performance, HDL-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Counter size is definable
- Includes terminal count when count is zero
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGCDxxAv



Description

The MGCDxxAv synchronous binary counter counts down on the rising edge of the clock. This counter is available in all of AMI's supported processes.

The "xx" in the name represents the number of bits in the counter. For example, an 8-bit counter built for minimum delay would be named MGCD08A2.

The counter has three input controls LOAD, CE, and RSTN. Both LOAD and CE must be asserted for the parallel input to be latched in on the next rising clock edge. When LOAD is low and CE is high the counter decrements by one on each rising clock edge. When the count reaches zero the TERM signal is asserted high. The RSTN is asynchronous and asserted low. The counter output (CNT) is the same size as the counter input (D).

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead. These Megacells are produced using parameterized synthesizers that allow the creation of various sizes and speeds. The synthesized Megacell can be optimized for either minimum delay, minimum gate count or can be designed to meet a specified delay. Each implementation is given a different version number. For example, an 8-bit counter that must run on a 20 ns clock cycle would be named MGCD08A20.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGCDxxAv
Decrement Counter

AMI
AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
LOAD	Input	Load new count. Data is latched when LOAD and CE are high and the clock transitions from low to high.
CE	Input	Count enable. Next count or input latched when CE is high and the clock transitions from low to high.
RSTN	Input	Reset signal. Asynchronously resets counter to 0 when low.
D((xx-1):0)	Input	Data inputs. Data appearing on these inputs is latched into the count when LOAD and CE are high and the clock transitions from low to high.
TERM	Output	Terminal count. Asserted high when the count is all zeros.
CNT((xx-1):0)	Output	Data outputs. The output is decremented by one when the clock transitions from low to high and the CE is asserted.

Sample Equivalent Gates

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI6S(0.6 micron)	AMI8S(0.8 micron)	AMI6G(0.6 micron)	AMI8G(0.8 micron)
MGCU08A1	120	130	166	155
MGCU08A2	188	183	205	222
MGCU12A1	179	176	225	238
MGCU12A2	288	277	329	327

Sample Clock Cycle Time[1]

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI6S(0.6 micron)	AMI8S(0.8 micron)	AMI6G(0.6 micron)	AMI8G(0.8 micron)
MGCU08A1	5.4 ns	7.0 ns	4.8 ns	6.4 ns
MGCU08A2	2.9 ns	3.3 ns	3.3 ns	3.6 ns
MGCU12A1	7.3 ns	8.9 ns	6.7 ns	8.3 ns
MGCU12A2	3.2 ns	3.6 ns	3.4 ns	4.0 ns

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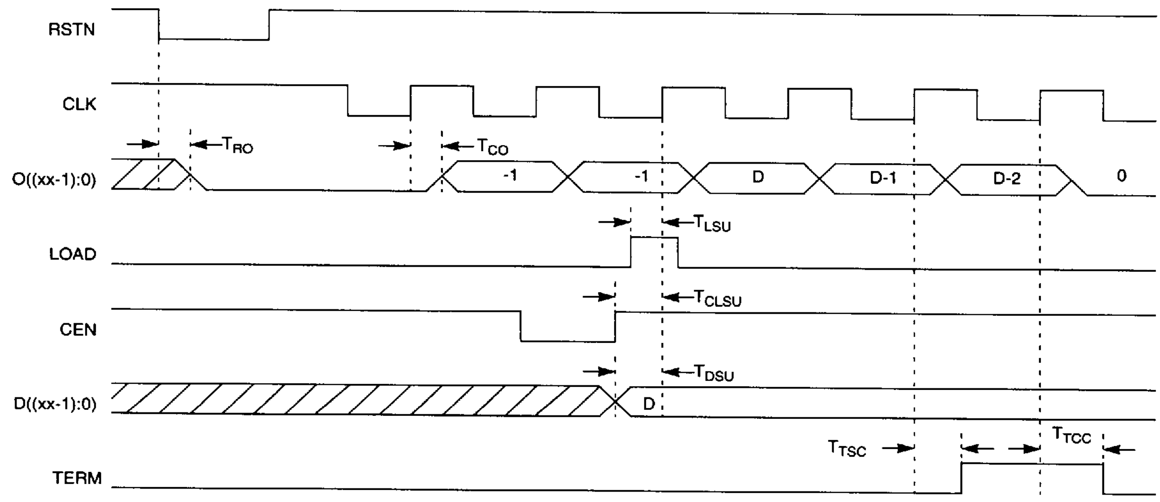
[1] These data are estimated and specified at 5.0V, Tj = 25°C and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage and temperature.

MGCDxxAv
Decrement Counter

Count Timing



Timing Characteristics

SYMBOL	CHARACTERISTIC	REFERENCED TO
T_{RO}	reset to output zero	RSTN falling
T_{CO}	clock to count valid	CLK rising
T_{LSU}	load set-up	CLK rising
T_{CLSU}	count enable load set-up	CLK rising
T_{DSU}	data set-up	CLK rising
T_{TSC}	term set valid	CLK rising
T_{TCC}	term clear valid	CLK rising

MGCUxxAv
Increment Counter

AMI
AMERICAN MICROSYSTEMS, INC.

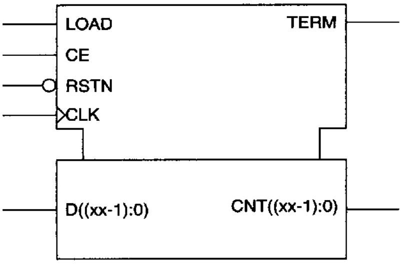
Digital Soft Megacells

Features

- High-performance, HDL-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Counter size is definable
- Includes terminal count when count is all ones
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGCUxxAv



Description

The MGCUxxAv synchronous binary counter counts on the rising edge of the clock. This counter is available in all of AMI's supported processes.

The "xx" in the name represents the number of bits in the counter. For example, an 8-bit counter built for minimum delay would be named MGCU08A2.

The counter has three input controls LOAD, CE, and RSTN. Both LOAD and CE must be asserted for the parallel input to be latched in on the next rising clock edge. When LOAD is low and CE is high the counter increments by one on each rising clock edge. When the count reaches the maximum count the TERM signal is asserted high. The RSTN is asynchronous and asserted low. The counter output (CNT) is the same size as the counter input (D).

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead. These Megacells are produced using parameterized synthesizers that allow the creation of various sizes and speeds. The synthesized Megacell can be optimized for either minimum delay, minimum gate count or can be designed to meet a specified delay. Each implementation is given a different version number. For example, an 8-bit counter that must run on a 20 ns clock cycle would be named MGCU08A20.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGCUxxAv
Increment Counter

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
LOAD	Input	Load new count. Data is latched when LOAD and CE are high and the clock transitions from low to high.
CE	Input	Count enable. Next count or input latched when CE is high and the clock transitions from low to high.
RSTN	Input	Reset signal. Asynchronously resets counter to 0 when low.
D((xx-1):0)	Input	Data inputs. Data appearing on these inputs is latched into the count when LOAD and CE are high and the clock transitions from low to high.
TERM	Output	Terminal count. Asserted high when the count is all ones.
CNT((xx-1):0)	Output	Data outputs. The output is incremented by one when the clock transitions from low to high and the CE is asserted.

Sample Equivalent Gates

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI6S(0.6 micron)	AMI8S(0.8 micron)	AMI6G(0.6 micron)	AMI8G(0.8 micron)
MGCU08A1	119	128	152	162
MGCU08A2	155	155	214	207
MGCU12A1	178	172	228	243
MGCU12A2	261	261	355	299

Sample Clock Cycle Time[1]

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI6S(0.6 micron)	AMI8S(0.8 micron)	AMI6G(0.6 micron)	AMI8G(0.8 micron)
MGCU08A1	5.6 ns	6.3 ns	4.9 ns	6.1 ns
MGCU08A2	3.0 ns	3.5 ns	3.1 ns	4.0 ns
MGCU12A1	7.1 ns	7.6 ns	6.6 ns	7.4 ns
MGCU12A2	3.3 ns	4.0 ns	3.3 ns	3.7 ns

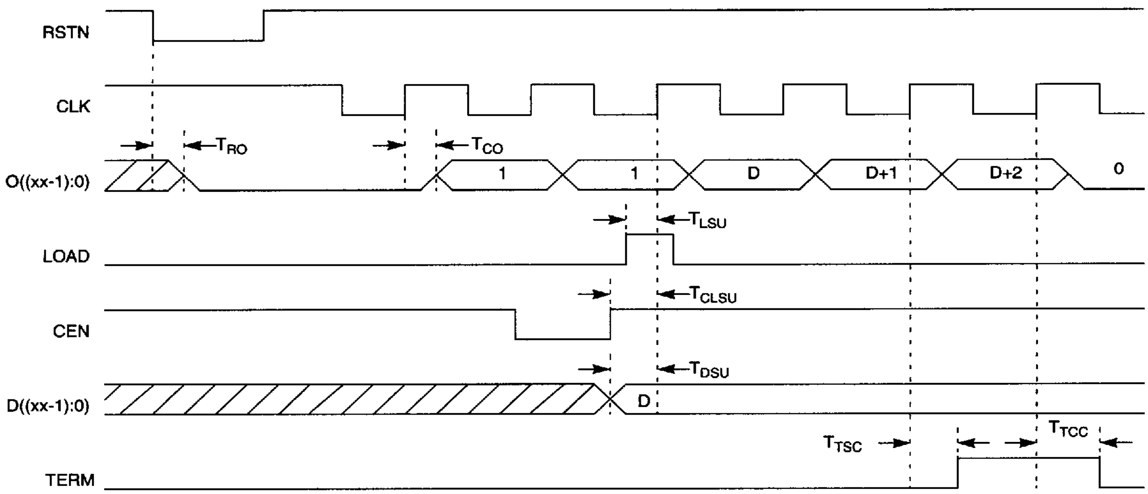
1. These data are estimated and specified at 5.0V, Tj = 25°C and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage and temperature.

MGCUxxAv
Increment Counter

AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Count Timing



Timing Characteristics

SYMBOL	CHARACTERISTIC	REFERENCED TO
T_{RO}	reset to output zero	RSTN falling
T_{CO}	clock to count valid	CLK rising
T_{LSU}	load set-up	CLK rising
T_{CLSU}	count enable load set-up	CLK rising
T_{DSU}	data set-up	CLK rising
T_{TSC}	term set valid	CLK rising
T_{TCC}	term clear valid	CLK rising

AMI
AMERICAN MICROSYSTEMS, INC.

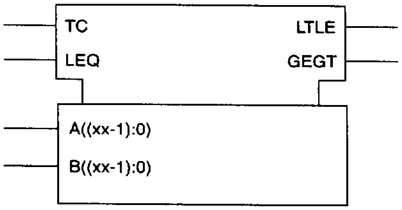
MGCxxAv
2-Function Comparator

Features

- High-performance, Schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength for inputs A and B are user definable
- Unsigned and two's complement data comparison
- Two comparison functions available
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGCxxAv



Description

The MGCxxAv comparator synthesizer builds xx-bit 2-function comparators. The comparator compares signed or unsigned numbers (A and B) and produces two output conditions (LTLE and GEGT).

The input signal LEQ determines what these two output conditions are (see Functional Description). The input TC determines whether the two inputs are compared as unsigned (TC = 0) or signed (TC = 1).

In the name, "xx" represents the A and B input size and the "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit comparator optimized for minimum delay would be named MGC24A2.

Functional Description

LEQ	Condition	LTLE	GEGT
1	A <= B	1	0
1	A > B	0	1
0	A < B	1	0
0	A => B	0	1

Contact the factory for information on specific speeds and sizes or to have a Comparator built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGCxxAv
2-Function Comparator

AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
TC	Input	When 1, signifies A and B inputs are two's complement.	1
LEQ	Input	Determines function of LTLE and GEGT pins.	1
A((xx-1):0)	Input	A Data inputs. A(0) is the LSB.	width > 0
B((xx-1):0)	Input	B Data inputs. B(0) is the LSB.	width > 0
LTLE	Output	'Less than' or 'less than or equal' depending on LEQ.	1
GEGT	Output	'Greater than or equal' or 'greater than' depending on LEQ.	1

Sample Equivalent Gates

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGC08A1	39	43	45	53
MGC08A2	92	102	94	110
MGC12A1	53	59	61	71
MGC12A2	100	111	118	138

Sample Delays[1]

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGC08A1	3.6 ns	3.0 ns	4.1 ns	2.9 ns
MGC08A2	2.1 ns	1.7 ns	2.4 ns	1.7 ns
MGC12A1	5.1 ns	4.2 ns	5.7 ns	4.0 ns
MGC12A2	2.4 ns	2.0 ns	2.8 ns	2.0 ns

1. These data are estimated and specified at 5.0V, Tj = 25°C and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage and temperature.

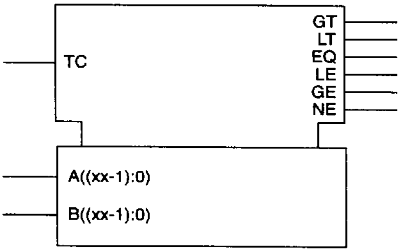
MGCxxBv
6-Function Comparator

Features

- High-performance, Schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength for inputs A and B are user definable
- Unsigned and two's complement data comparison
- Six comparison functions available
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGCxxBv



Description

The MGCxxBv comparator synthesizer builds xx-bit 6-function comparators. The comparator compares signed or unsigned numbers (A and B) and produces six output conditions (GT, LT, EQ, LE, GE, NE).

The input TC determines whether the two inputs are compared as unsigned (TC=0) or signed (TC=1).

In the name, "xx" represents the A and B input size and the "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit comparator optimized for minimum delay would be named MGC24B2.

Functional Description

Condition	GT	LT	EQ	LE	GE	NE
A > B	1	0	0	0	1	1
A < B	0	1	0	1	0	1
A = B	0	0	1	1	1	0

Contact the factory for information on specific speeds and sizes or to have an 6-function Comparator built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGCxxBv
6-Function Comparator

AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
TC	Input	When 1, signifies A and B inputs are two's complement.	1
A((xx-1):0)	Input	A Data inputs. A(0) is the LSB.	width > 0
B((xx-1):0)	Input	B Data inputs. B(0) is the LSB.	width > 0
GT	Output	Asserted when A is greater than B.	1
LT	Output	Asserted when A is less than B.	1
EQ	Output	Asserted when A equals B.	1
LE	Output	Asserted when A is less than or equal to B.	1
GE	Output	Asserted when A is greater than or equal to B.	1
NE	Output	Asserted when A does not equal B.	1

Sample Equivalent Gates

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGC08B1	70	78	77	90
MGC08B2	120	133	174	204
MGC12B1	98	109	108	126
MGC12B2	182	202	252	295

Sample Delays[1]

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGC08B1	4.7 ns	3.9 ns	4.4 ns	3.0 ns
MGC08B2	2.2 ns	1.8 ns	3.0 ns	2.1 ns
MGC12B1	6.0 ns	4.9 ns	6.3 ns	4.4 ns
MGC12B2	2.6 ns	2.1 ns	2.5 ns	1.8 ns

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1. These data are estimated and specified at 5.0V, Tj = 25°C and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage and temperature.

AMI
AMERICAN MICROSYSTEMS, INC.

MGDxxAv Decrementer

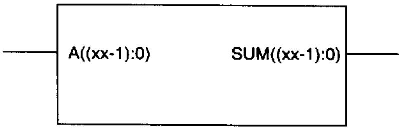
Digital Soft Megacells

Features

- High-performance, Schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength for input A is user definable
- Selects multiple architectures for size and speed efficiency
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGDxxAv



Description

The MGDxxAv decrementer synthesizer builds xx-bit decrementers. The decrementer subtracts 1 from input A to produce the output SUM.

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead.

The SUM output is the same size as the input A.

In the name, "xx" represents the A input size and the "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit decrementer optimized for minimum delay would be named MGD24A2.

Functional Description

A	SUM
A	A - 1

Contact the factory for information on specific speeds and sizes or to have a Decrementer built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGDxxAv
Decrementer

AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
A((xx-1):0)	Input	A Data inputs. A(0) is the LSB.	width > 0
SUM((xx-1):0)	Output	SUM Data outputs. SUM(0) is the LSB.	width > 0

Sample Equivalent Gates

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGD08A1	31	30	35	45
MGD08A2	53	66	71	91
MGD12A1	48	47	55	69
MGD12A2	88	112	118	154

Sample Delays[1]

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGD08A1	4.6 ns	3.4 ns	4.7 ns	3.24 ns
MGD08A2	1.5 ns	1.5 ns	1.7 ns	1.39 ns
MGD12A1	7.2 ns	5.0 ns	7.3 ns	4.88 ns
MGD12A2	1.6 ns	1.6 ns	1.9 ns	1.67 ns

1. These data are estimated and specified at 5.0V, Tj = 25°C and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage and temperature.

AMI

AMERICAN MICROSYSTEMS, INC.

MGIxxAv Incrementer

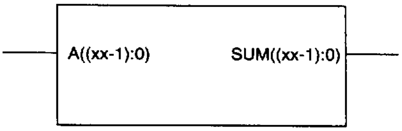
Digital Soft Megacells

Features

- High-performance, Schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength for input A is user definable
- Selects multiple architectures for size and speed efficiency
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGIxxAv



Description

The MGIxxAv Incrementer synthesizer builds xx-bit Incrementers. The incrementer adds 1 to input A to produce the output SUM.

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead.

In the name, "xx" represents the A and SUM input sizes, and the "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit incrementer optimized for minimum delay would be named MGI24A2.

Functional Description

A	SUM
A	A + 1

Contact the factory for information on specific speeds and sizes or to have an Incrementer built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGIxxAv
Incrementer

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
A((xx-1):0)	Input	A Data inputs. A(0) is the LSB.	width > 0
SUM((xx-1):0)	Output	SUM Data outputs. SUM(0) is the LSB.	width > 0

Sample Equivalent Gates

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGI08A1	33	37	39	46
MGI08A2	45	50	53	62
MGI12A1	52	58	62	73
MGI12A2	83	92	112	131

Sample Delays[1]

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGI08A1	2.7 ns	2.2 ns	3.0 ns	2.1 ns
MGI08A2	1.4 ns	1.2 ns	1.6 ns	1.1 ns
MGI12A1	3.0 ns	2.5 ns	4.7 ns	3.3 ns
MGI12A2	1.6 ns	1.3 ns	1.8 ns	1.3 ns

[1] These data are estimated and specified at 5.0V, Tj = 25°C and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage and temperature.

AMERICAN MICROSYSTEMS, INC.

MGIxxBv
Incrementer/Decrementer

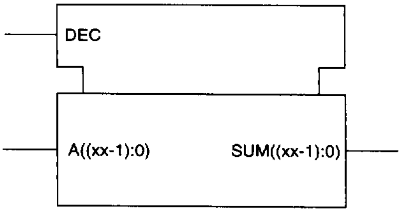
Digital Soft Megacells

Features

- High-performance, Schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength for input A is user definable
- Selects multiple architectures for size and speed efficiency
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGIxxBv



Description

The MGIxxBv Incrementer/Decrementer synthesizer builds xx-bit Incrementer/Decrementers. When the DEC input is active (DEC=1) the Incrementer/Decrementer subtracts 1 from input A. When DEC is not active (DEC=0) the Incrementer/Decrementer adds 1 to input A.

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead.

In the name, "xx" represents the A and SUM input sizes, and the "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit Incrementer/Decrementer optimized for minimum delay would be named MGI24B2.

Functional Description

A	DEC	SUM
A	0	A + 1
A	1	A - 1

Contact the factory for information on specific speeds and sizes or to have an Incrementer/Decrementer built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGIxxBv
Incrementer/Decrementer

AMI AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
DEC	Input	Decrement. Megacell decrements when input is high.	1
A((xx-1):0)	Input	A Data inputs. A(0) is the LSB.	width > 0
SUM((xx-1):0)	Output	SUM Data outputs. SUM(0) is the LSB.	width > 0

Sample Equivalent Gates

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGI08B1	60	67	78	91
MGI08B2	86	95	117	137
MGI12B1	95	105	128	150
MGI12B2	162	180	204	239

Sample Delays[1]

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGI08B1	7.5 ns	6.2 ns	7.0 ns	4.9 ns
MGI08B2	2.2 ns	1.8 ns	2.6 ns	1.8 ns
MGI12B1	12.2 ns	10.0 ns	11.1 ns	8.2 ns
MGI12B2	2.7 ns	2.2 ns	3.1 ns	2.2 ns

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[1] These data are estimated and specified at 5.0V, Tj = 25°C and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage and temperature.

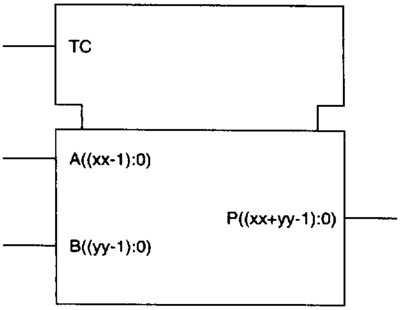
MGMxxyyDv Multiplier

Features

- High-performance, Schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Inputs and output sizes are user definable
- Selects multiple architectures for size and speed efficiency
- Two's complement control allows either unsigned or two's complement format
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGMxxyyDv



Description

The MGMxxyyDv Multiplier synthesizer builds multipliers of various sizes. The operands A and B are multiplied to produce the product P. The input and output data are interpreted as unsigned when TC=0 or two's complement when TC=1.

The "xxyy" represents a four character sequence assigned to each multiplier configuration where "xx" represents the number of A input bits and "yy" represents the number of B input bits. The number of products bits are equal to "xx" + "yy".

The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 16-bit by 12-bit multiplier optimized for minimum delay would be named MGM1612D2.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for information on specific speeds and sizes or to have a Multiplier built.

MGMxxyyDv
Multiplier

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS	LEGAL RANGE
TC	Input	Determines whether the input and output data are interpreted as unsigned (TC=0) or two's complement (TC=1) numbers.	1
A((xx-1):0)	Input	A input bits. A(0) is the LSB.	width > 0
B((yy-1):0)	Input	B input bits. B(0) is the LSB.	width > 0
P((xx+yy-1):0)	Output	Product bits. P(0) is the LSB.	xx + yy > width > 0

Sample Equivalent Gates

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGM0808D1	490	515	583	602
MGM0808D2	696	668	925	852
MGM1212D1	1,060	1,128	1,252	1,288
MGM1212D2	1,357	1,457	1,756	1,700

Sample Delays[1]

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGM0808D1	17.0 ns	12.5 ns	17.1 ns	11.4 ns
MGM0808D2	10.0 ns	7.9 ns	10.2 ns	6.8 ns
MGM1212D1	25.5 ns	18.4 ns	24.9 ns	15.8 ns
MGM1212D2	12.3 ns	9.2 ns	12.6 ns	8.7 ns

[1] These data are estimated and specified at 5.0V, Tj = 25°C and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage and temperature.

AMI
AMERICAN MICROSYSTEMS, INC.

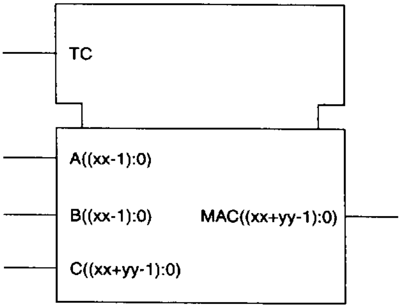
MGMxxyyEv
Multiplier-Accumulator

Features

- High-performance, Schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Widths for inputs A and B are definable
- Selects multiple architectures for size and speed efficiency
- Two's complement control allows unsigned or two's complement multiplication-accumulation
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGMxxyyEv



Description

The MGMxxyyEv multiplier-accumulator synthesizer builds multiplier-accumulators of various sizes. The operands A and B are multiplied and the product is added to C producing the result MAC. The input and output data are interpreted as unsigned when TC=0 or two's complement when TC=1.

The "xxyy" represents a four character sequence assigned to each multiplier-accumulator configuration where "xx" represents the number of A input bits and "yy" represents the number of B input bits. The number of MAC bits are equal to "xx" + "yy".

The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 16-bit by 12-bit multiplier-accumulator optimized for minimum delay would be named MGM1612E2.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for information on specific speeds and sizes or to have a Multiplier-Accumulator built.

MGMxxyyEv
Multiplier-Accumulator

AMI
AMERICAN MICROSYSTEMS, INC.

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTION	LEGAL RANGE
TC	Input	Determines whether the input and output data are interpreted as unsigned (TC=0) or two's complement (TC=1) numbers.	1
A((xx-1):0)	Input	A input bits. A(0) is the LSB.	width > 0
B((yy-1):0)	Input	B input bits. B(0) is the LSB.	width > 0
C((xx+yy-1):0)	Input	C input bits. C(0) is the LSB.	width = xx + yy
MAC((xx+yy-1):0)	Output	Result bits. MAC(0) is the LSB.	width = xx + yy

Sample Equivalent Gates

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGM0808E1	702	779	872	1,020
MGM0808E2	777	862	1,045	1,223
MGM1212E1	1,415	1,570	1,758	2,057
MGM1212E2	1,610	1,787	1,860	2,176

Sample Delays[1]

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGM0808E1	15.0 ns	12.3 ns	16.3 ns	11.4 ns
MGM0808E2	11.8 ns	9.7 ns	12.0 ns	8.4 ns
MGM1212E1	19.5 ns	16.0 ns	21.0 ns	14.7 ns
MGM1212E2	12.7 ns	10.4 ns	13.1 ns	9.2 ns

1. These data are estimated and specified at 5.0V, Tj = 25°C and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage and temperature.

AMI
AMERICAN MICROSYSTEMS, INC.

MGSxxyyAv Subtractor

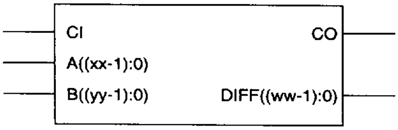
Digital Soft Megacells

Features

- High-performance, Schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength for inputs A and B are user definable
- Selects multiple architectures for size and speed efficiency
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGSxxyyAv



Description

The MGSxxyyAv subtractor synthesizer builds xx-bit by yy-bit subtractors. Input operands are A and B with an input carry CI to produce the output DIFF with a carry-out CO.

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead.

Inputs A and B and output DIFF can be interpreted to be either in the two's complement or unsigned number format. The DIFF output is the same format as the inputs, and its size is the same as the largest of inputs A or B.

In the name, "xx" represents the A input size and "yy" represents the B input size. The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit by 20-bit subtractor optimized for minimum delay would be named MGS2420A2.

Functional Description

A	B	CI	DIFF	CO
A	B	0	A - B	carry-out
A	B	1	A - B - 1	carry-out

Contact the factory for information on specific speeds and sizes or to have an Subtractor built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGSxxyyAv
Subtractor

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTION	LEGAL RANGE
CO	Output	Carry out, active high.	1
A((xx-1):0)	Input	A Data inputs. A(0) is the LSB.	width > 0
B((yy-1):0)	Input	B Data inputs. B(0) is the LSB.	width > 0
CI	Input	Carry in, active high.	1
DIFF((ww-1):0)	Output	DIFF Data outputs. DIFF(0) is the LSB.	width > 0

Sample Equivalent Gates

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGS0808A1	70	78	82	96
MGS0808A2	163	181	232	271
MGS1212A1	105	117	122	1,363
MGS1212A2	217	241	285	333

Sample Delays[1]

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI8S(0.8 micron)	AMI6S(0.6 micron)	AMI8G(0.8 micron)	AMI6G(0.6 micron)
MGS0808A1	7.4 ns	6.1 ns	8.2 ns	5.7 ns
MGS0808A2	2.7 ns	2.3 ns	3.3 ns	2.3 ns
MGS1212A1	10.5 ns	8.8 ns	11.8 ns	8.3 ns
MGS1212A2	3.3 ns	2.8 ns	3.8 ns	2.7 ns

[1] These data are estimated and specified at 5.0V, Tj = 25°C and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage and temperature.

AMI
AMERICAN MICROSYSTEMS, INC.

MGFxxyyC1
Latch-based FIFO

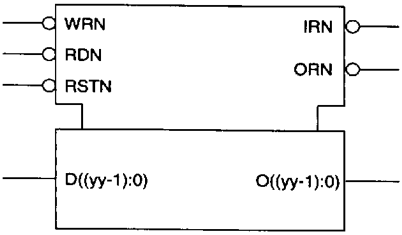
Digital Soft Megacells

Features

- High-performance, schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Uses latch-array, fall-through architecture
- Array sizes are definable
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGFxxyyC1



Description

The MGFxxyyC1 FIFO (First In, First Out) memory synthesizer builds latch based FIFOs of various sizes. FIFOs built with this synthesizer use the fall-through algorithm in which data is written to the top of the register stack and falls through to the bottom of the stack. If the FIFO is not empty the data stops falling through when valid data are encountered. Data fallen through to the bottom of the stack are available at the outputs.

These FIFOs have separate asynchronous read and write clocks. Flags include ORN (output ready not) which determines if the FIFO is empty and IRN (input ready not) which determines if the FIFO is full. Indeterminable results may occur during writes when IRN is active.

The "xxyy" in the name represents a four character sequence assigned to each FIFO configuration where "xx" represents the number of words and "yy" represents the number of bits per word. For example, a 32-word by 8-bit FIFO would be named MGF3208C1.

Contact the factory for information on specific speeds and sizes or to have a FIFO built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGFxxyyC1
Latch-based FIFO

Digital Soft Megacells

Pin Description

SIGNAL	TYPE	SIGNAL DESCRIPTIONS
WRN	Input	Write clock. Data is latched when WRN transitions from low to high.
RDN	Input	Read clock. On the low to high transition of RDN data on the bottom of the FIFO is replaced with data from immediately above.
RSTN	Input	Reset signal. Sets FIFO to empty.
D((yy-1):0)	Input	Data inputs. Data appearing on these inputs are written into the FIFO on the low to high transition of WRN. D(0) is the LSB.
IRN	Output	Input Ready Not. A low on this signal indicates the FIFO is either full or busy. Writing when IRN is low will cause data to be lost.
ORN	Output	Output Ready Not. A low on this signal indicates that data appearing on the outputs are valid.
O((yy-1):0)	Output	Data outputs. The data stored on the bottom of the stack are constantly available through these signals and are updated on the rising edge of RDN.

Sample Equivalent Gates

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI6S(0.6 micron)	AMI8S(0.8 micron)	AMI6G(0.6 micron)	AMI8G(0.8 micron)
MGF0232C1	260	253	320	323
MGF0809C1	290	274	368	369
MGF1616C1	843	761	1,030	1,031
MGF1632C1	1,542	1,366	1,846	1,863

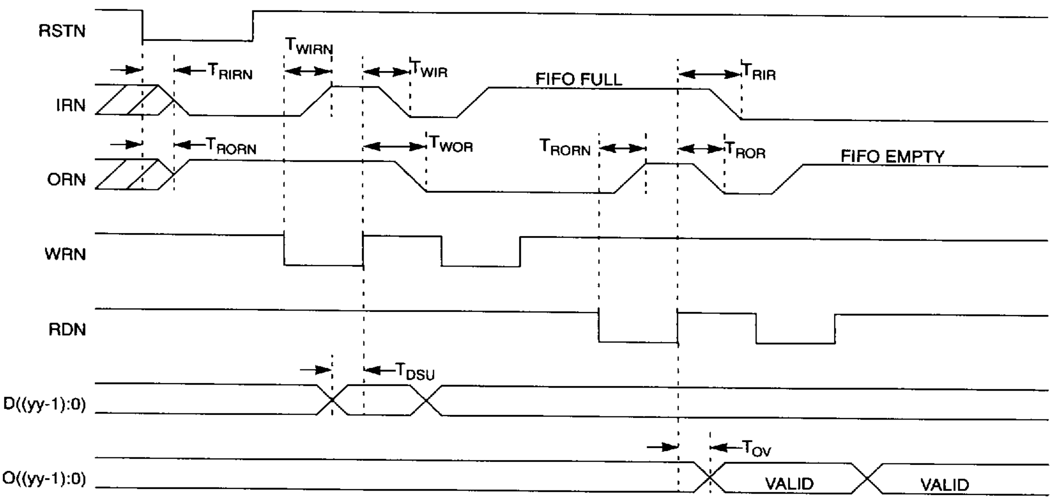
Sample Fall-through Delays[1]

CELL NAME	STANDARD CELL		GATE ARRAY	
	AMI6S(0.6 micron)	AMI8S(0.8 micron)	AMI6G(0.6 micron)	AMI8G(0.8 micron)
MGF0232C1	6.1 ns	6.4 ns	5.3 ns	6.2 ns
MGF0809C1	21.9 ns	23.1ns	18.7 ns	21.4 ns
MGF1616C1	43.1 ns	45.4 ns	36.9 ns	41.9 ns
MGF1632C1	44.5 ns	45.5 ns	39.1 ns	43.2 ns

1. These data are estimated and specified at 5.0V, Tj = 25°C and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage and temperature.

MGFxxyyC1
Latch-based FIFO

Read / Write Timing



Timing Characteristics

SYMBOL	CHARACTERISTIC	REFERENCED TO
T_{RIRN}	reset to input ready set	RSTN falling
T_{RORN}	reset to output ready clear	RSTN falling
T_{WIRN}	write to input ready clear	WRN falling
T_{WOR}	write to output ready set	WRN rising
T_{WIR}	write to input ready set	WRN rising
T_{RIR}	read to input ready set	RDN rising
T_{RORN}	read to output ready clear	RDN falling
T_{ROR}	read to output ready set	RDN rising
T_{DSU}	data setup to write	WRN rising
T_{OV}	read to output valid	RDN rising

MGFxxxxyyD
Synchronous FIFO

AMERICAN MICROSYSTEMS, INC.

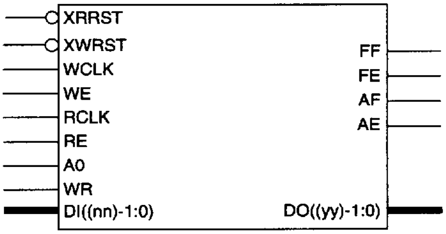
Digital Soft Megacells

Features

- Dual-port RAM architecture for zero fall-through time
- Dynamically programmable almost-full and almost-empty flags
- Synchronous design
- Word width and depth are user definable
- High-performance, Schematic-based megacell
- Uses the ASIC Standard Library for technology independence

LOGIC SYMBOL

MGFxxxxyyD



Description

The MGFxxxxyyD FIFO (First In, First Out) builds synchronous FIFOs of various sizes. These FIFOs use a Dual-Port Synchronous Static RAM to allow large FIFO depth without any fall-through time. This FIFO is available in the SDX (1.0 u Standard Cell) and AMI8S (0.8 u Standard Cell) technologies.

The "xxxx" in the name represents the number of words in the FIFO, and must be a power of 2 between five and ten. (i.e. 32 minimum to 1024 maximum) The "yy" is the number of bits per word and can be from one to any size needed. For example, a 128 word by 16 bit FIFO would be named MGF012816D.

Clock inputs WCLK and RCLK are free-running. Data is written into the FIFO on the falling edge of WCLK when WE is high. WE should only transition when WCLK is low. Data is read on the rising edge of RCLK when RE is high. The output data must be captured by external logic before the next rising edge of RCLK.

Inputs A0 and WR are used to write to the registers which control the AE (almost empty) and AF (almost full) flags. When A0 is low, data on the DI bus is written into the AE register on the rising edge of WR. When A0 is high data is written into the AF register. On reset the AE register defaults to 25% of "xxxx" and AF to 75% of "xxxx".

The width of the data input (DI) bus is equal to the greater of, the number of bits per word or log2 (number of words in FIFO).

Flags include FE, (FIFO empty) FF, (FIFO full) and the dynamically programmable AE (almost empty) and AF (almost full) flags.

The MGFxxxxyyD features a split reset line to allow implementation of a re-transmit function. XRRST and XWRST are synchronous active low resets for the read counter and write counter respectively. Each reset must be held active for at least one rising edge of its respective clock to initialize the FIFO.

To implement a re-transmit function the total number of writes since the last general reset must be LESS THAN the number of words in the FIFO. As long as this condition is met the read counter may be reset and all the words written since the general reset may be reread. Notice that if the AE register has been programed to a different value, the read reset will return it to the default.

Contact the factory for information on specific speeds and sizes or to have a FIFO built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGFxxxxyyD
Synchronous FIFO

Pin Description

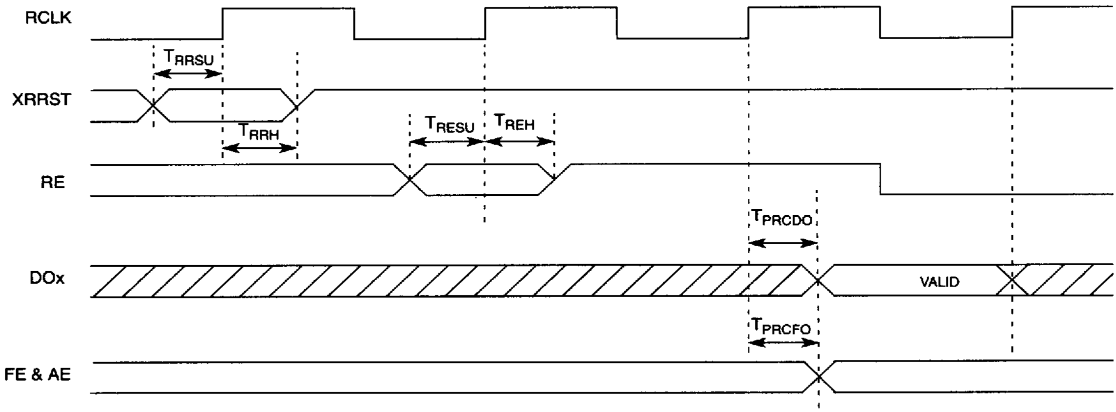
SIGNAL	TYPE	SIGNAL DESCRIPTIONS
XWRST	I	Synchronous write reset. Resets the write portion of the FIFO. Must be held low during a rising edge of WCLK.
WCLK	I	Free-running write clock.
WE	I	Write enable. Data appearing on DIn will be written into the FIFO on the falling edge of WCLK when WE is high. WE should transition only when WCLK is low.
XRRST	I	Synchronous read reset. Resets the read portion of the FIFO. Must be held low during a rising edge of RCLK.
RCLK	I	Free-running read clock.
RE	I	Read enable. Data is read from the FIFO on the rising edge of RCLK when RE is high.
A0	I	Address for determining if the AE or AF flag register is to be written. When A0 = 1 the AF flag register is written.
WR	I	Write control for AE and AF registers. Data appearing on DIn is written into either the AE or AF register on the rising edge of WR.
DI((nn)-1:0)	I	Data into the FIFO and the AE/AF registers.
DO((yy)-1:0)	O	Data out of the FIFO.
FF	O	FIFO full flag, active high. Synchronized to WCLK.
AF	O	FIFO almost full flag, active high. Synchronized to WCLK.
FE	O	FIFO empty flag, active high. Synchronized to RCLK.
AE	O	FIFO almost empty flag, active high. Synchronized to RCLK.

Sample Equivalent Gates[1]

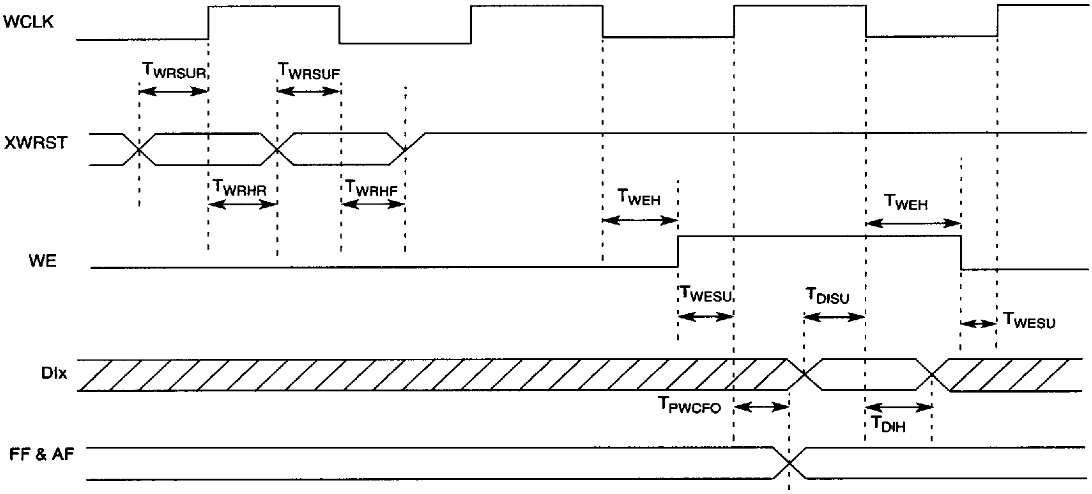
Cell Name	Standard Cell
	AMI8S(0.8 micron)
MGF0032yyD	470
MGF0064yyD	540
MGF0128yyD	640
MGF0256yyD	740
MGF0512yyD	840
MGF1024yyD	940

Note: 1. Does not include RAM.

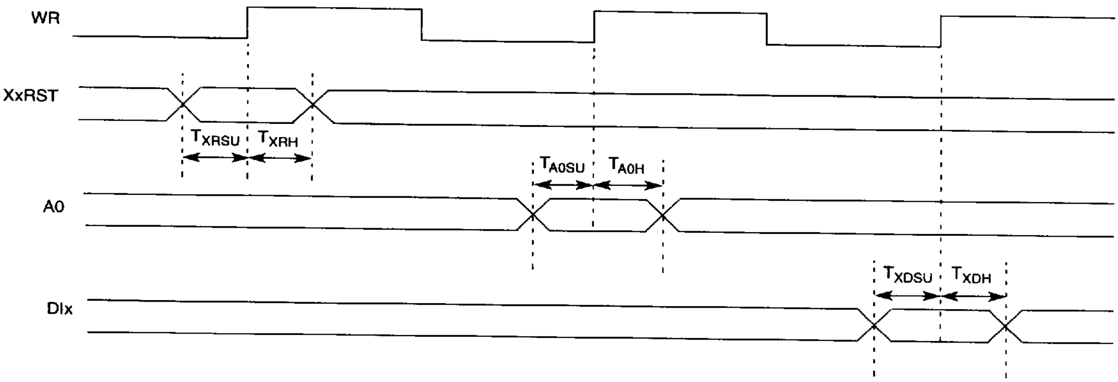
Read Timing



Write Timing



Register Write Timing



Timing Characteristics

Symbol	Characteristic	Referenced to
T_{RRSU}	read reset set-up	RCLK rising
T_{RRH}	read reset hold	RCLK rising
T_{RESU}	read enable set-up	RCLK rising
T_{REH}	read enable hold	RCLK rising
T_{PRCDO}	read clock to data out valid	RCLK rising
T_{PRCFO}	read clock to flag out valid	RCLK rising
T_{WRSUR}	write reset set-up	WCLK rising
T_{WRHR}	write reset hold	WCLK rising
T_{WRSUF}	write reset set-up	WCLK falling
T_{WRHF}	write reset hold	WCLK falling
T_{WESU}	write enable set-up	WCLK rising
T_{WEH}	write enable hold	WCLK falling
T_{DISU}	data in set-up	WCLK falling
T_{DIH}	data in hold	WCLK falling
T_{PWCFO}	write clock to flag out valid	WCLK rising
T_{XRSU}	either reset set-up	WR rising
T_{XRH}	either reset hold	WR rising
T_{A0SU}	A0 set-up	WR rising
T_{A0H}	A0 hold	WR rising
T_{XDSU}	data in set-up	WR rising
T_{XDH}	data in hold	WR rising

MGFxxxxyyE
Asynchronous FIFO

AMERICAN MICROSYSTEMS, INC.

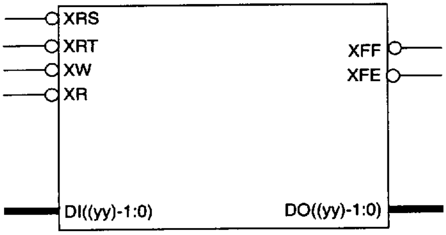
Digital Soft Megacells

Features

- Dual-port RAM architecture for zero fall-through time
- Asynchronous design
- Word width and depth are user definable
- High-performance, Schematic-based megacell
- Uses the ASIC Standard Library for technology independence

LOGIC SYMBOL

MGFxxxxyyE



Description

The MGFxxxxyyE FIFO (First In, First Out) builds asynchronous FIFOs of various sizes. These FIFOs use a Dual-Port Synchronous Static RAM to allow large FIFO depth without any fall-through time. This FIFO is available in the SDX (1.0 u Standard Cell) and AMI8S (0.8 u Standard Cell) technologies.

The "xxxx" in the name represents the number of words in the FIFO, and must be a power of 2 between five and ten (i.e. 32 minimum to 1024 maximum). The "yy" is the number of bits per word and can be from one to any size needed. For example, a 128 word by 16 bit FIFO would be named MGF012816E.

Data is written into the FIFO on the rising edge of XW, and read on the falling edge of XR. Flags are updated on the rising edge of XW and XR. Flags include XFE, (FIFO empty not) and XFF (FIFO full not).

The MGFxxxxyyE has a general reset, XRS pin, and a re-transmit function enabled by the XRT pin. Both pins are active low.

To use the re-transmit function the total number of writes since the last general reset MUST NOT EXCEED the number of words in the FIFO.

As long as this condition is met, pulling XRT low will reset the read counter and all the words written since the general reset may be read.

Contact the factory for information on specific speeds and sizes or to have a FIFO built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology- and process-independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGFxxxxyyE
Asynchronous FIFO

Pin Description

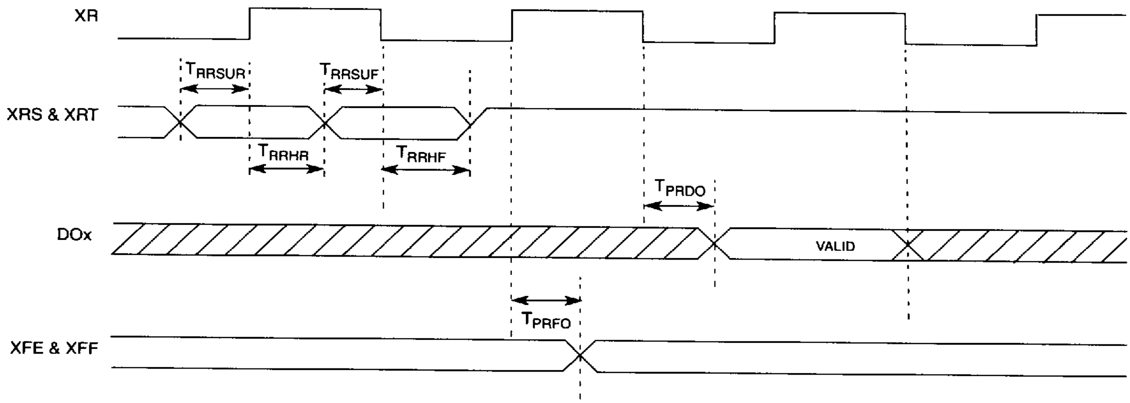
SIGNAL	TYPE	SIGNAL DESCRIPTIONS
XRS	I	Asynchronous reset. Resets FIFO when pulsed low.
XRT	I	Activates re-transmit function when pulsed low.
XW	I	Active low write signal. Data appearing on DIn will be written into the FIFO on the rising edge of XW.
XR	I	Active low read signal. Data is read from the FIFO on the falling edge of XR.
DI((yy)-1:0)	I	Data input into the FIFO.
DO((yy)-1:0)	O	Data output from the FIFO.
XFF	O	FIFO full flag, active low.
XFE	O	FIFO empty flag, active low.

Sample Equivalent Gates[1]

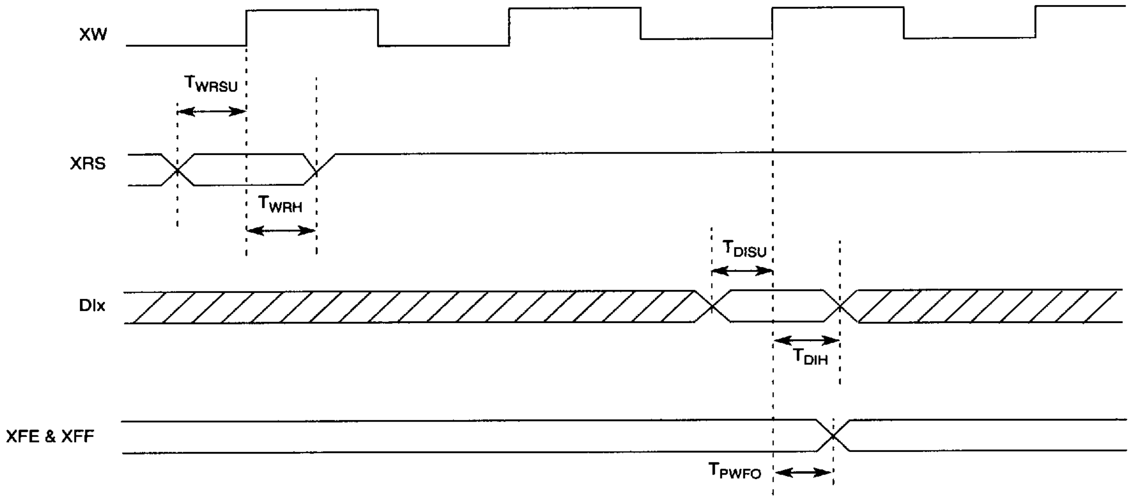
Cell Name	Standard Cell
	AMI8S(0.8 micron)
MGF0032yyE	300
MGF0064yyE	360
MGF0128yyE	430
MGF0256yyE	495
MGF0512yyE	560
MGF1024yyE	630

NOTE: 1. Does not include RAM.

Read Timing



Write Timing



Timing Characteristics

Symbol	Characteristic	Referenced to
T_{RRSUR}	read reset set-up	XR rising
T_{RRH}	read reset hold	XR rising
T_{RRSUF}	read reset set-up	XR falling
T_{RRHF}	read reset hold	XR falling
T_{PRDO}	read clock to data out valid	XR falling
T_{PRFO}	read clock to flag out valid	XR rising
T_{WRSU}	write reset set-up	XW rising
T_{WRH}	write reset hold	XW rising
T_{DISU}	data in set-up	XW rising
T_{DIH}	data in hold	XW rising
T_{PWFO}	write clock to flag out valid	XW rising

AMERICAN MICROSYSTEMS, INC.

RASGdwyz
Self-Timed Synchronous Static RAM

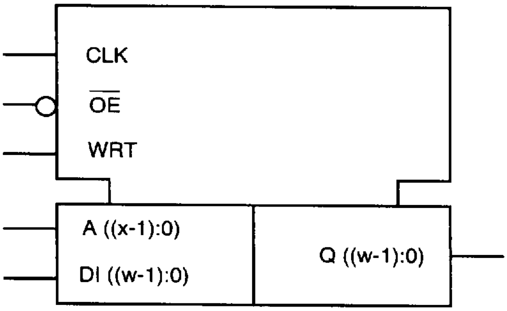
AMI8G 0.8 micron CMOS Gate Array

Features

- Self-timed design allows flexibility in clock duty cycle while maintaining fast cycle time
- 6.4 nsec typical cycle time for a 1K x 16 RAM
- 3-State or always active outputs
- Low standby power when the clock is stopped
- Separate input and output ports with full parallel access
- Functionally equivalent to AMI's Standard Cell Self-Timed Synchronous Static RAM
- Precharged design for faster operation with lower power consumption

FIGURE 1: LOGIC SYMBOL

RASGdwyz



Notes: 1. A0 is the LSB.
2. x represents the number of address lines.

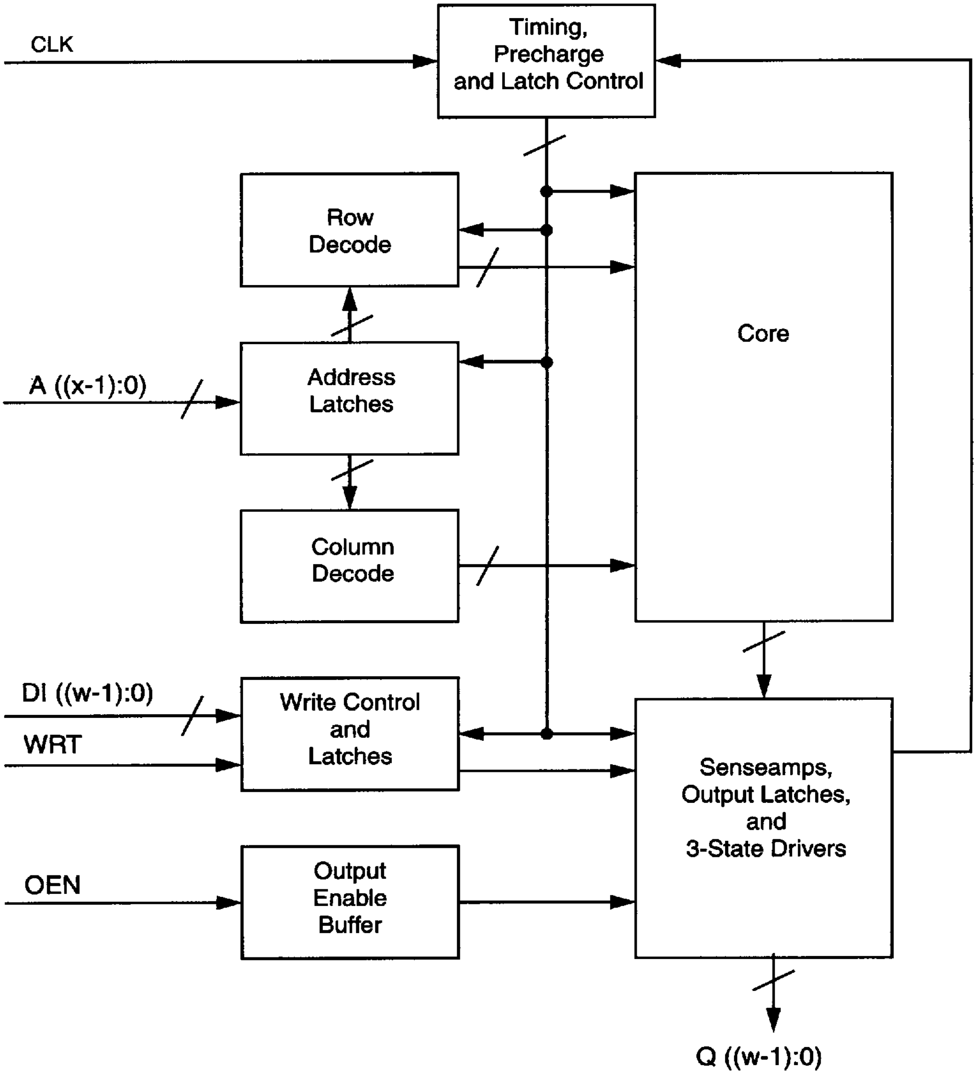
General Description

This series of 0.8 micron gate array compiled RAMs operates within a power supply voltage range of 4.5V to 5.5V and can operate with reduced performance at lower supply voltages. Contact the factory for low voltage performance specifications. These RAMs can be built with an option of 3-state or always active outputs. The self-timed feature of these RAMs allows flexibility in the clock duty cycle while maintaining fast cycle times. All timing is relative to the rising edge of the clock input (CLK). When CLK rises, all inputs are latched and the READ or WRITE operation occurs. The RAM will stay in the READ mode and not start precharging until the READ operation is complete, even if CLK falls.The outputs become valid a short time after the rising edge of CLK and stay valid until the next rising edge of CLK. All of the inputs including CLK can be held stable indefinitely with no loss of memory as long as power is supplied to the RAM.

Within limits shown below, the user has flexibility in specifying the logical size of the RAM, including both word size and number of address locations. The name of each RAM indicates the logical size and configuration as explained here. The "RAS" in the name indicates a single port RAM. The "G" is a version number for this particular configuration of RAM. The "d" variable in the name can be an "A" to indicate always active outputs or an "N" to indicate 3-state outputs with active low enable. The "w" represents the word length in a mod-36 alpha-numeric digit using the integers 1-9 and the letters A-Z excluding O, Q, and V. For example, "N" indicates a word length of 23 and "P" indicates a word length of 24. The "yz" represents a hexadecimal value for the number of address locations divided by 16. For example, RASGAG0C is a 192 x 16 single port RAM with always active outputs.

Performance data is listed in this data sheet for two example sizes. TBD numbers will be available in February 1994. To obtain performance data or a workstation symbol and model for a specific size, contact your sales representative or the factory.

FIGURE 2: RAM BLOCK DIAGRAM



AMI
AMERICAN MICROSYSTEMS, INC.

RASGdwyz
Self-Timed Synchronous Static RAM

AMI8G 0.8 micron CMOS Gate Array

Address and Word Size Ranges

PARAMETER	MINIMUM	MAXIMUM	INCREMENT
Address inputs	5	10	1
Address locations (words)	16	1024 (1K)	16
Word size (data outputs)	1-bit	32-bits	1-bit
Total bits in a core (word size times address locations)	16	32,768 (32K)	

Pin Loading (Equivalent Loads)

SIGNAL	TYPE	32 x 4 EQL	1K x 16 EQL	SIGNAL DESCRIPTIONS
Ai	I	0.0061	0.0061	Address inputs
CLK	I	0.028	0.048	Clock input
DI	I	0.0061	0.0061	Data inputs
OEN	I	0.017	0.031	3-State output control
WRT	I	0.0061	0.0061	Write control
Q (High-Z)	O	0.012	0.017	Data outputs

Area relative to a 2-Input Nand

32 x 4: 1,353
1K x 16: 39,313

Bolt Syntax

Q (w-1) ... Q1 Q0 .RAS8dwyz A(x-1) ... A1 A0 CLK DI(w-1) ... DI1 DI0 OEN WRT;

Note: A0 is the LSB.

Power Dissipation

PARAMETER	32 x 4	1K x 16
Typical EQL_{pd} (Equivalent Power Dissipation Load)	33 pF	440 pF
Typical Static I_{DD} ($T_J = 85°C$) (µA)	$6.2e^{-7}$A	$2.8e^{-5}$A

See power notes in data book.

Testing Notes

Testability of memory elements in IC designs must be considered when designing and simulating the circuits. Providing either direct or multiplexed input and output pins for controlling and observing the memory elements may greatly simplify the testing of the IC and any debugging to the system. The minimum pattern used to test a RAM should write and read both a zero and a one to every core bit. In addition, a variable pattern should be used to test for address decode faults and write disturb problems by writing the entire memory then reading it all back. One example of a variable pattern for these tests is to write the address value to each location. There are many methodologies for testing RAMs that have test time versus fault coverage trade-off. For more information on testing RAMs, refer to the AMI Application Note titled "Testing RAM Elements in IC Designs."

RASGdwyz
Self-Timed Synchronous Static RAM

AMERICAN MICROSYSTEMS, INC.

AMI8G 0.8 micron CMOS Gate Array

AC Characteristics: t(EQL) = tdx + Ktdx * EQL (TBD numbers will be available February 1994)

The data in the following examples are specified at 5.0V, T_J = 25°C, and typical process performance parameters. Performance at other operating points may be estimated by use of the voltage, process, and temperature derating curves. Contact the factory to obtain the AC characteristics and input load for different logical sizes of RAMs.

32 x 4

CHARACTERISTIC	SYMBOL	tdx (ns)	Ktdx (ns/EQL)	t(5EQL) (ns)
Min CLK high to CLK high cycle time	tcyc	5.2		
Min CLK width low	twcl	1.6		
Min CLK width high during read	twchr	1.6		
Min CLK width high during write	twchw	1.6		
Min address setup before CLK rises[1]	tasu	0.5		
Min address hold after CLK rises[1]	tah	1.7		
Min WRT setup before CLK rises	twsu	0.1		
Min WRT hold after CLK rises	twh	1.7		
Min data in setup before CLK rises	tdsu	0.1		
Min data in hold after CLK rises	tdh	1.7		
Min Q hold after CLK rises	tqh	1.2		
Max CLK rise to Q valid	tpcq	4.0	0.03	4.15
Max OEN rise to Q high impedance	toenz	1.0		
Max OEN fall to Q valid	toenq	0.7	0.03	0.85

Note: 1. If the timing terms tah and tasu are not met, the potential exists that the data in the RAM will be corrupted. This potential exists not only during the write cycle, but also during a read cycle. If the tah and/or tasu timing is violated, the simulation model will show an invalid read or write, but it may not show corrupted data during a read cycle.

RASGdwyz
Self-Timed Synchronous Static RAM

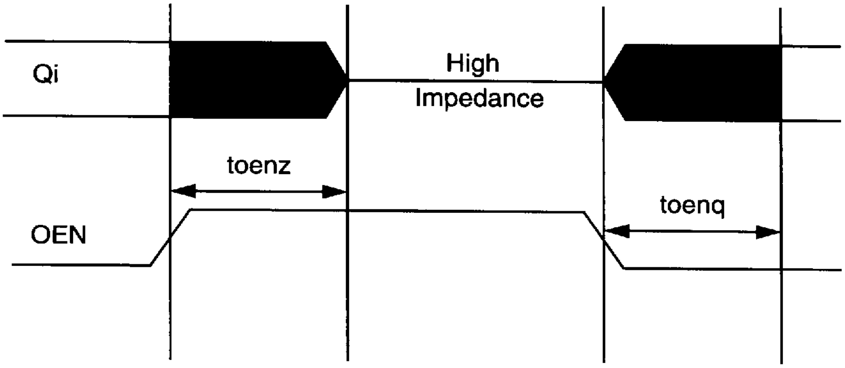
AMI8G 0.8 micron CMOS Gate Array

1K x 16

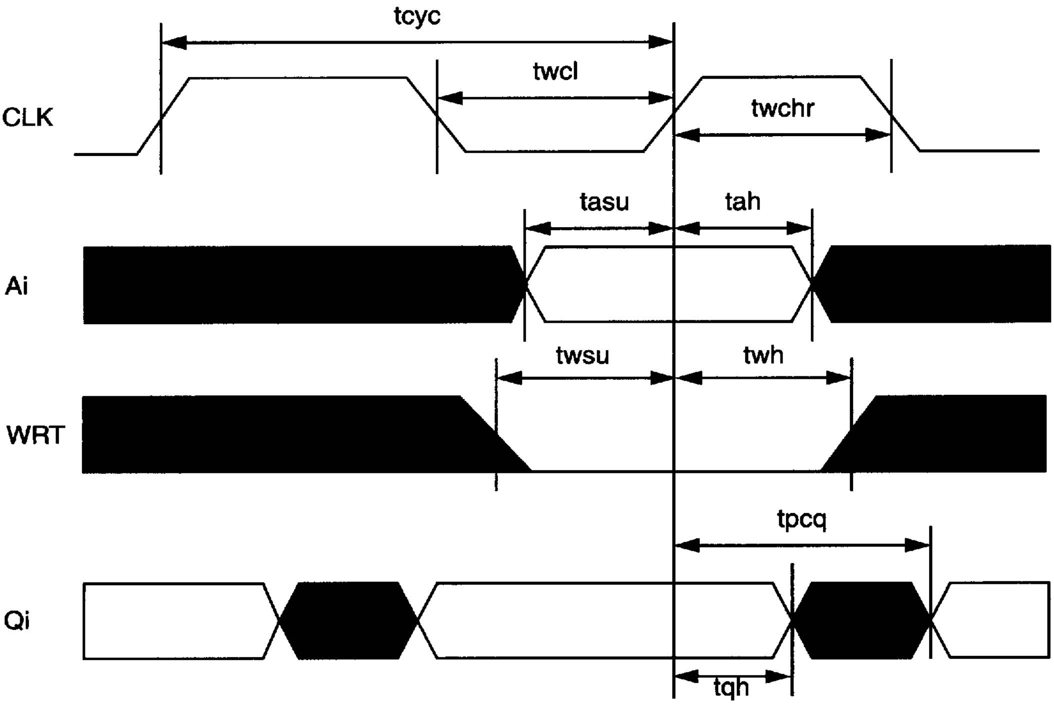
CHARACTERISTIC	SYMBOL	tdx (ns)	Ktdx (ns/EQL)	t(5EQL) (ns)
Min CLK high to CLK high cycle time	tcyc	9.6		
Min CLK width low	twcl	3.5		
Min CLK width high during read	twchr	2.0		
Min CLK width high during write	twchw	2.8		
Min address setup before CLK rises[1]	tasu	1.3		
Min address hold after CLK rises[1]	tah	2.3		
Min WRT setup before CLK rises	twsu	0.0		
Min WRT hold after CLK rises	twh	2.3		
Min data in setup before CLK rises	tdsu	0.0		
Min data in hold after CLK rises	tdh	2.3		
Min Q hold after CLK rises	tqh	1.5		
Max CLK rise to Q valid	tpcq	6.4	0.025	6.52
Max OEN rise to Q high impedance	toenz	1.4		
Max OEN fall to Q valid	toenq	0.7	0.025	0.83

Note: 1. If the timing terms tah and tasu are not met, the potential exists that the data in the RAM will be corrupted. This potential exists not only during the write cycle, but also during a read cycle. If the tah and/or tasu timing is violated, the simulation model will show an invalid read or write, but it may not show corrupted data during a read cycle.

3-State Control Timing



Read Cycle Timing



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Write Cycle Timing