1.0 INTRODUCTION

The AHA3211 is a single-chip CMOS lossless compression and decompression integrated circuit under development implementing the industry standard Data Compression Lempel Ziv (DCLZ) adaptive compression algorithm. The device processes data in compression, decompression or pass-through modes. The AHA3211 is based on the earlier 10 MBytes/sec device, AHA3210. It maintains the same pinout, performance, flexibility and I/O interface as AHA3210.

Content Addressable Memory within the DCLZ engine eliminates external SRAMs typically required for dictionary storage in a compression system. Other supporting system features include two 24-bit counters, automatic multiple-record transfer, compression ratio optimization and DCLZ error detection logic.

The DCLZ algorithm is approved by several standards organizations including QIC, DAT, ANSI, ISO and ECMA. DCLZ has been accepted by Hewlett-Packard and other system companies worldwide as their standard of choice in their tape storage peripherals. The algorithm exhibits an average compression ratio of 2 to 1 over typical computer data.

This specification contains a functional overview, operation modes, register descriptions, DC and AC Electrical characteristics, ordering information and Related Technical Publications. It is intended for hardware and software engineers designing a compression system using AHA3211.

AHA designs and develops lossless compression, forward error correction and data storage formatter/controller ICs. Technical publications are available upon request from us or our sales representatives/agents worldwide.

1.1 FEATURES

PERFORMANCE:

- 20 MBytes/sec data compression, decompression or pass-through rate with a 40 MHz clock
- 2 to 1 average compression ratio
- High compression of small records
- Automatic multiple-record transfers without microprocessor intervention
- Dynamic compression ratio monitoring
- Error checking in decompression mode reportable via an interrupt

FLEXIBILITY:

- In-Line and Look-Aside architectures supported
- Polled or interrupt driven I/O
- Two independent DMA ports programmable for 8 or 16-bit transfers; master or slave mode

SYSTEM INTERFACE:

- Single chip data compression solution
- No SRAM required
- Programmable interrupts
- Interfaces directly with AHA's tape format controller, AHA5140, and industry standard SCSI controllers

OTHERS:

- Open standard DCLZ adaptive lossless compression algorithm
- Standards include: QIC DDS-DAT, ANSI, ISO and ECMA
- Low power stand-by operation
- EIAJ-standard 100 pin plastic quad flat package
- Software emulation of the algorithm available

1.2 APPLICATIONS

- DDS-DAT, QIC, 8mm or DLT tape drives
- High performance laser printers

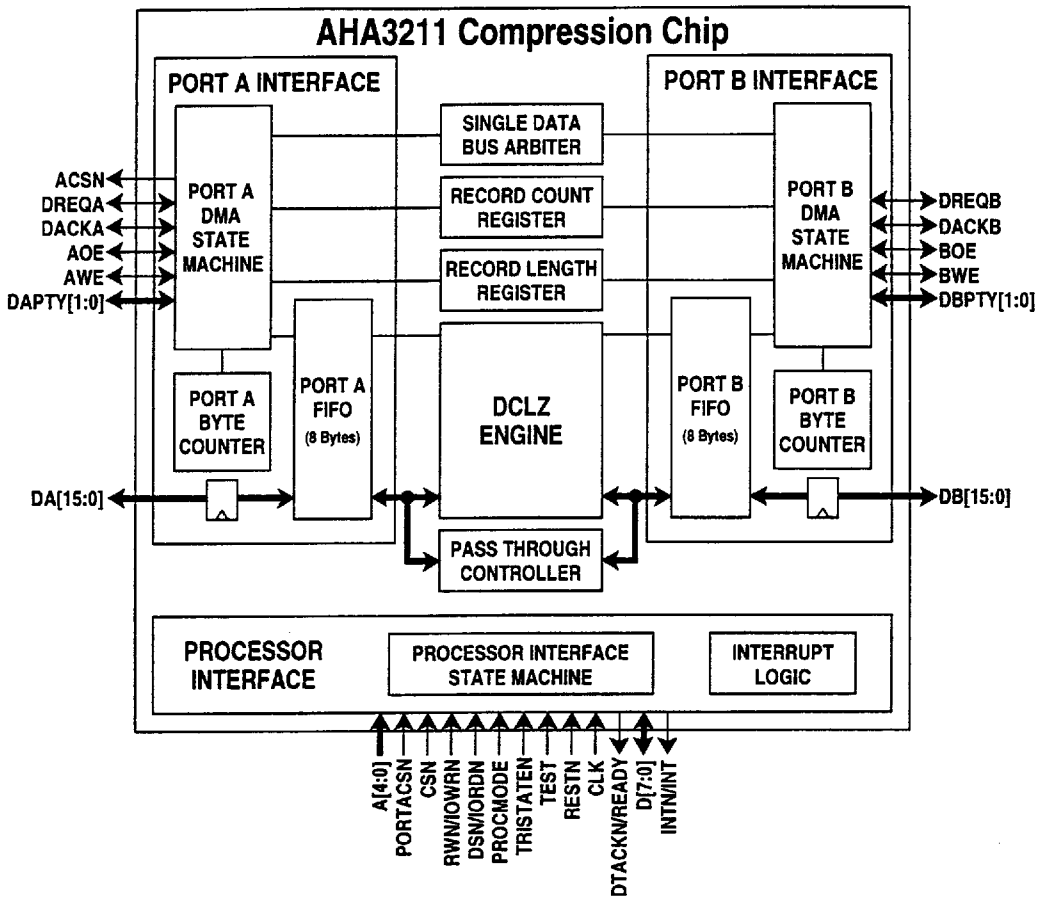
1.3 FUNCTIONAL OVERVIEW

The AHA3211 Data Compression Coprocessor IC is a high performance, single chip data compression solution, for use in tape drives, disk drives and embedded controller applications.

The processor interface is used to program the chip and monitor status via internal registers. The PROCMODE strapping pin selects between a Motorola and an Intel style processor interface.

The DCLZ Engine implements the DCLZ lossless data compression algorithm. It contains a compressor, which inputs uncompressed data from the Port A interface, compresses it, and sends the compressed codes to the Port B interface. The DCLZ Engine also contains a decompressor, which inputs compressed codes from the Port B interface, decompresses it, and sends the uncompressed data to the Port A interface. The Record Length register and Record Count register allow uncompressed data to be partitioned into fixed sized blocks, and then compressed and decompressed automatically.

Figure 1: Functional Block Diagram



The Pass Through Controller block allows data to be transferred between Port A and Port B without being compressed or decompressed.

Port A and Port B are two independent DMA interfaces. For compression and decompression operations, Port A transfers uncompressed data and Port B transfers compressed codes. Each port has a byte counter, which counts the number of bytes that are transferred through the port. The configuration of the DMA interface on each port is programmable. These functions include DMA master or slave, eight or sixteen bit transfers, and control pin enabling and polarity. The Port B Byte Count register has a Port B Byte Comparator register, allowing the chip to interrupt after a programmed amount of data has been transferred on the Port B data bus, DB[15:0]. Register accesses to a peripheral chip connected to Port A are also supported.

2.0 MODES OF OPERATION

There are two classes of the modes of operation for this chip. The first class is determined by the Port A and Port B DMA data bus configurations. Port A and Port B can be dual independent data buses, or Port A and Port B can be connected to create a single data bus. The second class is determined by the method data is processed through the chip in compression, decompression or pass through modes.

2.1 PORT A AND B PORT DATA BUS CONFIGURATION

Port A and Port B data bus configuration is controlled by the DATA BUS MODE[2:0] bits in the DMA Configuration register. These bits control the single and dual data bus modes, as well as Port A and Port B being the DMA bus master or slave (see Table 1).

Table 1: Data Bus Modes

DATA BUS MODE[2]	*DATA BUS MODE[1]*	*DATA BUS MODE[0]*	*FUNCTION*
0	0	0	Dual data bus: Port B slave, Port A slave
0	0	1	Dual data bus: Port B slave, Port A master
0	1	0	Dual data bus: Port B master, Port A slave
0	1	1	Dual data bus: Port B master, Port A master
1	0	0	Dual data bus: Port B slave, Port A slave with peripheral access
1	0	1	Reserved
1	1	0	Dual data bus: Port B master, Port A slave with peripheral access
1	1	1	Single data bus: Port B master, Port A master

2.1.1 DUAL DATA BUS MODE: IN-LINE APPLICATION

In dual data bus mode, Port A and Port B transfer data on unique, independent data buses. This is used for in-line applications, when data is transferred from the host interface, through the data compression coprocessor, and into the system buffer (see Figure 2).

In dual data bus mode, the data rate during compression is sustained at 10 MB/sec, except when the compression ratio is less than 1 (which occurs briefly when a compression dictionary is first being built, or when data is actually expanding). The data rate during decompression, pass through A to B, and pass through B to A modes is sustained at 20 MBytes/sec (see Figure 3).

2.1.2 SINGLE DATA BUS MODE: LOOK-ASIDE APPLICATION

In single data bus mode, Port A and Port B transfer data on a common data bus. This connection is made external to the chip, on the PC board. This is used in a look aside application, when the data compression coprocessor transfers data into and out of the system buffer.

2.1.3 DATA BUS WIDTH

The Data Bus widths can be programmed to 8-bits or 16-bits using the DATA BUS WIDTH bits in the *Port Control* registers. When a data bus is configured as 8-bit, the upper 8-bits and the upper parity bit must be left unconnected.

Figure 2: Dual Data Bus Mode

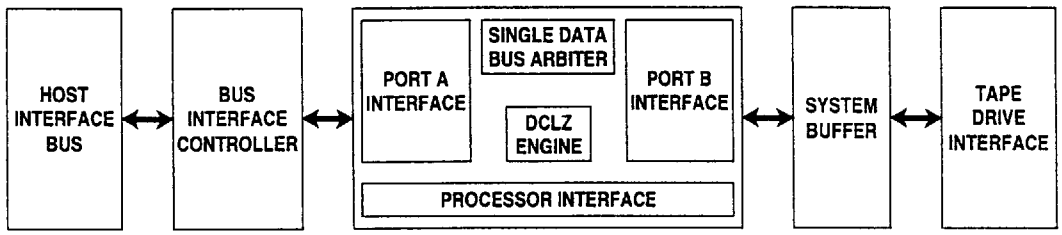
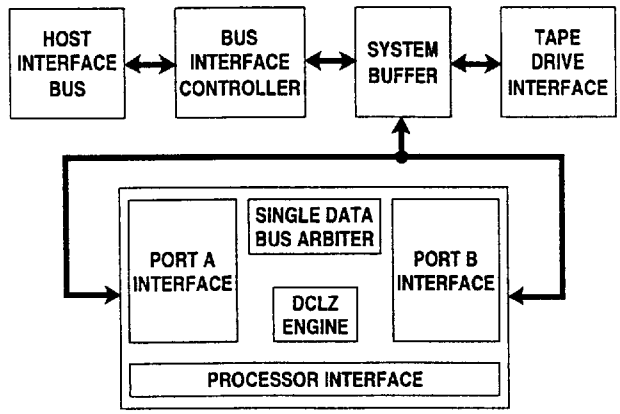


Figure 3: Single Data Bus Mode



2.1.4 PORT A PERIPHERAL CHIP INTERFACE

A peripheral chip can be connected to Port A, and have its registers accessed through the processor interface of the data compression chip (see Figure 4). This is used in in-line applications, for peripheral chips with a common DMA and processor data bus (such as the NCR 53C90A/B and the NCR 53C94/5/6 SCSI controllers).

It is the firmware's responsibility to ensure accesses to the peripheral chip's registers do not occur while DMA transfers are occurring on Port A. This mode is only supported when Port A is a DMA slave, in dual data bus mode.

2.2 DATA PROCESSING MODES

The data processing modes are controlled by the DCLZ MODE[2:0] bits in the DCLZ Control register.

2.2.1 COMPRESSION MODE

During compression mode, uncompressed data flows into Port A. It is then compressed by the DCLZ engine. The resulting compressed data is then transferred out of Port B (see Figure 5).

The uncompressed data is partitioned into fixed sized records. The size is stored in the Record Length register inside the chip. After a record has been compressed, an end of record codeword is inserted into the compressed data. The end of record codewords are then used during decompression, to control data flow.

Multiple records can be compressed without processor intervention. The Record Count register inside the chip stores the number of records to compress. A compression sequence has been completed after the last byte of the last record has been compressed and transferred out of Port B. This event sets the Port B End of Transfer interrupt.

Compression ratio is defined as the number of uncompressed bytes divided by the number of compressed bytes. The Port A Byte Counter counts the number of uncompressed bytes. The Port B Byte Counter counts the number of compressed bytes. The compression ratio can also be automatically controlled, by programming the Comp Ratio Optimization register.

The following sequence is used to program the chip to compress multiple, fixed size records:

- Program Record Length register
- Program Record Count register
- Program Interrupt Disable register
  - Enable PORT B END OF TRANSFER Interrupt
- Program Comp Ratio Optimization register
- Program DCLZ Control register

DCLZ MODE[2:0]	Compression
COMP RATIO OPT ENABLE	1
RESET DICT AFTER EOR	0
RESET DICT	0
PAUSE AFTER EOR	0
PAUSE	0

- The PORT B END OF TRANSFER interrupt signals compression completed

Figure 4: Port A Peripheral Chip Interface

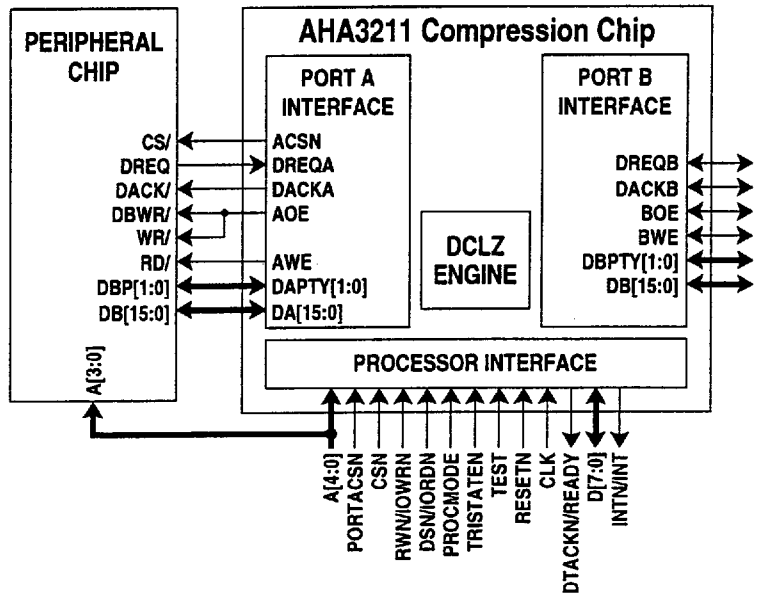
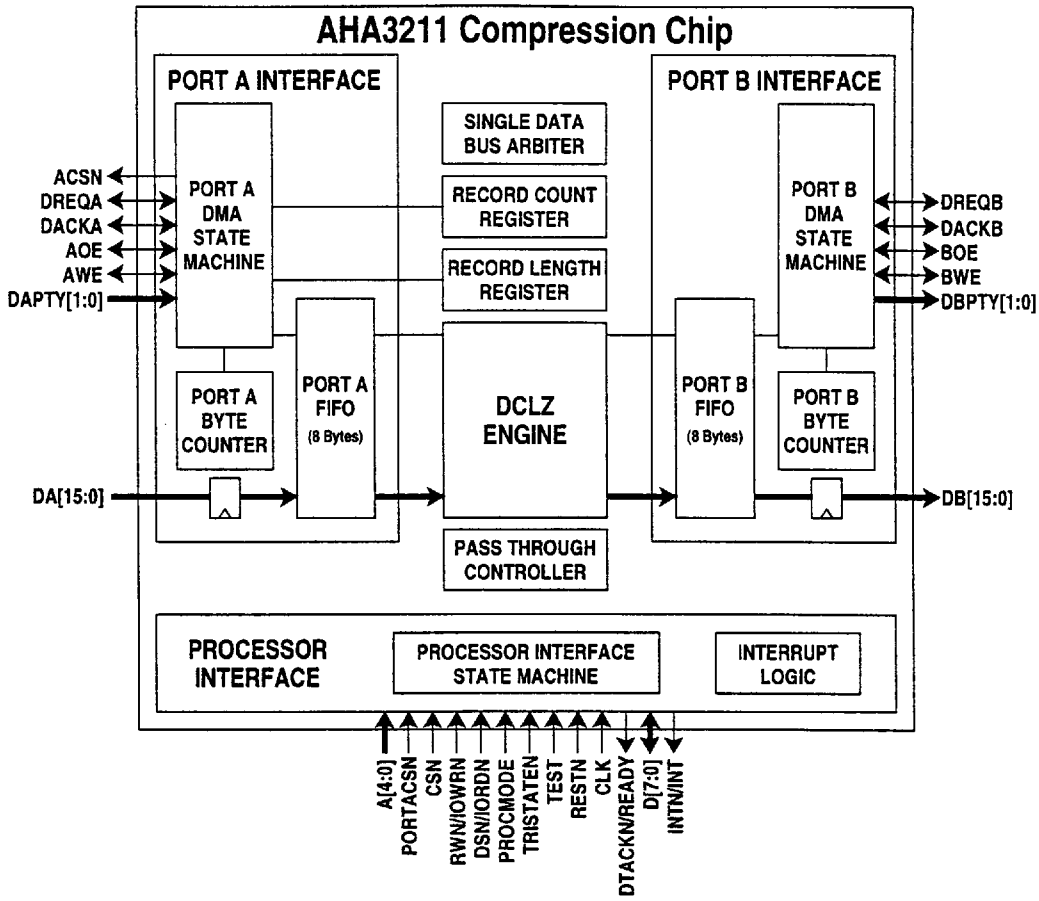


Figure 5: Compression Mode



2.2.2 COMPRESSION FLUSH MODE

Normal compression operations complete when the Record Length register and the Record Count register both decrement to zero. All data in the chip is then compressed, and transferred out of Port B. There is no data in the chip, and the chip is said to be flushed (see Figure 6).

Consider the scenario when a compression operation is required to complete prematurely (i.e., before the Record Length register and the Record Count register have both decremented to zero). In this scenario, Port A DMA is inactive, because there is no more uncompressed data to transfer into the chip. Due to the DCLZ data compression algorithm, there may be partially compressed data in the DCLZ engine at this time.

Compression flush mode is used to complete the compression operation, transfer all compressed data out of Port B, and get the chip into the flushed state. Note that the compression flush operation inserts an end of record code word at the appropriate location, near the end of the compressed data stream.

The chip should only be programmed into compression flush mode when the Port A Interface is empty (i.e., when the Port Interface Byte Count in the Port A Status register is zero) and the DCLZ engine contains data (i.e., when the DCLZ Engine Flushed bit in the DCLZ Status register is zero) and the DCLZ Engine is not already in the process of flushing (i.e., The DCLZ EOR bit in the DCLZ Status register is zero).

The following sequence is used to program the chip for Compression Flush mode for the scenario described above:

- Program DCLZ Control register

DCLZ MODE[2:0]	Compression
COMP RATIO OPT ENABLE	1
RESET DICT AFTER EOR	0
RESET DICT	0
PAUSE AFTER EOR	0
PAUSE	1

- Program Record Count register to 000000 hex
- Program Interrupt Disable register
  - Enable PORT B END OF TRANSFER Interrupt
- If the DCLZ Engine Flushed bit is zero and the DCLZ EOR bit is zero, then there is data in the DCLZ Engine to transfer out via compression flush mode.

  BEGIN
  - Program DCLZ Control register

DCLZ MODE[2:0]	Compression flush
COMP RATIO OPT ENABLE	1
RESET DICT AFTER EOR	0
RESET DICT	0
PAUSE AFTER EOR	0
PAUSE	0

  - The PORT B END OF TRANSFER interrupt signals compression completed

  END
- If the DCLZ Engine Flushed bit is zero and the DCLZ EOR bit is one, then the DCLZ Engine is already in the process of flushing.

  BEGIN
  - Program DCLZ Control register

DCLZ MODE[2:0]	Compression
COMP RATIO OPT ENABLE	1
RESET DICT AFTER EOR	0
RESET DICT	0
PAUSE AFTER EOR	0
PAUSE	0

  - The PORT B END OF TRANSFER interrupt signals compression completed

  END
- If the DCLZ Engine Flushed bit is one and the Port B Interface Byte Count is not zero, then there is data in the Port B Interface to transfer out.

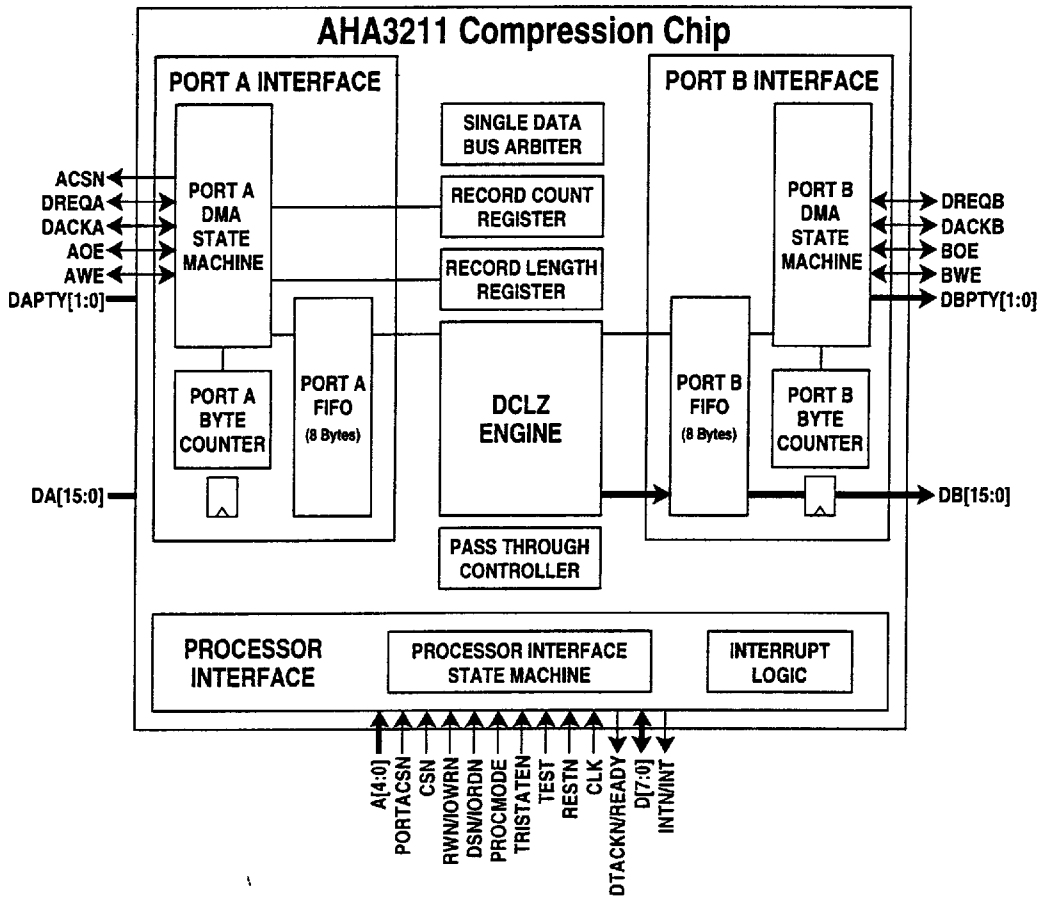
  BEGIN
  - Program DCLZ Control register

DCLZ MODE[2:0]	Compression
COMP RATIO OPT ENABLE	1
RESET DICT AFTER EOR	0
RESET DICT	0
PAUSE AFTER EOR	0
PAUSE	0

  - The PORT B END OF TRANSFER interrupt signals compression completed

  END
- If the DCLZ Engine Flushed bit is one and the Port B Interface Byte Count is zero, then the DCLZ Engine and the Port B Interface are already flushed.

Figure 6: Compression Flush Mode



2.2.3 DECOMPRESSION MODE

During decompression mode, compressed data flows into Port B. It is then uncompressed by the DCLZ engine. The resulting uncompressed data is then transferred out of Port A.

The compressed data is partitioned into records, with End of Record codewords embedded in the compressed data. Multiple records can be automatically decompressed, by programming the number of records into the Record Count register. A decompression sequence has been completed after the last byte of the last record has been uncompressed and then transferred out of Port A. This event sets the Port A End of Transfer interrupt.

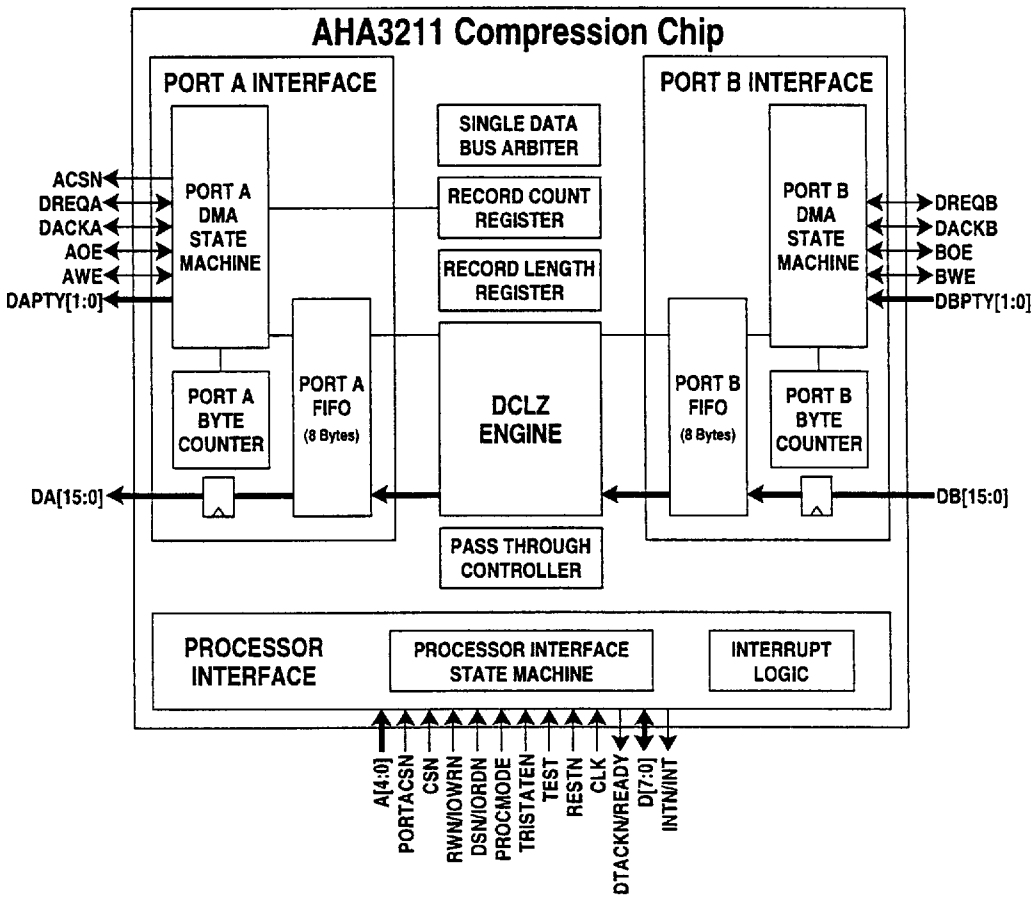
The following sequence is used to program the chip to decompress multiple records:

- Program Record Count register
- Program Interrupt Disable register
  - Enable PORT A END OF TRANSFER Interrupt
- Program DCLZ Control register

DCLZ MODE[2:0]	Decompression
COMP RATIO OPT ENABLE	0
RESET DICT AFTER EOR	0
RESET DICT	0
PAUSE AFTER EOR	0
PAUSE	0

- The PORT A END OF TRANSFER Interrupt signals decompression completed

Figure 7: Decompression Mode



2.2.4 DECOMPRESSION OUTPUT DISABLED MODE

The DCLZ algorithm allows the compression dictionary to be shared between multiple records. To decompress records in the middle of a multiple record sequence, the preceding records must first be decompressed, in order to properly build the compression dictionary.

Decompression output disabled mode allows the preceding records to be decompressed, while discarding the unwanted uncompressed data. Once this is completed, the chip can be programmed to decompression mode, to decompress and output the desired records.

In decompression output disabled mode, the data is discarded between the Port A Interface and the Port A pins. Port A DMA remains inactive. The Port B Byte Counter, the Port A Byte Counter, the Port B Interface Byte Count, the Port A Interface Byte Count, the Record Count register, and the Port A End of Transfer Interrupt operate as in decompression mode. It is recommended that the Port A Interface be empty and the chip paused before switching between decompression output disabled and decompression modes.

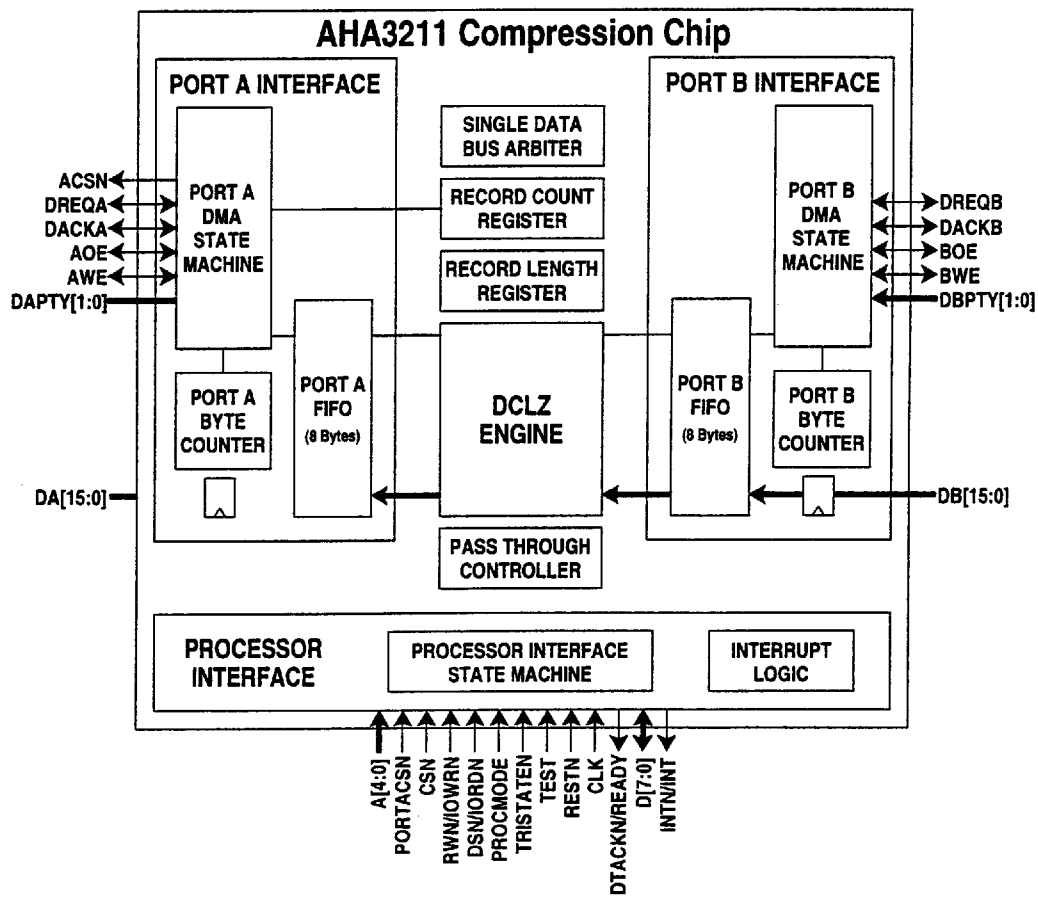
The following sequence is used to program the chip to decompress multiple records in output disabled mode:

- Program Record Count register
- Program Interrupt Disable register
  - Enable PORT A END OF TRANSFER Interrupt
- Program DCLZ Control register

DCLZ MODE[2:0]	Decomp; Output Disabled Mode
COMP RATIO OPT ENABLE	0
RESET DICT AFTER EOR	0
RESET DICT	0
PAUSE AFTER EOR	0
PAUSE	0

- The PORT A END OF TRANSFER Interrupt signals decompression output disabled completed

Figure 8: Decompression Output Disabled Mode



2.2.5 PASS THROUGH A TO B MODE

During pass through A to B mode, data enters Port A, is transferred through the Port A Interface and the Port B Interface, and then transferred out of Port B. The data is not altered as it passes through the chip.

The Record Length register determines the number of bytes in a record. The Record Count register determines the number of records. Multiply the values of these two registers to determine the total number of bytes that will be transferred through the chip. The pass through sequence has been completed after the last byte of the last record has been transferred out of Port B. This event sets the Port B End of Transfer interrupt.

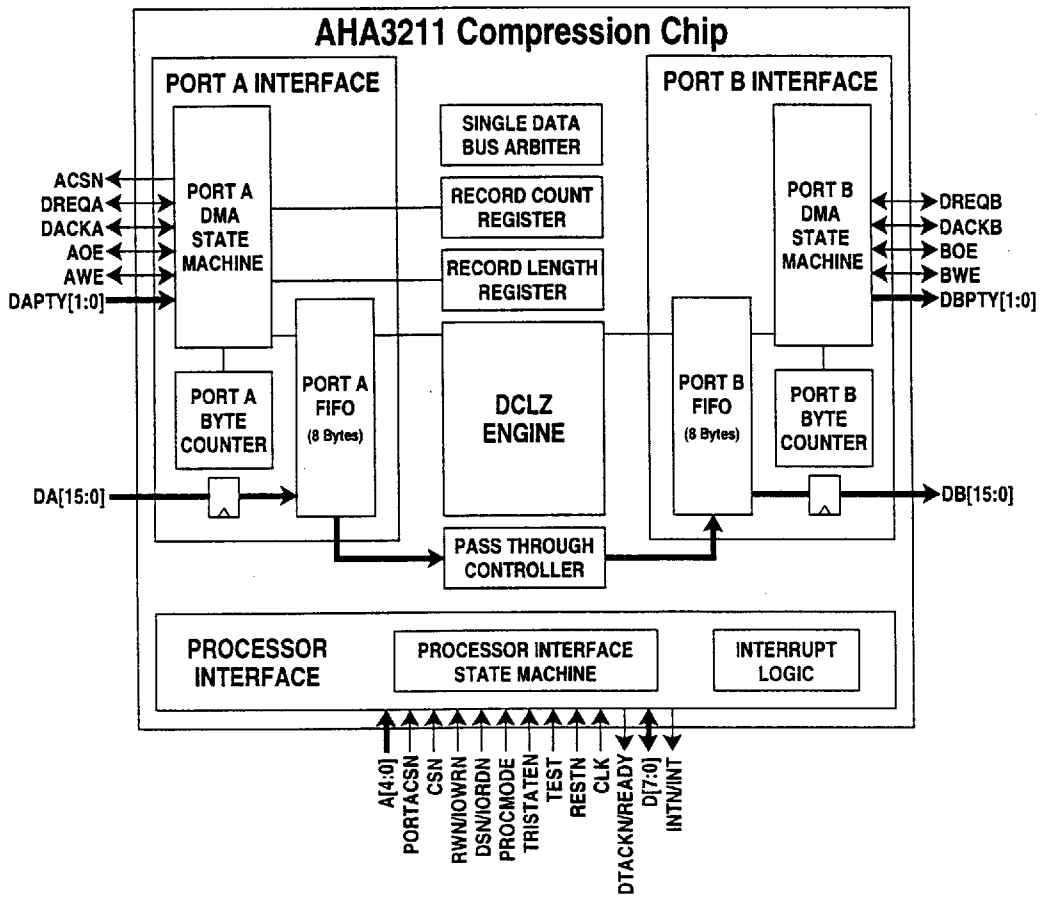
The following sequence is used to program the chip to pass through data from Port A to Port B:

- Program Record Length register
- Program Record Count register
- Program Interrupt Disable register
  - Enable PORT B END OF TRANSFER Interrupt
- Program DCLZ Control register

DCLZ MODE[2:0]	Pass through A to B
COMP RATIO OPT ENABLE	0
RESET DICT AFTER EOR	0
RESET DICT	0
PAUSE AFTER EOR	0
PAUSE	0

- The PORT B END OF TRANSFER interrupt signals pass through A to B completed

Figure 9: Pass Through A to B Mode



2.2.6 PASS THROUGH B TO A MODE

During pass through B to A mode, data enters Port B, is transferred through the Port B Interface and Port A Interface, and is then transferred out of Port A. The data is not altered as it passes through the chip.

The Record Length register determines the number of bytes in a record. The Record Count register determines the number of records. Multiply the values of these two registers to determine the total number of bytes that will be transferred through the chip. The pass through sequence has been completed after the last byte of the last record has been transferred out of Port A. This event sets the Port A End of Transfer interrupt.

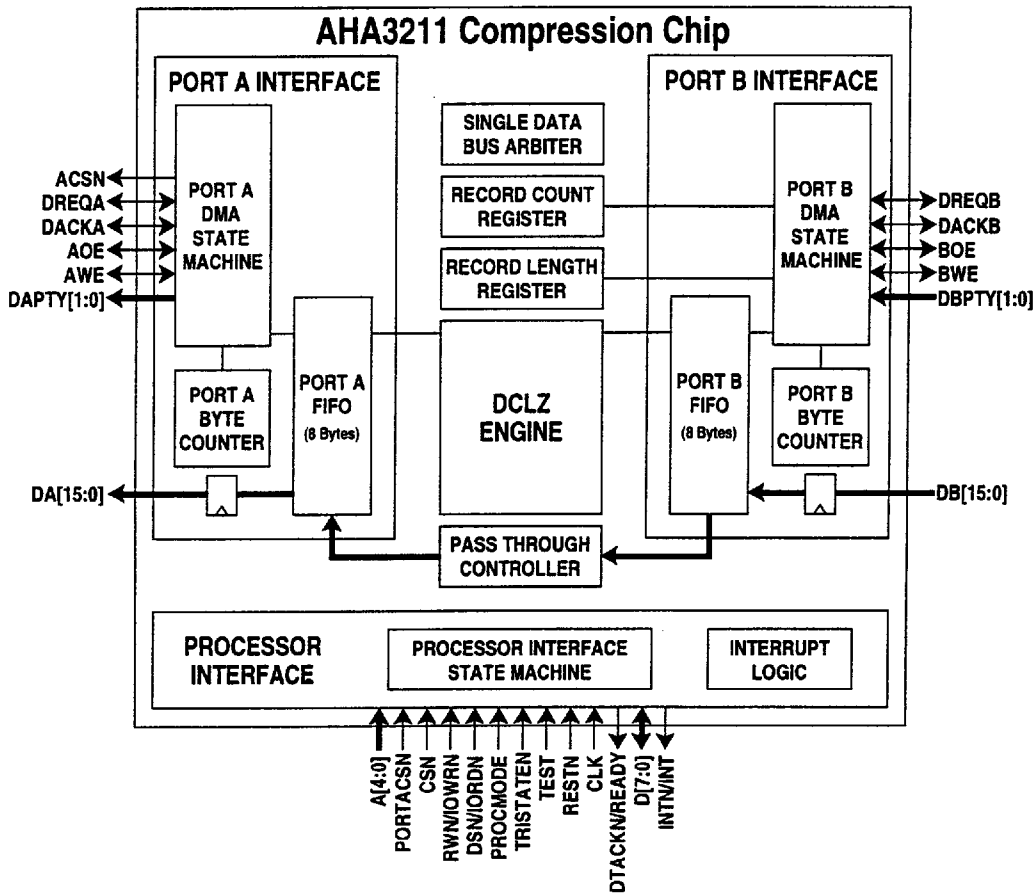
The following sequence is used to program the chip to pass through data from Port B to Port A:

- Program Record Length register
- Program Record Count register
- Program Interrupt Disable register
  - Enable PORT A END OF TRANSFER Interrupt
- Program DCLZ Control register

DCLZ MODE[2:0]	Pass through B to A
COMP RATIO OPT ENABLE	0
RESET DICT AFTER EOR	0
RESET DICT	0
PAUSE AFTER EOR	0
PAUSE	0

- The PORT A END OF TRANSFER interrupt signals pass through B to A completed

Figure 10: Pass Through B to A Mode



3.0 REGISTER DESCRIPTION

Table 2: Register Address Map

ADDRESS	READ	WRITE	HARD RESET	SOFT** RESET
0x00	DCLZ Control	DCLZ Control	1110,0000	111U,UUUU
0x01	DCLZ Status	*Reserved*	0000,0011	0000,0011
0x02	Comp Ratio Optimization	Comp Ratio Optimization	0000,0000	Unchanged
0x03	*DMA Configuration	DMA Configuration	0000,0101	Unchanged
0x04	Port A Control 0	Port A Control 0	0000,0000	Unchanged
0x05	*Port A Control 1	Port A Control 1	x000,00xx	Unchanged
0x06	Port A Status	*Reserved*	0000,0000	0U00,0000
0x07	Port A Byte Count [7:0]	Port A Byte Count [7:0]	0000,0000	Unchanged
0x08	Port A Byte Count [15:8]	Port A Byte Count [15:8]	0000,0000	Unchanged
0x09	Port A Byte Count [23:16]	Port A Byte Count [23:16]	0000,0000	Unchanged
0x0A	Port B Control 0	Port B Control 0	0000,0000	Unchanged
0x0B	*Port B Control 1	Port B Control 1	x000,00xx	Unchanged
0x0C	Port B Status	*Reserved*	0000,0000	0U00,0000
0x0D	Port B Byte Count [7:0]	Port B Byte Count [7:0]	0000,0000	Unchanged
0x0E	Port B Byte Count [15:8]	Port B Byte Count [15:8]	0000,0000	Unchanged
0x0F	Port B Byte Count [23:16]	Port B Byte Count [23:16]	0000,0000	Unchanged
0x10	Port B Byte Comparator [7:0]	Port B Byte Comparator [7:0]	Undefined	Unchanged
0x11	Port B Byte Comparator [15:8]	Port B Byte Comparator [15:8]	Undefined	Unchanged
0x12	Port B Byte Comparator [23:16]	Port B Byte Comparator [23:16]	Undefined	Unchanged
0x13	Record Length [7:0]	Record Length [7:0]	Undefined	Unchanged
0x14	Record Length [15:8]	Record Length [15:8]	Undefined	Unchanged
0x15	Record Length [23:16]	Record Length [23:16]	Undefined	Unchanged
0x16	Record Count [7:0]	Record Count [7:0]	Undefined	Unchanged
0x17	Record Count [15:8]	Record Count [15:8]	Undefined	Unchanged
0x18	Record Count [23:16]	Record Count [23:16]	Undefined	Unchanged
0x19	Interrupt Status	Interrupt Clear	0000,0000	Unchanged
0x1A	*Interrupt Disable	Interrupt Disable	0011,1111	Unchanged
0x1F	Identification	*Reserved*	Y	Y

Notations:

* *These registers have one or more reserved bits set to '0'. These registers read back '0' from these reserved bits.*

** *A soft reset is generated by writing a reset command to DCLZ MODE[2:0].*

U - These bits remain unchanged after a soft reset.

x - Indicates undefined bit.

Y - Contact AHA Applications Engineering.

3.1 DCLZ CONTROL: ADDRESS 00 HEX - READ/WRITE

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00	DCLZ MODE[2:0]			COMP RATIO OPT ENABLE	RESET DICT AFTER EOR	RESET DICT	PAUSE AFTER EOR	PAUSE

DCLZ MODE[2:0] = DCLZ Control register [7:5]:

The DCLZ MODE bits determine how the chip will process data as follows.

- Pass through modes transfer data through the chip without any compression or decompression operation. Pass through A to B transfers data into Port A and out of Port B. Pass through B to A transfers data into Port B and out of Port A.
- Compression mode transfers uncompressed data into Port A, compresses it, and transfers compressed data out of Port B.
- Compression flush mode causes all data in the DCLZ Engine to be compressed including an end of record codeword, and then flushed out of the chip through Port B.
- Decompression mode transfers compressed data into Port B, decompresses it, and transfers uncompressed data out of Port A.
- Decompression output disabled mode transfers compressed data into Port B, decompresses it and builds the decompression dictionary, but does not transfer any uncompressed data out of Port A.
- Reset mode resets all state machines and data in Port A, Port B, single data bus arbiter, and the DCLZ engine. It also resets the dictionary. It resets the registers as shown in Table 2.

The DCLZ Control bits should always be programmed to the reset mode, when switching between all modes, except between compression and compression flush modes and between decompression and decompression output disabled modes. It is recommended that the Port A Interface be empty and the chip paused before switching between decompression output disabled and decompression modes. The DCLZ MODE bits are set to one when the chip is reset from the RESETN pin. The DCLZ MODE bits are decoded as shown below:

Table 3: DCLZ Mode Bit Decode

DCLZ MODE[2]	DCLZ MODE[1]	DCLZ MODE[0]	FUNCTION
0	0	0	Pass through A to B
0	0	1	Pass through B to A
0	1	0	Compression
0	1	1	Compression flush
1	0	0	Decompression
1	0	1	Decompression output disable
1	1	0	Reserved
1	1	1	Reset

COMP RATIO OPT ENABLE:

The COMPRESSION RATIO OPTIMIZATION ENABLE bit enables the automatic compression ratio optimizer during compression. This bit enables the THRESH[5:0] and PERIOD[1:0] bits in the Comp Ratio Optimization register. A one enables optimization, and a zero disables optimization. This bit is cleared to zero when the chip is reset from the RESETN pin.

RESET DICT AFTER EOR:

During compression, the RESET DICTIONARY AFTER END OF RECORD bit causes the DCLZ engine to reset the compression dictionary after each end of record, and before the first subsequent byte which is not designated as an end of record. A one resets the dictionary after end of record, and a zero has no effect on the dictionary. This bit is cleared to zero when the chip is reset from the RESETN pin.

RESET DICT

The RESET DICTIONARY bit causes the compression dictionary to be reset after completing the current byte, and before the next byte which is not designated as an end of record. A one causes the dictionary to be reset, and a zero has no effect on the dictionary. The RESET DICT bit will be automatically cleared, once a dictionary reset has occurred. This bit is cleared to zero when the chip is reset from the RESETN pin.

PAUSE AFTER EOR:

Writing a one to the PAUSE AFTER END OF RECORD bit causes the Port A interface, the DCLZ Engine and the Port B interface to pause after each end of record has been processed. The PAUSED status bit in the DCLZ Status register is then set. To allow the chip to continue, a zero must be written to the PAUSE bit. This bit is cleared to zero when the chip is reset from the RESETN pin.

PAUSE:

Writing a one to the PAUSE bit causes the Port A interface, the DCLZ Engine, and the Port B interface to pause. The PAUSED status bit in the DCLZ Status register is then set. Writing a zero to the PAUSE bit allows the chip to resume operation after it has been paused or paused after end of record. PAUSE bit operation is supported during processor write cycles which program the DCLZ Control bits out of the Reset state. This bit is cleared to zero when the chip is reset from the RESETN pin.

Table 4: Supported Modes for DCLZ Control Register Bits

MODE	*COMP RATIO OPT ENABLE*	*RESET DICT AFTER EOR*	*RESET DICT*	*PAUSE AFTER EOR*	*PAUSE*
Compression	YES	YES	YES	YES	YES
Compression flush	YES	YES	YES	YES	YES
Decompression	NO	NO	NO	YES	YES
Decompression output disabled	NO	NO	NO	YES	YES
Pass through A to B	NO	NO	NO	YES	YES
Pass through B to A	NO	NO	NO	YES	YES

3.2 DCLZ STATUS: ADDRESS 01 HEX - READ ONLY

	bit7	*bit6*	*bit5*	*bit4*	*bit3*	*bit2*	*bit1*	*bit0*
0x01	res					DCLZ EOR	DCLZ ENGINE FLUSHED	PAUSED

res - Reserved. Bits read back zeros.

DCLZ EOR:

The DCLZ EOR bit indicates if an end of record is in the DCLZ Engine. This bit operates in compression, compression flush, decompression, and decompression output disabled mode. This bit is cleared to zero when the reset or pass through A to B or pass through B to A code is programmed to the DCLZ MODE bits in the DCLZ Control register, or when the chip is reset by the RESETN pin. The DCLZ EOR bit can transition frequently when the DCLZ Engine is actively processing data (i.e., when it is not paused). Therefore, the DCLZ EOR bit should only be considered valid when the PAUSED bit is one.

DCLZ ENGINE FLUSHED:

This bit operates in compression, compression flush, decompression, and decompression output disabled modes only. When the DCLZ ENGINE FLUSHED bit is a one, there is no data in the DCLZ Engine. This occurs after an end of record has been processed through the DCLZ Engine, and before the first byte of the next record has entered the DCLZ Engine. Once the first byte of the next record enters the DCLZ Engine, the DCLZ ENGINE FLUSHED bit is cleared to zero. The DCLZ ENGINE FLUSHED bit is set to one when the DCLZ MODE bits are programmed to pass through A to B, pass through B to A, or reset mode. Also, the DCLZ ENGINE FLUSHED bit is set to one when the chip is reset by the RESETN pin. The DCLZ ENGINE FLUSHED bit can transition frequently when the DCLZ Engine is actively processing data (i.e., when it is not paused). Therefore, the DCLZ ENGINE FLUSHED bit should only be considered valid when the PAUSED bit is one.

PAUSED:

When the PAUSED bit is one, the Port A interface, the DCLZ Engine, and the Port B interface are paused. The Port A Byte Count registers, the Port B Byte Count registers, the Port A Status register, the Port B Status register, the Record Length registers, and the Record Count registers are stable at this time. This bit is set to one when the chip is reset from the RESETN pin, or when the DCLZ Control bits are programmed to the Reset state.

3.3 COMP RATIO OPTIMIZATION: ADDRESS 02 HEX - READ/WRITE

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x02	THRESH[5:0]						PERIOD[1:0]	

This register is used to control the compression ratio during compression mode, by automatically resetting the compression dictionary if the compression ratio is below the programmed threshold. If the compression dictionary is less than half full the optimization circuit will check for expanding data every 1024 input bytes and reset the dictionary if expansion occurs. After the dictionary is greater than half full, the optimizer will check the compression ratio against a threshold every n bytes, where n is determined by the value of the PERIOD bits. The threshold is set by the value of the THRESH bits. Optimization is enabled by setting COMP RATIO OPT ENABLE bit in the DCLZ Control register. The compression ratio is specified by the threshold bits according to the following formula:

$$\text{compression ratio} = \frac{64}{64 - \text{THRESH}}$$

For example, if THRESH is set at 32 the compression ratio is 2. This compression ratio is a target. After every N number of bytes as specified by the PERIOD field has been input, the actual compression ratio is checked against the target. If the actual is less than the target, the dictionary is automatically reset. The THRESH[5:0] and PERIOD[1:0] bits are zero when the chip is reset by the RESETN pin.

PERIOD		
bit 1	bit 0	Size
0	0	512 bytes
0	1	1024 bytes
1	0	2048 bytes
1	1	4096 bytes

COMPRESSION RANGES	
Compression Ratio	Threshold Value
1 → 2	0 → 32
2 → 3	33 → 42
3 → 4	43 → 48
4 → 8	49 → 56
8 → 64	57 → 63

3.4 DMA CONFIGURATION: ADDRESS 03 HEX - READ/WRITE

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x03	FASA	FASB	res			DATA BUS MODE[2:0]		

FASA:

When asserted, this bit shortens the DACKA active time from three clock periods down to two clock periods.

FASB:

When asserted, this bit shortens the DACKB active time from three clock periods down to two clock periods.

res -Reserved. Bits must always be written with zeros. They read back zeros.

DATA BUS MODE [2:0]:

The DATA BUS MODE bits determine the data configuration for the Port A and Port B DMA buses. In dual data bus mode, Port A and Port B are independent, isolated data buses. Data transfers on each bus may occur simultaneously. In this mode, Port A and Port B can be any combination of DMA bus masters or slaves. This mode is intended for in line applications. In single bus mode, the Port A and Port B data buses are connected together on the PC board.

Both Port A and Port B are DMA bus masters. The Single Data Bus Arbiter circuit inside the chip resolves all bus contention on this single data bus. Port A and Port B will never simultaneously request the data bus in this mode. This mode is intended for look aside applications.

The Port A interface supports register accesses to a peripheral chip on the Port A data bus. register and DMA accesses between the Port A interface and the peripheral chip occur on a single data bus, DA[7:0]. This mode is only supported when Port A is a DMA slave in dual data bus mode.

Data bus mode bits are set to 101 after the chip is reset by RESETN.

Table 5: DATA BUS MODE Bit Decode

DATA BUS MODE[2]	*DATA BUS MODE[1]*	*DATA BUS MODE[0]*	*FUNCTION*
0	0	0	Dual data bus: Port B slave, Port A slave
0	0	1	Dual data bus: Port B slave, Port A master
0	1	0	Dual data bus: Port B master, Port A slave
0	1	1	Dual data bus: Port B master, Port A master
1	0	0	Dual data bus: Port B slave, Port A slave with peripheral access
1	0	1	Reserved
1	1	0	Dual data bus: Port B master, Port A slave with peripheral access
1	1	1	Single data bus: Port B master, Port A master

The Port A and Port B DMA control pins change direction, based on the master or slave mode. The following table shows the DMA control pin direction for DMA bus master and slave modes: Port A DMA Bus Master/Slave Pin Configuration

Table 6: Port A DMA Bus Master/Slave Pin Configuration

PIN NAME	*PORT A DMA BUS MASTER*	*PORT A DMA BUS SLAVE*
DREQA	Output	Input
DACKA	Input	Output
AOE	Input	Output
AWE	Input	Output

Table 7: Port B DMA Bus Master/Slave Pin Configuration

PIN NAME	*PORT B DMA BUS MASTER*	*PORT B DMA BUS SLAVE*
DREQB	Output	Input
DACKB	Input	Output
BOE	Input	Output
BWE	Input	Output

3.5 PORT A CONTROL 0: ADDRESS 04 HEX - READ/WRITE

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x04	ENABLE DA PULLUP	ENABLE DAPTY PULLUP	AWE ENABLE	AOE ENABLE	AWE POLARITY	AOE POLARITY	DREQA POLARITY	DACKA POLARITY

ENABLE DA PULLUP:
A one enables the pullups on the DA[15:0] pins. A zero tristates the pullups on the DA[15:0] pins. This bit is cleared to zero when the chip is reset by the RESETN pin.

ENABLE DAPTY PULLUP:
A one enables the pullups on the DAPTY[1:0] pins. A zero tristates the pullups on the DAPTY[1:0] pins. This bit is cleared to zero when the chip is reset by the RESETN pin.

AWE ENABLE:
A one enables the AWE input when Port A is a DMA bus master, and enables the AWE output when Port A is a DMA bus slave. A zero disables the AWE input when Port A is a DMA bus master, and tristates the AWE output when Port A is a DMA bus slave. This bit is cleared to zero when the chip is reset by the RESETN pin.

AOE ENABLE:
A one enables the AOE input when Port A is a DMA bus master, and enables the AOE output when Port A is a DMA bus slave. A zero disables the AOE input when Port A is a DMA bus master, and tristates the AOE output when Port A is a DMA bus slave. This bit is cleared to zero when the chip is reset by the RESETN pin.

AWE POLARITY:
A one makes AWE high active. A zero makes AWE low active. This bit is cleared to zero when the chip is reset by the RESETN pin.

AOE POLARITY:
A one makes AOE high active. A zero makes AOE low active. This bit is cleared to zero when the chip is reset by the RESETN pin.

DREQA POLARITY:
A one makes DREQA high active. A zero makes DREQA low active. This bit is cleared to zero when the chip is reset by the RESETN pin.

DACKA POLARITY:
A one makes DACKA high active. A zero makes DACKA low active. This bit is cleared to zero when the chip is reset by the RESETN pin.

3.6 PORT A CONTROL 1: ADDRESS 05 HEX - READ/WRITE

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x05	DATA BUS WIDTH	DATA15TO8	res	PORT A DISABLE	CLEAR INTERFACE	CLEAR BYTE COUNTER	ENABLE PARITY	ODD PARITY

DATA BUS WIDTH:
A one makes the Port A data bus 16 bits wide, with data transferred on the DA[15:0] pins. A zero makes the Port A data bus 8 bits wide, with data transferred on the DA[7:0] pins. This bit should only be changed after the reset code has been programmed to the DCLZ Control bits in the DCLZ Control register. This bit is undefined when the chip is reset from the RESETN pin.

DATA15TO8:
The DATA15TO8 bit causes one byte to be transferred on DA[15:8] on the next DMA cycle into or out of Port A, when Port A is in 16 bit mode. The intended use of this bit is to transfer a single byte on DA[15:8] only during the first DMA cycle of a contiguous data transfer sequence. The DATA15TO8 bit only functions when Port A is in 16 bit mode, and is ignored when Port A is in 8 bit mode. The DATA15TO8

bit should only be changed after the reset code has been programmed into the DCLZ Control bits in the DCLZ Control register, or after the chip has paused after end of record, or after the chip has paused because the Port A or Port B end of transfer interrupt has occurred. DATA15TO8 takes effect only on the next DMA cycle, which is defined as the next occurrence when DACKA pulses active, and is supported when Port A is a DMA bus master or a DMA bus slave. After the DMA cycle occurs, the DATA15TO8 bit is automatically cleared. DATA15TO8 is cleared to zero when the chip is reset from the RESETN pin.

res -Reserved. Bit must always be written with a zero. It reads back a zero.

PORT A DISABLE:

A one disables the Port A control and data buses. The Port A output control signals are made hi-impedance. The Port A input control signals are ignored. The DA[15:0] and DAPTY[1:0] data pins are put into a hi-impedance state and any transitions on them are ignored. A zero in this bit position places Port A into normal operational mode. This bit should only be changed while the chip is paused at an End of Transfer condition. The contents of the DCLZ Control register, the DMA Configuration register, and the Port A Control 0 register, should not be changed while this bit is a one. This bit is cleared to zero when the chip is reset from the RESETN pin.

CLEAR INTERFACE:

Writing a one creates a pulse, which clears the Port A Interface. Writing a zero has no effect on the Port A Interface. This bit is always a zero when it is read. The CLEAR INTERFACE bit is intended to be used only when the chip has paused after end of record, or paused because the Port A or Port B end of transfer interrupt has occurred.

CLEAR BYTE COUNTER:

Writing a one creates a pulse, which clears the Port A Byte Count register. Writing a zero has no effect on the Port A Byte Count register. This bit is always a zero when it is read.

ENABLE PARITY:

A one enables parity on DAPTY[1:0] when Port A is in 16 bit mode, and on DAPTY[0] when Port A is in 8 bit mode. Writing a zero disables parity on Port A. This bit is undefined when the chip is reset from the RESETN pin.

ODD PARITY:

A one selects odd parity on Port A. A zero selects even parity on Port A. This bit is undefined when the chip is reset from the RESETN pin.

3.7 PORT A STATUS: ADDRESS 06 HEX - READ ONLY

	bit7	*bit6*	*bit5*	*bit4*	*bit3*	*bit2*	*bit1*	*bit0*
0x06	res	DATA7TO0	EOR COUNT[1:0]		INTERFACE BYTE COUNT[3:0]			

res -Reserved. Bit reads back zero.

DATA7TO0:

When Port A is in 16 bit mode, the DATA7TO0 bit shows whether the last DMA cycle of a data transfer sequence out of Port A contains one or two valid bytes. This occurs for the last byte of the last record, as determined by the Record Count register. If the last byte of the last record is the first byte in the sequence to output a word, that byte is output on DA[7:0], the data on DA[15:8] is undefined, and the DATA7TO0 bit is set. If the last byte of the last record is the second byte in the sequence to output a word, the second to last byte is output on DA[7:0], the last byte is output on DA[15:8], and the DATA7TO0 bit is cleared. The DATA7TO0 bit is cleared during all DMA cycles into Port A, during all DMA cycles when Port A is in 8 bit mode, and when the chip is reset from the RESETN pin.

EOR COUNT[1:0]:

The EOR COUNT[1:0] bits show the number of bytes with active end of record flags contained in the Port A Interface. These bits operate in compression, compression flush, decompression, decompression output disabled, pass through A to B, and pass through B to A modes. These bits are cleared to zero when a one is written to the CLEAR INTERFACE bit in Port A Control 1 register, or when the reset code is programmed to the DCLZ MODE bits in the DCLZ Control register, or when the chip is reset by the RESETN pin. During data transfers, these bits should only be read when the PAUSED bit in the DCLZ Status register is a one.

INTERFACE BYTE COUNT[3:0]:

The INTERFACE BYTE COUNT[3:0] bits show the number of bytes that are held in the Port A Interface. These bits are cleared to zero when a one is written to the CLEAR INTERFACE bit in Port A Control 1 register, or when the reset code is programmed to the DCLZ MODE bits in the DCLZ Control register, or when the chip is reset by the RESETN pin. During data transfers, these bits should only be read when the PAUSED bit in the DCLZ Status register is a one.

3.8 PORT A BYTE COUNT: ADDRESS 07,08,09 HEX - READ/WRITE

Least Significant Byte (address 07 hex):

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x07	[7:0]							

Middle Byte (address 08 hex)

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x08	[15:8]							

Most Significant Byte (address 09 hex):

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x09	[23:16]							

The Port A Byte Count register counts the number of bytes that are transferred by the Port A DMA State Machine. This register counts in compression, compression flush, decompression, decompression output disabled, pass through A to B, and pass through B to A modes. The register is cleared to zero when a one is written to the CLEAR BYTE COUNTER bit in Port A Control 1 register, or when the chip is reset by the RESETN pin. During data transfers, this register should only be written or read when the PAUSED bit in the DCLZ Status register is a one. The counter rolls over from FFFFFF hex to 000000 hex.

3.9 PORT B CONTROL 0: ADDRESS 0A HEX - READ/WRITE

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x0A	ENABLE DB PULLUP	ENABLE DBPTY PULLUP	BWE ENABLE	BOE ENABLE	BWE POLARITY	BOE POLARITY	DREQB POLARITY	DACKB POLARITY

ENABLE DB PULLUP:

A one enables the pullups on the DB[15:0] pins. A zero tristates the pullups on the DB[15:0] pins. This bit is cleared to zero when the chip is reset by the RESETN pin.

ENABLE DBPTY PULLUP:

A one enables the pullups on the DBPTY[1:0] pins. A zero tristates the pullups on the DBPTY[1:0] pins. This bit is cleared to zero when the chip is reset by the RESETN pin.

BWE ENABLE:

A one enables the BWE input when Port B is a DMA bus master, and enables the BWE output when Port B is a DMA bus slave. A zero disables the BWE input when Port B is a DMA bus master, and tristates the BWE output when Port B is a DMA bus slave. This bit is cleared to zero when the chip is reset by the RESETN pin.

BOE ENABLE:

A one enables the BOE input when Port B is a DMA bus master, and enables the BOE output when Port B is a DMA bus slave. A zero disables the BOE input when Port B is a DMA bus master, and tristates the BOE output when Port B is a DMA bus slave. This bit is cleared to zero when the chip is reset by the RESETN pin.

BWE POLARITY:

A one makes BWE high active. A zero makes BWE low active. This bit is cleared to zero when the chip is reset by the RESETN pin.

BOE POLARITY:

A one makes BOE high active. A zero makes BOE low active. This bit is cleared to zero when the chip is reset by the RESETN pin.

DREQB POLARITY:

A one makes DREQB high active. A zero makes DREQB low active. This bit is cleared to zero when the chip is reset by the RESETN pin.

DACKB POLARITY:

A one makes DACKB high active. A zero makes DACKB low active. This bit is cleared to zero when the chip is reset by the RESETN pin.

3.10 PORT B CONTROL 1: ADDRESS 0B HEX - READ/WRITE

	bit7	*bit6*	*bit5*	*bit4*	*bit3*	*bit2*	*bit1*	*bit0*
0x0B	DATA BUS WIDTH	DATA15TO8	res	ENABLE PORT B COMPARATOR	CLEAR INTERFACE	CLEAR BYTE COUNTER	ENABLE PARITY	ODD PARITY

DATA BUS WIDTH:

A one makes the Port B data bus 16 bits wide, with data transferred on the DB[15:0] pins. A zero makes the Port B data bus 8 bits wide, with data transferred on the DB[7:0] pins. This bit should only be changed after the reset code has been programmed to the DCLZ Control bits in the DCLZ Control register. This bit is undefined when the chip is reset from the RESETN pin.

DATA15TO8:

The DATA15TO8 bit causes one byte to be transferred on DB[15:8] on the next DMA cycle into or out of Port B, when Port B is in 16 bit mode. The intended use of this bit is to transfer a single byte on DB[15:8] only during the first DMA cycle of a contiguous data transfer sequence. The DATA15TO8 bit only functions when Port B is in 16 bit mode, and is ignored when Port B is in 8 bit mode. The DATA15TO8 bit should only be changed after the reset code has been programmed into the DCLZ Control bits in the DCLZ Control register, or after the chip has paused after end of record, or after the chip has paused because the Port A or Port B end of transfer interrupt has occurred. DATA15TO8 takes effect only on the next DMA cycle, which is defined as the next occurrence when DACKB pulses active, and is supported when Port B is a DMA bus master or a DMA bus slave. After the DMA cycle occurs, the DATA15TO8 bit is automatically cleared. DATA15TO8 is cleared to zero when the chip is reset from the RESETN pin.

res -Reserved. Bit must always be written with a zero. It reads back a zero.

ENABLE PORT B COMPARATOR:

A one enables the comparison of the Port B Byte Count register with the Port B Byte Comparator register, allowing the Port B Comparator Interrupt to be set and the chip to pause. A zero disables the Port B Byte Comparator register and prohibits the Port B Comparator Interrupt.

CLEAR INTERFACE:

Writing a one creates a pulse, which clears the Port B Interface. Writing a zero has no effect on the Port B Interface. This bit is always zero when it is read. This bit is intended to be used in Port B slave input or output and master output modes. The CLEAR INTERFACE bit is intended to be used only when the chip has paused after end of record, or paused because the Port A or Port B end of transfer has occurred.

CLEAR BYTE COUNTER:

Writing a one creates a pulse, which clears the Port B Byte Count register. Writing a zero has no effect on the Port B Byte Count register. This bit is always zero when it is read.

ENABLE PARITY:

A one enables parity on DBPTY[1:0] when Port B is in 16 bit mode, and on DBPTY[0] when Port B is in 8 bit mode. Writing a zero disables parity on Port B. This bit is undefined when the chip is reset from the RESETN pin.

ODD PARITY:

A one selects odd parity on Port B. A zero selects even parity on Port B. This bit is undefined when the chip is reset from the RESETN pin.

3.11 PORT B STATUS: ADDRESS 0C HEX - READ ONLY

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x0C	res	DATA7TO0	EOR COUNT[1:0]		INTERFACE BYTE COUNT[3:0]			

res -Reserved. Bit must always be written with a zero. It reads back a zero.

DATA7TO0:

When Port B is in 16 bit mode, the DATA7TO0 bit shows whether the last DMA cycle of a data transfer sequence out of Port B contains one or two valid bytes. This occurs for the last byte of the last record, as determined by the Record Count register. If the last byte of the last record is the first byte in the sequence to output a word, that byte is output on DB[7:0], the data on DB[15:8] is undefined, and the DATA7TO0 bit is set. If the last byte of the last record is the second byte in the sequence to output a word, the second to last byte is output on DB[7:0], the last byte is output on DB[15:8], and the DATA7TO0 bit is cleared. The DATA7TO0 bit is cleared during all DMA cycles into Port B, during all DMA cycles when Port B is in 8 bit mode, and when the chip is reset from the RESETN pin.

EOR COUNT[1:0]:

The EOR COUNT[1:0] bits show the number of bytes with active end of record flags contained in the Port B Interface. These bits operate in compression, compression flush, pass through A to B modes. These bits are cleared to zero when a one is written to the CLEAR INTERFACE bit in Port B Control 1 register, or when the reset or decompression or decompression output disabled or pass through B to A code is programmed to the DCLZ MODE bits in the DCLZ Control register, or when the chip is reset by the RESETN pin. During data transfers, these bits should only be read when the PAUSED bit in the DCLZ Status register is a one.

INTERFACE BYTE COUNT[3:0]:

The INTERFACE BYTE COUNT[3:0] bits show the number of bytes that are held in the Port B Interface. These bits are cleared to zero when a one is written to the CLEAR INTERFACE bit in Port B Control 1 register, or when the reset code is programmed to the DCLZ MODE bits in the DCLZ Control register, or when the chip is reset by the RESETN pin. During data transfers, these bits should only be read when the PAUSED bit in the DCLZ Status register is a one.

3.12 PORT B BYTE COUNT: ADDRESS 0D,0E,0F HEX - READ/WRITE

Least Significant Byte (address 0D hex):

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x0D	[7:0]							

Middle Byte (address 0E hex):

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x0E	[15:8]							

Most Significant Byte (address 0F hex):

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x0F	[23:16]							

The Port B Byte Count register counts the number of bytes that are transferred by the Port B DMA State Machine. This register counts in compression, compression flush, decompression, decompression output disabled, pass through A to B, and pass through B to A modes. The register is cleared to zero when a one is written to the CLEAR BYTE COUNTER bit in Port B Control 1 register, or when the chip is reset by the RESETN pin. During data transfers, this register should only be written or read when the PAUSED bit in the DCLZ Status register is a one. This counter rolls over from FFFFFF hex to 000000.

3.13 PORT B BYTE COMPARATOR: ADDRESS 10,11,12 HEX - READ/WRITE

Least Significant Byte (address 10 hex):

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x10	[7:0]							

Middle Byte (address 11 hex):

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x11	[15:8]							

Most Significant Byte (address 12 hex):

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x12	[23:16]							

The Port B Byte Comparator register is used to pause the chip after a programmed amount of data has been transferred across the Port B data bus pins, DB[15:0]. This register operates in compression, compression flush, decompression, decompression output disabled, pass through A to B, and pass through B to A modes. When the Port B DMA state machine updates the 24 bit Port B Byte Count register, this updated value is compared to the 24 bit Port B Byte Comparator register. If the updated Port B Byte Count value equals or exceeds the Port B Comparator value, the Port B Comparator Interrupt is set, and the chip is immediately paused. This function is enabled by the ENABLE PORT B COMPARATOR bit in Port B Control 1 register. If the ENABLE PORT B COMPARATOR bit is zero (inactive), the Port B Byte Comparator register is unused, and the Port B Comparator Interrupt and pause functions are disabled. During data transfers, this register should only be written or read when the PAUSED bit in the DCLZ Status register is a one.

3.14 RECORD LENGTH: ADDRESS 13,14,15 HEX - READ/WRITE

Least Significant Byte (address 13 hex):

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x13	[7:0]							

Middle Byte (address 14 hex):

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x14	[15:8]							

Most Significant Byte (address 15 hex):

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x15	[23:16]							

The twenty four bit Record Length register is used to count the number of bytes of uncompressed data that comprise one record. The counter operates in compression, pass through A to B, and pass through B to A modes. Note that in decompression, the end of record codewords in the compressed data stream determine where the end of records occur. The Record Length register contains a binary down counter. The initial value of the record length is written into the Record Length register. The current value of the down counter is transferred during read cycles from this register. This register is used in conjunction with the Record Count register. When the Record Length register reaches zero, the Record Count register is decremented. If the Record Count register is greater than zero, the Record Length register down counter is reloaded, to allow another record to be processed automatically. The three bytes of the Record Count register should be read from, or written to, only after the reset code has been written to the DCLZ Control bits in the DCLZ Control register, or when the PAUSED bit in the DCLZ Status register is one. The Record Length register is undefined when the chip is reset by the RESETN pin.

3.15 RECORD COUNT: ADDRESS 16,17,18 HEX - READ/WRITE

Least Significant Byte (address 16 hex):

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x16	[7:0]							

Middle Byte (address 17 hex):

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x17	[15:8]							

Most Significant Byte (address 18 hex):

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x18	[23:16]							

The twenty four bit Record Count register is used to count the number of records in a multi-record transfer. This register is used in compression, compression flush, decompression, decompression output disabled, pass through A to B, and pass through B to A modes. The Record Count and Record Length registers allow multiple records to be processed without processor intervention. If only one record is to be compressed, then the Record Count register should be initialized to one. The initial value of the record count is written into the Record Count register. The Record Count register is a binary down counter. The current value of the down counter is transferred during read cycles from this register. The three bytes of the Record Count register should be read from, or written to, only after the reset code has been written to the DCLZ Control bits in the DCLZ Control register, or when the PAUSED bit in the DCLZ Status register is one. The Record Count register is undefined when the chip is reset by the RESETN pin.

3.16 INTERRUPT STATUS: ADDRESS 19 HEX - READ ONLY

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x19	res		PORT B COMPARATOR INT	DCLZ ERROR INT	PORT B PARITY ERROR INT	PORT A PARITY ERROR INT	PORT B END OF TRANSFER INT	PORT A END OF TRANSFER INT

res -Reserved. Bit reads back a zero.

PORT B COMPARATOR INT:

The PORT B COMPARATOR INTERRUPT bit is set after a byte is transferred over the Port B data bus pins, when the Port B Byte Count register is updated and then equals or exceeds the value in the Port B Byte Comparator register. The PORT B COMPARATOR INT bit is cleared to zero when the chip is reset from the RESETN pin. Note that the PORT B COMPARATOR INTERRUPT bit can only be set when the ENABLE PORT B COMPARATOR bit in Port B Control 1 register is one (active).

DCLZ ERROR INT:

The DCLZ ERROR INTERRUPT bit is set when any of the following errors occur during decompression or decompression output disabled modes: a grow codeword was read when the codeword size was already at the maximum 12 bits in length; an unknown codeword was read; a codeword was read which corresponded to greater than the maximum limit of 128 uncompressed bytes. Once the DCLZ ERROR INT bit is set, the reset code should be written to the DCLZ MODE bits in the DCLZ Control register, followed by writing a one to the CLEAR DCLZ ERROR bit in the Interrupt Clear register. The DCLZ ERROR INT bit is cleared to zero when the chip is reset from the RESETN pin.

PORT B PARITY ERROR INT:

The PORT B PARITY ERROR INTERRUPT is set when Port B parity is enabled, and erroneous parity is detected when data is read into Port B. Once the PORT B PARITY ERROR INT bit is set, the reset code should be written to the DCLZ MODE bits in the DCLZ Control register, followed by writing a one to the CLEAR PORT B PARITY ERROR bit in the Interrupt Clear register. The PORT B PARITY ERROR INT bit is cleared to zero when the chip is reset from the RESETN pin.

PORT A PARITY ERROR INT:

The PORT A PARITY ERROR INTERRUPT is set when Port A parity is enabled, and erroneous parity is detected when data is read into Port A. Once the PORT A PARITY ERROR INT bit is set, the reset code should be written to the DCLZ MODE bits in the DCLZ Control register, followed by writing a one to the CLEAR PORT A PARITY ERROR bit in the Interrupt Clear register. The PORT A PARITY ERROR INT bit is cleared to zero when the chip is reset from the RESETN pin.

PORT B END OF TRANSFER INT:

The PORT B END OF TRANSFER INTERRUPT is used in compression, compression flush, and pass through A to B modes. The interrupt occurs when the Record Count register and the Record Length register are both zero, and the last byte of the last record has been transferred through the Port B interface. The PORT B END OF TRANSFER INT bit is cleared to zero when the chip is reset from the RESETN pin.

PORT A END OF TRANSFER INT:

The PORT A END OF TRANSFER INTERRUPT is used in decompression, decompression output disabled, and pass through B to A modes. The interrupt occurs in pass through B to A mode when the Record Count register and the Record Length register are both zero, and the last byte of the last record has been transferred through the Port A interface. The interrupt occurs in decompression and decompression output disabled modes when the Record Count register is zero, and the last byte of the last record has been transferred through the Port A interface. The PORT A END OF TRANSFER INT bit is cleared to zero when the chip is reset from the RESETN pin.

3.17 INTERRUPT CLEAR: ADDRESS 19 HEX - WRITE ONLY

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x19	res		CLEAR PORT B COMPARATOR INT	CLEAR DCLZ ERROR INT	CLEAR PORT B PARITY ERROR INT	CLEAR PORT A PARITY ERROR INT	CLEAR PORT B END OF TRANSFER INT	CLEAR PORT A END OF TRANSFER INT

res -Reserved. Bit reads back a zero.

All other bits in the register clear the interrupt bits in the Interrupt Status register. Writing a one to a clear bit creates a pulse which clears the corresponding bit in the Interrupt Status register. Writing a zero to a clear bit has no effect on the corresponding interrupt bit in the Interrupt Status register.

3.18 INTERRUPT DISABLE: ADDRESS 1A HEX - READ/WRITE

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x1A	res		DISABLE PORT B COMPARATOR INT	DISABLE DCLZ ERROR INT	DISABLE PORT B PARITY ERROR INT	DISABLE PORT A PARITY ERROR INT	DISABLE PORT B END OF TRANSFER INT	DISABLE PORT A END OF TRANSFER INT

res -Reserved. Bit reads back a zero.

All other bits in the register gate the interrupts between the Interrupt Status register and the INTN/INT pin of the chip. Writing a one to a disable bit disables the corresponding interrupt. Writing a zero to a disable bit enables the corresponding interrupt. Note that software polling is possible by disabling all the interrupts, and using the Interrupt Status register and Interrupt Clear registers. The disable bits are one when the chip is reset by the RESETN pin.

3.19 IDENTIFICATION: ADDRESS 1F HEX - READ ONLY

This register provides an identification code for firmware to read.

4.0 PIN DESCRIPTION

This section describes the function of the pins of the chip. A low active signal has an "N" appended to the end of the signal name.

4.1 PROCESSOR INTERFACE

NAME	TYPE	DESCRIPTION
PROCMODE	I	PROCessor MODE select pin. Connect to VDD to select a processor interface controlled by a data strobe (DSN), a read/write signal (RWN), with an open drain data transfer acknowledge output (DTACKN), and an open drain, low active interrupt (INTN). Connect to GND to select processor interface controlled by an I/O read strobe (IORDN), an I/O write strobe (IOWRN), with a high active ready output (READY), and a high active interrupt (INT).
A[4:0]	I	Address for registers accessed through the processor interface.
RWN/IOWRN	I	When the PROCMODE pin is a high voltage this signal functions as ReadWriteN. A high voltage denotes a processor read cycle. A low voltage denotes a write cycle. When the PROCMODE pin is a low voltage, this signal functions as I/O WRiteN. A low voltage denotes a processor I/O write cycle is occurring, and the rising edge denotes the end of the processor access. As IOWRN, this signal is used as a strobe signal, and must not glitch.
CSN	I	Chip SelectN. When the PROCMODE pin is a high voltage, a low voltage on this signal and on the DSN/IORDN signal denotes the start of a processor access to a register internal to the chip. This signal can glitch when DSN/IORDN is a high voltage. It must not glitch once DSN/IORDN is a low voltage. When the PROCMODE pin is a low voltage, a low voltage on CSN and either DSN/IORDN or RWN/IOWRN denotes the start of a processor access to a register internal to the chip. The CSN signal can glitch when both DSN/IORDN and RWN/IOWRN are at high voltage. CSN must not glitch once DSN/IORDN or RWN/IOWRN are at low voltage. CSN is active low.
PORTACSN	I	Port A Chip SelectN. When the PROCMODE pin is a high voltage, a low voltage on this signal and on the DSN/IORDN signal denotes the start of a processor access to a peripheral chip on Port A. This signal can glitch when DSN/IORDN is a high voltage. It must not glitch once DSN/IORDN is a low voltage. When the PROCMODE pin is a low voltage, a low voltage on PORTACSN and either DSN/IORDN or RWN/IOWRN denotes the start of a processor access to a peripheral chip on Port A. The PORTACSN signal can glitch when both DSN/IORDN and RWN/IOWRN are at high voltage. PORTACSN must not glitch once DSN/IORDN or RWN/IOWRN are at low voltage. PORTACSN is active low.
DSN/IORDN	I	When the PROCMODE pin is a high voltage, this pin functions as DataStrobeN. Allow voltage on this signal and on the CSN signal denotes the start of a processor access. The rising edge of DSN/IORDN denotes the end of a processor access. This signal is used as a strobe signal. It must not glitch. DSN/IORDN is active low. When the PROCMODE pin is a low voltage, this pin functions as I/O ReaDN. A low voltage denotes a processor I/O read cycle is occurring, and the rising edge denotes the end of the processor access. As IORDN, this signal is used as a strobe signal, and must not glitch.

NAME	TYPE	DESCRIPTION
DTACKN/READY	O	When the PROCMODE pin is a high voltage, this signal functions as a Data Transfer Acknowledge open drain output. A low voltage indicates that processor data has been latched on processor write cycles. On read cycles, a low voltage indicates that data is valid on the D[7:0] bus for the processor to latch. When the PROCMODE pin is a low voltage, this signal functions as a READY output. At the beginning of processor cycles, this output is driven to a low voltage, indicating that the chip is not ready. The pin is driven high when data is valid on the D[7:0] bus during read cycles, and after data has been internally latched during write cycles. This signal is tristated when processor cycles are inactive. The reset state of this pin is high impedance.
D[7:0]	I/O	Bidirectional processor data bus, to access all registers internal to the chip. The reset state of these pins is high impedance.
INTN/INT	O	When the PROCMODE pin is a high voltage, this signal functions as a low active interrupt, with an open drain output. A low voltage indicates that an internal interrupt is active. The reset state of the pin in this mode is tristate. When the PROCMODE pin is a low voltage, this signal functions as a high active interrupt. A high voltage denotes that an internal interrupt is active. In this mode, the pin is never tristated. The reset state of the pin in this mode is low voltage.
CLK	I	Input Clock.
RESETN	I	A low voltage on this pin will reset the chip.
TRISTATEN	I	A low voltage on this pin will tristate all I/O and output signal drivers, and will disable the pad pullup resistors on all other pins. The TRISTATEN pin has a pullup resistor on the pin. For normal operation, it should be left open circuited on the PC board.
TEST[3:0]	I	Test input pins. These pins should always be grounded on the PC board.

4.2 PORT A INTERFACE

NAME	TYPE	DESCRIPTION
DREQA	I/O	Port A DMA request pin, with programmable polarity. This pin is an output when Port A is a DMA bus master, and an input when Port A is a DMA bus slave. This signal pulses once for every DMA transfer into or out of Port A in master mode. This signal may be held active for multiple transfers in slave mode. The reset state of this pin is high impedance.
DACKA	I/O	Port A DMA channel DMA acknowledge pin, with programmable polarity. This pin is an input when Port A is a DMA bus master, and an output when Port A is a DMA bus slave. This signal pulses once for every DMA transfer into or out of Port A. The reset state of this pin is high impedance.
ACSN	O	Port A peripheral chip select pin. This signal pulses low during read and write accesses to registers to a peripheral chip connected to Port A. The reset state of this pin is high voltage.
AWE	I/O	Port A write enable pin, with programmable polarity. This pin pulses during each DMA transfer into Port A. AWE is an input pin when Port A is a DMA bus master, and is used by an external DMA bus slave to strobe data into Port A. AWE is an output pin when Port A is a DMA bus slave, and is used to enable an external DMA bus master's data output drivers. This pin can be enabled/ disabled with the AWE ENABLE bit in Port A Control 0 register. The reset state of this pin is high impedance.
AOE	I/O	Port A output enable pin, with programmable polarity. This pin pulses during each DMA transfer out of Port A. AOE is an input pin when Port A is a DMA bus master, and is used by an external DMA bus slave to enable Port A data output drivers. AOE is an output pin when Port A is a DMA bus slave, and is used to latch data into an external DMA bus master. This pin can be enabled/ disabled with the AOE ENABLE bit in Port A Control 0 register. The reset state of this pin is high impedance.
DA[15:0]	I/O	Port A bidirectional data bus. These pins have internal 10K ohm pullup resistors, which are enabled by the ENABLE DA PULLUP bit in Port A Control 0 register. When Port A is in 16 bit mode, data is transferred on DA[15:0]. In reference to a byte ordered data flow, the first byte is transferred on DA[7:0] and the second byte on DA[15:8]. When Port A is in 8 bit mode, data is transferred on DA[7:0]. The reset state of these pins has the output drivers tristated, and the internal pullup resistors disabled. (Note 1)
DAPTY[1:0]	I/O	Bidirectional parity bits for the DA[15:0] bus. Parity can be enabled/disabled, and odd/even parity programmed through Port A Control 1 register. DAPTY[1] provides parity for the DA[15:8] bus. DAPTY[0] provides parity for the DA[7:0] bus. If Port A parity is disabled, these pins are always tristated. These pins have an internal 10K ohm pullup resistors, which are enabled with the ENABLE DAPTY PULLUP bit in Port A Control 0 register. The reset state of these pins is high impedance, with the internal pullup resistors disabled. (Note 1)

Note:

1) While RESETN is active and TRISTATEN is inactive these pins are in high impedence with the internal pullups enabled. When TRISTATEN is active these pins are in high impedence with internal pullups disabled.

4.3 PORT B INTERFACE

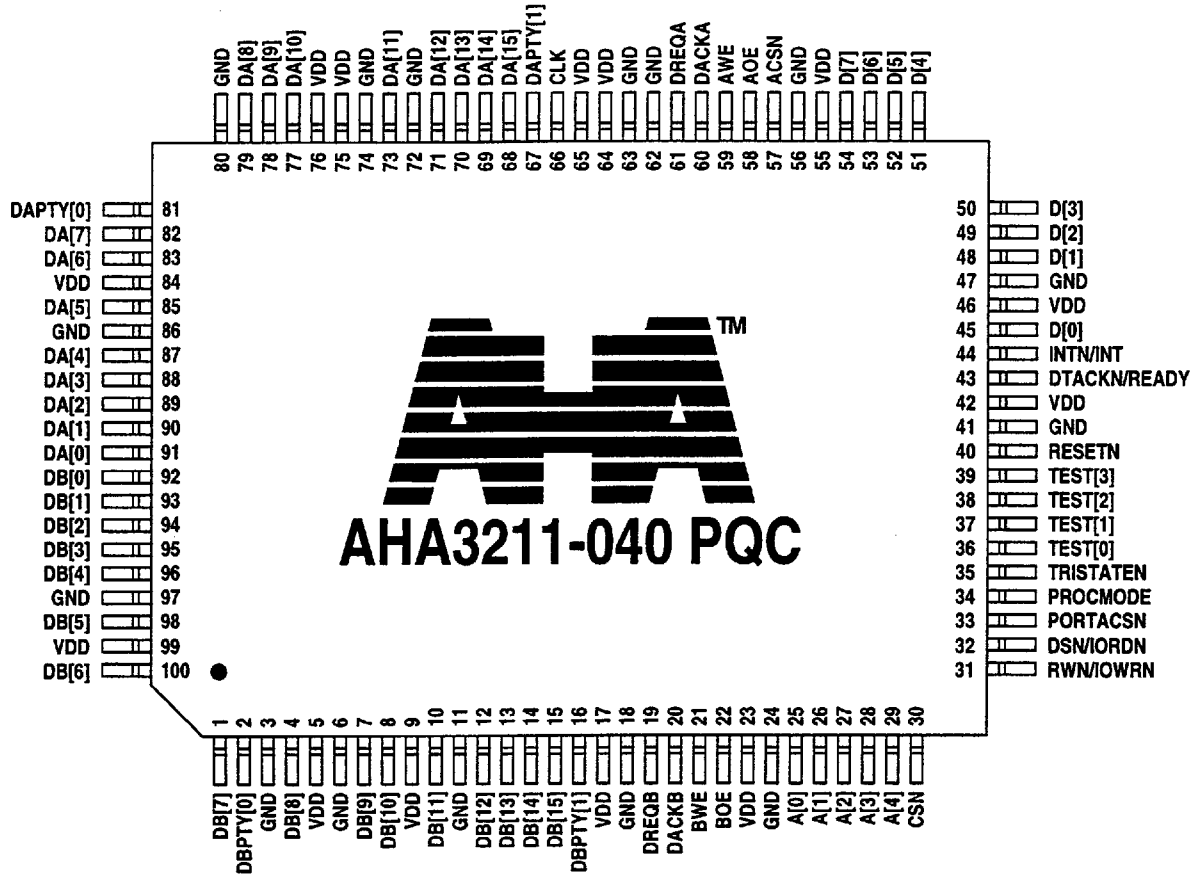
NAME	TYPE	DESCRIPTION
DREQB	I/O	Port B DMA request pin, with programmable polarity. This pin is an output when Port B is a DMA bus master, and an input when Port B is a DMA bus slave. This signal pulses once for every DMA transfer into or out of Port B in master mode. This signal may be held active for multiple transfers in slave mode. The reset state of this pin is high impedance.
DACKB	I/O	Port B DMA channel DMA acknowledge pin, with programmable polarity. This pin is an input when Port B is a DMA bus master, and an output when Port B is a DMA bus slave. This signal pulses once for every DMA transfer into or out of Port B. The reset state of this pin is high impedance.
BWE	I/O	Port B write enable pin, with programmable polarity. This pin pulses during each DMA transfer into Port B. BWE is an input pin when Port B is a DMA bus master, and is used by an external DMA bus slave to strobe data into Port B. BWE is an output pin when Port B is a DMA bus slave, and is used to enable an external DMA bus master's data output drivers. This pin can be enabled/ disabled with the BWE ENABLE bit in Port B Control 0 register. The reset state of this pin is high impedance.
BOE	I/O	Port B output enable pin, with programmable polarity. This pin pulses during each DMA transfer out of Port B. BOE is an input pin when Port B is a DMA bus master, and is used by an external DMA bus slave to enable Port B data output drivers. BOE is an output pin when Port B is a DMA bus slave, and is used to latch data into an external DMA bus master. This pin can be enabled/ disabled with the BOE ENABLE bit in Port B Control 0 register. The reset state of this pin is high impedance.
DB[15:0]	I/O	Port B bidirectional data bus. These pins have internal 10K ohm pullup resistors, which are enabled by the ENABLE DB PULLUP bit in Port B Control 0 register. When Port B is in 16 bit mode, data is transferred on DB[15:0]. In reference to a byte ordered data flow, the first byte is transferred on DB[7:0] and the second byte on DB[15:8]. When Port B is in 8 bit mode, data is transferred on DB[7:0]. The reset state of these pins has the output drivers tristated, and the internal pullup resistors disabled. (Note 1)
DBPTY[1:0]	I/O	Bidirectional parity bits for the DB[15:0] bus. Parity can be enabled/disabled, and odd/even parity programmed through Port B Control 1 register. DBPTY[1] provides parity for the DB[15:8] bus. DAPTY[0] provides parity for the DB[7:0] bus. If Port B parity is disabled, these pins are always tristated. These pins have an internal 10K ohm pullup resistors, which are enabled with the ENABLE DBPTY PULLUP bit in Port B Control 0 register. The reset state of these pins is high impedance, with the internal pullup resistors disabled. (Note 1)

Note:

1) While RESETN is active and TRISTATEN is inactive these pins are in high impedence with the internal pullups enabled. When TRISTATEN is active these pins are in high impedence with internal pullups disabled.

5.0 PINOUT

Figure 11: Pinout Diagram



6.0 ELECTRICAL SPECIFICATIONS

6.1 ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNITS
Vdd	Power supply voltage		7.0	Volts
Vpin	Voltage applied to any pin	-0.5	7.0	Volts

Absolute maximum voltage ratings are for voltage excursions which are transitory in nature.

6.2 RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
Vdd	Power supply voltage	4.75	5.25	Volts
Ta	Operating temperature	0	70	Degrees C

6.2.1 DC SPECIFICATIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
Vil	Input low voltage CLK All other inputs			0.8	Volts
Vih	Input high voltage CLK All other inputs		2.0		Volts
Vol	All output low voltage	Iol = 4.0 mAmps		0.4	Volts
Voh	Output high voltage	Ioh = 4.0 mAmps	2.4		Volts
Iil	Input low current	Vin = 0 Volts	-10		µAmps
Iih	Input high current	Vin = VDD Volts		10	µAmps
Iozl	Output tristate low current	Vout 0 Volts		10	µAmps
Iozh	Output tristate high current	Vout VDD Volts	-10		µAmps
IddA	Active Idd current	Vdd = 5.25 Volts		350	mAmps
Idd	Supply current (static)	Vdd = 5.25 Volts		1	mAmps
Iol	DTACKN/READY, INTN/INT All other inputs			8 4	mAmps
Ioh	DTACKN/READY, INTN/INT All other inputs			8 4	mAmps

6.2.2 AC SPECIFICATIONS

PIN NAMES	MAXIMUM CAPACITIVE LOAD
DTACKN/READY, D[7:0], INTN/INT	50 pF
DREQA, DACKA, AOE, DA[15:0], DAPTY[1:0], ACSN, DREQB, DACKB, BOE, BWE, DB[15:0], DBPTY[1:0]	50 pF

6.2.3 PIN CAPACITANCE

SYMBOL	PARAMETER	MAX	UNITS
Cin	Input capacitance	10	pF
Cout	Output capacitance	10	pF
Cio	I/O capacitance	10	pF

7.0 TIMING SPECIFICATIONS

Figure 12: Clock Timing

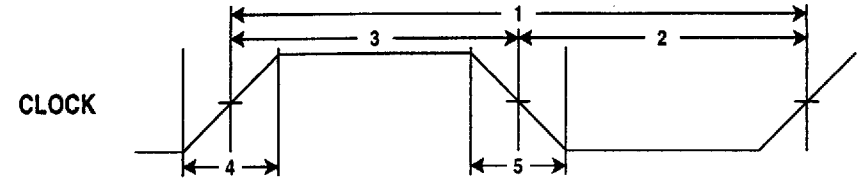


Table 8: Clock Timing Specification

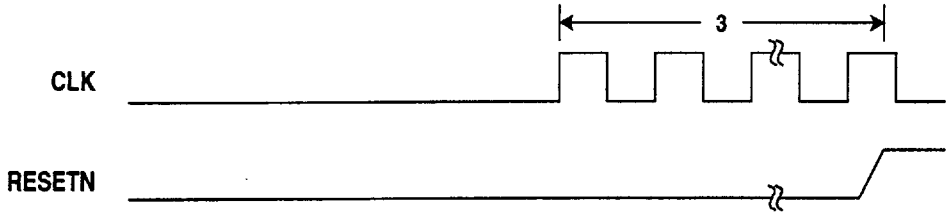
NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	CLK period	25		nsec	1
2	CLK low pulsewidth	8		nsec	1
3	CLK high pulsewidth	8		nsec	1
4	CLK rise time		3	nsec	2
5	CLK fall time		3	nsec	2

Notes:

1) All AC Timings are referenced to 1.4 Volts.

2) Rise and fall times are between 0.8 Volts and 2.0 Volts.

Figure 13: Reset Timing - Power Up



Refer to Table 9 for Timing Specification

Figure 14: Reset Timing

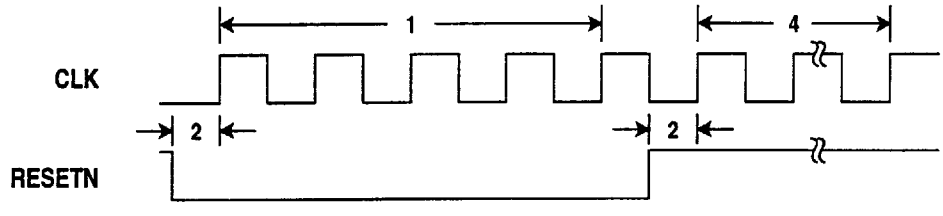


Table 9: Reset Timing Specifications

NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	RESETN low pulsewidth	5		clocks	
2	RESETN setup to CLK rise	10		nsec	1
3	RESETN power up period	5		clocks	2
4	RESETN inactive to first microprocessor access	12		clocks	3

Notes:

1) The RESETN signal can be asynchronous to the CLK signal. It is internally synchronized to the rising edge of CLK.

2) RESETN signal must stay low until a minimum of 5 clocks occur. See Figure 13.

3) RESETN signal must be inactive a minimum of 12 clocks before the first microprocessor access.

Figure 15: Processor Read Cycle – DSN, RWN Controlled

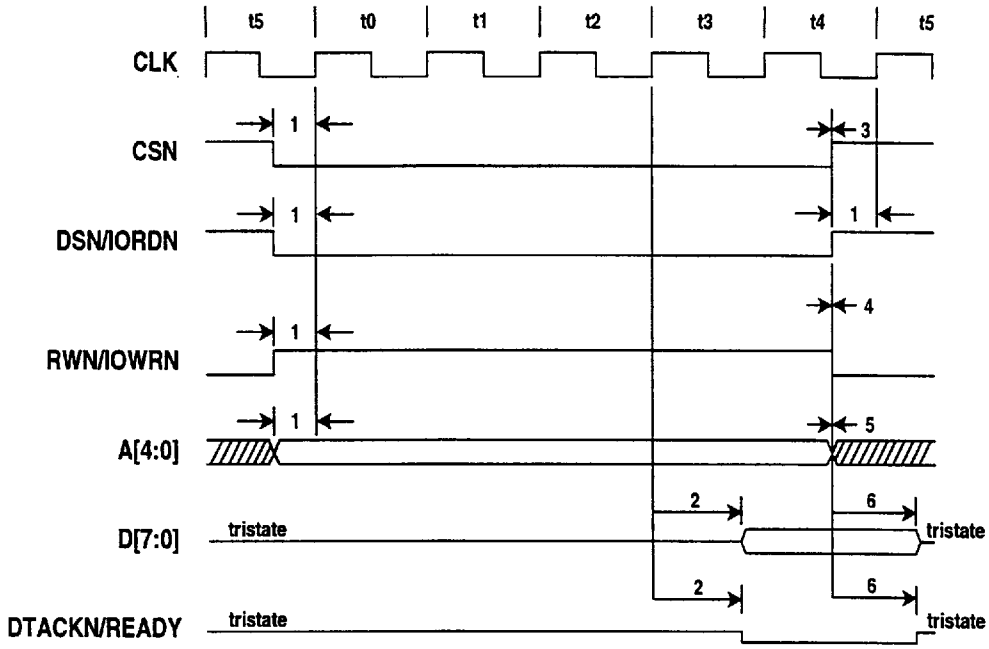


Table 10: Processor Read Cycle Timings - DSN, RWN Controlled

NUMBER	PARAMETER	MIN	MAX	UNITS
1	CSN, DSN/IORDN, RWN/IOWRN and A[4:0] setup to CLK rise	10		ns
2	CLK rise to D[7:0] valid and DTACKN/READY low	0	20	ns
3	CSN hold from DSN/IORDN high	0		ns
4	RWN/IOWRN hold from DSN/IORDN high	0		ns
5	A[4:0] hold from DSN/IORDN high	0		ns
6	DSN/IORDN high to D[7:0] and DTACKN/READY high-Z	0	20	ns

Notes:

1) *CSN, DSN/IORDN and RWN/IOWRN are assumed to be asynchronous with respect to the AHA3211 clock. These signals are synchronized internally to the AHA3211 clock to drive internal state machines.*
2) *CSN may be held low during back-to-back register access cycles.*
3) *If a strobe to clock setup is missed at the beginning of an access cycle, then the access cycle begins on the following clock cycle at which the specification is met.*
4) *If a strobe to clock setup is missed at the end of an access cycle, then the access cycle terminator is delayed until the low to high transition of the strobe meets the specified setup time.*
5) *The minimum active or inactive pulsewidth on CSN, DSN/IORDN and RWN/IOWRN is one clock.*

Figure 16: Processor Write Cycle – DSN, RWN Controlled

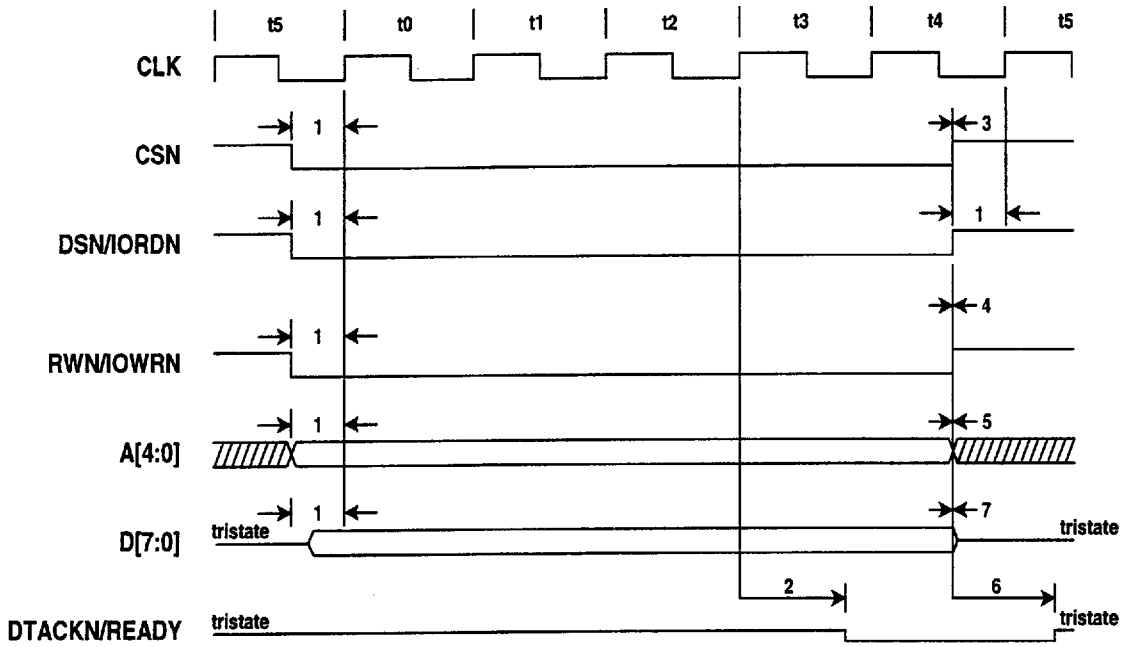


Table 11: Processor Write Cycle Timings - DSN, RWN Controlled

NUMBER	PARAMETER	MIN	MAX	UNITS
1	CSN, DSN/IORDN, RWN/IOWRN, A[4:0] and D[7:0] setup to CLK rise	10		ns
2	CLK rise to DTACKN/READY low	0	20	ns
3	CSN hold from DSN/IORDN high	0		ns
4	RWN/IOWRN hold from DSN/IORDN high	0		ns
5	A[4:0] hold from DSN/IORDN high	0		ns
6	DSN/IORDN high to DTACKN/READY high-Z	0	20	ns
7	D[7:0] hold from DSN/IORDN high	0		ns

Notes:

1) *CSN, DSN/IORDN and RWN/IOWRN are assumed to be asynchronous with respect to the AHA3211 clock. These signals are synchronized internally to the AHA3211 clock to drive internal state machines.*
2) *CSN may be held low during back-to-back register access cycles.*
3) *If a strobe to clock setup is missed at the beginning of an access cycle, then the access cycle begins on the following clock cycle at which the specification is met.*
4) *If a strobe to clock setup is missed at the end of an access cycle, then the access cycle terminator is delayed until the low to high transition of the strobe meets the specified setup time.*
5) *The minimum active or inactive pulsewidth on CSN, DSN/IORDN and RWN/IOWRN is one clock.*

Figure 17: Processor Read Cycle – IORDN Controlled

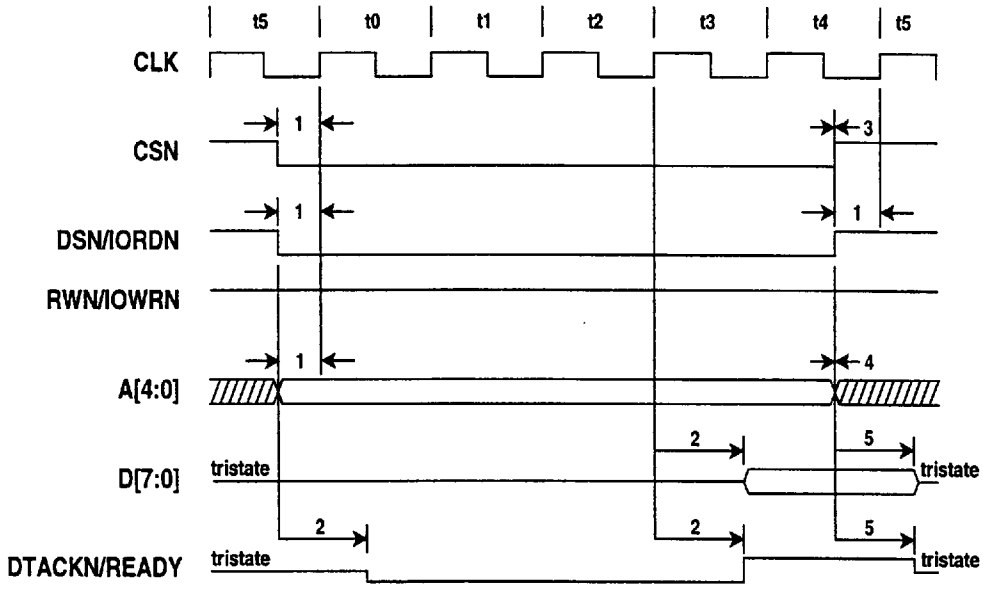


Table 12: Processor Read Cycle Timings - IORDN Controlled

NUMBER	PARAMETER	MIN	MAX	UNITS
1	CSN, DSN/IORDN and A[4:0] setup to CLK rise	10		ns
2	CSN and DSN/IORDN low to DTACKN/READY low; CLK rise to D[7:0] valid and DTACKN/READY high	0	20	ns
3	CSN hold from DSN/IORDN high	0		ns
4	A[4:0] hold from DSN/IORDN high	0		ns
5	DSN/IORDN high to D[7:0] and DTACKN/READY high-Z	0	20	ns

Notes:

1) *CSN and DSN/IORDN are assumed to be asynchronous with respect to the AHA3211 clock. These signals are synchronized internally to the AHA3211 clock to drive internal state machines.*
2) *CSN may be held low during back-to-back register access cycles.*
3) *If a strobe to clock setup is missed at the beginning of an access cycle, then the access cycle begins on the following clock cycle at which the specification is met.*
4) *If a strobe to clock setup is missed at the end of an access cycle, then the access cycle terminator is delayed until the low to high transition of the strobe meets the specified setup time.*
5) *The minimum active or inactive pulsewidth on CSN, DSN/IORDN and RWN/IOWRN is one clock.*

Figure 18: Processor Write Cycle – IOWRN Controlled

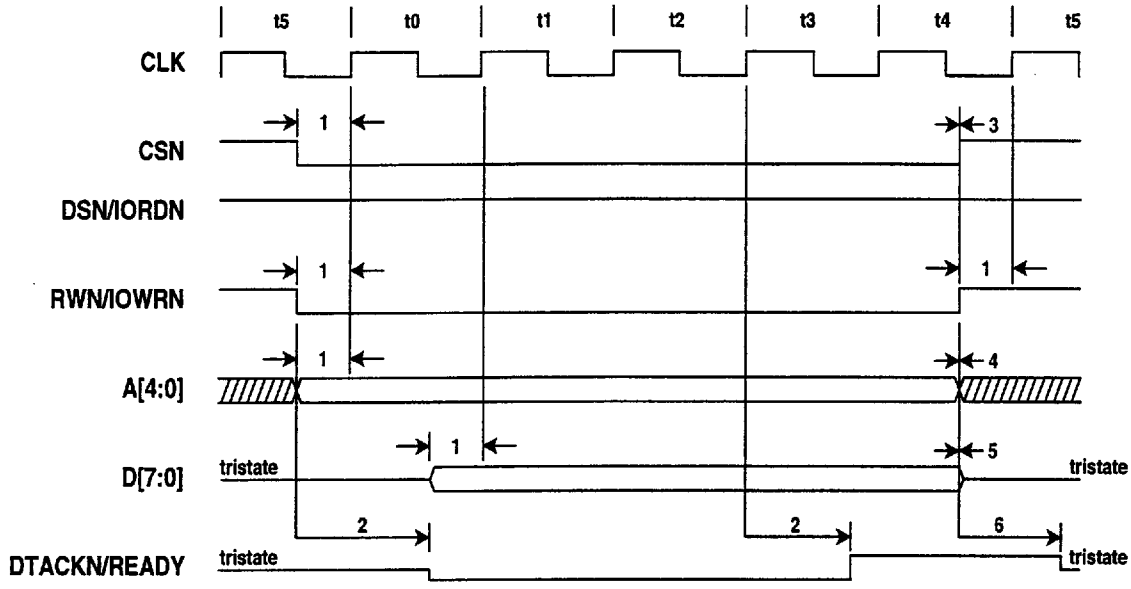


Table 13: Processor Write Cycle Timings - IOWRN Controlled

NUMBER	PARAMETER	MIN	MAX	UNITS
1	CSN, RWN/IOWRN, A[4:0] and D[7:0] setup to CLK rise	10		ns
2	CSN and RWN/IOWRN low to DTACKN/READY low; CLK rise to DTACKN/READY high	0	20	ns
3	CSN hold from RWN/IOWRN high	0		ns
4	A[4:0] hold from RWN/IOWRN high	0		ns
5	D[7:0] hold from RWN/IOWRN high	0		ns
6	RWN/IOWRN high to DTACKN/READY high-Z	0	20	ns

Notes:

1) *CSN and RWN/IOWRN are assumed to be asynchronous with respect to the AHA3211 clock. These signals are synchronized internally to the AHA3211 clock to drive internal state machines.*
2) *CSN may be held low during back-to-back register access cycles.*
3) *If a strobe to clock setup is missed at the beginning of an access cycle, then the access cycle begins on the following clock cycle at which the specification is met.*
4) *If a strobe to clock setup is missed at the end of an access cycle, then the access cycle terminator is delayed until the low to high transition of the strobe meets the specified setup time.*
5) *The minimum active or inactive pulsewidth on CSN, DSN/IORDN and RWN/IOWRN is one clock.*

Figure 19: Processor Read Cycle from Port A Peripheral – DSN, RWN Controlled

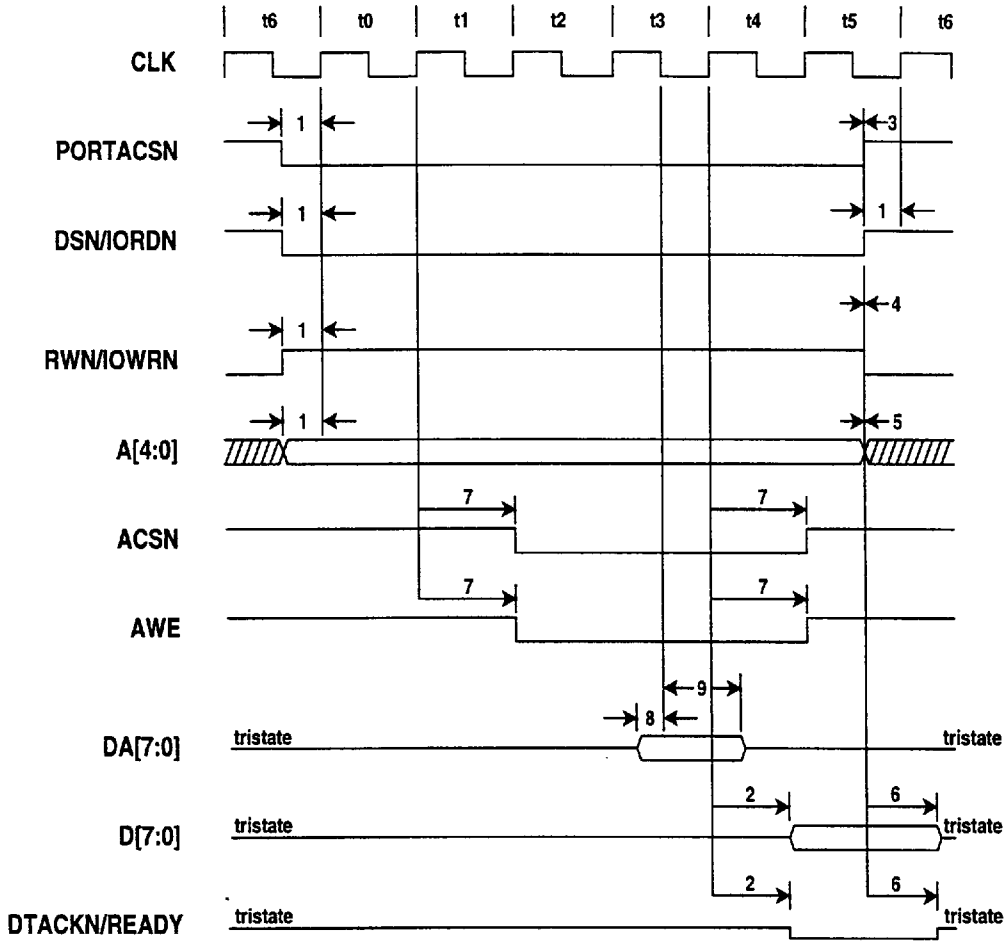


Table 14: Processor Read Cycle Timings from Port A Peripheral - DSN, RWN Controlled

NUMBER	PARAMETER	MIN	MAX	UNITS
1	PORTACSN, DSN/IORDN, RWN/IOWRN and A[4:0] setup to CLK rise	10		ns
2	CLK rise to D[7:0] valid and DTACKN/READY low	0	20	ns
3	PORTACSN hold from DSN/IORDN high	0		ns
4	RWN/IOWRN hold from DSN/IORDN high	0		ns
5	A[4:0] hold from DSN/IORDN high	0		ns
6	DSN/IORDN high to D[7:0] and DTACKN/READY high-Z	0	20	ns
7	CLK rise to ACSN/AWE Valid		25	ns
8	DA[7:0] setup to CLK fall	5		ns
9	DA[7:0] hold from CLK fall	20		ns

Notes:

1) *PORTACSN, DSN/IORDN and RWN/IOWRN are assumed to be asynchronous with respect to the AHA3211 clock. These signals are synchronized internally to the AHA3211 clock to drive internal state machines.*
2) *PORTACSN may be held low during back-to-back register access cycles.*
3) *If a strobe to clock setup is missed at the beginning of an access cycle, then the access cycle begins on the following clock cycle at which the specification is met.*
4) *If a strobe to clock setup is missed at the end of an access cycle, then the access cycle terminator is delayed until the low to high transition of the strobe meets the specified setup time.*
5) *The minimum active or inactive pulsewidth on CSN, DSN/IORDN and RWN/IOWRN is one clock.*

Figure 20: Processor Write Cycle to Port A Peripheral – DSN, RWN Controlled

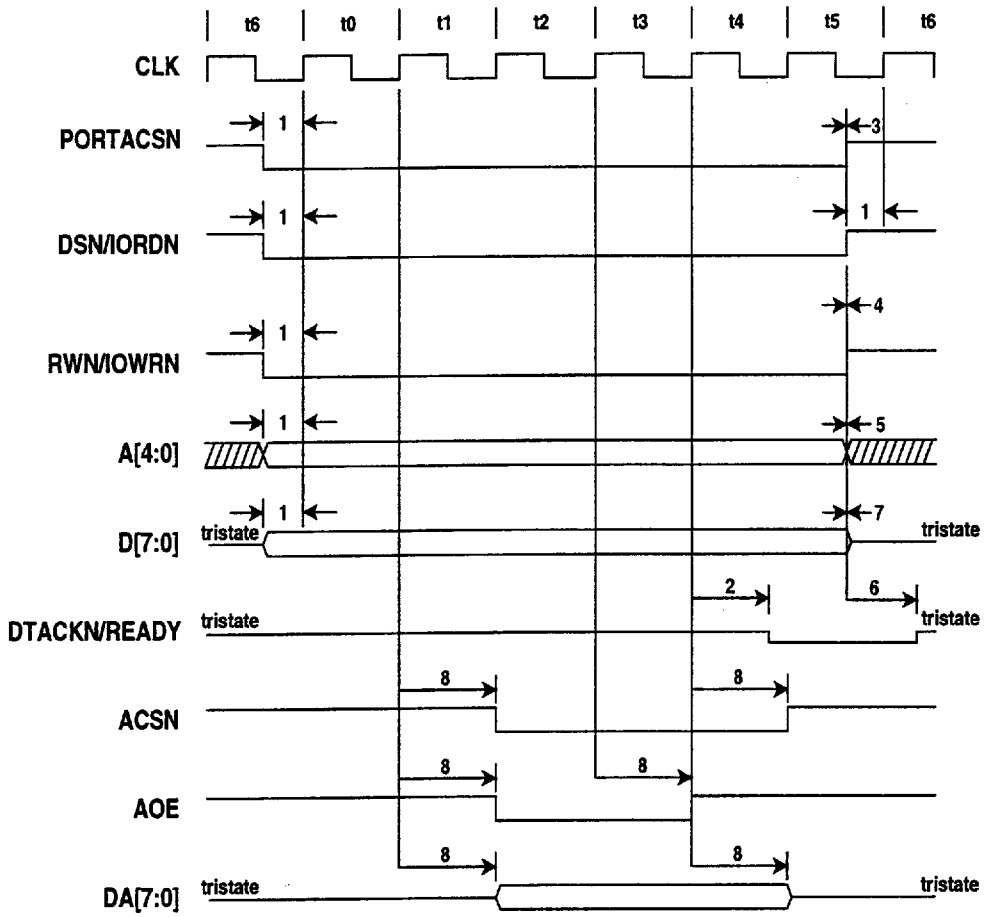


Table 15: Processor Write Cycle to Port A Peripheral Timings - DSN, RWN Controlled

NUMBER	PARAMETER	MIN	MAX	UNITS
1	PORTACSN, DSN/IORDN, RWN/IOWRN, A[4:0] and D[7:0] setup to CLK rise	10		ns
2	CLK rise to DTACKN/READY low	0	20	ns
3	PORTACSN hold from DSN/IORDN high	0		ns
4	RWN/IOWRN hold from DSN/IORDN high	0		ns
5	A[4:0] hold from DSN/IORDN high	0		ns
6	DSN/IORDN high to DTACKN/READY high-Z	0	20	ns
7	D[7:0] hold from DSN/IORDN high	0		ns
8	CLK rise to ACSN/AOE, DA[7:0] valid	0	25	ns

Notes:

1) *PORTACSN, DSN/IORDN and RWN/IOWRN are assumed to be asynchronous with respect to the AHA3211 clock. These signals are synchronized internally to the AHA3211 clock to drive internal state machines.*
2) *PORTACSN may be held low during back-to-back register access cycles.*
3) *If a strobe to clock setup is missed at the beginning of an access cycle, then the access cycle begins on the following clock cycle at which the specification is met.*
4) *If a strobe to clock setup is missed at the end of an access cycle, then the access cycle terminator is delayed until the low to high transition of the strobe meets the specified setup time.*
5) *The minimum active or inactive pulsewidth on CSN, DSN/IORDN and RWN/IOWRN is one clock.*

Figure 21: Processor Read Cycle from Port A Peripheral – IORDN Controlled

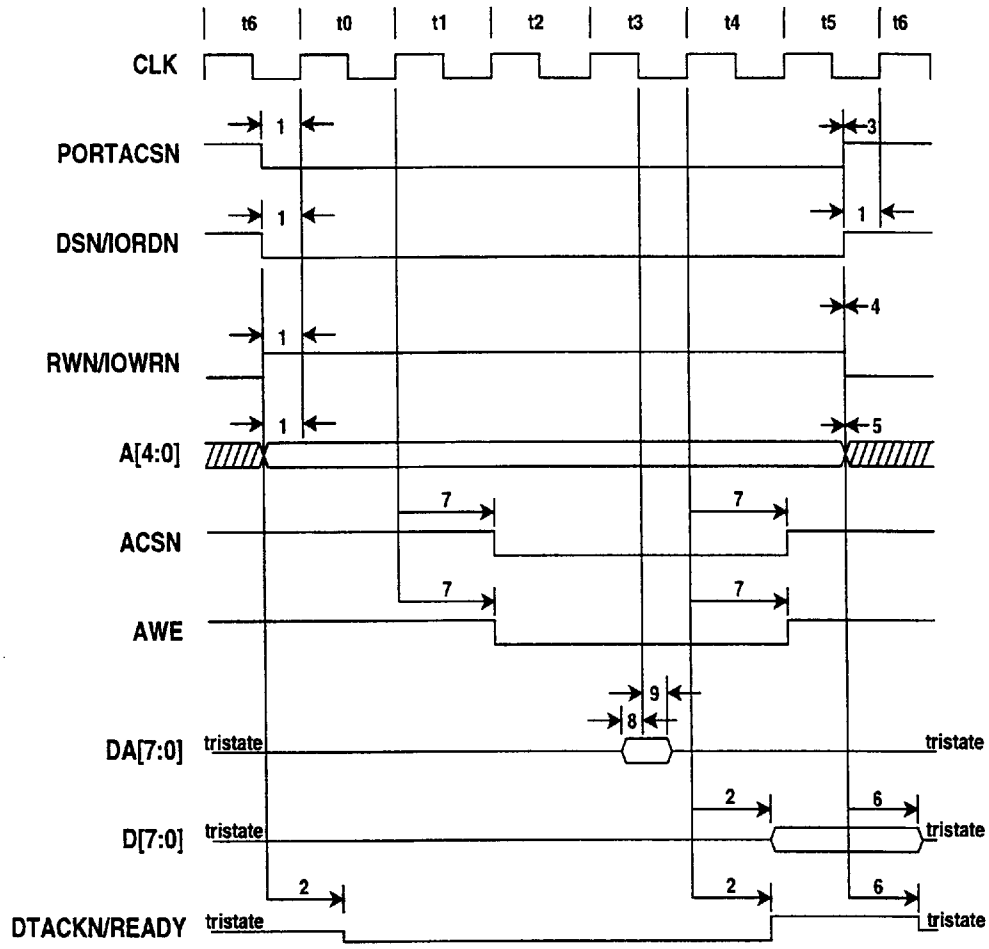


Table 16: Processor Read Cycle from Port A Peripheral Timings - IORDN Controlled

NUMBER	PARAMETER	MIN	MAX	UNITS
1	PORTACSN, DSN/IORDN, RWN/IOWRN and A[4:0] setup to CLK rise	10		ns
2	PORTACSN and DSN/IORDN low to DTACKN/READY low; CLK rise to D[7:0] valid and DTACKN/READY high	0	20	ns
3	PORTACSN hold from DSN/IORDN high	0		ns
4	RWN/IOWRN hold from DSN/IORDN high	0		ns
5	A[4:0] hold from DSN/IORDN high	0		ns
6	DSN/IORDN high to D[7:0] and DTACKN/READY high-Z	0	20	ns
7	CLK rise to ACSN/AWE Valid		25	ns
7	DA[7:0] setup to CLK fall	5		ns
9	DA[7:0] hold from CLK fall	20		ns

Notes:

1) *PORTACSN, DSN/IORDN and RWN/IOWRN are assumed to be asynchronous with respect to the AHA3211 clock. These signals are synchronized internally to the AHA3211 clock to drive internal state machines.*
2) *PORTACSN may be held low during back-to-back register access cycles.*
3) *If a strobe to clock setup is missed at the beginning of an access cycle, then the access cycle begins on the following clock cycle at which the specification is met.*
4) *If a strobe to clock setup is missed at the end of an access cycle, then the access cycle terminator is delayed until the low to high transition of the strobe meets the specified setup time.*
5) *The minimum active or inactive pulsewidth on CSN, DSN/IORDN and RWN/IOWRN is one clock.*

Figure 22: Processor Write Cycle to Port A Peripheral – IOWRN Controlled

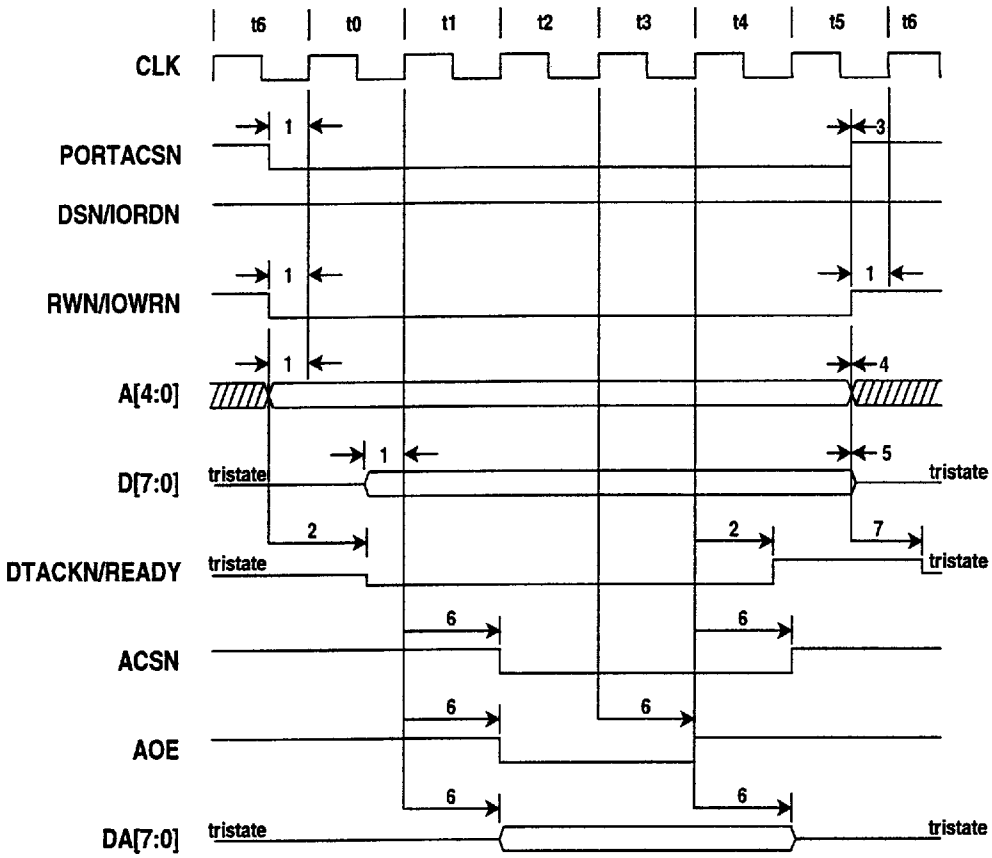


Table 17: Processor Write Cycle to Port A Peripheral Timings - IOWRN Controlled

NUMBER	PARAMETER	MIN	MAX	UNITS
1	PORTACSN, RWN/IOWRN, A[4:0] and D[7:0] setup to CLK rise	10		ns
2	PORTACSN and RWN/IOWRN low to DTACKN/READY low; CLK rise to DTACKN/READY high	0	20	ns
3	PORTACSN hold from RWN/IOWRN high	0		ns
4	A[4:0] hold from RWN/IOWRN high	0		ns
5	D[7:0] hold from RWN/IOWRN high	0		ns
6	CLK rise to ACSN/AOE, DA[7:0] valid	0	25	ns
7	RWN/IOWRN high to DTACKN/READY high-Z	0	20	ns

Notes:

1) *PORTACSN and RWN/IOWRN are assumed to be asynchronous with respect to the AHA3211 clock. These signals are synchronized internally to the AHA3211 clock to drive internal state machines.*
2) *PORTACSN may be held low during back-to-back register access cycles.*
3) *If a strobe to clock setup is missed at the beginning of an access cycle, then the access cycle begins on the following clock cycle at which the specification is met.*
4) *If a strobe to clock setup is missed at the end of an access cycle, then the access cycle terminator is delayed until the low to high transition of the strobe meets the specified setup time.*
5) *The minimum active or inactive pulsewidth on CSN, DSN/IORDN and RWN/IOWRN is one clock.*

Figure 23: DMA Slave Transfer Timing for Data Into Port A,B – FASA and FASB = 0

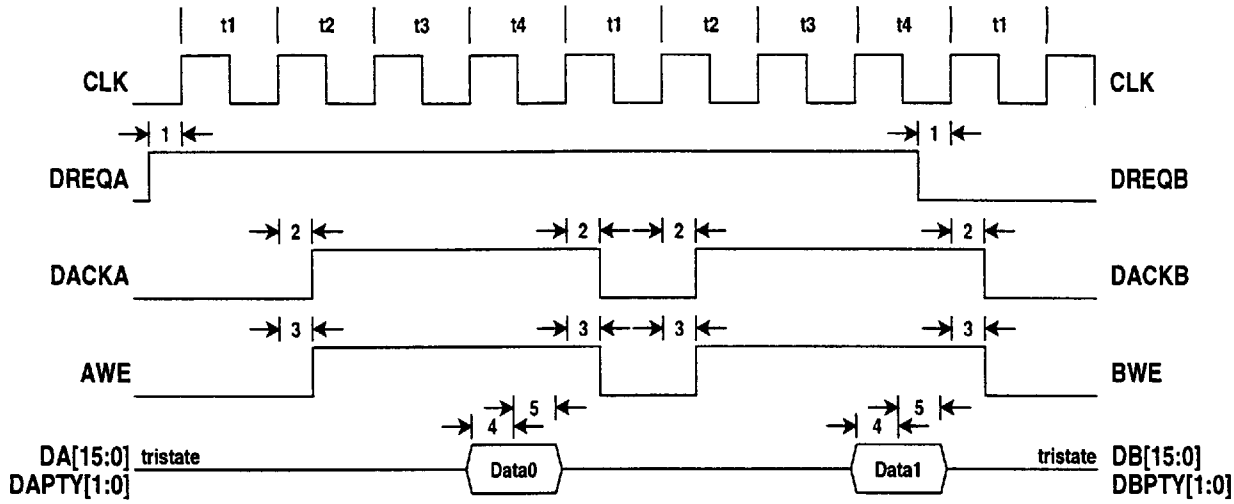


Table 18: DMA Slave Transfer Timing for Data Into Port A,B

NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	DREQA valid setup to CLK rise	5		nsec	1
2	CLK rise to DACKA valid	0	25	nsec	
3	CLK rise to AWE valid	0	25	nsec	2
4	DA[15:0], DAPTY[1:0] setup to CLK fall	5		nsec	
5	DA[15:0], DAPTY[1:0] hold from CLK fall	20		nsec	

Notes:

1) *The DREQA signal can be asynchronous to the CLK signal. It is internally synchronized to the rising edge of CLK. The DREQA signal is polled at T1. If the setup time number 1 is met, the maximum data transfer rate will be achieved.*
2) *If the AWE pin is programmed to be disabled, the pin will be tristated.*
3) *Port A and Port B have the same timing for their DMA interfaces. For Port B specifications, substitute the Port B name for the corresponding Port A name.*
4) *The timing diagram is for a transfer of two consecutive DMA cycles. The signals DACKA, and AWE are chip outputs. DREQA, DAPTY[1:0] and DA[15:0] are chip inputs. DREQA, DACKA, AWE are programmed to be active high.*

Figure 24: DMA Slave Transfer Timing for Data Into Port A,B – FASA and FASB = 1

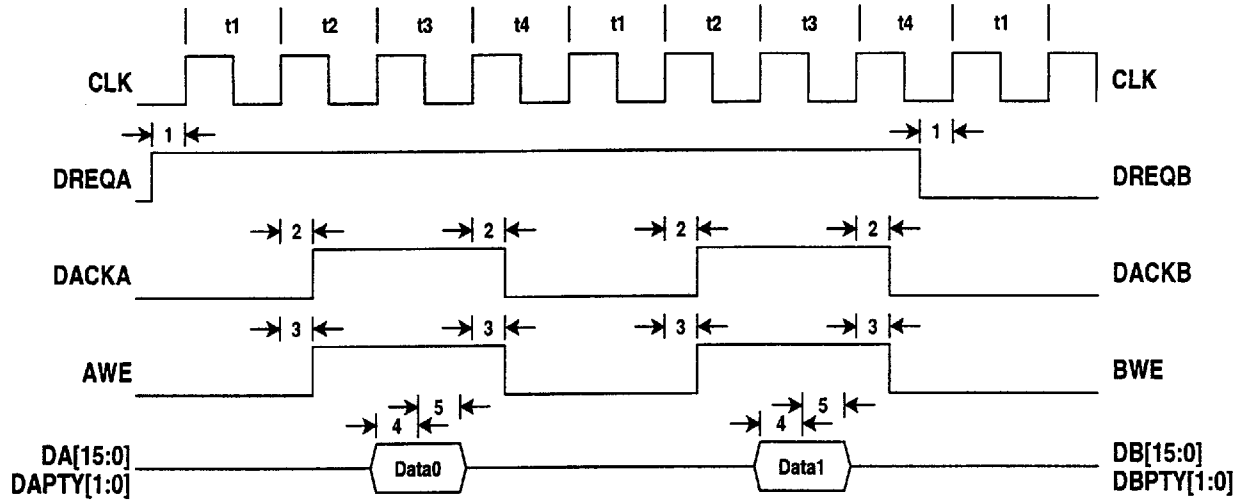


Table 19: DMA Slave Transfer Timing for Data Into Port A,B

NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	DREQA valid setup to CLK rise	5		nsec	1
2	CLK rise to DACKA valid	0	25	nsec	
3	CLK rise to AWE valid	0	25	nsec	2
4	DA[15:0], DAPTY[1:0] setup to CLK fall	5		nsec	
5	DA[15:0], DAPTY[1:0] hold from CLK fall	20		nsec	

Notes:

1) *The DREQA signal can be asynchronous to the CLK signal. It is internally synchronized to the rising edge of CLK. The DREQA signal is polled at T1. If the setup time number 1 is met, the maximum data transfer rate will be achieved.*
2) *If the AWE pin is programmed to be disabled, the pin will be tristated.*
3) *Port A and Port B have the same timing for their DMA interfaces. For Port B specifications, substitute the Port B name for the corresponding Port A name.*
4) *The timing diagram is for a transfer of two consecutive DMA cycles. The signals DACKA, and AWE are chip outputs. DREQA, DAPTY[1:0] and DA[15:0] are chip inputs. DREQA, DACKA, AWE are programmed to be active high.*

Figure 25: DMA Slave Transfer Timing for Data Out of Port A,B – FASA and FASB = 0

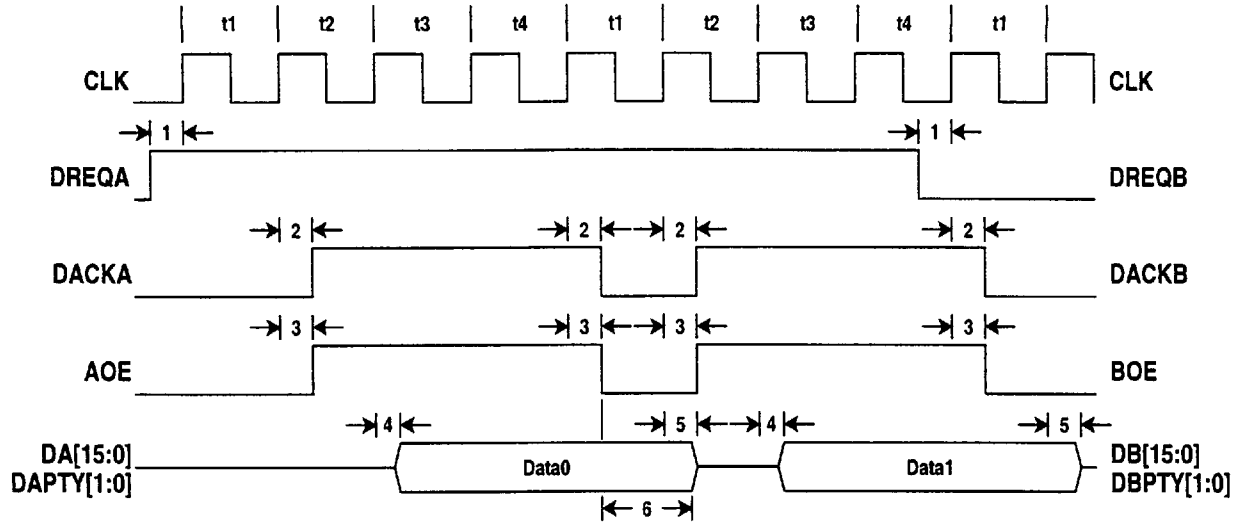


Table 20: DMA Slave Transfer Timing for Data Out of Port A,B

NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	DREQA valid setup to CLK rise	5		nsec	1
2	CLK rise to DACKA valid	0	25	nsec	
3	CLK rise to AOE valid	0	25	nsec	2
4	CLK rise to DA[15:0], DAPTY[1:0] valid	0	25	nsec	3
5	CLK rise to DA[15:0], DAPTY[1:0] tristate	0	25	nsec	3, 4
6	DATA HOLD from DACKA invalid	5		nsec	4

Notes:

1) *The DREQA signal can be asynchronous to the CLK signal. It is internally synchronized to the rising edge of CLK. The signal DREQA is polled at T1. If the setup time number 1 is met, the maximum data transfer rate will be achieved.*
2) *If the AOE pin is programmed to be disabled, the pin will be tristated.*
3) *If the ENABLE PARITY bit in Port A Control 1 register is zero (inactive), the DAPTY[1:0] pins will always be tristated.*
4) *This specification has been proven by worst case timing simulations. It is not fully tested in production.*
5) *Port A and Port B have the same timing for their DMA interfaces. For Port B specifications, substitute the Port B name for the corresponding Port A name.*
6) *The timing diagram is for a transfer of two consecutive DMA cycles. The signals DACKA, AOE, DAPTY[1:0], and DA[15:0] are chip outputs. DREQA is a chip input. DREQA, DACKA, AOE are programmed to be active high.*

Figure 26: DMA Slave Transfer Timing for Data Out of Port A,B – FASA and FASB = 1

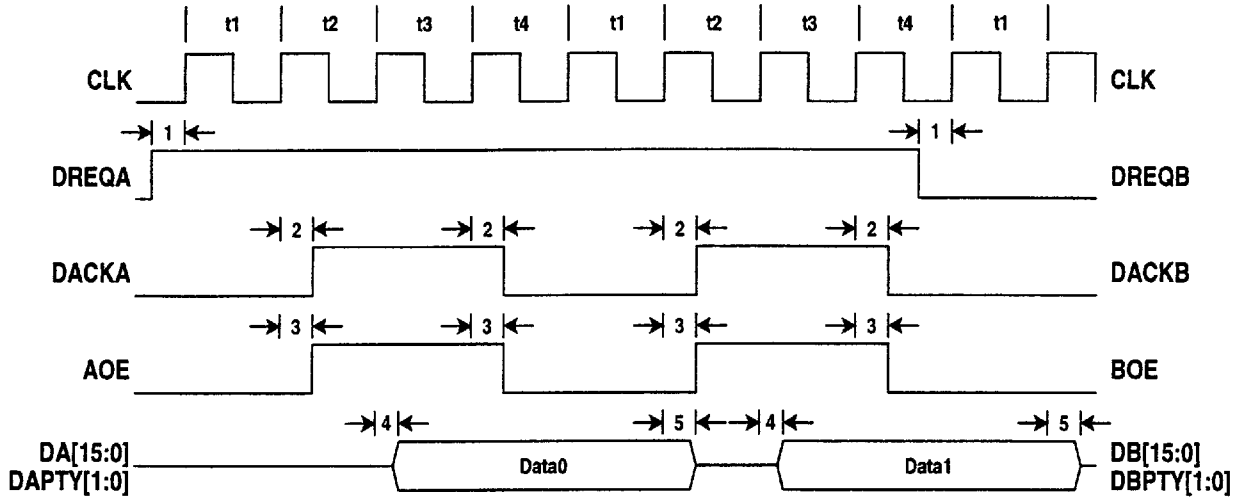


Table 21: DMA Slave Transfer Timing for Data Out of Port A,B

NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	DREQA valid setup to CLK rise	5		nsec	1
2	CLK rise to DACKA valid	0	25	nsec	
3	CLK rise to AOE valid	0	25	nsec	2
4	CLK rise to DA[15:0], DAPTY[1:0] valid	0	25	nsec	3
5	CLK rise to DA[15:0], DAPTY[1:0] tristate	0	25	nsec	3, 4

Notes:

1) *The DREQA signal can be asynchronous to the CLK signal. It is internally synchronized to the rising edge of CLK. The signal DREQA is polled at T1. If the setup time number 1 is met, the maximum data transfer rate will be achieved.*
2) *If the AOE pin is programmed to be disabled, the pin will be tristated.*
3) *If the ENABLE PARITY bit in Port A Control 1 register is zero (inactive), the DAPTY[1:0] pins will always be tristated.*
4) *This specification has been proven by worst case timing simulations. It is not fully tested in production.*
5) *Port A and Port B have the same timing for their DMA interfaces. For Port B specifications, substitute the Port B name for the corresponding Port A name.*
6) *The timing diagram is for a transfer of two consecutive DMA cycles. The signals DACKA, AOE, DAPTY[1:0], and DA[15:0] are chip outputs. DREQA is a chip input. DREQA, DACKA, AOE are programmed to be active high.*

Figure 27: DMA Master Transfer Timing for Data Into Port A,B

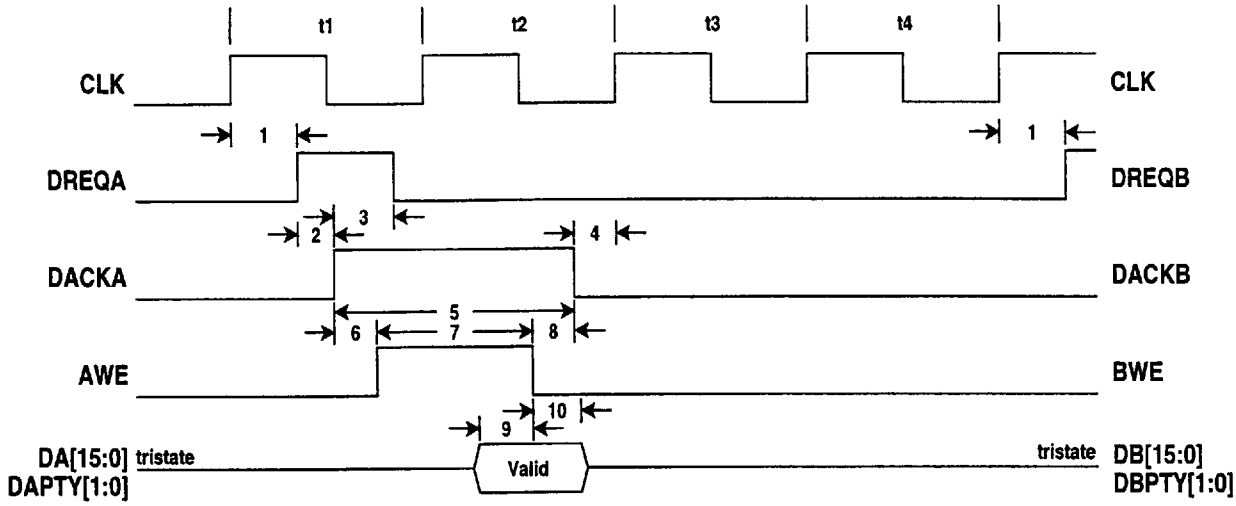


Table 22: DMA Master Transfer Timing for Data Into Port A,B

NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	CLK rise to DREQA high	0	25	nsec	
2	DREQA high to DACKA high	0		nsec	
3	DACKA high to DREQA low	0	25	nsec	
4	DACKA low setup to CLK rise	5		nsec	1
5	DACKA high pulsewidth	25		nsec	
6	DACKA high to AWE high	0		nsec	
7	AWE high pulsewidth	25		nsec	
8	AWE low to DACKA low	0		nsec	
9	DA[15:0], DAPTY[1:0] setup to AWE fall	10		nsec	2
10	DA[15:0], DAPTY[1:0] hold from AWE fall	10		nsec	2

Notes:

1) *The DACKA signal can be asynchronous to the CLK signal. It is internally synchronized to the rising edge of CLK. If the setup time number 4 is met at T3, the maximum data transfer rate will be achieved.*
2) *If the AWE pin is programmed to be disabled, substitute the DACKA pin for the AWE pin in the timing specifications.*
3) *If AWE is used as an input to the AHA3211 part it may be valid only during DACKA valid. This restriction also applies to BWE being valid during DACKB.*
4) *Port A and Port B have the same timing for their DMA interfaces. For Port B specifications, substitute the Port B name for the corresponding Port A name.*
5) *The signal DREQA is a chip output. DACKA, AWE, DAPTY[1:0] and DA[15:0] are chip inputs. DREQA, DACKA, AWE are programmed to be active high.*

Figure 28: DMA Master Transfer Timing for Data Out of Port A,B

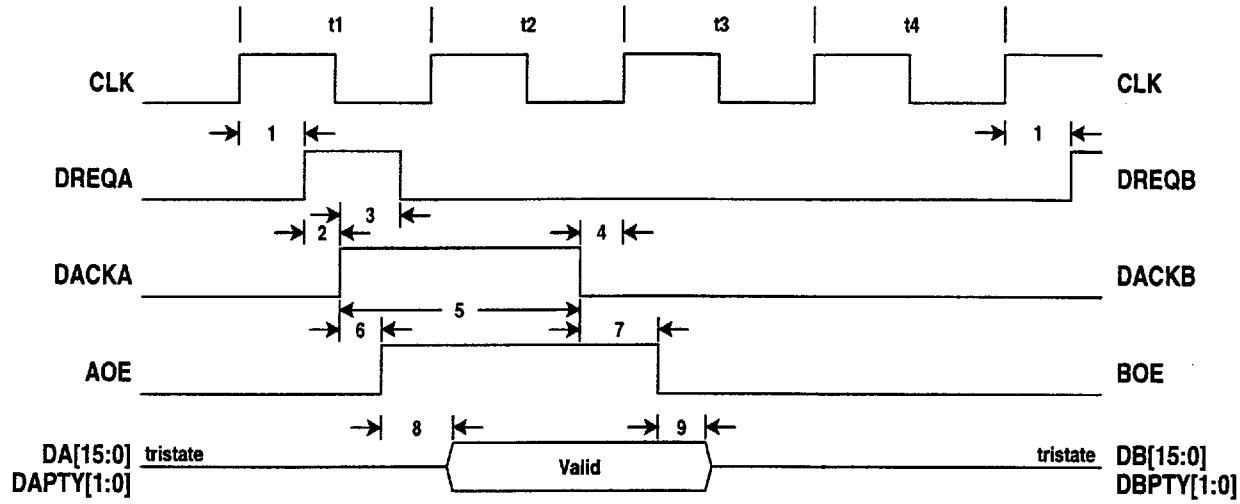


Table 23: DMA Master Transfer Timing for Data Out of Port A,B

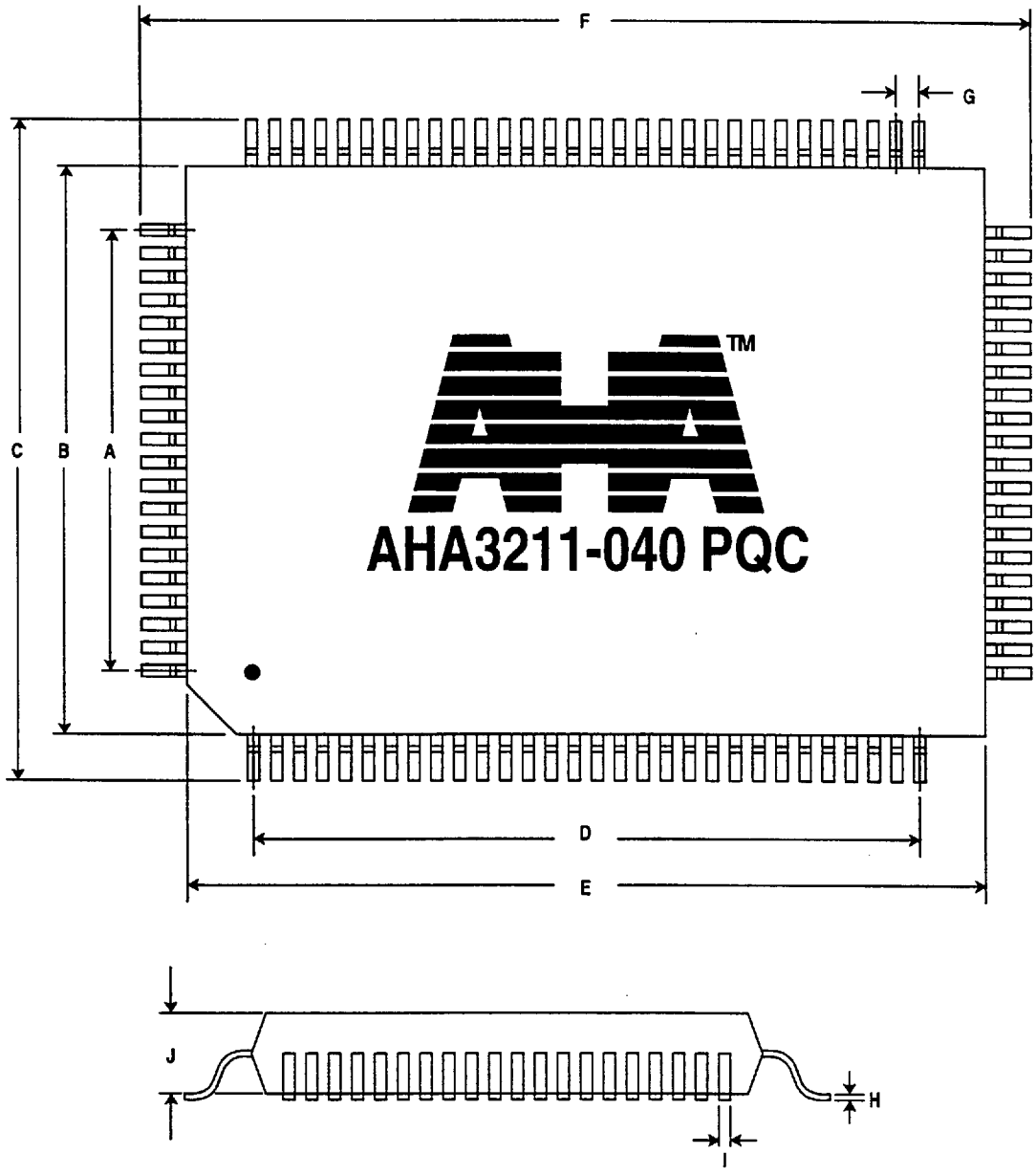
NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	CLK rise to DREQA high	0	25	nsec	
2	DREQA high to DACKA high	0		nsec	
3	DACKA high to DREQA low	0	25	nsec	
4	DACKA low setup to CLK rise	5		nsec	1
5	DACKA high pulsewidth	25		nsec	
6	DACKA high to AOE high	0		nsec	
7	DACKA low to AOE low		50	nsec	
8	AOE high to DA[15:0], DAPTY[1:0] valid	0	25	nsec	2
9	AOE low to DA[15:0], DAPTY[1:0] tristate	0	25	nsec	2

Notes:

1) *The DACKA signal can be asynchronous to the CLK signal. It is internally synchronized to the rising edge of CLK. If the setup time number 4 is met at T3, the maximum data transfer rate will be achieved.*
2) *If the AOE pin is programmed to be disabled, substitute the DACKA pin for the AOE pin in the timing specifications.*
3) *Port A and Port B have the same timing for their DMA interfaces. For Port B specifications, substitute the Port B name for the corresponding Port A name.*
4) *The signals DREQA, DAPTY[1:0], and DA[15:0] are chip outputs. DACKA, AOE, are chip inputs. DREQA, DACKA, AOE are programmed to be active high.*

8.0 PACKAGING

Figure 29: AHA3211 Package Specifications



AHA3211 CHIP DIMENSIONS									
A	*B*	*C*	*D*	*E*	*F*	*G*	*H*	*I*	*J*
12.35	14.0±0.1	17.9±0.4	18.85	20.0±0.1	23.9±0.4	0.65±0.12	0.15±0.050	0.3±0.1	2.75±0.10

Notes: All dimensions are in millimeters
Package type is 100 pin quad flat pack

9.0 ORDERING INFORMATION

9.1 AVAILABLE PARTS

PART NUMBER	DESCRIPTION
AHA3211A-040 PQC	20 MBytes/sec DCLZ Data Compression Coprocessor IC

9.2 PART NUMBERING

AHA	3211	A-	040	P	Q	C
Manufacturer	Device Number	Revision Level	Speed Designation	Package Material	Package Type	Test Specification

Device Number:
3211
Revision Letter:
A
Package Material Codes:
P Plastic
Package Type Codes:
Q Q - Quad Flat Pack
Test Specifications:
C Commercial 0°C to +70°C

10.0 AHA RELATED TECHNICAL PUBLICATIONS

DOCUMENT #	DESCRIPTION
ABDC02	AHA Application Brief – DCLZ Software Licensing Procedure
ABDC05	AHA Application Brief – Interfacing Requirements to CMOS Devices
ABDC07	AHA Application Brief – Compression Optimization in AHA3101 and AHA3210 Systems
ABSTD1	AHA Application Brief – AHA Data Compression and Forward Error Correction Standards
ANDC01	AHA Application Note – Primer: Data Compression Lempel Ziv (DCLZ)
ANDC04	AHA Application Note – Data Management for the AHA3210B
ANDC05	AHA Application Note – AHA3210B Designer's Guide
ANDC07	AHA Application Note – DCLZ Evaluation Software
ANDC09	AHA Application Note – Error Detection and Recovery in Data Compression System Using AHA3210B
ANDC10	AHA Application Note – Compression Performance: DCLZ Algorithm on the Calgary Corpus
GLGEN1	General Glossary of Terms
PB3101	AHA3101 Product Brief – DCLZ 2.5 MBytes/sec Data Compression Coprocessor IC
PB3210B	AHA3210B Product Brief – DCLZ 10 MBytes/sec Data Compression Coprocessor IC
PB3211	AHA3211 Product Brief – DCLZ 20 MBytes/sec Data Compression Coprocessor IC
PS3101	AHA3101 Product Specification – DCLZ 2.5 MBytes/sec Data Compression Coprocessor IC
PS3210B	AHA3210B Product Specification – DCLZ 10 MBytes/sec Data Compression Coprocessor IC
RAECMA-0791	"DCLZ Emerges as an Open Data Compression Standard," article reprint *Computer Technology Review*, Summer 1991
DCEVAL	DCLZ Evaluation Software (Windows™ 3.1)