T-46-07-08

GigaBit Logic

10G021A
10G021AM

Dual Precision D Flip Flop
2.7 GHz Clock Rate
10G PicoLogic™ Family

FEATURES

- DC to 2.7 GHz operation
- 0°C to +85°C operating temperature range
- -55°C to +125°C military temperature range
- Ultra-low input sampling skew
- Individual clock, preset, and clear inputs on each flip flop
- Negative edge triggered flip-flop design
- ECL & PicoLogic™ compatible complementary outputs
- High gain ECL compatible differential inputs
- Output stage supports a wide range of load resistor and termination voltage combinations
- Available in 40 pin leaded or leadless chip carrier and dice form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

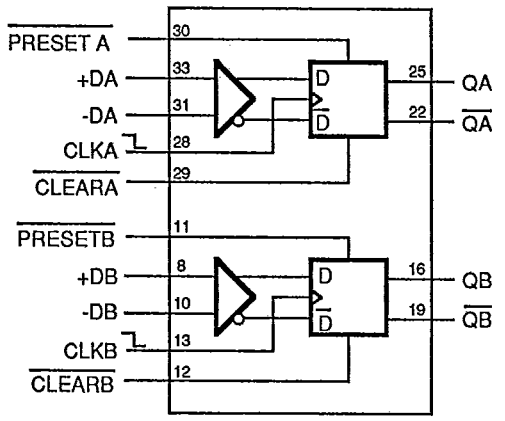
- Data repeaters/regenerators
- Decision circuits
- Synchronizers
- Data samplers

FUNCTIONAL DESCRIPTION

The 10G021A consists of two negative edge triggered precision D flip-flops capable of operating at clock frequencies of over 2 GHz. Each flip-flop features individual clock, preset, and clear inputs. Each half of the 10G021A contains a high speed differential data input to which the input signal is applied. When the input stage is used as a line receiver or amplifier the data inputs can be driven differentially for maximum noise immunity. The - D input may also be used as a reference input to allow selection of the switching threshold. When the - D input is connected to an ECL generated VBB the + D input can be driven from an ECL compatible source. The complementary outputs are ECL and PicoLogic compatible, and support a wide range of load resistor and termination voltage combinations. The output driver has been designed for maximum symmetry between Q and $\overline{Q}$ output waveforms.The design of the 10G021A is such that high and low input data are sampled at the same point in time relative to the falling clock edge. This eliminates pulse lengthening or shrinking encountered with traditional D flip-flops which sample high and low data a gate delay apart in time. The 10G021A's precise data sampling translates to ultra low data sampling skew. Thus the 10G021A's output data eye pattern is highly symmetrical minimizing distortion of regenerated data.

The 10G021A is fabricated using GigaBit's high volume GaAs MESFET process technology.

BLOCK DIAGRAM



10G021A ORDERING INFORMATION

Pkg. Type	Min. Speed (0°C to 85°C)		
	2.3 GHz	2.0 GHz	1.5 GHz
C L Dice	10G021A-2C 10G021A-2L	10G021A-C 10G021A-L	10G021A-3C 10G021A-3L 10G021A-3X
Pkg. Type	**Min. Speed (-55°C°C to +125°C)**		
	2.0 GHz	1.7 GHz	1.2 GHz
C L Dice	10G021AM-2C 10G021AM-2L	10G021AM-C 10G021AM-L	10G021AM-3C 10G021AM-3L 10G021AM-3X

T-46-07-08

GigaBit Logic

10G021A
10G021AM

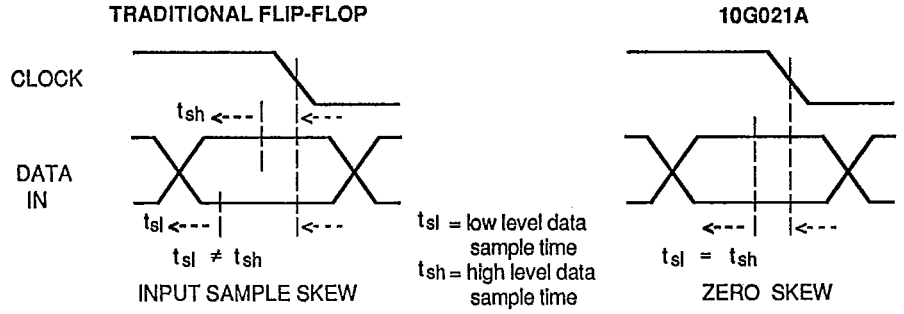
FUNCTIONAL DESCRIPTION (cont.)

The data at the D input is transferred to the Q output on the negative going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect on the output. The preset and clear input signals can set the condition of the flip-flop at any time, regardless of the presence or absence of a clock edge. The detailed operation of the 10G021A is summarized in the truth table.

TRUTH TABLE

$\overline{PRESET}$	$\overline{CLEAR}$	CLOCK	DATA	Q	$\overline{Q}$
H	H	⌐	0	0	1
H	H	⌐	1	1	0
H	H	1	X	Q(t-1)	$\overline{Q}$(t-1)
L	L	NOT ALLOWED			
L	H	X	X	1	0
H	L	X	X	0	1

DATA SAMPLING



PIN DESCRIPTIONS

+D, -D	Differential data inputs. The effective data input voltage is the difference between the +D and -D inputs [i.e., (+D) - (-D)].
CLOCK	Clock input (falling edge triggered). The input sampling rate of the +D and -D inputs is equal to the CLOCK frequency.
$\overline{CLEAR}$	Active low clear input.
$\overline{PRESET}$	Active low preset input.
Q	True data output. The effective output data rate is equal to one half the CLOCK rate.
$\overline{Q}$	Complementary data output.
VDDO	Output driver ground (0V). VDDOA and VDDOB are electrically separate. Side A and B output drivers can be powered separately.
VDDL	Internal logic ground (0V).
VEE	- 5.2V supply voltage
VSS	-3.4 V supply voltage
VBBS	GaAs threshold reference voltage. VBBS is internally connected to VBB for easy PicoLogic interfacing.
VTTC	VDDO internal decoupling capacitor return. VTTC is brought into the 10G021A package as the AC return lead for the internal VDDO output driver power supply decoupling capacitor. It is not brought onto the 10G021A die. VTTC is typically equal to VTT (nominally - 2.0 V).
VDCH	Output driver high level clamp voltage. When not used, VDCH should be connected to VDDO. When driving ECL, VDCH may be used to limit VOH. See Application Note 4 for details.

GigaBit Logic

10G021A
10G021AM

DC CHARACTERISTICS

Tc = 0°C to 85°C (10G021A); -55°C to 125°C (10G021AM), VSS = -3.5 V to -3.3 V, VEE = -5.5 V to -5.1 V, VDDL = VDDO = 0 V, unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Input Voltage High; Clock, Preset, Clear inputs	-0.8		VDDL	V	
VIL	Input Voltage Low; Clock, Preset, Clear inputs	VTT		-1.7	V	
I IN	Input Current Clock, Preset, Clear inputs	-250	225	600	µA	VIN: -0.8 V to -1.7 V
ISS	Power Supply Current		150	250	mA	
IEE	Power Suppy Current		35	100	mA	No Load
PD	Power Dissipation		700	1400	mW	

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

		10G021A-2							10G021AM-2								
Symbol	Parameter	0°C		Tc = +25°C			+85°C		-55°C		Tc = +25°C			+125°C		Units	Notes
		Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max		
1/T1	Max Clock Frequency	2.3		2.7			2.3		2.0		2.7			2.0		GHz	2, 6
T2	(+D)-(-D) Hold Time	0		0	-60		0		0		0	-60		0		ps	
T3	(+D)-(-D) Setup Time	250		250	165		250		265		250	165		265		ps	
T4	$\overline{\text{Preset}}$ Pulse Width	750		750	500		750		1000		750	500		1000		ps	
T5	$\overline{\text{Preset}}$ Low to Q High		700		575	700		700		850		575	700		850	ps	
T6	$\overline{\text{Preset}}$ Low to $\overline{Q}$ Low		700		575	700		700		850		575	700		850	ps	
T7	$\overline{\text{Clear}}$ Pulse Width	750		750	500		750		1000		750	500		1000		ps	
T8	$\overline{\text{Clear}}$ Low to Q Low		750		625	750		750		900		625	750		900	ps	
T9	$\overline{\text{Clear}}$ Low to $\overline{Q}$ High		750		625	750		750		900		625	750		900	ps	
T10	Clock Low to Q High		625		525	625		625		750		525	625		750	ps	
T11	Clock Low to $\overline{Q}$ Low		625		525	625		625		750		525	625		750	ps	
T12	Clock Low to Q Low		625		525	625		625		750		525	625		750	ps	
T13	Clock Low to $\overline{Q}$ High		625		525	625		625		750		525	625		750	ps	
Tr	Output Rise Time		220		180	220		220		240		180	220		240	ps	3
Tf	Output Fall Time		140		125	140		140		160		125	140		160	ps	3
	Clock to Output Skew		100		60	75		100		100		60	75		100	ps	4
	Input Sample Skew				25							25				ps	5
Tw	Clock Pulsewidth	200		180			200		200		180			200		ps	

T-46-07-08

GigaBit Logic

10G021A
10G021AM

AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

Symbol	Parameter	10G021A 0°C Min	10G021A 0°C Max	10G021A Tc = +25°C Min	10G021A Tc = +25°C Typ	10G021A Tc = +25°C Max	10G021A +85°C Min	10G021A +85°C Max	10G021AM -55°C Min	10G021AM -55°C Max	10G021AM Tc = +25°C Min	10G021AM Tc = +25°C Typ	10G021AM Tc = +25°C Max	10G021AM +125°C Min	10G021AM +125°C Max	Units	Notes
1/T1	Max Clock Frequency	2.0		2.3			2.0		1.7		2.3			1.7		GHz	2, 6
T2	(+D)-(-D) Hold Time	0		0	-50		0		0		0	-50		0		ps	
T3	(+D)-(-D) Setup Time	265		265	175		265		300		265	175		300		ps	
T4	$\overline{\text{Preset}}$ Pulse Width	1000		1000	670		1000		1300		1000	670		1300		ps	
T5	$\overline{\text{Preset}}$ Low to Q High		850		650	850		850		1050		650	850		1050	ps	
T6	$\overline{\text{Preset}}$ Low to $\overline{\text{Q}}$ Low		850		650	850		850		1050		650	850		1050	ps	
T7	$\overline{\text{Clear}}$ Pulse Width	1000		1000	670		1000		1300		1000	670		1300		ps	
T8	$\overline{\text{Clear}}$ Low to Q Low		900		700	900		900		1200		700	900		1200	ps	
T9	$\overline{\text{Clear}}$ Low to $\overline{\text{Q}}$ High		900		700	900		900		1200		700	900		1200	ps	
T10	Clock Low to Q High		750		600	750		750		950		600	750		950	ps	
T11	Clock Low to Q Low		750		600	750		750		950		600	750		950	ps	
T12	Clock Low to $\overline{\text{Q}}$ Low		750		600	750		750		950		600	750		950	ps	
T13	Clock Low to $\overline{\text{Q}}$ High		750		600	750		750		950		600	750		950	ps	
Tr	Output Rise Time		240		200	240		240		275		200	240		275	ps	3
Tf	Output Fall Time		160		150	160		160		220		150	160		220	ps	3
	Clock to Output Skew				75	100						75	100			ps	4
	Input Sample Skew				30							30				ps	5

AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

Symbol	Parameter	10G021A-3 0°C Min	10G021A-3 0°C Max	10G021A-3 Tc = +25°C Min	10G021A-3 Tc = +25°C Typ	10G021A-3 Tc = +25°C Max	10G021A-3 +85°C Min	10G021A-3 +85°C Max	10G021AM-3 -55°C Min	10G021AM-3 -55°C Max	10G021AM-3 Tc = +25°C Min	10G021AM-3 Tc = +25°C Typ	10G021AM-3 Tc = +25°C Max	10G021AM-3 +125°C Min	10G021AM-3 +125°C Max	Units	Notes
1/T1	Max Clock Frequency	1.5		1.8			1.5		1.2		1.8			1.2		GHz	2, 6
T2	(+D)-(-D) Hold Time	0		0	-40		0		0		0	-40		0		ps	
T3	(+D)-(-D) Setup Time	300		300	190		300		350		300	190		350		ps	
T4	$\overline{\text{Preset}}$ Pulse Width	1300		1300	870		1300		1500		1300	870		1500		ps	
T5	$\overline{\text{Preset}}$ Low to Q High		1150		900	1150		1150		1350		900	1150		1350	ps	
T6	$\overline{\text{Preset}}$ Low to $\overline{\text{Q}}$ Low		1150		900	1150		1150		1350		900	1150		1350	ps	
T7	$\overline{\text{Clear}}$ Pulse Width	1300		1300	870		1300		1500		1300	870		1500		ps	
T8	$\overline{\text{Clear}}$ Low to Q Low		1200		950	1200		1200		1400		950	1200		1400	ps	
T9	$\overline{\text{Clear}}$ Low to $\overline{\text{Q}}$ High		1200		950	1200		1200		1400		950	1200		1400	ps	
T10	Clock Low to Q High		1050		850	1050		1050		1250		850	1050		1250	ps	
T11	Clock Low to $\overline{\text{Q}}$ Low		1050		850	1050		1050		1250		850	1050		1250	ps	
T12	Clock Low to Q Low		1050		850	1050		1050		1250		850	1050		1250	ps	
T13	Clock Low to $\overline{\text{Q}}$ High		1050		850	1050		1050		1250		850	1050		1250	ps	
Tr	Output Rise Time		275		250	275		275		320		250	275		320	ps	3
Tf	Output Fall Time		220		200	220		220		275		200	220		275	ps	3
	Clock to Output Skew				125	175						125	175			ps	4
	Input Sample Skew				40							40				ps	5

T-46-07-08

GigaBit Logic

10G021A
10G021AM

NOTES: 1. Test conditions (unless otherwise indicated):

-D = -1.2V	VDCH = VDDL	VTTC = VTT
VTT = -2.0V	VOH ≥ -0.7V	
RLOAD = 50 Ohms to VTT	VOL ≤ -1.7V	

Data rate = one half the clock rate
Clock logic swing = 2V P/P sinusoid centered at -1.2V
Preset, Clear, and data input logic swing = 1V P/P pulse centered at -1.2V

2. 50% duty cycle at maximum clock frequency.
3. Output edge rates are specified at 20% to 80% output transition.
4. Clock to Output Skew is the maximum delay difference among T10, T11, T12, and T13.
5. Input Sample Skew is the relative difference in time between the point at which high level data and low level data are sampled by the falling edge of the Clock input.
6. Clock input rise and fall times should be less than or equal to 1 ns.

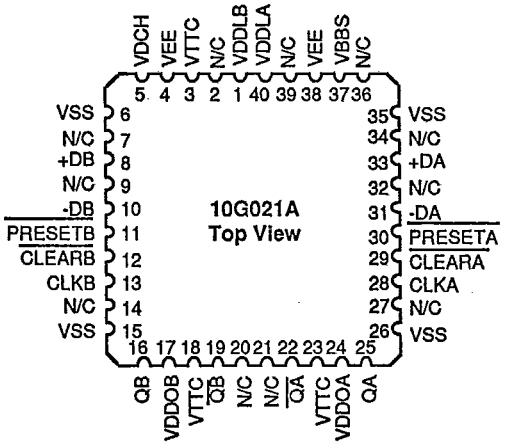
CLOCK SOURCES

GaAs logic will typically be used to drive the 10G021A CLOCK input. Alternatively, GigaBit Logic recommends the use of inexpensive VCO generators with 10 dBm or greater output power. Because ECL logic is typically limited to clock rates less than 500 MHz, the 10G021A CLOCK input will normally not be driven with ECL logic levels.

The 10G021A will operate with smaller peak to peak clock swings. The table below indicates the typical reduction in maximum clock frequency as a function of P/P sinusoidal clock levels.

2.0V P/P	1.4V P/P	1.0V P/P
0	15%	30%

PIN FUNCTIONS - PACKAGE TYPES "C" OR "L"



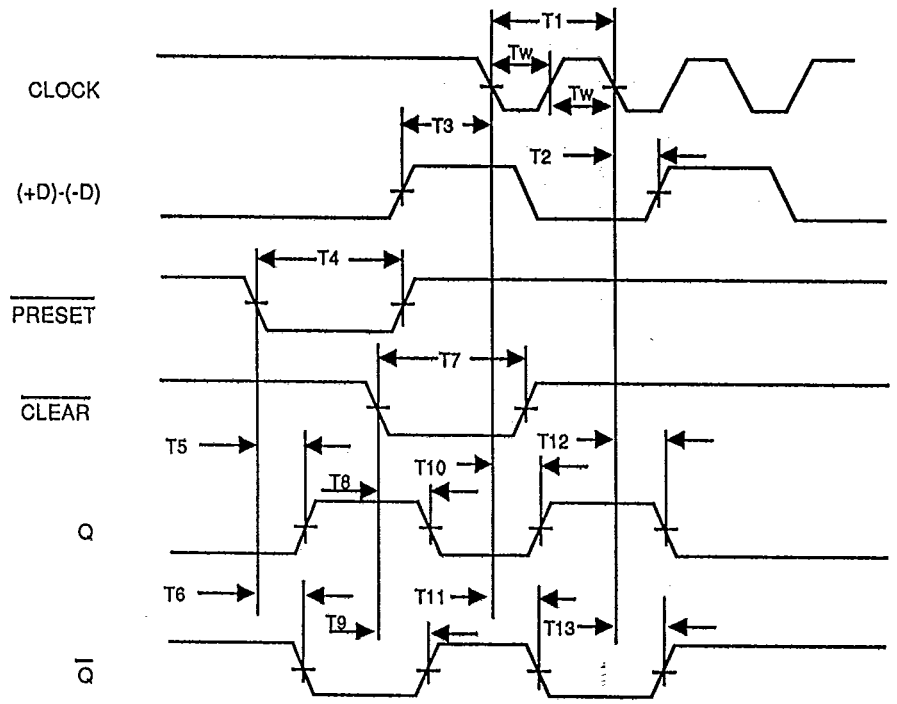
N/C: No Connection

T-46-07-08

GBL GigaBit Logic

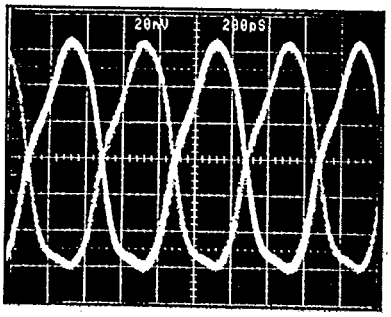
10G021A
10G021AM

SWITCHING WAVEFORMS

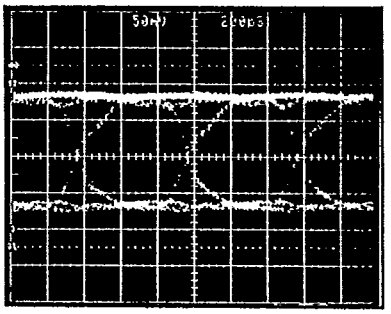


TYPICAL OUTPUT WAVEFORMS

10G021A Q Output Eye Pattern
2.5 GHz Clock Rate
Sinusoidal data rate = 1.25 GHz
(corrected vertical = 200mV/div.)



10G021A Q Output Eye Pattern
Data Input = 1.6 Gbps 2^7 - 1 pseudorandom bit stream generated by the 10G040 Multiplexer
1.6 GHz Clock Rate
(corrected vertical = 500 mV/div.)



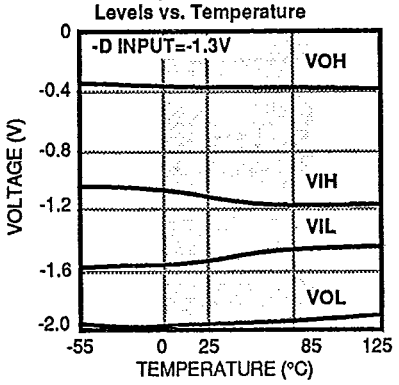
T-46-07-08

GigaBit Logic

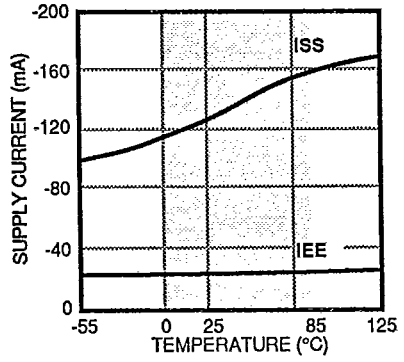
10G021A
10G021AM

TYPICAL PERFORMANCE CHARACTERISTICS

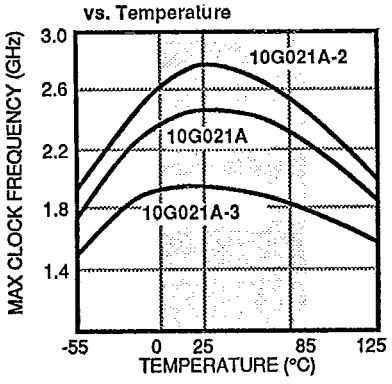
Data Input and Q Output Levels vs. Temperature



ISS & IEE vs. Temperature



Maximum Clock Frequency vs. Temperature

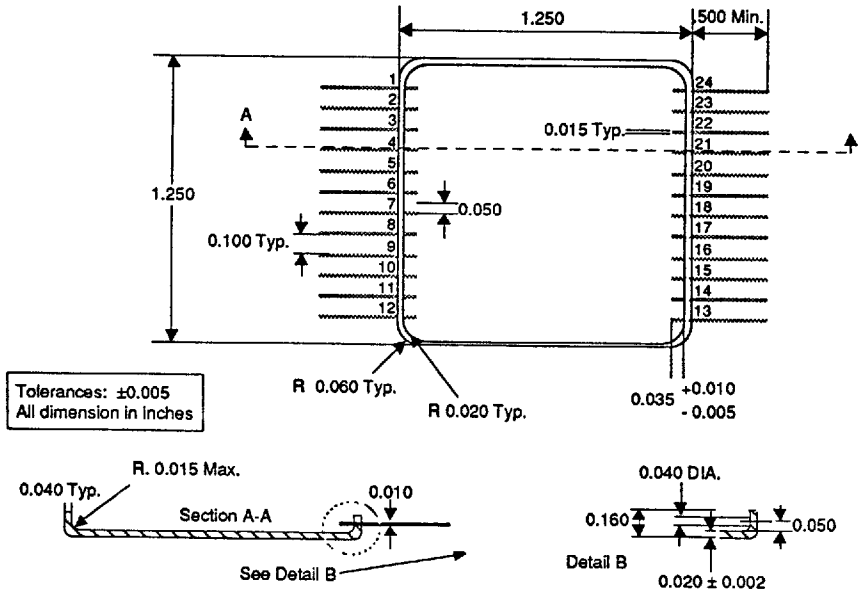


T-90-20

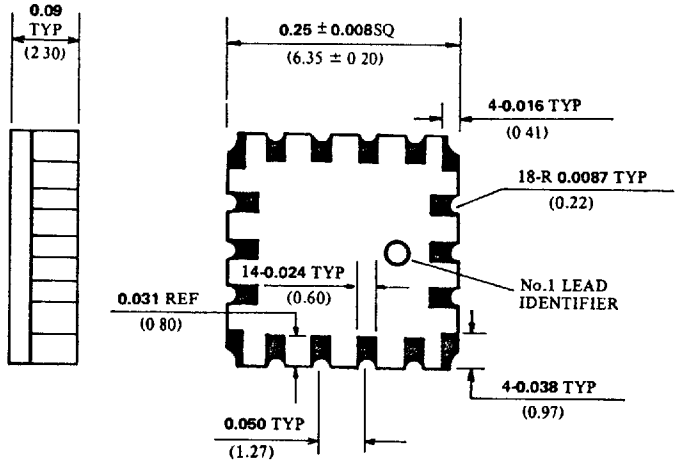
GigaBit Logic

24 PIN METAL FLATPACK
18 PIN PACKAGE

24 PIN METAL FLATPACK
Type H



18 PIN LEADLESS CHIP CARRIER
TYPE L1



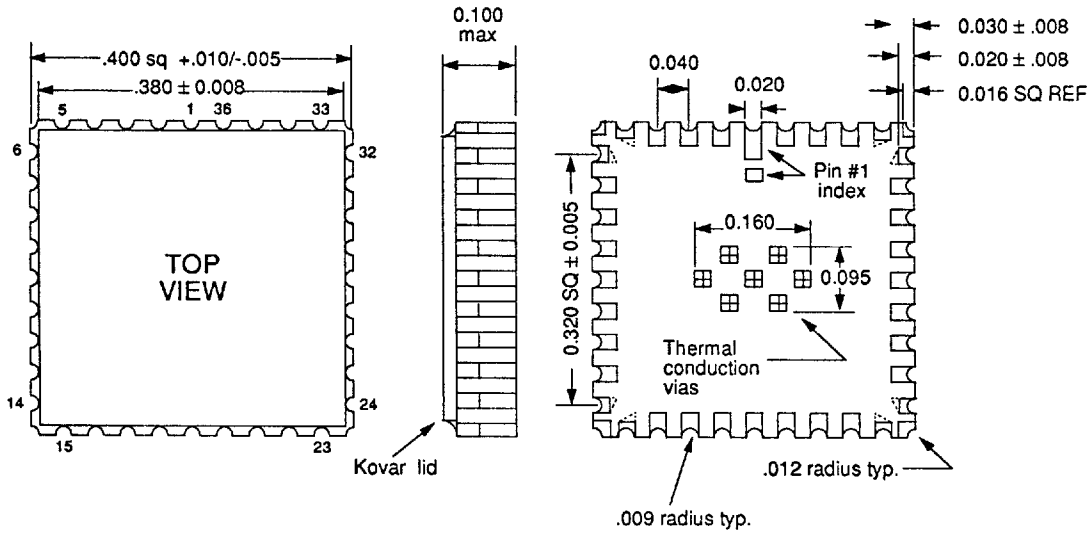
All dimensions shown in inches and (millimeters)

11

GigaBit Logic

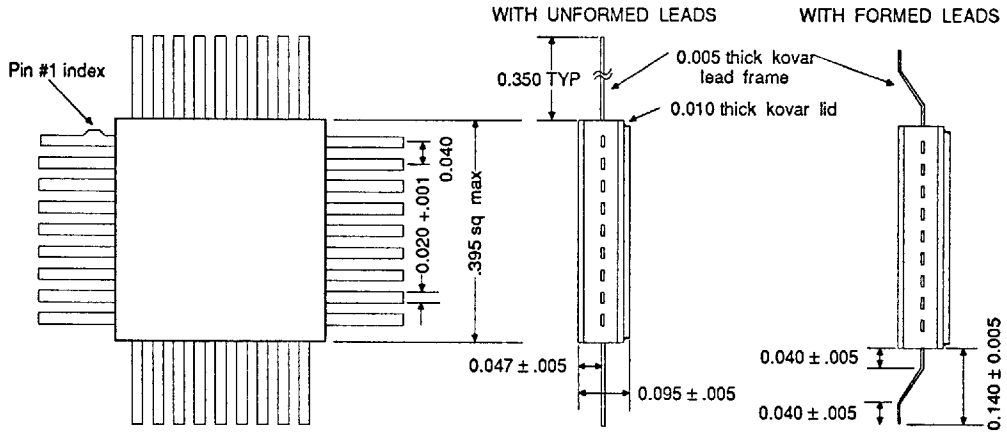
36 PIN PACKAGES

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Plin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F

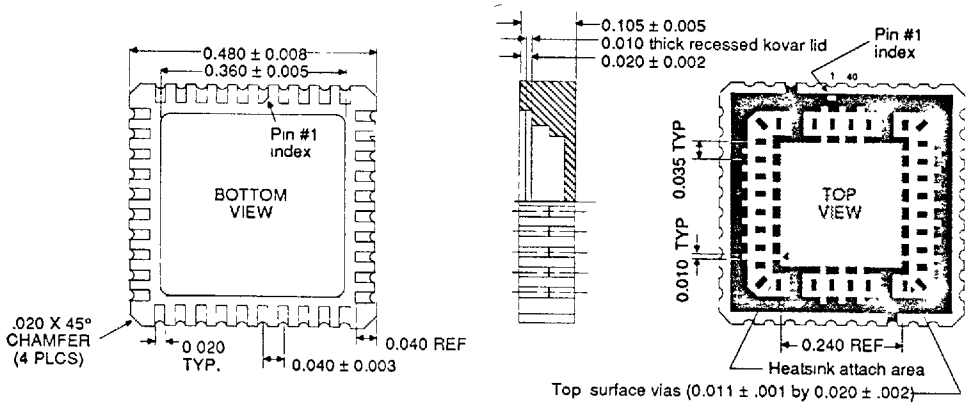


T-90-20

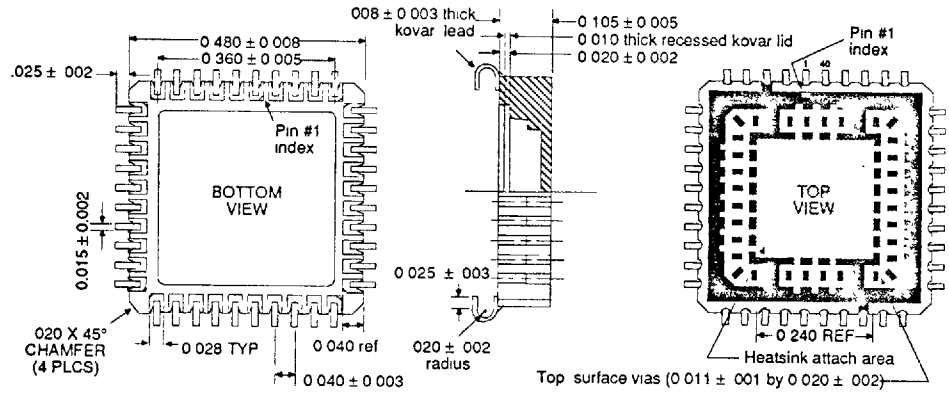
GigaBit Logic

40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L

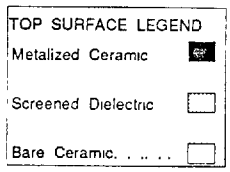


40 PIN LEADED CHIP CARRIER
TYPE C

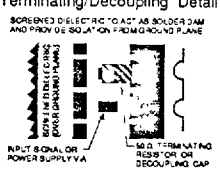


NOTES

(1) Footprint is JEDEC standard outline
(2) Top surface v as (for terminating resistors and decoupling capacitors) are not available on pins 3 4 17 18 23 24 37 and 38
(3) Top surface metal (not including vias) and p ns 3 and 23 are fixed at VTT potential
(4) Recommended top surface chip res stors are 0 040 long by 0 020 w de by 0 010 thick typ 100 mw min nominal power rating (M ni-Systems MSR 21 or equivalent)
(5) Recommended top surface ch p capac tors are 0 040 ong by 0 030 wide by 0 020 thick typ 25V VDCW 1000 pf min (Johanson R09 case or equivalent)
(6) Recommended heatsinks a e GBL P/Ns 90GHS 40 A and 90GHS 40 B
(7) Thermally conductive, e ectrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789 4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width



Top Surface Terminating/Decoupling Detail

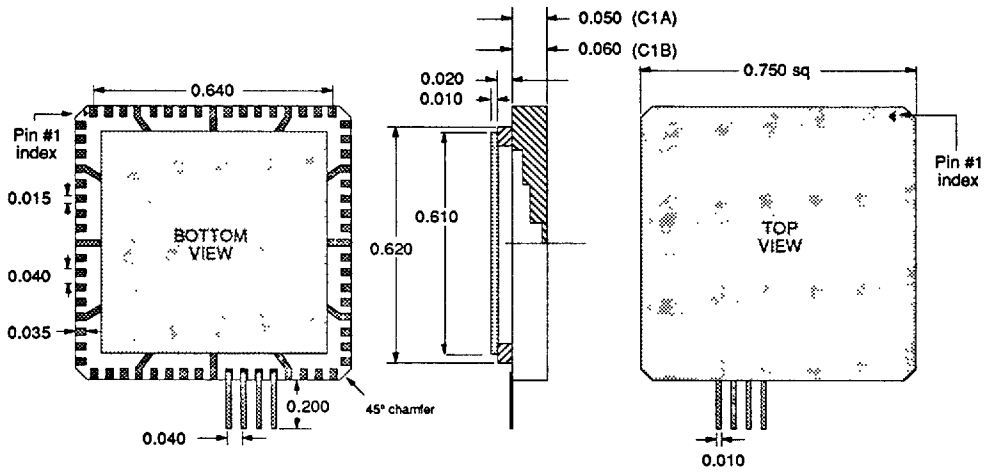


T-90-20

GigaBit Logic

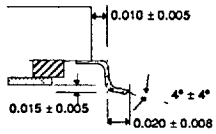
68 & 132 PIN PACKAGES

68 PIN LEADED CHIP CARRIER
TYPE C1



1. All dimensions in inches.
2. C1A PACKAGE: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
3. C1B PACKAGE: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
4. Tolerance on all dimensions is ± 1 % but not larger than ± 0.005. Tolerance on 0.640 end pad to end pad dimension is ± 0.003.

GULLWING LEADS



132 PIN LEADED CHIP CARRIER
TYPE C3