ADMA-T1P Device
1.544 Mbit/s to VT1.5/TU-11 Async Mapper-Desync
TXC-04011

DATA SHEET
Preliminary

FEATURES

- Add/drop two 1.544 Mbit/s signals from an STS-1, an STS-3/AU-3, or an STM-1 VC-4
- Independent add and drop bus timing modes
- Selectable AMI or B8ZS positive/negative rail or NRZ T1 interface. Performance counter provided for illegal coding violations
- Digital desynchronizer reduces systemic jitter in the presence of multiple pointer movements. A register is also provided to control the internal FIFO leak rate
- Drop buses are monitored for parity, loss of clock, and H4 multiframe errors
- Performance counters are provided for VT/TU pointer movements, BIP-2 errors and Far End Block Errors (FEBEs)
- VT/TUs are monitored for Loss Of Pointer, New Data Flags (NDFs), AIS, Remote Defect Indication (RDI), and size errors (S-bits)
- V5 byte Signal Label Mismatch and Unequipped detection
- Loopback, generate BIP-2 errors, and send RDI capability
- Intel microprocessor interface
- 120-pin plastic quad flat package

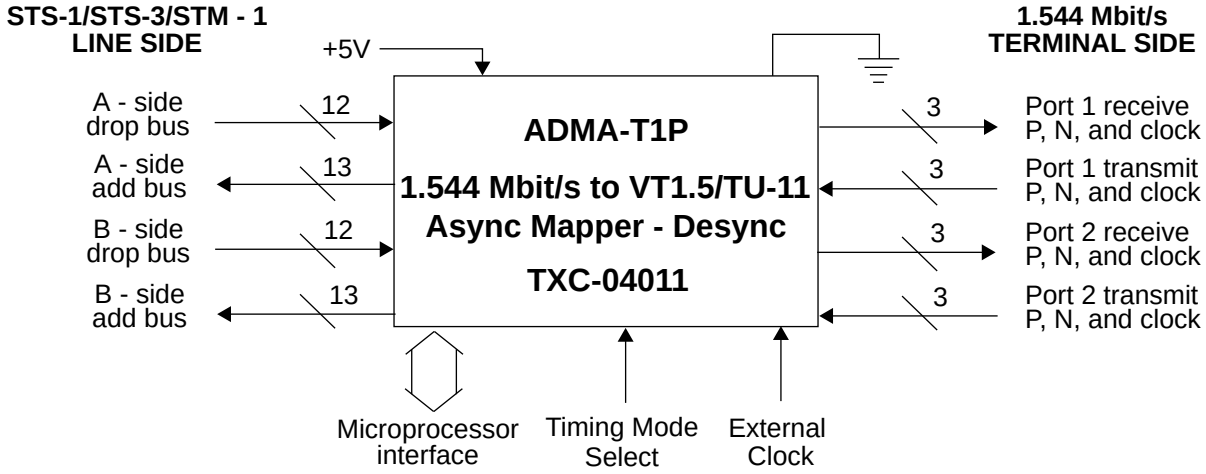
DESCRIPTION

The ADMA-T1P device is designed for add/drop multiplexer, terminal multiplexer, and dual and single unidirectional ring applications. Two T1 1.544 Mbit/s signals are mapped to and from asynchronous 1.5 Virtual Tributaries (VT1.5s) or Tributary Unit - 11s (TU-11s). The ADMA-T1P interfaces to a multiple-segment, byte-parallel SONET/SDH-formatted bus at the 19.44 Mbit/s byte rate for STM-1/STS-3 operation or at the 6.48 Mbit/s byte rate for STS-1 operation. The T1 1.544 Mbit/s signals can be either AMI/B8ZS positive/negative rail- or NRZ-formatted signals. The ADMA-T1P provides performance counters, alarm detection, and the ability to generate errors and Alarm Indication Signals (AIS). T1 port loopback capability is also provided. The dual timing mode Plus feature increases the I/O signal pin count by 7 from the ADMA-T1 device level so that the ADMA-T1P has a 120-pin package.

The ADMA-T1P bus interface is used to connect to other TranSwitch devices such as the STM-1/STS-3/STS-3c Overhead Terminator (SOT-3), TXC-03003, to form an STS-3/STM-1 add/drop or terminal system.

APPLICATIONS

- STS-1/STS-3/STM-1 to 1.544 Mbit/s add/drop mux/demux
- Unidirectional or bidirectional ring applications
- STS-1/STS-3/STM-1 termination terminal mode multiplexer
- STS-1/STS-3/STM-1 test equipment



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TranSwitch Corporation • 8 Progress Drive • Shelton, CT 06484 • USA • Tel: 203-929-8810 • Fax: 203-926-9453

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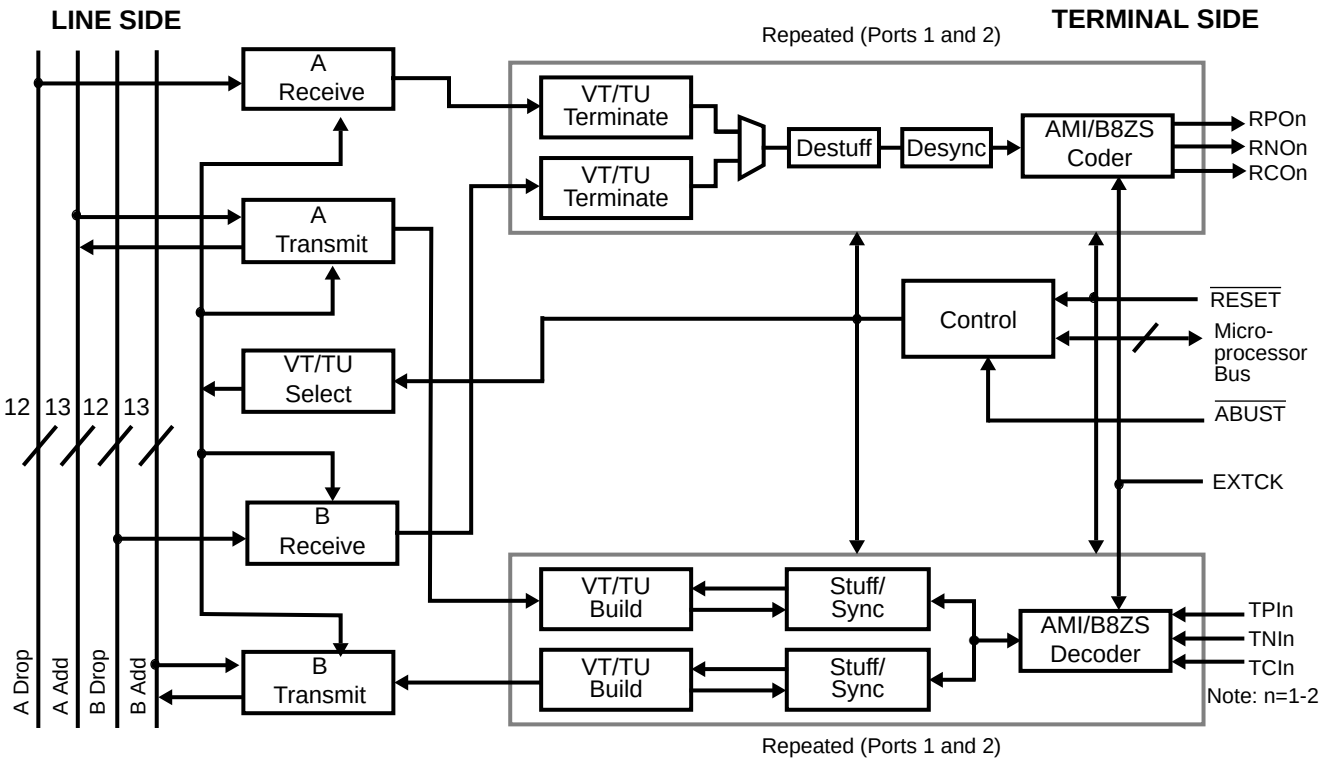


Figure 1. ADMA-T1P TXC-04011 Block Diagram

BLOCK DIAGRAM DESCRIPTION

The block diagram for the ADMA-T1P is shown in Figure 1. The ADMA-T1P interfaces to four buses, designated as A Drop, A Add, B Drop and B Add. The four buses run at the STS-3/STM-1 rate of 19.44 Mbytes/s, or at the STS-1 rate of 6.48 Mbytes/s. For North American applications, the asynchronous T1 signals are carried in floating Virtual Tributary 1.5s (VT1.5s) in a Synchronous Transport Signal -1 (STS-1), or in STS-1s that are carried in the Synchronous Transport Signal - 3 (STS-3). For ITU-T applications, the T1 signals are carried in floating mode Tributary Unit - 11s (TU-11s) in the STM-1 Virtual Container - 4 structure (VC-4) using Tributary Unit Group - 3 (TUG-3), or in the STM-1 Virtual Container - 3 structure (VC-3) using Tributary Unit Group - 2 (TUG-2) mapping schemes. Two T1 signals can be connected (dropped) from one bus (A Drop or B Drop), or both of the drop buses to the T1 lines. Two asynchronous T1 signals are formatted into VT1.5s or TUs and are connected (added) to either of the add buses (or both, depending upon the mode of operation). When the ABUST input is set high to configure the ADMA-T1P for the drop bus timing mode, the add buses are, by definition, byte, frame, and multiframe synchronous with their like-named drop buses, but delayed because of internal processing. For example, if a byte from a VT1.5 or TU-11 is to be added to the A Add bus, the time of its placement on the bus is derived from A Drop bus timing, and from software instructions specifying which VT/TU number is to be dropped. When the device is configured for the add bus timing mode (ABUST set low), the add bus data, parity and add indicator signals are derived from the add clock, C1J1V1 and SPE signals. There will be a delay of either one or two clock cycles for the output signals relative to the add bus C1J1V1 and SPE signals.

The A Receive Block is identical to the B Receive Block. The VT/TU Terminate, Destuff, Desync, and AMI/B8ZS Line Coder Blocks are also repeated for both ports. Twelve leads are connected between a drop bus and the ADMA-T1P A or B Drop bus interface. The interface consists of a byte clock, byte-wide data, a C1J1 indicator signal, a payload identification signal (SPE) and parity. Parity is selectable for odd or even parity, and for data only.

Depending upon the application, buffers and latches may be used between the system buses and an ADMA-T1P. Each bus interface is monitored for parity, loss of clock, and H4 multiframe errors. Under microprocessor control, the two receive blocks extract a VT1.5 or TU-11 from the STS-3 or VC-4 in the VT/TU Terminate Blocks.

Each Terminate Block performs pointer processing (V1 and V2), overhead byte (V5) processing, and provides a bit status of the eight receive overhead communications bits located in the control bytes in the VT/TU (see Figure 2). The pointer bytes are monitored for an NDF indication, and for AIS, and Loss Of Pointer alarms. In addition, the size (S-bits) in the pointer bytes are monitored for the correct value. Overhead byte (V5) processing includes a BIP-2 parity check, along with the count of detected errors, counting the number of received Far End Block Errors (FEBE), the states of the receive signal label, mismatch of the receive signal label against a microprocessor written value, unequipped status detection, and the status of the Remote Defect Indication (RDI) bit, and the Remote Failure Indication (RFI) bit.

Depending on the drop bus selected, the VT/TU is destuffed using majority rule for the two sets of three justification control bits (Cn) which determines whether the two S-bits are data bits or justification bits.

The Desync Block removes the effects on the output of systemic jitter that might occur due to signal mappings and pointer movements. The Desync Block contains two parts, a pointer leak buffer and a T1 loop buffer. The function of the pointer leak buffer is to accept up to five consecutive positive or negative pointer adjustments and to ramp out the effect over a specified period of time. The T1 Loop Buffer consists of a digital loop filter, which is designed to track the frequency of the received T1 signal and to remove both transmission and stuffing jitter.

An option for each port provides either NRZ data and clock or an AMI/B8ZS-coded positive and negative rail signals for the T1 line interface. Transmit data (towards the T1 line) is clocked out of the ADMA-T1P on rising edges of the clock.

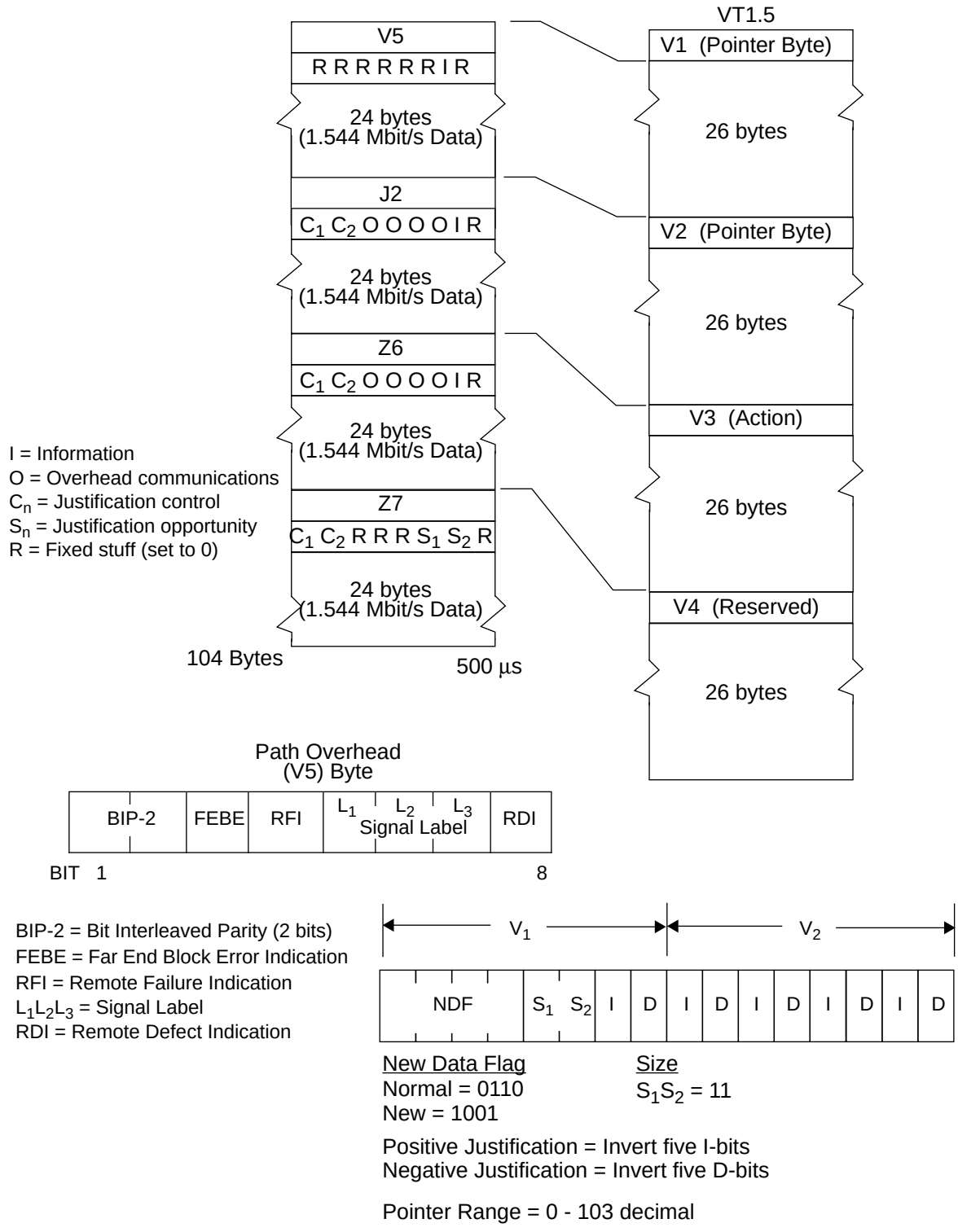
Towards the SONET/SDH add buses, the ADMA-T1P accepts either T1 AMI/B8ZS-coded positive and negative rail signals or NRZ data. A 16-bit performance counter is provided that counts illegal AMI or B8ZS coding violations. The T1 line is monitored for AIS, and loss of clock or signal.

The Stuff/Sync Block time buffers the T1 signal for frequency justification by the Stuff Block. The Stuff/Sync Block contains a FIFO and uses threshold modulation for the VT/TU justification process.

This Block also permits tracking of the incoming T1 signal having an average frequency offset as high as 120 ppm, and up to 5 UI of peak-to-peak jitter. The interface between this Block and the VT/TU Build Block is bidirectional. The VT/TU Build Block request bits from the FIFO based on the VT/TU phase. The justification algorithm fixes the first S-bit (S1) to the pattern 1110 every four multiframes. The second S-bit contains either data or a justification bit based on a length measurement. Since the ADMA-T1P supports a ring system architecture, two sets of Blocks are provided for each port.

The VT/TU Block formats the VT/TU into an STS-1, STS-3 or STM-1 structure for asynchronous 1.544 Mbit/s signals, as shown in Figure 2. The pointer value (in the V1 and V2 bytes) is fixed to a value of 78. Access is provided for determining the states of the overhead communications channel (O-bits) located in two justification control bytes in the VT/TU format. Access is also provided for transmitting the signal label and the Remote Defect Indication (RDI) bit, both of which are located in the V5 overhead byte. The Far End Block Error (FEBE) bit state is determined by the BIP-2 detector in the drop side. In addition, a control bit is provided for generating a VT/TU AIS (all ones).

Figure 2. 1.544 Mbit/s Mapping



PIN DIAGRAM

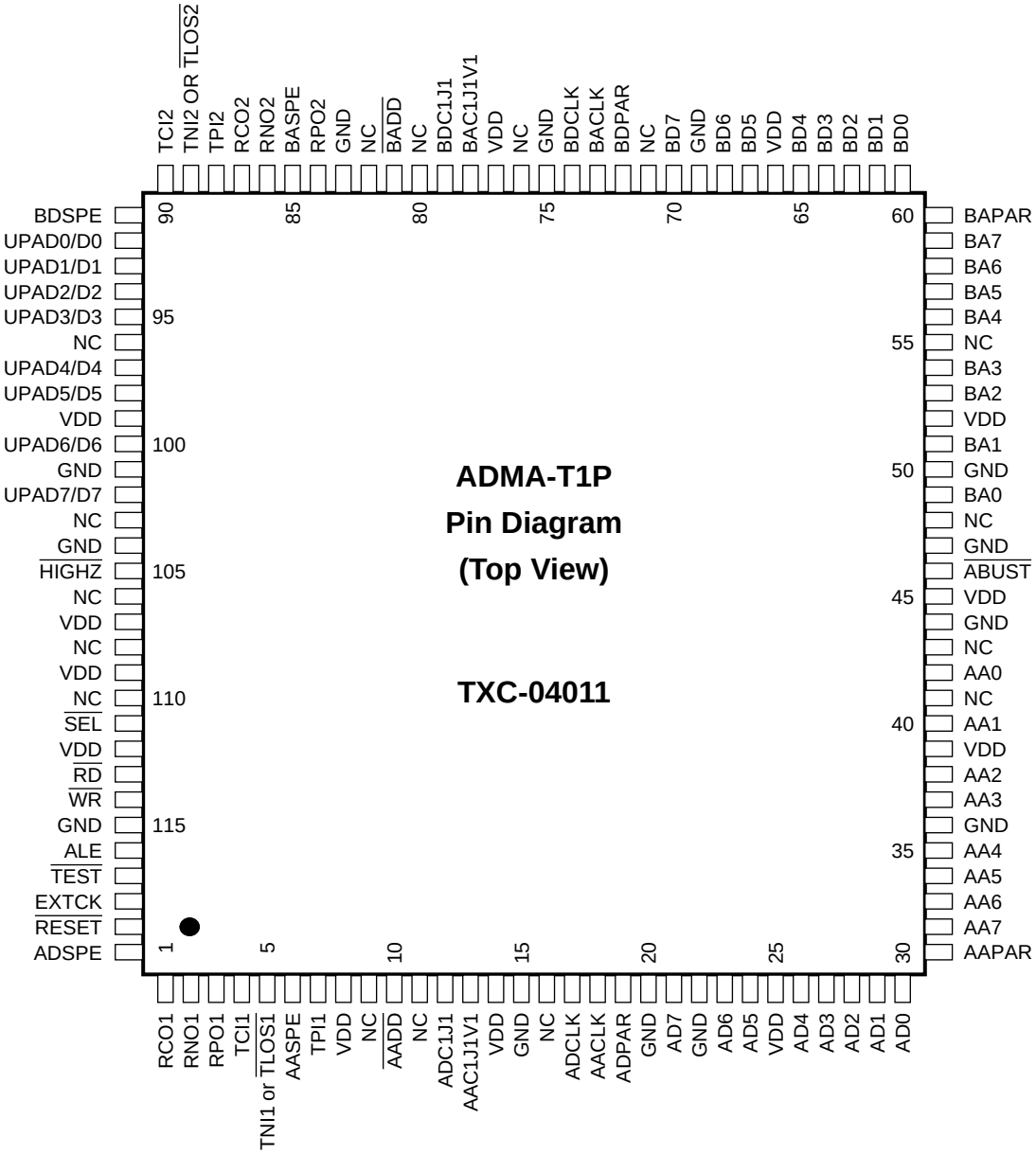


Figure 3. ADMA-T1P TXC-04011 Pin Diagram

PIN DESCRIPTIONS

POWER SUPPLY AND GROUND

Symbol	Pin No.	I/O/P *	Type	Name/Function
VDD	8, 14, 25, 39, 45, 52, 66, 77, 99, 107, 109, 112	P	I	**VDD:** +5-volt supply voltage, ±5%.
GND	15, 20, 22, 36, 44, 47, 50, 69, 75, 83, 101, 104, 115	P	I	**Ground:** 0 volts reference

Note: I = Input; O = Output; P = Power

Symbol	Pin No.	I/O/P	Type	Name/Function
NC	9, 11, 16, 41, 43, 48, 55, 71, 76, 80, 82, 96, 103, 106, 108, 110	--	--	**No Connect**: NC pins are not to be connected, not even to another NC pin, but must be left floating. Connection of NC pins may impair performance or cause damage to the device.

A DROP AND A ADD BUS I/O

Symbol	Pin No.	I/O/P	Type *	Name/Function
ADCLK	17	I	TTL	**A Drop Bus Clock:** This clock operates at 19.44 MHz for STS-3/STM-1 operation, and at 6.48 MHz for STS-1 operation. A Drop bus byte-wide data (AD7-AD0), the parity bit (ADPAR), SPE indication (ADSPE), and the C1J1 byte indicator (ADC1J1) inputs are detected on falling edges of this clock. In the drop timing mode (lead $\overline{\text{ABUST}}$ is high) this clock is also used for timing and deriving the like-named add bus byte-wide data (AA7-AA0), add indicator ($\overline{\text{AADD}}$), and parity bit (AAPAR). These signals are clocked out on rising edges of this clock during the time slots that correspond to the selected VT/TU.
ADPAR	19	I	TTL	**A Drop Bus Parity Bit:** Odd parity bit input signal representing the parity calculation for each data byte (AD7-AD0), SPE indication (ADSPE), and the C1J1 byte indicator (ADC1J1) from the drop bus. Control register bits are provided which allow choice of even parity instead, and/or restrict the parity bit detection to the data byte only.
AD(7-0)	21, 23, 24, 26, 27, 28, 29, 30	I	TTL	**A Drop Bus Data Byte:** Byte-wide data corresponding to the STS-1/STS-3/STM-1 signal from the bus. The first bit received (dropped) from the bus corresponds to bit 7 (pin 21).
ADSPE	120	I	TTL	**A Drop Bus SPE Indicator:** A signal that is active high during each byte of the STS-1/STS-3/STM-1 payload.
ADC1J1	12	I	TTL	**A Drop Bus C1/J1 Indications:** An active high timing signal that carries STS-1/STS-3/STM-1 frame and SPE information. The C1 pulse identifies the location of the first C1 byte in the STS-3/STM-1 signal and the C1 byte in the STS-1 signal. A J1 pulse, one clock cycle wide, identifies the location of the J1 byte in the STM-1 VC-4 signal. Three J1 pulses are provided to identify the J1 byte locations in the STM-1 AU-3s or STS-3/STS-1 SPEs. One J1 pulse is provided to identify the location of the J1 pulse for STS-1 SPE bus operation. If one or more V1 pulses are present in the signal, they are ignored.

*See Input, Output and I/O Parameters section below for Type definitions.

Symbol	Pin No.	I/O/P	Type	Name/Function
AACLK	18	I	TTL	**A Add Bus Clock:** When the $\overline{\text{ABUST}}$ lead is low, this clock must be provided for add bus timing. This clock operates at 19.44 MHz for STS-3/STM-1 operation, and at 6.48 MHz for STS-1 operation. The add bus SPE indication and the C1J1 indicators are input into the ADMA-T1P on falling edges of this clock. The add bus byte-wide data, add indicator, and parity bits are clocked out on rising edges of the clock during the time slots that correspond to the selected VT (TU). When $\overline{\text{ABUST}}$ is high, this input is disabled.
AAPAR	31	O (tristate)	CMOS 4mA	**A Add Bus Parity Bit:** An odd parity output signal calculated over the byte-wide add data. This 3-state lead is only active when there are data being added to the add bus. A control bit is provided that allows even parity to be calculated.
AA(7-0)	32, 33, 34, 35, 37, 38, 40, 42	O (tristate)	CMOS 4mA	**A Add Bus Data Byte:** 3-state byte-wide data that corresponds to the selected VT (TU). The first bit transmitted (added) to the bus corresponds to bit 7 on pin 32.
AASPE	6	I	TTL	**A Add Bus SPE Indicator:** When the $\overline{\text{ABUST}}$ lead is low, this signal must be provided for add bus timing. This signal is active high during each byte of the STS-1/STS-3/STM-1 payload.
AAC1J1V1	13	I	TTL	**A Add Bus C1J1V1 Indication:** When the $\overline{\text{ABUST}}$ lead is low, this signal must be provided for add bus timing. This signal carries STS-1/STS-3/STM-1 frame and SPE information. The C1 pulse identifies the first C1 byte time in the STS-3/STM-1 signal and the C1 byte time in the STS-1 signal. A J1 pulse, one clock cycle wide, identifies the location of the J1 byte in the STM-1 VC-4 signal. Three J1 pulses are provided to identify the locations of the STM-1 AU-3s or STS-3 SPEs. One J1 pulse is provided to identify the location of the J1 pulse for STS-1 SPE bus operation. The V1 pulses are used as multiframe indications.
$\overline{\text{AADD}}$	10	O	CMOS 4mA	**A Add Bus Add Data Present Indicator:** This normally active low signal is present when output data to the A Add bus are valid. It identifies the location of the VT (TU) time slots being selected. A control bit is provided that allows this bit to be active high instead of active low.

B DROP AND B ADD BUS I/O

Symbol	Pin No.	I/O/P	Type	Name/Function
BDCLK	74	I	TTL	**B Drop Bus Clock:** This clock operates at 19.44 MHz for STS-3/STM-1 operation, and at 6.48 MHz for STS-1 operation. B Drop bus byte-wide data (BD7-BD0), the parity bit (BDPAR), SPE indication (BDSPE), and the C1J1 byte indicator (BDC1J1) inputs are detected on falling edges of this clock. In the drop timing mode (lead $\overline{\text{ABUST}}$ is high) this clock is also used for timing and deriving the like-named add bus byte-wide data (BA7-BA0), add indicator ($\overline{\text{BADD}}$), and parity bit (BAPAR). These signals are clocked out on rising edges of this clock during the time slots that correspond to the selected VT/TU.
BDPAR	72	I	TTL	**B Drop Bus Parity Bit:** Odd parity bit input signal representing the parity calculation for each data byte (BD7-BD0), SPE indication (BDSPE), and the C1J1 byte indicator (BDC1J1) from the drop bus. Control register bits are provided which allow choice of even parity instead, and/or restrict the parity bit detection to the data byte only.
BD(7-0)	70, 68, 67, 65, 64, 63, 62, 61	I	TTL	**B Drop Bus Data Byte:** Byte-wide data corresponding to the STS-1/STS-3/STM-1 signal from the bus. The first bit received (dropped) from the bus corresponds to bit 7 (pin 70).
BDSPE	91	I	TTL	**B Drop Bus SPE Indicator:** A signal that is active high during each byte of the STS-1/STS-3/STM-1 payload.
BDC1J1	79	I	TTL	**B Drop Bus C1/J1 Byte Indicators:** An active high timing signal that carries STS-1/STS-3/STM-1 frame and SPE information. The C1 pulse identifies the location of the first C1 byte in the STS-3/STM-1 signal and the C1 byte in the STS-1 signal. A J1 pulse, one clock cycle wide, identifies the location of the J1 byte in the STM-1 VC-4 signal. Three J1 pulses are provided to identify the J1 byte locations in the STM-1 AU-3s or STS-3/STS-1 SPEs. One J1 pulse is provided to identify the location of the J1 pulse for STS-1 SPE bus operation. If one or more V1 pulses are present in this signal, they are ignored.
BACLK	73	I	TTL	**B Add Bus Clock:** When the $\overline{\text{ABUST}}$ lead is low, this clock must be provided for add bus timing. This clock operates at 19.44 MHz for STS-3/STM-1 operation, and at 6.48 MHz for STS-1 operation. The add bus SPE indication and the C1J1 indicators are input into the ADMA-T1P on falling edges of this clock. The add bus byte-wide data, add indicator, and parity bits are clocked out on rising edges of the clock during the time slots that correspond to the selected VT (TU). When $\overline{\text{ABUST}}$ is high, this input is disabled.

Symbol	Pin No.	I/O/P	Type	Name/Function
BAPAR	60	O (tristate)	CMOS 4mA	**B Add Bus Parity Bit:** An odd parity output signal calculated over the byte-wide add data. This 3-state lead is only active when there are data being added to the add bus. A control bit is provided that allows even parity to be calculated.
BA(7-0)	59, 58, 57, 56, 54, 53, 51, 49	O (tristate)	CMOS 4mA	**B Add Bus Data Byte:** 3-state byte-wide data that corresponds to the selected VT (TU). The first bit transmitted (added) to the bus corresponds to bit 7 on pin 59.
BASPE	85	I	TTL	**B Add Bus SPE Indicator:** When the $\overline{\text{ABUST}}$ lead is low, this signal must be provided for add bus timing. This signal is active high during each byte of the STS-1/STS-3/STM-1 payload.
BAC1J1V1	78	I	TTL	**B Add Bus C1J1 Indications:** When the $\overline{\text{ABUST}}$ lead is low, this signal must be provided for add bus timing. This signal carries STS-1/STS-3/STM-1 frame and SPE information. The C1 pulse identifies the first C1 byte time in the STS-3/STM-1 signal and the C1 byte time in the STS-1 signal. A J1 pulse, one clock cycle wide, identifies the location of the J1 byte in the STM-1 VC-4 signal. Three J1 pulses are provided to identify the locations of the STM-1 AU-3s or STS-3 SPEs. One J1 pulse is provided to identify the location of the J1 pulse for STS-1 SPE bus operation. The V1 pulses are used as multiframe indications.
$\overline{\text{BADD}}$	81	O	CMOS 4mA	**B Add Bus Add Data Present Indicator:** This normally active low signal is present when output data to the B Add bus are valid. It identifies the location of the VT (TU) time slots being selected. A control bit is provided that allows this bit to be active high instead of active low.

DS1 PORT 1 INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
RCO1	1	O (tristate)	CMOS 4mA	**Receive DS1 Output Clock, Port 1:** A 1.544 MHz clock output. Data are clocked out of the ADMA-T1P on rising edges of this clock. Control bits are provided for inverting this clock and for forcing this lead to 3-state.
RPO1	3	O (tristate)	CMOS 4mA	**Receive DS1 Data Positive Rail or NRZ, Port 1:** When the ADMA-T1P is operating with a rail interface, positive rail data are provided on this lead. When operating in the bypass mode, an NRZ signal is provided on this lead. A control bit is provided for forcing this lead to 3-state.
RNO1	2	O (tristate)	CMOS 4mA	**Receive DS1 Data Negative Rail, Port 1:** When the ADMA-T1P is operating with a rail interface, negative rail data are provided on this lead. A control bit is provided for forcing this lead to 3-state. In the NRZ mode, this lead is forced to a high impedance state.

Symbol	Pin No.	I/O/P	Type	Name/Function
TCI1	4	I	TTLs	**Transmit DS1 Input Clock, Port 1:** A 1.544 MHz clock input. Data are clocked into the ADMA-T1P on falling edges of this clock. A control bit is provided for inverting this clock.
TPI1	7	I	TTL	**Transmit DS1 Data Positive Rail or NRZ, Port 1:** When the ADMA-T1P is operating with a rail interface, positive rail input data are provided on this lead. When operating in the bypass mode, an NRZ signal is provided on this lead.
TNI1/ $\overline{\text{TLOS1}}$	5	I	TTL	**Transmit DS1 Data Negative Rail, Port 1/External Transmit Loss of Signal, Port 1:** When the ADMA-T1P is operating with a rail interface, negative rail input data are provided on this lead. When the NRZ interface is selected, this lead can be used to provide an input for an active low external transmit loss of signal indication. If this pin is not used for indicating a loss of signal then it must be held high.

DS1 PORT 2 INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
RCO2	87	O (tristate)	CMOS 4mA	**Receive DS1 Output Clock, Port 2:** A 1.544 MHz clock output. Data are clocked out of the ADMA-T1P on rising edges of this clock. Control bits are provided for inverting this clock and for forcing this lead to 3-state.
RPO2	84	O (tristate)	CMOS 4mA	**Receive DS1 Data Positive Rail or NRZ, Port 2:** When the ADMA-T1P is operating with a rail interface, positive rail data are provided on this lead. When operating in the bypass mode, an NRZ signal is provided on this lead. A control bit is provided for forcing this lead to 3-state.
RNO2	86	O (tristate)	CMOS 4mA	**Receive DS1 Data Negative Rail, Port 2:** When the ADMA-T1P is operating with a rail interface, negative rail data are provided on this lead. A control bit is provided for forcing this lead to 3-state. In the NRZ mode, this lead is forced to a high impedance state.
TCI2	90	I	TTLs	**Transmit DS1 Input Clock, Port 2:** A 1.544 MHz clock input. Data are clocked into the ADMA-T1P on falling edges of this clock. A control bit is provided for inverting this clock.
TPI2	88	I	TTL	**Transmit DS1 Data Positive Rail or NRZ, Port 2:** When the ADMA-T1P is operating with a rail interface, positive rail input data are provided on this lead. When operating in the bypass mode, an NRZ signal is provided on this lead.

Symbol	Pin No.	I/O/P	Type	Name/Function
TNI2/ $\overline{\text{TLOS2}}$	89	I	TTL	**Transmit DS1 Data Negative Rail, Port 2/External Transmit Loss or Signal, Port 2:** When the ADMA-T1P is operating with a rail interface, negative rail input data are provided on this lead. When the NRZ interface is selected, this lead can be used to provide an input for an active low external transmit loss of signal indication. If this pin is not used for indicating a loss of signal then it must be held high.

MICROPROCESSOR BUS INTERFACE

Symbol	Pin No.	I/O/P	Type	Name/Function
UPAD(7-0) or D(7-0)	102, 100, 98, 97, 95, 94, 93, 92	I/O	TTL 8mA	**Address/Data Bus:** These leads constitute the time multiplexed address and data bus for accessing the registers which reside in the ADMA-T1P. UPAD7/D7 is the most significant bit. High is logic 1.
$\overline{\text{SEL}}$	111	I	TTLs	**Select:** A low enables the microprocessor to access the memory map registers for control, status, and alarm information.
$\overline{\text{RD}}$	113	I	TTLs	**Read:** An active low signal generated by the microprocessor for reading the registers which reside in the memory map.
$\overline{\text{WR}}$	114	I	TTLs	**Write:** An active low signal generated by the microprocessor for writing to the registers which reside in the memory map.
ALE	116	I	TTLs	**Address Latch Enable:** An active high signal generated by the microprocessor. Used by the processor for holding an address stable during a read/write cycle.

CONTROLS

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{TEST}}$	117	I	TTLs	**TranSwitch Test Bit:** Must be held high.
EXTCK	118	I	CMOS	**External Reference Clock**: A 48.6360 MHz (+/- 32 ppm over life) clock that has a duty cycle of 50 +/- 10% must be applied to this pin for operating the desynchronizer, generating line AIS, and driving other internal circuitry.
$\overline{\text{RESET}}$	119	I	TTLs	**Hardware Reset**: An active low pulse that must be applied to this pin for a minimum of 150 nanoseconds after power is first applied. The reset clears all performance counters and alarms, resets the control bits, and initializes the internal FIFO. The microprocessor must initialize the control bits for normal operation.
$\overline{\text{HIGHZ}}$	105	I	TTLs	**High Impedance Select:** A 0 sets all output pins to the high impedance state for testing purposes. Otherwise, this pin must be held high.
$\overline{\text{ABUST}}$	46	I	TTL	**Add Bus Timing Select:** A low selects the add bus timing mode. The add bus clock (AACLK, BACLK), SPE (AASPE, BASPE) and C1J1V1 (AAC1J1V1, BAC1J1V1) input signals are used for deriving data, parity and add indicator signals for the A and B buses. A high selects the drop bus timing mode. The add bus data, parity and add indicator signals are derived from the drop bus timing signals.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min *	Max *	Unit
Supply voltage	V_{DD}	-0.5	+6.0	V
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
Ambient operating temperature	T_A	-40	85	^oC
Operating junction temperature	T_J		150	^oC
Storage temperature range	T_S	-55	150	^oC

*Note: Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance: junction to ambient	--	61	--	$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
I_{DD}			133	mA	STS-1
P_{DD}			700	mW	STS-1
I_{DD}			175	mA	STS-3 or STM-1
P_{DD}			920	mW	STS-3 or STM-1

INPUT, OUTPUT AND I/O PARAMETERS

INPUT PARAMETERS FOR CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	3.15			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			1.65	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	

INPUT PARAMETERS FOR TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			$\pm$1.0	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	

INPUT PARAMETERS FOR TTLs

Parameter	Min	Typ	Max	Unit	Test Conditions
VT- Negative going, threshold voltage			0.8	V	
VT+ Positive going, threshold voltage	2.0			V	
Input leakage current			1.0	µA	$V_{DD} = 5.25$
Input capacitance		3.5		pF	
Vhys Hysteresis (VT+ - VT-)	0.3		0.7	V	

OUTPUT PARAMETERS FOR CMOS 4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.8			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.5	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
I_{OZ} (HIGHZ output current)			±10.0	µA	

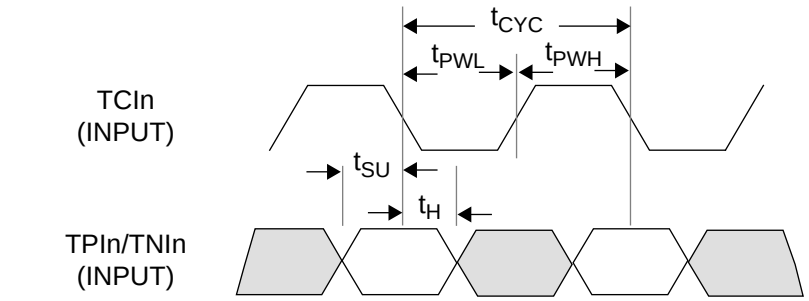
INPUT/OUTPUT PARAMETERS FOR TTL 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			±1.0	µA	V_{DD} = 5.25
Input capacitance		5.5		pF	
V_{OH}	V_{DD} - 0.8			V	V_{DD} = 4.75; I_{OH} = -8.0
V_{OL}			0.5	V	V_{DD} = 4.75; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	

TIMING CHARACTERISTICS

Detailed timing diagrams for the ADMA-T1P device are illustrated in Figures 4 through 11, with values of the timing intervals tabulated below each timing diagram. All output times are measured with a maximum 45 pF load capacitance. Timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ for input signals or $(V_{OH} + V_{OL})/2$ for output signals.

Figure 4. Ports 1 and 2 DS1 Transmit Timing

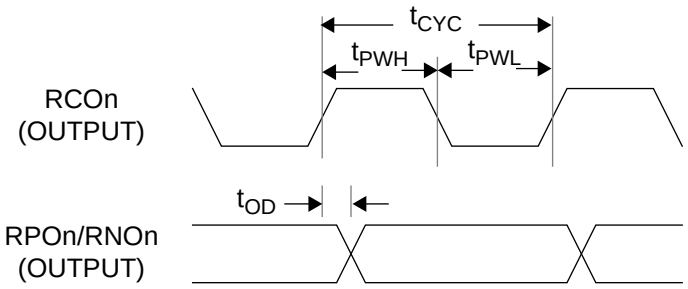


Note: n = 1 - 2

Note: TCIn is shown for TCLKI = 0, where data are clocked in on falling edges. Data are clocked in on rising edges when TCLKI =1. For NRZ operation, TNIn may be used to input an external loss of signal indication. Otherwise, this pin must be held high.

Parameter	Symbol	Min	Typ	Max	Unit
TCIn clock period	t_{CYC}	560.0	647.7		ns
TCIn clock low time	t_{PWL}	280.0			ns
TCIn clock high time	t_{PWH}	280.0			ns
TPIn/TNIn data set-up time before TCIn↓	t_{SU}	10.0			ns
TPIn/TNIn data hold time after TCIn↓	t_H	2.0			ns

Figure 5. Ports 1 and 2 DS1 Receive Timing

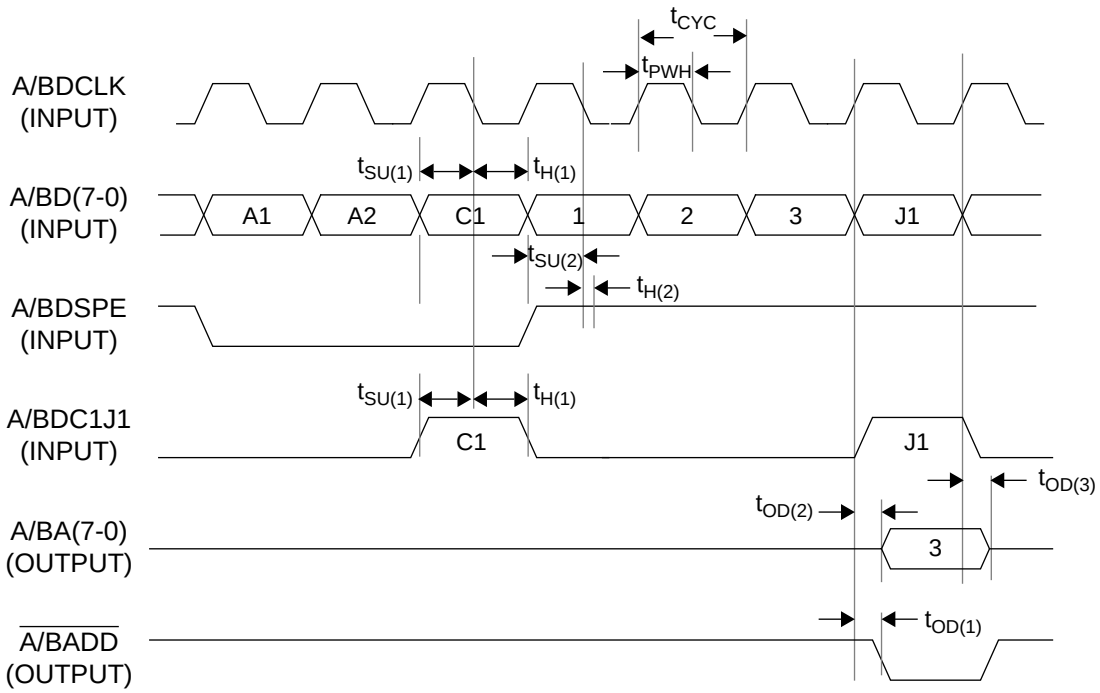


Note: n = 1 - 2

Note: RCOn is shown for RCLKI=0, where data are clocked out on rising edges. Data are clocked out on falling edges when RCLKI=1.

Parameter	Symbol	Min	Typ	Max	Unit
RCOn clock period	t_{CYC}	637		658	ns
RCOn clock low time	t_{PWL}	318		329	ns
RCOn clock high time	t_{PWH}	318		329	ns
RPOn/RNOn data delay from RCOn↑	t_{OD}	0.0		5.0	ns

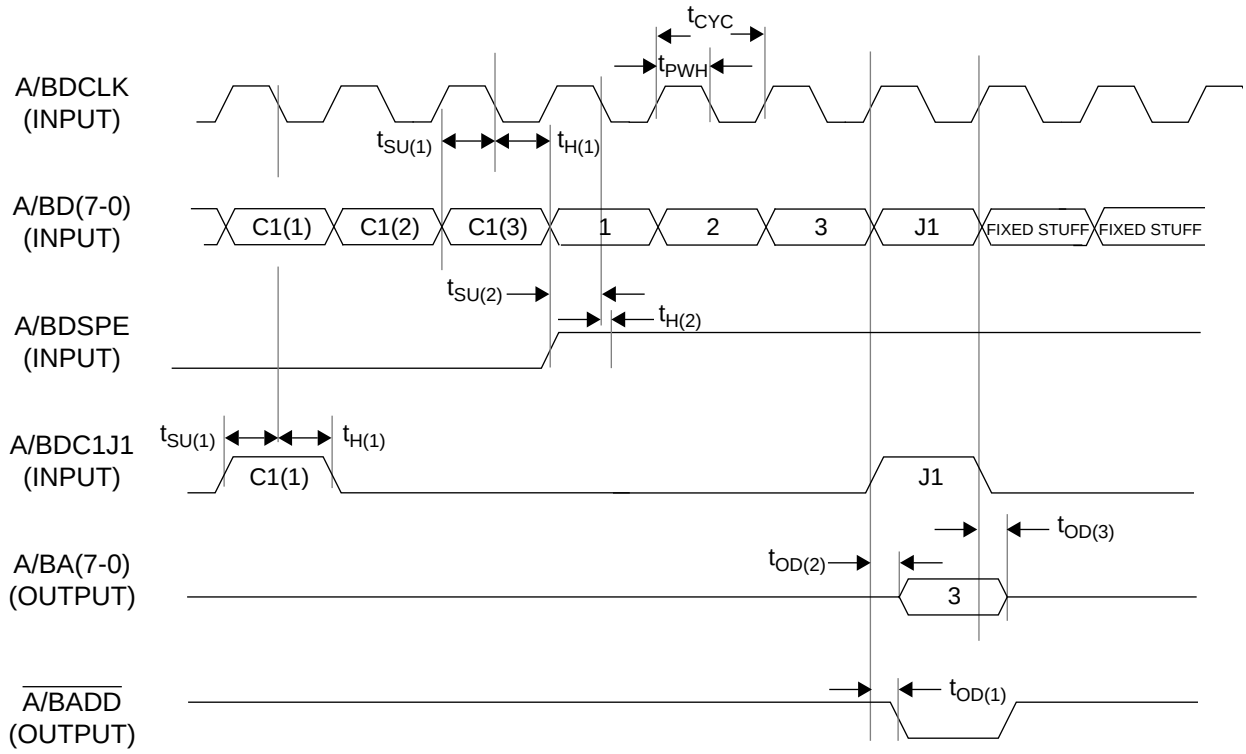
Figure 6. STS-1 A/B Drop and Add Bus Signals, Timing Derived from Drop Bus



Note: The add bus output A/BA(7-0) shown above corresponds to the 0 state of control bit ABD, when there is one data byte (or one clock cycle) of delay between the drop and add buses. This delay is increased to two data bytes when control bit ABD is set to 1.

Parameter	Symbol	Min	Typ	Max	Unit
A/BDCLK drop clock period	t_{CYC}		154.32		ns
A/BDCLK drop clock duty cycle, t_{PWH}/t_{CYC}		40	50	60	%
A/BD(7-0) drop data and A/BDC1J1 set-up time before A/BDCLK↓	$t_{SU(1)}$	4.0			ns
A/BD(7-0) drop data and A/BDC1J1 hold time after A/BDCLK↓	$t_{H(1)}$	5.0			ns
A/BDSPE set-up time before A/BDCLK↓	$t_{SU(2)}$	4.0			ns
A/BDSPE hold time after A/BDCLK↓	$t_{H(2)}$	5.0			ns
A/BA(7-0) add data out (from tri-state) delay from A/BDCLK↑	$t_{OD(2)}$	6.0		18.5	ns
A/BA(7-0) add data out (to tri-state) delay from A/BDCLK ↑	$t_{OD(3)}$	6.0		20.0	ns
$\overline{\text{A/BADD}}$ add indicator delay from A/BDCLK↑	$t_{OD(1)}$	6.0		19.0	ns

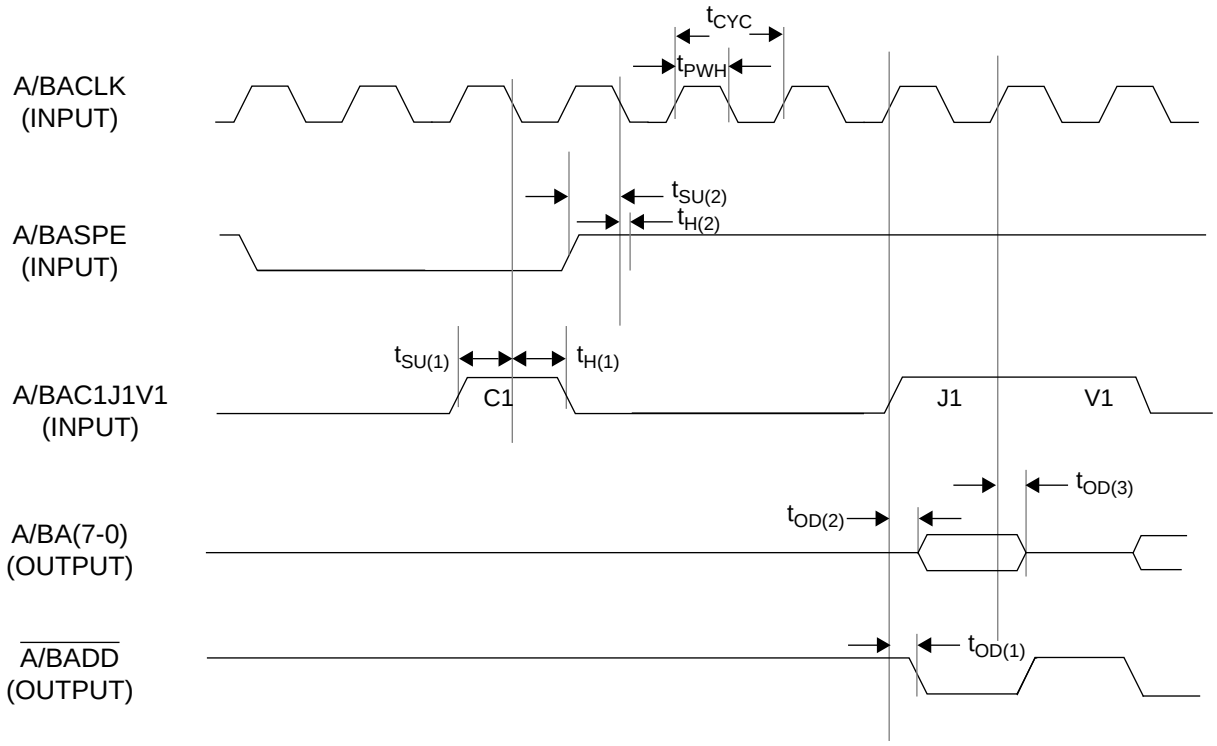
Figure 7. STS-3/STM-1 A/B Drop and Add Bus Signals, Timing Derived from Drop Bus



Note: The add bus output A/BA(7-0) shown above corresponds to the 0 state of control bit ABD, when there is one data byte (or one clock cycle) of delay between the drop and add buses. This delay is increased to two data bytes when control bit ABD is set to 1.

Parameter	Symbol	Min	Typ	Max	Unit
A/BDCLK drop clock period	t_{CYC}		51.44		ns
A/BDCLK drop clock duty cycle, t_{PWH}/t_{CYC}	-	45	50	55	%
A/BD(7-0) drop data and A/BDC1J1 set-up time before A/BDCLK↓	$t_{SU(1)}$	4.0			ns
A/BD(7-0) drop data and A/BDC1J1 hold time after A/BDCLK↓	$t_{H(1)}$	5.0			ns
A/BDSPE set-up time before A/BDCLK↓	$t_{SU(2)}$	4.0			ns
A/BDSPE hold time after A/BDCLK↓	$t_{H(2)}$	5.0			ns
A/BA(7-0) add data out (from tri-state) delay from A/BDCLK↑	$t_{OD(2)}$	6.0		18.3	ns
A/BA(7-0) add data out (to tri-state) delay from A/BDCLK↑	$t_{OD(3)}$	6.0		19.8	ns
$\overline{\text{A/BADD}}$ add indicator delay from A/BDCLK↑	$t_{OD(1)}$	6.0		18.8	ns

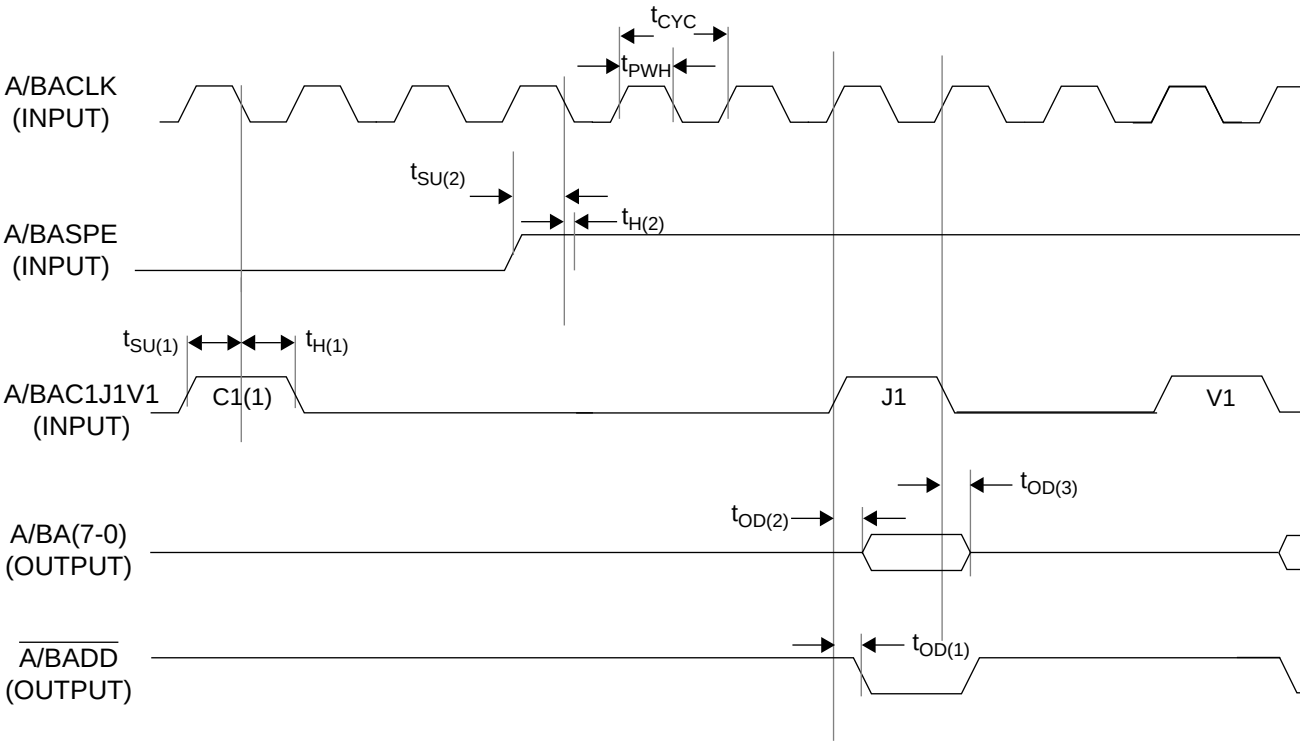
Figure 8. STS-1 A/B Add Bus Signals, Timing Derived from Add Bus



Note: The add bus output A/BA(7-0) shown above corresponds to the 0 state of control bit ABD, when there is one data byte (or one clock cycle) of delay between the drop and add buses. This delay is increased to two data bytes when control bit ABD is set to 1.

Parameter	Symbol	Min	Typ	Max	Unit
A/BACLK drop clock period	t_{CYC}		154.32		ns
A/BACLK duty cycle, t_{PWH}/t_{CYC}		40	50	60	%
A/BAC1J1V1 set-up time to A/BACLK↓	$t_{SU(1)}$	4.0			ns
A/BAC1J1V1 hold time after A/BACLK↓	$t_{H(1)}$	5.0			ns
A/BASPE set-up time to A/BACLK↓	$t_{SU(2)}$	4.0			ns
A/BASPE hold time after A/BACLK↓	$t_{H(2)}$	5.0			ns
A/BA(7-0) data out (from tristate) delay from A/BACLK↑	$t_{OD(2)}$	6.0		18.5	ns
A/BA(7-0) data to tristate delay from A/BACLK↑	$t_{OD(3)}$	6.0		20.0	ns
$\overline{\text{A/BADD}}$ add indicator delay from A/BACLK↑	$t_{OD(1)}$	6.0		19.0	ns

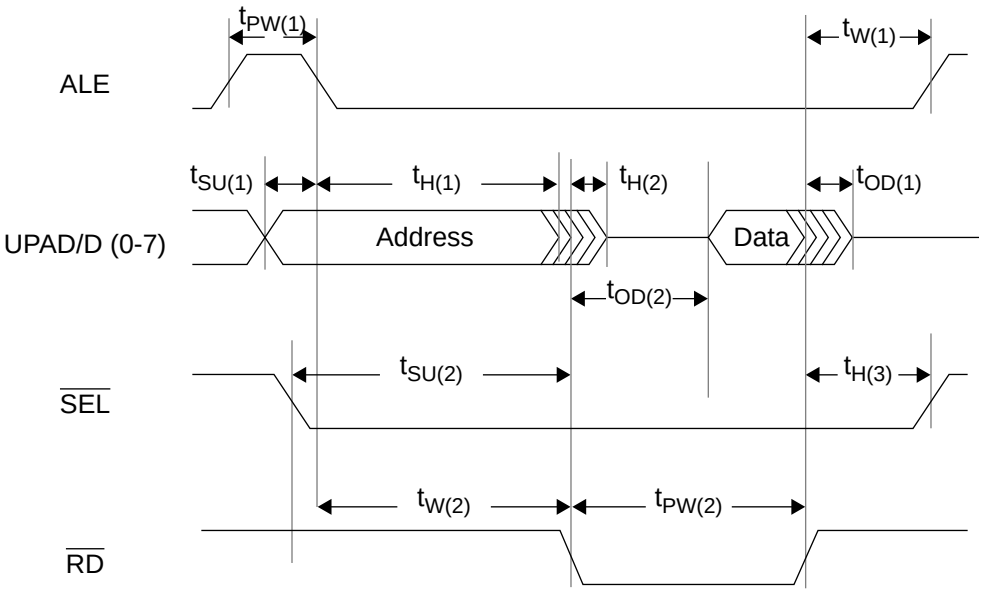
Figure 9. STS-3/STM-1 A/B Add Bus Signals, Timing Derived from Add Bus



Note: The add bus output A/BA(7-0) shown above corresponds to the 0 state of control bit ABD, when there is one data byte (or one clock cycle) of delay between the drop and add buses. This delay is increased to two data bytes when control bit ABD is set to 1.

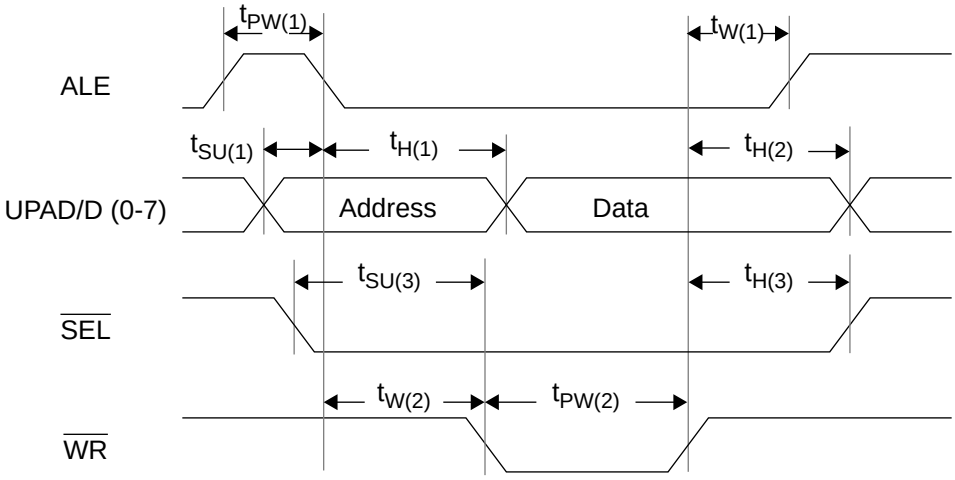
Parameter	Symbol	Min	Typ	Max	Unit
A/BACLK drop clock period	t_{CYC}		51.44		ns
A/BACLK duty cycle, t_{PWH}/t_{CYC}		40	50	60	%
A/BAC1J1V1 set-up time to A/BACLK ↓	$t_{SU(1)}$	4.0			ns
A/BAC1J1V1 hold time after A/BACLK ↓	$t_{H(1)}$	5.0			ns
A/BASPE set-up time to A/BACLK ↓	$t_{SU(2)}$	4.0			ns
A/BASPE hold time after A/BACLK ↓	$t_{H(2)}$	5.0			ns
A/BA(7-0) data out (from tristate) delay from A/BACLK ↑	$t_{OD(2)}$	6.0		18.5	ns
A/BA(7-0) data to tristate delay from A/BACLK ↑	$t_{OD(3)}$	6.0		20.0	ns
$\overline{\text{A/BADD}}$ add indicator delay from A/BACLK ↑	$t_{OD(1)}$	6.0		19.0	ns

Figure 10. Microprocessor Read Cycle - Intel Timing



Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	20.0			ns
UPAD(0-7) address set-up time before ALE↓	$t_{SU(1)}$	5.0			ns
UPAD(0-7) address hold time after ALE↓	$t_{H(1)}$	3.0			ns
UPAD(0-7) address hold time after $\overline{RD}$↓	$t_{H(2)}$			0.0	ns
D(0-7) data available delay time after $\overline{RD}$↓	$t_{OD(2)}$	5.0		17.0	ns
D(0-7) data delay time to tri-state after $\overline{RD}$↑	$t_{OD(1)}$	2.0		8.0	ns
ALE wait after $\overline{RD}$↑	$t_{W(1)}$	0.0			ns
$\overline{SEL}$ set-up time before $\overline{RD}$↓	$t_{SU(2)}$	0.0			ns
$\overline{SEL}$ hold time after $\overline{RD}$↑	$t_{H(3)}$	0.0			ns
$\overline{RD}$ wait after ALE ↓	$t_{W(2)}$	20.0			ns
$\overline{RD}$ pulse width	$t_{PW(2)}$	45.0			ns

Figure 11. Microprocessor Write Cycle - Intel Timing



Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	20.0			ns
ALE wait after $\overline{WR}\uparrow$	$t_{W(1)}$	0.0			ns
UPAD(0-7) address set-up time before ALE$\downarrow$	$t_{SU(1)}$	5.0			ns
UPAD(0-7) address hold time after ALE$\downarrow$	$t_{H(1)}$	3.0			ns
D(0-7) data input hold time after $\overline{WR}\uparrow$	$t_{H(2)}$	16.0			ns
$\overline{SEL}$ set-up time before $\overline{WR}\downarrow$	$t_{SU(3)}$	0.0			ns
$\overline{SEL}$ hold time after $\overline{WR}\uparrow$	$t_{H(3)}$	0.0			ns
$\overline{WR}$ wait after ALE$\downarrow$	$t_{W(2)}$	20.0			ns
$\overline{WR}$ pulse width	$t_{PW(2)}$	45.0			ns

MEMORY MAP

The ADMA-T1P memory map consists of counters and register bit positions which may be accessed by the microprocessor. Addresses which are shown as TranSwitch test registers or as wholly 'Unused' bytes in the memory map must not be accessed by the microprocessor. No value is specified for the content to be read from an 'Unused' bit position when the address which contains it is selected for a read cycle, but the bit position should be written as 0 when the address is selected for a write cycle (if it is a R/W or W address).

COMMON CONTROL

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	W	RESET	RESETS	RESETC	Unused				
01	R/W	T1SEL1	T1SEL0	BYPAS1	BYPAS2	T1LOOP	T2LOOP	R1EN	R2EN
02	R/W	MOD1	MOD0	T1B8ZS	T2B8ZS	T1AIS	T2AIS	Unused	TCLKI
03	R/W	TAISE	UQAE	R1AIS	R2AIS	RDIEN	T2SEL1	T2SEL0	RCLKI
40	R/W	AAHZE	BAHZE	ADDI	ABD	APE	Unused		PTALTE
41	R/W		NPIA	NPIB	NPIC	E1AISD	DPE	PDDO	Unused
42		TranSwitch Test Register							
43		TranSwitch Test Register							
44		TranSwitch Test Register							

* R=Read Only; R(L)=Read Only (Latched); R/W=Read/Write; W=Write only.

A-SIDE DROP BUS STATUS REGISTERS

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04	R(L)	ADLOC	Unused	AALOC	Unused		A2DH4E	A1DH4E	ADPAR
05	R	Unused							
06	R	Unused							
07	R	Unused							

PORT 1 STATUS/TRANSMIT REGISTERS

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08	R/W	Port 1 Pointer Leak Rate							
09	R	Port 1 B8ZS/AMI Coding Errors (low order byte)							
0A	R(L)	Unused					R1FFE	T1LOCS	T1AIS
0B	R	Port 1 B8ZS/AMI Coding Errors (high order byte)							
0C	R	Unused							
0D	R/W	T1VTAIS	T1FB2	T1FFB	T1RDI	T1RFI	A1 TX Label		
0E	R/W	Port 1 TX O-Bits							
0F	R/W	R1SEL	VTN1 (VT#)						

PORT 1 A-SIDE DROP BUS RECEIVE REGISTERS

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10	R	A1BIP2 Error Count							
11	R	A1FEBE Count							
12	R(L)	A1UNEQ	A1SLER	Unused		A1NDF	Unused		TA1FE
13	R(L)	A1AIS	A1LOP	A1SIZE	A1RDI	A1RFI	A1 RX Label		
14	R	A1PJ Counter				A1NJ Counter			
15	R	A1 RX O-Bits							
16	R/W	Unused					A1UPSL		
17		TranSwitch Test Register							

PORT 1 B-SIDE DROP BUS RECEIVE REGISTERS

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
18	R	B1BIP2 Error Count							
19	R	B1FEBE Count							
1A	R(L)	B1UNEQ	B1SLER	Unused		B1NDF	Unused		TB1FE
1B	R(L)	B1AIS	B1LOP	B1SIZE	B1RDI	B1RFI	B1 RX Label		
1C	R	B1PJ Counter				B1NJ Counter			
1D	R	B1 RX O-Bits							
1E	R/W	Unused					B1UPSL		
1F		TranSwitch Test Register							

B-SIDE DROP BUS STATUS REGISTERS

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
24	R(L)	BDLOC	Unused	BALOC	Unused		B2DH4E	B1DH4E	BDPAR
25		Unused							
26		Unused							
27		Unused							

PORT 2 STATUS/TRANSMIT REGISTERS

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
28	R/W	Port 2 Pointer Leak Rate							
29	R	Port 2 B8ZS/AMI Coding Errors (low order byte)							
2A	R(L)	Unused					R2FFE	T2LOCS	T2AIS
2B	R	Port 2 B8ZS/AMI Coding Errors (high order byte)							
2C		Unused							
2D	R/W	T2VTAIS	T2FB2	T2FFB	T2RDI	T2RFI	A2 TX Label		
2E	R/W	Port 2 TX O-Bits							
2F	R/W	R2SEL	VTN2 (VT#)						

PORT 2 A-SIDE DROP BUS RECEIVE REGISTERS

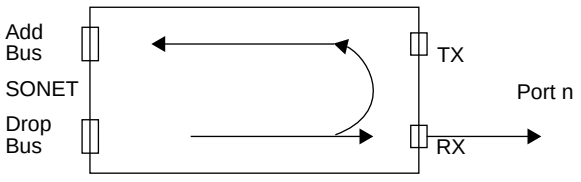
Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
30	R	A2BIP2 Error Count							
31	R	A2FEBE Count							
32	R(L)	A2UNEQ	A2SLER	Unused		A2NDF	Unused		TA2FE
33	R(L)	A2AIS	A2LOP	A2SIZE	A2RDI	A2RFI	A2 RX Label		
34	R	A2PJ Counter				A2NJ Counter			
35	R	A2 RX O-Bits							
36	R/W	Unused					A2UPSL		
37	R	TranSwitch Test Register							

PORT 2 B-SIDE DROP BUS RECEIVE REGISTERS

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
38	R	B2BIP2 Error Count							
39	R	B2FEBE Count							
3A	R(L)	B2UNEQ	B2SLER	Unused		B2NDF	Unused		TB2FE
3B	R(L)	B2AIS	B2LOP	B2SIZE	B2RDI	B2RFI	B2 RX Label		
3C	R	B2PJ Counter				B2NJ Counter			
3D	R	B2 RX O-Bits							
3E	R/W	Unused					B2UPSL		
3F		TranSwitch Test Register							

MEMORY MAP DESCRIPTIONS

CONTROL REGISTERS

Address	Bit	Symbol	Description
00	7	RESET	**Reset ADMA-T1P:** A 1 configures the controls to their power-up states, resets all the performance counters to 0, and re-centers the internal FIFOs. Afterwards this bit is self-clearing and resets to a 0. Note: Upon power-up all control bits, except the BPASn, MODn, AAHZE, and BAHZE, are reset to 0 (where n represents port 1 or 2). Upon power-up, all alarms, except AnLOP and BnLOP, are reset to 0. The MODn control bits select the STS-3 format, while the BPASn, AAHZE, BAHZE, AnLOP, and BnLOP control bits are set to 1.
	6	RESETS	**Reset Selected Functions:** A 1 resets the performance counters and alarms to 0, and re-centers the internal FIFOs. The control register bits are not reset, and will maintain their existing states. Afterwards this bit is self-clearing and resets to a 0. See Note 1.
	5	RESETC	**Reset Counters:** A 1 causes all the performance counters to reset to 0. Afterwards this bit is self-clearing and resets to a 0. See Note 1.
01	7 6	T1SEL1 T1SEL0	**Port 1 Transmit A/B-side Add Bus Selection:** This bit works in conjunction with the R1SEL bit to provide the following modes of operation for port 1. Timing for the VT/TU to be added to the A (or B) Add bus is derived from either the A (or B) Drop bus. T1SEL1 T1SEL0 R1SEL Mode 0 0 0 A-side drop only 0 0 1 B-side drop only 0 1 0 A-side drop, A-side add 0 1 1 B-side drop, B-side add 1 0 0 A-side drop, B-side add 1 0 1 B-side drop, A-side add 1 1 0 A-side drop, A-side and B-side add 1 1 1 B-side drop, B-side and A-side add
	5	BYPAS1	**Bypass CODEC Port 1:** A 1 arranges the B8ZS/AMI CODEC for port 1 to be bypassed for NRZ operation. A 0 enables the CODEC for port 1.
	4	BYPAS2	**Bypass CODEC Port 2:** A 1 arranges the B8ZS/AMI CODEC for port 2 to be bypassed for NRZ operation. A 0 enables the CODEC for port 2.
	3	T1LOOP	**Port 1 T1 Loopback:** A 1 causes a T1 loopback for port 1. The receive output data and clock signals are looped back as the transmit input, and the receive data signals are provided as an output. The input signal from the line is disabled. 

Note 1: This bit position should be written to 1 after device initialization and after any mode changes (i.e., after changing any of the T1SEL1, T1SEL0, T2SEL1, T2SEL0, R1SEL, VTN1, R2SEL or VTN2 bits) in order to prevent a FIFO error from occurring.

Address	Bit	Symbol	Description
01 (cont.)	2	T2LOOP	**Port 2 T1 Loopback:** A 1 causes a T1 loopback for port 2. The receive output data and clock signals are looped back as the transmit input, and the receive data signals are provided as an output. The input signal from the line is disabled.
	1	R1EN	**Receive Port 1 Enable:** A 1 enables the receive data (NRZ or rail) output and clock output for port 1. A 0 forces the data and clock output leads to a high impedance state.
	0	R2EN	**Receive Port 2 Enable:** A 1 enables the receive data (NRZ or rail) output and clock output for port 2. A 0 forces the data and clock output leads to a high impedance state.
02	7 6	MOD1 MOD0	**SONET/SDH Bus Format Selection:** The SONET/SDH bus format selection is according to the table below: MOD1 MOD0 Bus Format Selected 0 0 STS-1 format 0 1 STS-3 format 1 0 STM-1 AU3 format 1 1 STM-1 TUG-3/VC-4 format
	5	T1B8ZS	**Port 1 B8ZS CODEC Enable:** A 1 selects the B8ZS CODEC function for port 1. A 0 selects the AMI CODEC function for port 1.
	4	T2B8ZS	**Port 2 B8ZS CODEC Enable:** A 1 selects the B8ZS CODEC function for port 2. A 0 selects the AMI CODEC function for port 2.
	3	T1AIS	**Port 1 Transmit AIS:** A 1 causes a T1 AIS (unframed all ones signal) to be generated in the transmit (add) direction for port 1.
	2	T2AIS	**Port 2 Transmit AIS:** A 1 causes a T1 AIS (unframed all ones signal) to be generated in the transmit (add) direction for port 2.
	0	TCLKI	**Port 1 and 2 Transmit Clock Inversion:** A 1 causes the T1 data for ports 1 and 2 to be clocked in on positive clock edges. A 0 causes data to be clocked in on negative clock edges.
03	7	TAISE	**Port 1 and 2 Transmit AIS Enable:** A 1 enables a T1 AIS to be sent when loss of signal or clock is detected in the port 1 or port 2 T1 interface signals. A T1 AIS is an unframed all ones data signal.
	6	UQAE	**Unequipped Alarm AIS Enable:** A 1 enables receive AIS and RDI to be sent when an unequipped status is detected in either the A-side or B-side drop data. An unequipped status is defined as 000 in the VT/TU signal label.

Address	Bit	Symbol	Description
03 (cont.)	5	R1AIS	**Generate Receive AIS for Port 1:** A 1 causes a T1 AIS to be generated for the receive data for port 1, independent of internal alarm detection. A T1 AIS is an unframed all ones data signal. The conditions for generating a T1 AIS for port 1 are: When control bit R1SEL is a 0 and any one or more of the following: - R1AIS=1. - Loss of Pointer (A1LOP). - VT/TU AIS (A1AIS). - A-side drop bus loss of clock (ADLOC). - A-side H4 Error (A1DH4E). - Unequipped signal label (A1UNEQ), and UQAE is a 1. - Mismatch signal label (A1SLER). - VT/TU selection out of range or equal to 0. When control bit R1SEL is a 1 and any one or more of the following: - R1AIS=1. - Loss of Pointer (B1LOP). - VT/TU AIS (B1AIS). - B-side drop bus loss of clock (BDLOC). - B-side H4 Error (B1DH4E). - Unequipped signal label (B1UNEQ), and UQAE is a 1. - Mismatch signal label (B1SLER). - VT/TU selection out of range or equal to 0. Microprocessor writes a 1 to R1AIS.
	4	R2AIS	**Generate Receive AIS for Port 2:** A 1 causes a T1 AIS to be generated for the receive data for port 2, independent of internal alarm detection. A T1 AIS is an unframed all ones data signal. The conditions for generating a T1 AIS for port 2 are: When control bit R2SEL is a 0 and any one or more of the following: - R2AIS=1. - Loss of Pointer (A2LOP). - VT/TU AIS (A2AIS). - A-side drop bus loss of clock (ADLOC). - A-side H4 Error (A2DH4E). - Unequipped signal label (A2UNEQ), and UQAE is a 1. - Mismatch signal label (A2SLER). - VT/TU selection out of range or equal to 0. When control bit R2SEL is a 1 and any one or more of the following: - R2AIS=1. - Loss of Pointer (B2LOP). - VT/TU AIS (B2AIS). - B-side drop bus loss of clock (BDLOC). - B-side H4 Error (B2DH4E). - Unequipped signal label (B2UNEQ), and UQAE is a 1. - Mismatch signal label (B2SLER). - VT/TU selection out of range or equal to 0. Microprocessor writes a 1 to R2AIS.

Address	Bit	Symbol	Description
03 (cont.)	3	RDIEN	**Transmit Receive Defect Indication Enable:** A 1 enables the ADMA-T1P to send RDI when a receive alarm occurs. A 0 disables the automatic insertion, and allows the microprocessor to control both states of the transmitted RDI status bit (Bit 8 in V5). For port 1 the alarms causing RDI are a function of the R1SEL, T1SEL1 and T1SEL0 control bits. For port 2 the alarms causing RDI are a function of the R2SEL, T2SEL1 and T2SEL0 control bits. The following is a summary of the various alarms and control bits that may cause an RDI. The n represents port 1 or 2. When RDIEN is a 1: - Loss Of Pointer (AnLOP, BnLOP). - VT/TU AIS (AnAIS, BnAIS). - A/B-side drop bus H4 Error (AnDH4E, BnDH4E). - Unequipped signal label (AnUNEQ, BnUNEQ), and UQAE is a 1. - Signal label mismatch (AnSLER, BnSLER). When RDIEN is a 0: - Microprocessor writes a 1 to TnRDI. Note. The microprocessor may send an RDI anytime by writing a 1 to TnRDI. However, to prevent contention between the internal alarms causing RDI and microprocessor controlling RDI, control bit RDIEN must be written with a 0.
	2 1	T2SEL1 T2SEL0	**Port 2 Transmit A/B-side Add Bus Selection:** This bit works in conjunction with the R2SEL bit to provide the following modes of operation for port 2. Timing for the VT/TU to be added to the A (or B) Add bus is derived from either the A (or B) Drop bus. T2SEL1 T2SEL0 R2SEL Mode 0 0 0 A-side drop only 0 0 1 B-side drop only 0 1 0 A-side drop, A-side add 0 1 1 B-side drop, B-side add 1 0 0 A-side drop, B-side add 1 0 1 B-side drop, A-side add 1 1 0 A-side drop, A-side and B-side add 1 1 1 B side drop, B-side and A-side add
	0	RCLKI	**Port 1 and 2 Receive Clock Inversion:** A 1 causes the receive clock to clock out data on the negative edge instead of on the positive edge for both ports.

Address	Bit	Symbol	Description
40	7	AAHZE	**A-side Add Bus High Impedance Enable:** A 1 forces the A-side add bus output signals to a high impedance state. A 0 allows normal operation.
	6	BAHZE	**B-side Add Bus High Impedance Enable:** A 1 forces the B-side add bus outputs signals to a high impedance state. A 0 allows normal operation.
	5	ADDI	**Add Indicator Inversion:** A 1 enables the A and B-side add indicator signals to be active high instead of active low. A 0 enables the A and B-side add indicator signals to be active low instead of active high.
	4	ABD	**Add Bus Delayed:** A 1 causes the add bus data to be delayed by two clock cycles with respect to the drop bus data. A 0 causes the add bus data to be delayed by one clock cycle with respect to the drop bus data.
	3	APE	**A/B-side Add Bus Even Parity Generated:** A 1 enables even parity to be generated, while 0 enables odd parity to be generated.
	0	PTALTE	**Pointer Tracking AIS to LOP Transition Enabled**: A 1 enables the AIS to LOP transition in the pointer tracking state machine, as required per ITU-T requirements. A 0 disables the transition as required per Bellcore standards.
41	6 5 4	NPIA NPIB NPIC	**Null Pointer Indicator Selection:** A 1 enables the null pointer indicator to be generated for one or more of the TUG-3s when the STM-1 TUG-3 format is selected. A null pointer indicator is defined as a 1001 in bits 1-4, bits 5 and 6 are unspecified and set to 0, five 1s in bits 7-11, followed by five zeros in bits 12-16 (two bytes). Those bytes which are designated as stuff are not generated, and the data bus is forced to a high impedance state during those time slots.
	3	E1AISD	**Receive E1 Byte AIS Disable:** A 1 disables the add/drop bus TOH E1 byte from generating a T1 AIS for ports 1 and 2 when the E1 byte is all ones.
	2	DPE	**A/B-side Drop Bus Even Parity Detected:** A 1 enables even parity to be detected in the A/B-side drop buses. A 0 enables odd parity to be detected.
	1	PDDO	**A/B-side Drop Bus Parity Detected on Data Only:** A 1 causes parity to be detected for the data byte only. A 0 causes parity to be detected for the data byte, C1J1 and the SPE signals.

A-SIDE DROP BUS STATUS REGISTERS

Address	Bit	Symbol	Description
04	7	ADLOC	**A-side Drop Bus Loss Of Clock:** A latched bit position that indicates a loss of clock in the A-side drop bus has been detected. A loss of clock alarm causes a receive AIS for the duration of the alarm, and sets the like-named add bus signals (data and PAR signal) to the high impedance state. The $\overline{\text{AADD}}$ indication signal becomes inactive for the duration of the alarm. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch. The loss of clock alarm occurs when the input drop clock (ADCLK) is stuck high or low for 10 or more clock cycles. Recovery occurs on the first drop clock transition.
	5	AALOC	**A Add Bus Loss Of Clock:** A latched bit position which indicates that the A Add bus has detected a loss of clock, when control lead $\overline{\text{ABUST}}$ is low. A loss of clock alarm causes the add data and parity bit to 3-state, and sets the add indicator off for the duration of the alarm. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch. The loss of clock alarm occurs when the input add clock (AACLK) is stuck high or low for 10 or more clock cycles. Recovery occurs on the first add clock transition.
	2	A2DH4E	**A-side Drop Bus Port 2 Loss of H4 Indication:** A latched bit position that indicates that the anticipated received H4 multiframe sequence of 00, 01, 10, 11 has not been received properly. The ADMA-T1P will continue to operate in a free running mode, but will lock to a new H4 sequence after two consecutive sequences have been received properly. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	1	A1DH4E	**A-side Drop Bus Port 1 Loss of H4 Indication:** A latched bit position which indicates that the anticipated received H4 multiframe sequence of 00, 01, 10, 11 has not been received properly. The ADMA-T1P will continue to operate in a free running mode, but will lock to a new H4 sequence after two consecutive sequences have been received properly. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	0	ADPAR	**A-side Drop Bus Parity Error Detected:** A latched bit position which indicates that an odd parity error has been detected in the A-side drop bus signals. Even parity detection is enabled by writing a 1 to the Drop Bus Parity Even (DPE) control bit. Other than an alarm indication, no other action is taken. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.

PORT 1 STATUS/TRANSMIT REGISTERS

Address	Bit	Symbol	Description
08	7-0	Port 1 Pointer Leak Rate Value	**Port 1 FIFO Leak Rate Register:** The count written into this location is used for the internal leak buffer, and represents the average leak rate. A count of one represents 8 frames, or 2 multiframes, in the rate of occurrence of pointer movements from the number of counts read from positive/negative stuff counters. A count of 0 is invalid, and no selection takes place.
09	7-0	Port 1 Coding Error Counter Low Order Byte	**Port 1 Transmit Coding Violation Counter:** Low order byte of a 16-bit saturating counter that counts the number of coding errors that have occurred in the AMI or B8ZS line codes. During a read cycle internal logic holds a count of 1 until the read cycle is complete, and then updates the counter. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle. This location must be read first before the high order byte.
0A	2	R1FFE	**Port 1 Receive FIFO Error:** A latched bit position which indicates that the receive FIFO for port 1 has overflowed or underflowed. The FIFO will reset automatically. Other than an alarm indication, no other action will be taken. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position re-latches.
	1	T1LOCS	**Port 1 Transmit Loss Of T1 Clock or Signal:** A latched bit position which indicates that the Port 1 T1 clock or data signal has failed. This bit position is cleared on a microprocessor read cycle, but if either of the alarms is then active this bit position re-latches. Loss of clock occurs when the T1 input clock (TCI1) is stuck high or low for 10 or more clock cycles. Recovery occurs on the first T1 input clock transition. Loss of signal for the rail interface occurs when no TPI1 signal transitions occur in a period of 175 ± 75 consecutive pulse positions. Recovery occurs when there is an average pulse density of at least 12.5% over a period of 175 ± 75 contiguous pulse positions starting with the receipt of a detected pulse.
	0	T1AIS	**Port 1 Transmit AIS Detected:** A latched bit position which indicates that a T1 AIS (unframed all ones) has been detected in the Port 1 data. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position re-latches.
0B	7-0	Port 1 Coding Error Counter High Order Byte	**Port 1 Transmit Coding Violation Counter:** High order byte of a 16-bit saturating counter which counts the number of coding errors that have occurred in the AMI or B8ZS line codes. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle.

Address	Bit	Symbol	Description
0D	7	T1VTAIS	**Port 1 Transmit VT/TU AIS:** A 1 causes a VT/TU AIS to be generated and transmitted. A VT/TU AIS consists of all ones in the entire VT, including bytes V1 through V4.
	6	T1FB2	**Port 1 Transmit BIP-2 Error Mask (Force BIP-2 Error):** A 1 causes bits 1 and 2 (BIP-2 value) in the transmitted V5 byte to be sent inverted from the calculated value continuously.
	5	T1FFB	**Port 1 Transmit Force FEBE Error:** A 1 causes bit 3 (FEBE) in the V5 byte to be transmitted inverted from its normally transmitted value.
	4	T1RDI	**Port 1 Transmit Remote Defect Indication (Yellow/FERF):** A 1 causes an RDI alarm to be transmitted (Bit 8 in V5 = 1).
	3	T1RFI	**Port 1 Transmit Remote Failure Indication:** A 1 causes an RFI alarm to be transmitted (Bit 4 in V5 = 1).
	2-0	A1 TX Label	**Port 1 Transmit Signal Label:** The three bit positions written by the processor correspond to bits 5 through 7 in the V5 byte. Bit 2 corresponds to bit 7 in the V5 byte.
0E	7-0	Port 1 Transmit O-bits	**Port 1Transmit Overhead Communication Channel Bits:** Bits 3-0 correspond to bits 3-6 in the first justification control byte, while bits 7-4 correspond to bits 3-6 in the second justification control byte in the VT/TU format.
0F	7	R1SEL	**Port 1 Receive A or B-side VT/TU Bus Selection:** Determines the drop bus VT/TU selection. A 1 selects the B-side drop bus, and a 0 selects the A-side drop bus.
	6-0	VTN1	**Port 1 VT/TU Selection:** Works in conjunction with the R1SEL control bit. The seven bit binary code written into this location selects the VT or TU that is to be dropped from the A or B-side drop bus. The binary value of 0 and a value above the range will not select a VT or TU. For example, the VT selection in an STS-3 format is given below: Bit 6 5 4 3 2 1 0 STS-3 Mapping 0 0 0 0 0 0 0 No VT# selected, AIS generated 0 0 0 0 0 0 1 STS-1#1, GP#1, VT#1 selected 0 0 1 1 1 0 1 STS-1#2, GP#1, VT#1 selected 0 1 1 1 0 0 1 STS-1#3, GP#1, VT#1 selected - - - - - - - 1 0 1 0 1 0 0 STS-1#3, GP#7, VT#4 selected 1 0 1 0 1 0 1 No VT# selected, AIS generated - - - - - - - 1 1 1 1 1 1 1 No VT# selected, AIS generated Note: AIS may be over-written by writing a 0 to R1EN which will 3-state the port 1 data and clock output leads.

PORT 1 A-SIDE DROP BUS RECEIVE REGISTERS

Address	Bit	Symbol	Description
10	7-0	A1BIP2 Count	**Port 1 A-side Drop Bus BIP-2 Counter:** An 8-bit saturating counter which counts the number of BIP-2 errors detected in the receive direction. A maximum of two errors can be detected each frame. During a read cycle internal logic holds an incoming error count until the read cycle is complete, and then updates the counter. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle.
11	7-0	A1FEBE Count	**Port 1 A-side Drop Bus FEBE Counter:** An 8-bit saturating counter which counts the number of FEBE errors received (Bit 3 in V5 = 1). During a read cycle internal logic holds an incoming error count until the read cycle is complete, and then updates the counter. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle.
12	7	A1UNEQ	**Port 1 A-side Drop Bus Unequipped Indication:** A latched bit position which indicates an Unequipped status has been detected in the V5 signal label bits (Bits 5-7 in V5 = 0). This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	6	A1SLER	**Port 1 A-side Drop Bus Signal Label Mismatch Indication:** A latched bit position which indicates that the receive signal label bits (Bits 5-7 in V5) did not match the microprocessor-written signal label. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position re-latches.
	3	A1NDF	**Port 1 A-side Drop Bus New Data Flag Indication:** A latched bit position which indicates a New Data Flag (1001) has been detected in the V1 pointer byte (Bits 1-4 in V1 are the inverse of the 0110). This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position re-latches.
	0	TA1FE	**Port 1 Transmit A-side Add Bus FIFO Error:** A latched bit position which indicates that the A-side add bus FIFO has overflowed or underflowed. The FIFO resets automatically. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position re-latches.

Address	Bit	Symbol	Description
13	7	A1AIS	**Port 1 A-side Drop Bus VT AIS Alarm:** A latched bit position which indicates a VT (TU) AIS has been detected. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	6	A1LOP	**Port 1 A-side Drop Bus Loss Of Pointer Alarm:** A latched bit position which indicates a loss of pointer has been detected. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	5	A1SIZE	**Port 1 A-side Drop Bus Pointer Size Error Indication:** A latched bit position which indicates that the receive size indicator in the pointer (Bits 5 and 6 in the V1 pointer byte) does not = 11. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	4	A1RDI	**Port 1 A-side Drop Bus Remote Defect Indication (FERF):** A latched bit position which indicates an RDI (FERF/Yellow) alarm has been detected (Bit 8 in V5 = 1). This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	3	A1RFI	**Port 1 A-side Drop Bus Remote Failure Indication:** A latched bit position which indicates an RFI alarm has been detected (Bit 4 in V5 = 1). This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	2-0	A1 RX Label	**Port 1 A-side Drop Bus Received Signal Label:** The three bit positions correspond to the three signal label bits found in bits 5 through 7 in V5. These bits are updated each V5 time. Bit 2 corresponds to bit 7 in the V5 byte. These bits are also compared against the microprocessor-written mismatch signal label bits for a mismatch indication.
14	7-4	A1PJ Count	**Port 1 A-side Drop Bus Positive Pointer Justification Counter:** A four bit counter that increments on a positive pointer movement. During a read cycle internal logic holds the count until the read cycle is complete, and then updates the counter. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle.
	3-0	A1NJ Count	**Port 1 A-side Drop Bus Negative Pointer Justification Counter:** A four bit counter that increments on a negative pointer movement. During a read cycle internal logic holds the count until the read cycle is complete, and then updates the counter. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle.
15	7-0	A1 RX O-bits	**Port 1 A-side Drop Bus Receive 0-bits:** The eight bits indicate the states of the eight overhead communication bits received in the VT/TU. Bits 3-0 correspond to bits 3-6 in the first justification control byte, while bits 7-4 correspond to bits 3-6 in the second justification control byte in the VT/TU format.
16	2-0	A1UPSL	**Port 1 A-side Drop Bus Microprocessor-Written Signal Label:** The three bit positions correspond to the three signal label bits found in bits 5 through 7 in V5. Bit 2 corresponds to bit 7 in the V5 byte. These bits are written by the microprocessor, and compared against the received signal label for a mismatch signal label alarm.

PORT 1 B-SIDE DROP BUS RECEIVE REGISTERS

Address	Bit	Symbol	Description
18	7-0	B1BIP2 Count	**Port 1 B-side Drop Bus BIP-2 Counter:** An 8-bit saturating counter which counts the number of BIP-2 errors detected in the receive direction. A maximum of two errors can be detected each frame. During a read cycle internal logic holds the incoming error count until the read cycle is complete, and then updates the counter. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle.
19	7-0	B1FEBE Count	**Port 1 B-side Drop Bus FEBE Counter:** An 8-bit saturating counter which counts the number of FEBE errors received (Bit 3 in V5 = 1). During a read cycle internal logic holds an incoming error count until the read cycle is complete, and then updates the counter. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle.
1A	7	B1UNEQ	**Port 1 B-side Drop Bus Unequipped Indication:** A latched bit position which indicates an Unequipped status has been detected in the V5 signal label bits (Bits 5-7 in V5 = 0). This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	6	B1SLER	**Port 1 B-side Drop Bus Signal Label Mismatch Indication:** A latched bit position which indicates that the receive signal label bits (Bits 5-7 in V5) did not match the microprocessor-written signal label. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position re-latches.
	3	B1NDF	**Port 1 B-side Drop Bus New Data Flag Indication:** A latched bit position which indicates a New Data Flag (1001) has been detected in the V1 pointer byte (Bits 1-4 in V1 are the inverse of the 0110). This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position re-latches.
	0	TB1FE	**Port 1 Transmit B-side Add Bus FIFO Error:** A latched bit position which indicates that the B-side add bus FIFO has overflowed or underflowed. The FIFO will reset automatically. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position re-latches.
1B	7	B1AIS	**Port 1 B-side Drop Bus VT AIS Alarm:** A latched bit position which indicates a VT (TU) AIS has been detected. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	6	B1LOP	**Port 1 B-side Drop Bus Loss Of Pointer Alarm:** A latched bit position which indicates a loss of pointer has been detected. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	5	B1SIZE	**Port 1 B-side Drop Bus Pointer Size Error Indication:** A latched bit position which indicates that the receive size indicator in the pointer (Bits 5 and 6 in the V1 pointer byte) does not = 11. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.

Address	Bit	Symbol	Description
1B (cont.)	4	B1RDI	**Port 1 B-side Drop Bus Remote Defect Indication (FERF):** A latched bit position which indicates an RDI (FERF/Yellow) alarm has been detected (Bit 8 in V5 = 1). This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	3	B1RFI	**Port 1 B-side Drop Bus Remote Failure Indication:** A latched bit position which indicates an RFI alarm has been detected (Bit 4 in V5 = 1). This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	2-0	B1 RX Label	**Port 1 B-side Drop Bus Received Signal Label:** The three bit positions correspond to the three signal label bits found in bits 5 through 7 in V5. These bits are updated each V5 time. Bit 2 corresponds to bit 7 in the V5 byte. These bits are also compared against the microprocessor-written mismatch signal label bits for a mismatch indication.
1C	7-4	B1PJ Count	**Port 1 B-side Drop Bus Positive Pointer Justification Counter:** A four bit counter that increments on a positive pointer movement. During a read cycle internal logic holds an incoming count of 1 until the read cycle is complete, and then updates the counter. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle.
	3-0	B1NJ Count	**Port 1 B-side Drop Bus Negative Pointer Justification Counter:** A four bit counter that increments on a negative pointer movement. During a read cycle internal logic holds an incoming count of 1 until the read cycle is complete, and then updates the counter. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle.
1D	7-0	B1 RX O-bits	**Port 1 B-side Drop Bus Receive 0-bits:** The eight bits indicate the states of the eight overhead communication bits received in the VT. Bits 3-0 correspond to bits 3-6 in the first justification control byte, while bits 7-4 correspond to bits 3-6 in the second justification control byte in the VT/TU format.
1E	2-0	B1UPSL	**Port 1 B-side Drop Bus Microprocessor-Written Signal Label:** The three bit positions correspond to the three signal label bits found in bits 5 through 7 in V5. Bit 2 corresponds to bit 7 in the V5 byte. These bits are written by the microprocessor, and compared against the received signal label for a mismatch signal label alarm.

B-SIDE DROP BUS STATUS REGISTERS

Address	Bit	Symbol	Description
24	7	BDLOC	**B-side Drop Bus Loss Of Clock:** A latched bit position that indicates a loss of clock in the B-side drop bus has been detected. A loss of clock alarm causes a receive AIS for the duration of the alarm, and sets the like-named add bus signals (data and PAR signal) to the high impedance state. The $\overline{\text{BADD}}$ indication signal becomes inactive for the duration of the alarm. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch. The loss of clock alarm occurs when the input drop clock (BDCLK) is stuck high or low for 10 or more clock cycles. Recovery occurs on the first drop clock transition.
	5	BALOC	**B Add Bus Loss Of Clock:** A latched bit position which indicates that the B Add bus has detected a loss of clock, when control lead $\overline{\text{ABUST}}$ is low. A loss of clock alarm causes the add data and parity bit to 3-state, and sets the add indicator off for the duration of the alarm. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch. The loss of clock alarm occurs when the input add clock (BACLK) is stuck high or low for 10 or more clock cycles. Recovery occurs on the first add clock transition.
	2	B2DH4E	**B-side Drop Bus Port 2 Loss of H4 Indication:** A latched bit position that indicates that the anticipated received H4 multiframe sequence of 00, 01, 10, 11 has not been received properly. The ADMA-T1P will continue to operate in a free running mode, but will lock to a new H4 sequence after two consecutive sequences have been received properly. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	1	B1DH4E	**B-side Drop Bus Port 1 Loss of H4 Indication:** A latched bit position which indicates that the anticipated received H4 multiframe sequence of 00, 01, 10, 11 has not been received properly. The ADMA-T1P will continue to operate in a free running mode, but will lock to a new H4 sequence after two consecutive sequences have been received properly. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	0	BDPAR	**B-side Drop Bus Parity Error Detected:** A latched bit position which indicates that an odd parity error has been detected in the B-side drop bus signals. Even parity detection is provided by writing a 1 to the Drop Bus Parity Even (DPE) control bit. Other than an alarm indication, no other action is taken. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.

PORT 2 STATUS/TRANSMIT REGISTERS

Address	Bit	Symbol	Description
28	7-0	Port 2 Pointer Leak Rate Value	**Port 2 FIFO Leak Rate Register:** The count written into this location is used for the internal leak buffer, and represents the average leak rate. A count of one represents 8 frames, or 2 multiframes in the rate of occurrence of pointer movements from the number of counts read from positive/negative stuff counters. A count of 0 is invalid, and no selection takes place.
29	7-0	Port 2 Coding Error Counter Low Order Byte	**Port 2 Transmit Coding Violation Counter:** Low order byte of a 16-bit saturating counter that counts the number of coding errors that have occurred in the AMI or B8ZS line codes. During a read cycle internal logic holds a count of 1 until the read cycle is complete, and then updates the counter. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle. This location must be read first before reading the high order byte.
2A	2	R2FFE	**Port 2 Receive FIFO Error:** A latched bit position which indicates that the receive FIFO for port 2 has overflowed or underflowed. The FIFO will reset automatically. Other than an alarm indication, no other action will be taken. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position re-latches.
	1	T2LOCS	**Port 2 Transmit Loss Of T1 Clock or Signal:** A latched bit position which indicates that the Port 2 T1 clock or data signal has failed. This bit position is cleared on a microprocessor read cycle, but if either of the alarms is then active this bit position re-latches. Loss of clock occurs when the T1 input clock (TCI2) is stuck high or low for 10 or more clock cycles. Recovery occurs on the first T1 input clock transition. Loss of signal for the rail interface occurs when no TPI2 signal transitions occur in a period of 175 ± 75 consecutive pulse positions. Recovery occurs when there is an average pulse density of at least 12.5% over a period of 175 ± 75 contiguous pulse positions starting with the receipt of a detected pulse.
	0	T2AIS	**Port 2 Transmit AIS Detected:** A latched bit position which indicates that a T1 AIS (unframed all ones) has been detected in the Port 2 data. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position re-latches.
2B	7-0	Port 2 Coding Error Counter High Order Byte	**Port 2 Transmit Coding Violation Counter:** High order byte of an 16-bit saturating counter which counts the number of coding errors that have occurred in the AMI or B8ZS line codes. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle.

Address	Bit	Symbol	Description
2D	7	T2VTAIS	**Port 2 Transmit VT/TU AIS:** A 1 causes a VT/TU AIS to be generated and transmitted. A VT/TU AIS consists of all ones in the entire VT, including bytes V1 through V4.
	6	T2FB2	**Port 2 Transmit BIP-2 Error Mask (Force BIP-2 Error):** A 1 causes bits 1 and 2 (BIP-2 value) in the transmitted V5 byte to be sent inverted from the calculated value continuously.
	5	T2FFB	**Port 2 Transmit Force FEBE Error:** A 1 causes bit 3 (FEBE) in the V5 byte to be transmitted inverted from its normally transmitted value.
	4	T2RDI	**Port 2 Transmit Remote Defect Indication (Yellow/FERF):** A 1 causes an RDI alarm to be transmitted (Bit 8 in V5 = 1).
	3	T2RFI	**Port 2 Transmit Remote Failure Indication:** A 1 causes an RFI alarm to be transmitted (Bit 4 in V5 = 1).
	2-0	A2 TX Label	**Port 2 Transmit Signal Label:** The three bit positions written by the processor correspond to bits 5 through 7 in the V5 byte. Bit 2 corresponds to bit 7 in the V5 byte.
2E	7-0	Port 2 Transmit O-bits	**Port 2 Transmit Overhead Communication Channel Bits:** Bits 3-0 correspond to bits 3-6 in the first justification control byte, while bits 7-4 correspond to bits 3-6 in the second justification control byte in the VT/TU format.
2F	7	R2SEL	**Port 2 Receive A or B-side VT/TU Bus Selection:** Determines the drop bus VT/TU selection. A 1 selects the B-side drop bus, and a 0 selects the A-side drop bus.
	6-0	VTN2	**Port 2 VT/TU Selection:** Works in conjunction with the R2SEL control bit. The seven bit binary code written into this location selects the VT or TU that is to be dropped from the A or B-side drop bus. The binary value of 0 and a value above the range will not select a VT or TU. For example, the VT selection in an STS-3 format is given below: Bit 6 5 4 3 2 1 0 STS-3 Mapping 0 0 0 0 0 0 0 No VT# selected, AIS generated 0 0 0 0 0 0 1 STS-1#1, GP#1, VT#1 selected 0 0 1 1 1 0 1 STS-1#2, GP#1, VT#1 selected 0 1 1 1 0 0 1 STS-1#3, GP#1, VT#1 selected - - - - - - - 1 0 1 0 1 0 0 STS-1#3, GP#7, VT#4 selected 1 0 1 0 1 0 1 No VT# selected, AIS generated - - - - - - - 1 1 1 1 1 1 1 No VT# selected, AIS generated Note: AIS may be over-written by writing a 0 to R2EN which will 3-state the port 2 data and clock output leads.

PORT 2 A-SIDE DROP BUS RECEIVE REGISTERS

Address	Bit	Symbol	Description
30	7-0	A2BIP2 Count	**Port 2 A-side Drop Bus BIP-2 Counter:** An 8-bit saturating counter which counts the number of BIP-2 errors detected in the receive direction. A maximum of two errors can be detected each frame. During a read cycle internal logic holds the incoming error count until the read cycle is complete, and then updates the counter. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle.
31	7-0	A2FEBE Count	**Port 2 A-side Drop Bus FEBE Counter:** An 8-bit saturating counter which counts the number of FEBE errors received (Bit 3 in V5 = 1). During a read cycle internal logic holds an incoming error count until the read cycle is complete, and then updates the counter. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle.
32	7	A2UNEQ	**Port 2 A-side Drop Bus Unequipped Indication:** A latched bit position which indicates an Unequipped status has been detected in the V5 signal label bits (Bits 2-0 in V5 = 0). This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	6	A2SLER	**Port 2 A-side Drop Bus Signal Label Mismatch Indication:** A latched bit position which indicates that the receive signal label bits (Bits 2-0 in V5) did not match the microprocessor-written signal label. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position re-latches.
	3	A2NDF	**Port 2 A-side Drop Bus New Data Flag Indication:** A latched bit position which indicates a New Data Flag (1001) has been detected in the V1 pointer byte (Bits 1-4 in V1 are the inverse of the 0110). This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position re-latches.
	0	TA2FE	**Port 2 Transmit A-side Add Bus FIFO Error:** A latched bit position which indicates that the A-side add bus FIFO has overflowed or underflowed. The FIFO will reset automatically. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position re-latches.
33	7	A2AIS	**Port 2 A-side Drop Bus VT AIS Alarm:** A latched bit position which indicates a VT (TU) AIS has been detected. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	6	A2LOP	**Port 2 A-side Drop Bus Loss Of Pointer Alarm:** A latched bit position which indicates a loss of pointer has been detected. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	5	A2SIZE	**Port 2 A-side Drop Bus Pointer Size Error Indication:** A latched bit position which indicates that the receive size indicator in the pointer (Bits 5 and 6 in the V1 pointer byte) does not = 11. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.

Address	Bit	Symbol	Description
33 (cont.)	4	A2RDI	**Port 2 A-side Drop Bus Remote Defect Indication (FERF):** A latched bit position which indicates an RDI (FERF/Yellow) alarm has been detected (Bit 8 in V5 = 1). This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	3	A2RFI	**Port 2 A-side Drop Bus Remote Failure Indication:** A latched bit position which indicates an RFI alarm has been detected (Bit 4 in V5 = 1). This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	2-0	A2 RX Label	**Port 2 A-side Drop Bus Received Signal Label:** The three bit positions correspond to the three signal label bits found in bits 5 through 7 in V5. These bits are updated each V5 time. Bit 2 corresponds to bit 7 in the V5 byte. These bits are also compared against the microprocessor written mismatch signal label bits for a mismatch indication.
34	7-4	Port 2 A2PJ Count	**Port 2 A-side Drop Bus Positive Pointer Justification Counter:** A four bit counter that increments on a positive pointer movement. During a read cycle internal logic holds an incoming count of 1 until the read cycle is complete, and then updates the counter. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle.
	3-0	Port 2 A2NJ Count	**Port 2 A-side Drop Bus Negative Pointer Justification Counter:** A four bit counter that increments on a negative pointer movement. During a read cycle internal logic holds an incoming count of 1 until the read cycle is complete, and then updates the counter. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle.
35	7-0	A2 RX O-bits	**Port 2 A-side Drop Bus Receive 0-bits:** The eight bits indicate the states of the eight overhead communication bits received in the VT/TU. Bits 3-0 correspond to bits 3-6 in the first justification control byte, while bits 7-4 correspond to bits 3-6 in the second justification control byte in the VT/TU format.
36	2-0	A2UPSL	**Port 2 A-side Drop Bus Microprocessor-Written Signal Label:** The three bit positions correspond to the three signal label bits found in bits 5 through 7 in V5. Bit 2 corresponds to bit 7 in the V5 byte. These bits are written by the microprocessor, and compared against the received signal label for a mismatch signal label alarm.

PORT 2 B-SIDE DROP BUS RECEIVE REGISTERS

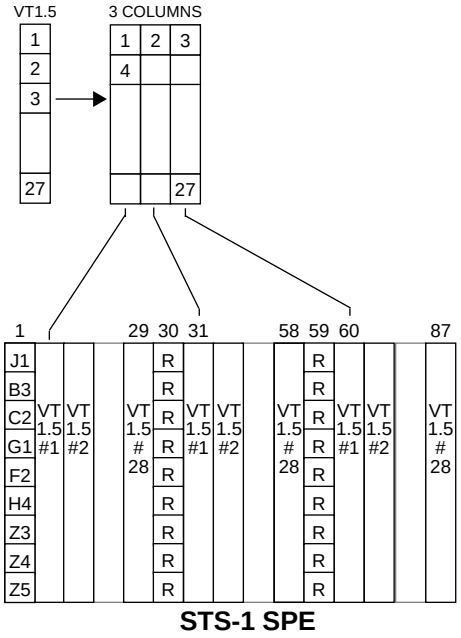
Address	Bit	Symbol	Description
38	7-0	B2BIP2 Count	**Port 2 B-side Drop Bus BIP-2 Counter:** An 8-bit saturating counter which counts the number of BIP-2 errors detected in the receive direction. A maximum of two errors can be detected each frame. During a read cycle internal logic holds the incoming error count until the read cycle is complete, and then updates the counter. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle.
39	7-0	B2FEBE Count	**Port 2 B-side Drop Bus FEBE Counter:** An 8-bit saturating counter which counts the number of FEBE errors received (Bit 3 in V5 = 1). During a read cycle internal logic holds an incoming error count until the read cycle is complete, and then updates the counter. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle.
3A	7	B2UNEQ	**Port 2 B-side Drop Bus Unequipped Indication:** A latched bit position which indicates an Unequipped status has been detected in the V5 signal label bits (Bits 2-0 in V5 = 0). This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	6	B2SLER	**Port 2 B-side Drop Bus Signal Label Mismatch Indication:** A latched bit position which indicates that the receive signal label bits (Bits 2-0 in V5) did not match the microprocessor-written signal label. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position re-latches.
	3	B2NDF	**Port 2 B-side Drop Bus New Data Flag Indication:** A latched bit position which indicates a New Data Flag (1001) has been detected in the V1 pointer byte (Bits 1-4 in V1 are the inverse of the 0110). This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position re-latches.
	0	TB2FE	**Port 2 Transmit B-side Add Bus FIFO Error:** A latched bit position which indicates that the B-side add bus FIFO has overflowed or underflowed. The FIFO will reset automatically. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position re-latches.
3B	7	B2AIS	**Port 2 B-side Drop Bus VT AIS Alarm:** A latched bit position which indicates a VT (TU) AIS has been detected. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	6	B2LOP	**Port 2 B-side Drop Bus Loss Of Pointer Alarm:** A latched bit position which indicates a loss of pointer has been detected. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	5	B2SIZE	**Port 2 B-side Drop Bus Pointer Size Error Indication:** A latched bit position which indicates that the receive size indicator in the pointer (Bits 5 and 6 in the V1 pointer byte) does not = 11. This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.

Address	Bit	Symbol	Description
3B (cont.)	4	B2RDI	**Port 2 B-side Drop Bus Remote Defect Indication (FERF):** A latched bit position which indicates an RDI (FERF/Yellow) alarm has been detected (Bit 8 in V5 = 1). This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	3	B2RFI	**Port 2 B-side Drop Bus Remote Failure Indication:** A latched bit position which indicates an RFI alarm has been detected (Bit 4 in V5 = 1). This bit position is cleared on a microprocessor read cycle. If the alarm is active, this bit position will re-latch.
	2-0	B2 RX Label	**Port 2 B-side Drop Bus Received Signal Label:** The three bit positions correspond to the three signal label bits found in bits 5 through 7 in V5. These bits are updated each V5 time. Bit 2 corresponds to bit 7 in the V5 byte. These bits are also compared against the microprocessor-written mismatch signal label bits for a mismatch indication.
3C	7-4	B2PJ Count	**Port 2 B-side Drop Bus Positive Pointer Justification Counter:** A four bit counter that increments on a positive pointer movement. During a read cycle internal logic holds an incoming count of 1 until the read cycle is complete, and then updates the counter. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle.
	3-0	B2NJ Count	**Port 2 B-side Drop Bus Negative Pointer Justification Counter:** A four bit counter that increments on a negative pointer movement. During a read cycle internal logic holds an incoming count of 1 until the read cycle is complete, and then updates the counter. This counter is cleared on a reset pulse, when a 1 is written to the reset counter control bit (RESETC), or by a read cycle.
3D	7-0	B2 RX O-bits	**Port 2 B-side Drop Bus Receive 0-bits:** The eight bits indicate the states of the eight overhead communication bits received in the VT. Bits 3-0 correspond to bits 3-6 in the first justification control byte, while bits 7-4 correspond to bits 3-6 in the second justification control byte in the VT/TU format.
3E	2-0	B2UPSL	**Port 2 B-side Drop Bus Microprocessor-Written Signal Label:** The three bit positions correspond to the three signal label bits found in bits 5 through 7 in V5. Bit 2 corresponds to bit 7 in the V5 byte. These bits are written by the microprocessor, and compared against the received signal label for a mismatch signal label alarm.

MULTIPLEX FORMAT AND MAPPING INFORMATION

STS-1 VT1.5 (1.544 Mbit/s) Multiplex Format

The following diagram and table illustrate the mapping of the 28 VT1.5s into a STS-1 SPE. Column 1 is assigned to carry the path overhead bytes.



STS-1 SPE

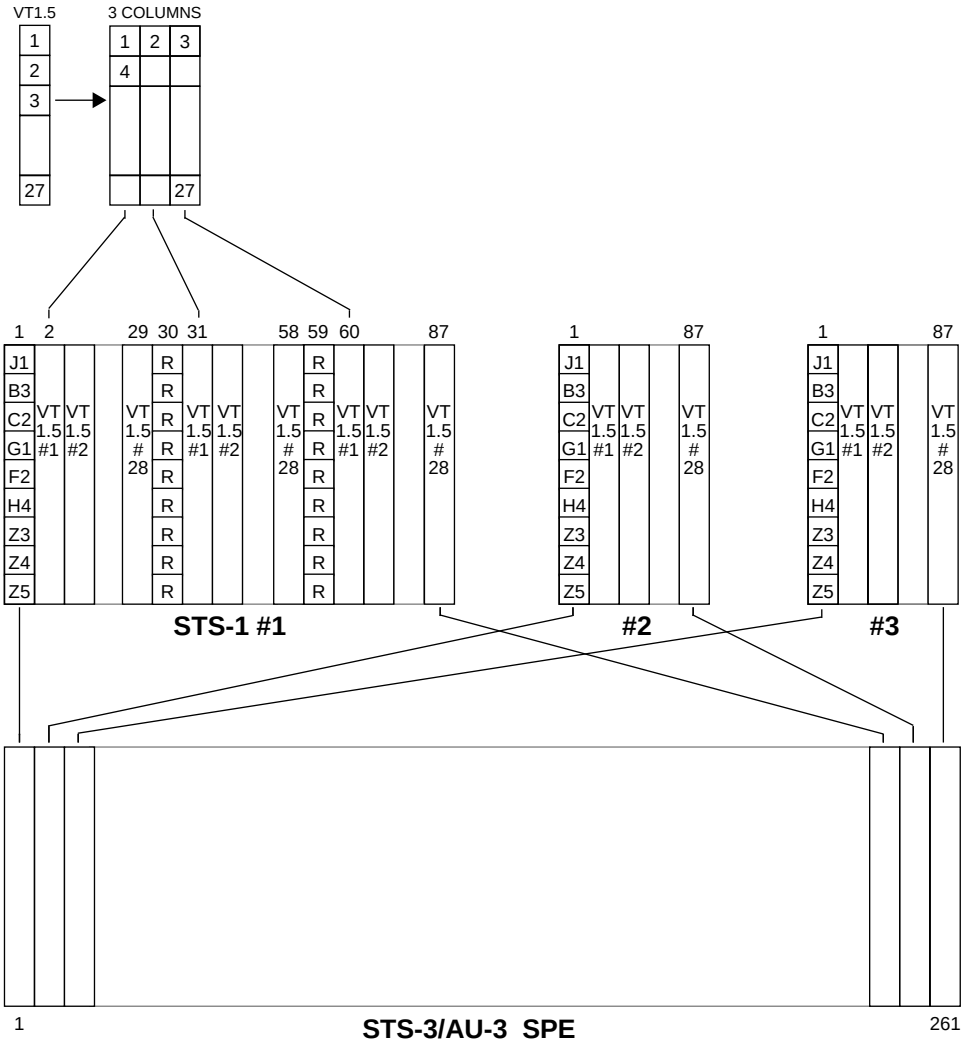
STS-1 Mapping

VT#	0F & 2F Registers							VT1.5 Column Numbers*
	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	No VT Selected
1	0	0	0	0	0	0	1	2, 31, 60
2	0	0	0	0	0	1	0	3, 32, 61
3	0	0	0	0	0	1	1	4, 33, 62
4	0	0	0	0	1	0	0	5, 34, 63
5	0	0	0	0	1	0	1	6, 35, 64
6	0	0	0	0	1	1	0	7, 36, 65
7	0	0	0	0	1	1	1	8, 37, 66
8	0	0	0	1	0	0	0	9, 38, 67
9	0	0	0	1	0	0	1	10, 39, 68
10	0	0	0	1	0	1	0	11, 40, 69
11	0	0	0	1	0	1	1	12, 41, 70
12	0	0	0	1	1	0	0	13, 42, 71
13	0	0	0	1	1	0	1	14, 43, 72
14	0	0	0	1	1	1	0	15, 44, 73
15	0	0	0	1	1	1	1	16, 45, 74
16	0	0	1	0	0	0	0	17, 46, 75
17	0	0	1	0	0	0	1	18, 47, 76
18	0	0	1	0	0	1	0	19, 48, 77
19	0	0	1	0	0	1	1	20, 49, 78
20	0	0	1	0	1	0	0	21, 50, 79
21	0	0	1	0	1	0	1	22, 51, 80
22	0	0	1	0	1	1	0	23, 52, 81
23	0	0	1	0	1	1	1	24, 53, 82
24	0	0	1	1	0	0	0	25, 54, 83
25	0	0	1	1	0	0	1	26, 55, 84
26	0	0	1	1	0	1	0	27, 56, 85
27	0	0	1	1	0	1	1	28, 57, 86
28	0	0	1	1	1	0	0	29, 58, 87

* Note: Columns 30 and 59 carry fixed Stuff bytes. Column 1 is assigned for the POH bytes.

STS-3/AU-3 VT1.5/TU-11 (1.544 Mbit/s) Multiplex Format Mapping

The following diagram and table illustrate the mapping of the VT1.5/TU-11s into a STS-3/AU-3 SPE. Each STS-3 carries three STS-1s. Column 1 in each STS-1/AU-3 is assigned to carry the path overhead bytes.



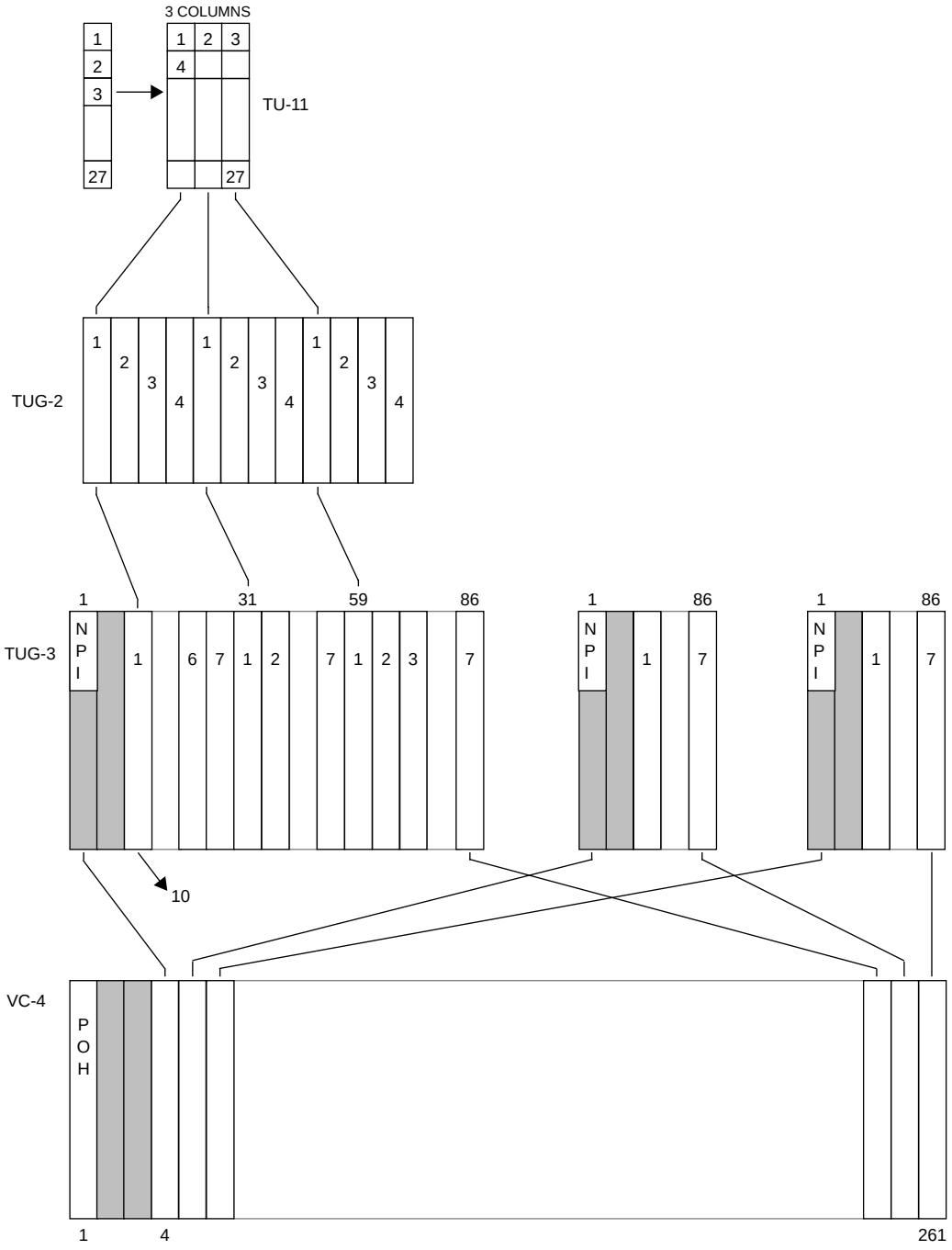
STS-3 AU-3 Mapping

VT TU #	0F & 2F Registers 6 5 4 3 2 1 0	VT/TU Column Numbers	VT TU #	0F & 2F Registers 6 5 4 3 2 1 0	VT/TU Column Numbers	VT TU #	0F & 2F Registers 6 5 4 3 2 1 0	VT/TU Column Numbers*
	0 0 0 0 0 0 0	No TU Selected						
1	0 0 0 0 0 0 1	4 91 178	29	0 0 1 1 1 0 1	5 92 179	57	0 1 1 1 0 0 1	6 93 180
2	0 0 0 0 0 1 0	7 94 181	30	0 0 1 1 1 1 0	8 95 182	58	0 1 1 1 0 1 0	9 96 183
3	0 0 0 0 0 1 1	10 97 184	31	0 0 1 1 1 1 1	11 98 185	59	0 1 1 1 0 1 1	12 99 186
4	0 0 0 0 1 0 0	13 100 187	32	0 1 0 0 0 0 0	14 101 188	60	0 1 1 1 1 0 0	15 102 189
5	0 0 0 0 1 0 1	16 103 190	33	0 1 0 0 0 0 1	17 104 191	61	0 1 1 1 1 0 1	18 105 192
6	0 0 0 0 1 1 0	19 106 193	34	0 1 0 0 0 1 0	20 107 194	62	0 1 1 1 1 1 0	21 108 195
7	0 0 0 0 1 1 1	22 109 196	35	0 1 0 0 0 1 1	23 110 197	63	0 1 1 1 1 1 1	24 111 198
8	0 0 0 1 0 0 0	25 112 199	36	0 1 0 0 1 0 0	26 113 200	64	1 0 0 0 0 0 0	27 114 201
9	0 0 0 1 0 0 1	28 115 202	37	0 1 0 0 1 0 1	29 116 203	65	1 0 0 0 0 0 1	30 117 204
10	0 0 0 1 0 1 0	31 118 205	38	0 1 0 0 1 1 0	32 119 206	66	1 0 0 0 0 1 0	33 120 207
11	0 0 0 1 0 1 1	34 121 208	39	0 1 0 0 1 1 1	35 122 209	67	1 0 0 0 0 1 1	36 123 210
12	0 0 0 1 1 0 0	37 124 211	40	0 1 0 1 0 0 0	38 125 212	68	1 0 0 0 1 0 0	39 126 213
13	0 0 0 1 1 0 1	40 127 214	41	0 1 0 1 0 0 1	41 128 215	69	1 0 0 0 1 0 1	42 129 216
14	0 0 0 1 1 1 0	43 130 217	42	0 1 0 1 0 1 0	44 131 218	70	1 0 0 0 1 1 0	45 132 219
15	0 0 0 1 1 1 1	46 133 220	43	0 1 0 1 0 1 1	47 134 221	71	1 0 0 0 1 1 1	48 135 222
16	0 0 1 0 0 0 0	49 136 223	44	0 1 0 1 1 0 0	50 137 224	72	1 0 0 1 0 0 0	51 138 225
17	0 0 1 0 0 0 1	52 139 226	45	0 1 0 1 1 0 1	53 140 227	73	1 0 0 1 0 0 1	54 141 228
18	0 0 1 0 0 1 0	55 142 229	46	0 1 0 1 1 1 0	56 143 230	74	1 0 0 1 0 1 0	57 144 231
19	0 0 1 0 0 1 1	58 145 232	47	0 1 0 1 1 1 1	59 146 233	75	1 0 0 1 0 1 1	60 147 234
20	0 0 1 0 1 0 0	61 148 235	48	0 1 1 0 0 0 0	62 149 236	76	1 0 0 1 1 0 0	63 150 237
21	0 0 1 0 1 0 1	64 151 238	49	0 1 1 0 0 0 1	65 152 239	77	1 0 0 1 1 0 1	66 153 240
22	0 0 1 0 1 1 0	67 154 241	50	0 1 1 0 0 1 0	68 155 242	78	1 0 0 1 1 1 0	69 156 243
23	0 0 1 0 1 1 1	70 157 244	51	0 1 1 0 0 1 1	71 158 245	79	1 0 0 1 1 1 1	72 159 246
24	0 0 1 1 0 0 0	73 160 247	52	0 1 1 0 1 0 0	74 161 248	80	1 0 1 0 0 0 0	75 162 249
25	0 0 1 1 0 0 1	76 163 250	53	0 1 1 0 1 0 1	77 164 251	81	1 0 1 0 0 0 1	78 165 252
26	0 0 1 1 0 1 0	79 166 253	54	0 1 1 0 1 1 0	80 167 254	82	1 0 1 0 0 1 0	81 168 255
27	0 0 1 1 0 1 1	82 169 256	55	0 1 1 0 1 1 1	83 170 257	83	1 0 1 0 0 1 1	84 171 258
28	0 0 1 1 1 0 0	85 172 259	56	0 1 1 1 0 0 0	86 173 260	84	0 0 1 0 1 0 0	87 174 261
	STS-1 #1, AU-3 A			STS-1 #2, AU-3 B			STS-1 #3, AU-3 C	

* Note: Columns 88, 89, 90, 175, 176, 177 are fixed stuff.

TU-11 - VC-4 Multiplex Format Mapping

The following diagram and table illustrate the mapping of TU-11s into a VC-4. The ADMA-T1P provides control bits for enabling the Null Pointer Indicators (NPIs) for the columns indicated.

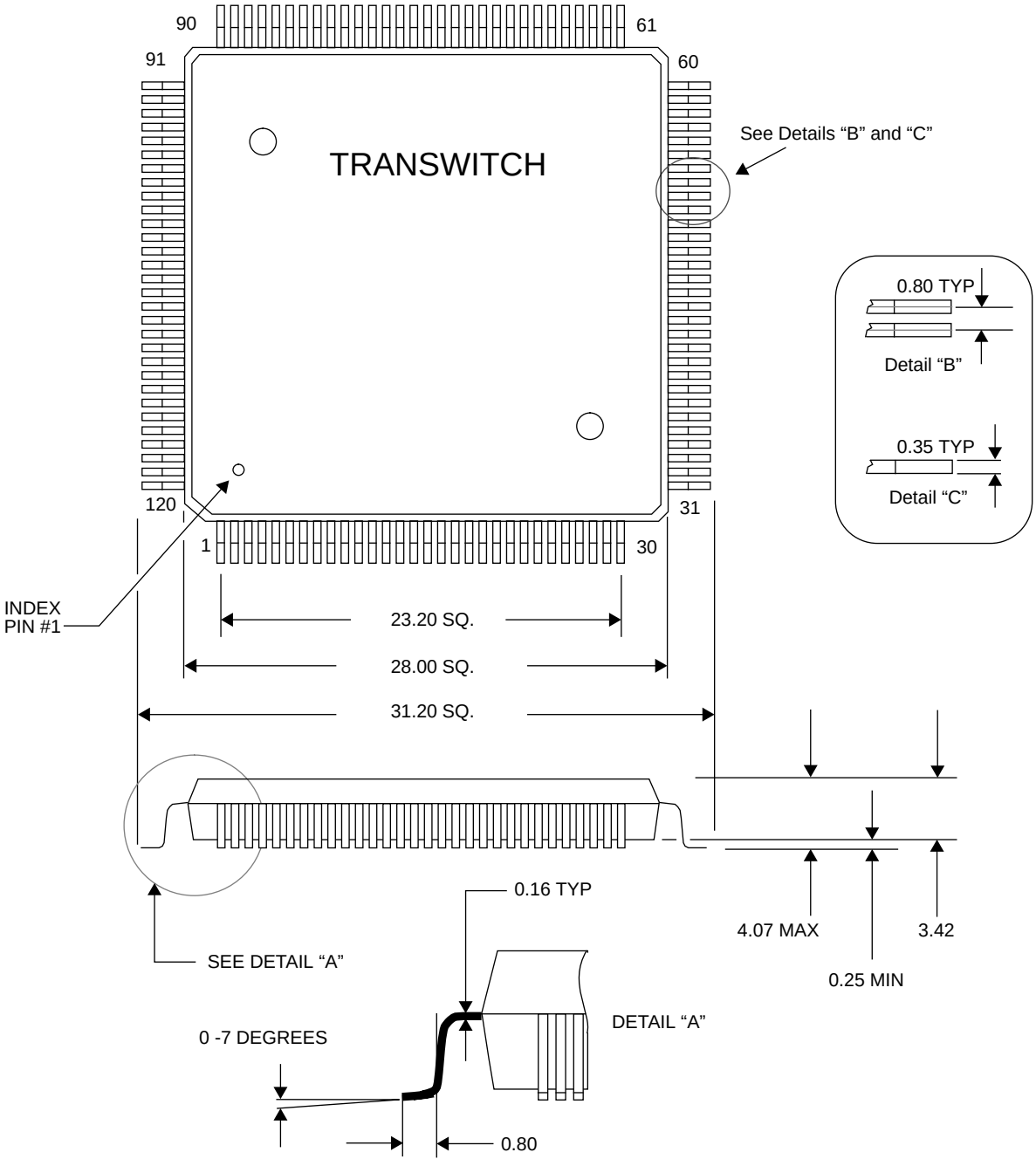


TU-11 - VC-4 Multiplex Format Mapping

TU #	0F & 2F Registers 6 5 4 3 2 1 0	VC-4 Column Numbers	TU #	0F & 2F Registers 6 5 4 3 2 1 0	VC-4 Column Numbers	TU #	0F & 2F Registers 6 5 4 3 2 1 0	VC-4 Column Numbers
	0 0 0 0 0 0 0	No TU Selected						
1	0 0 0 0 0 0 1	10 94 178	29	0 0 1 1 1 0 1	11 95 179	57	0 1 1 1 0 0 1	12 96 180
2	0 0 0 0 0 1 0	13 97 181	30	0 0 1 1 1 1 0	14 98 182	58	0 1 1 1 0 1 0	15 99 183
3	0 0 0 0 0 1 1	16 100 184	31	0 0 1 1 1 1 1	17 101 185	59	0 1 1 1 0 1 1	18 102 186
4	0 0 0 0 1 0 0	19 103 187	32	0 1 0 0 0 0 0	20 104 188	60	0 1 1 1 1 0 0	21 105 189
5	0 0 0 0 1 0 1	22 106 190	33	0 1 0 0 0 0 1	23 107 191	61	0 1 1 1 1 0 1	24 108 192
6	0 0 0 0 1 1 0	25 109 193	34	0 1 0 0 0 1 0	26 110 194	62	0 1 1 1 1 1 0	27 111 195
7	0 0 0 0 1 1 1	28 112 196	35	0 1 0 0 0 1 1	29 113 197	63	0 1 1 1 1 1 1	30 114 198
8	0 0 0 1 0 0 0	31 115 199	36	0 1 0 0 1 0 0	32 116 200	64	1 0 0 0 0 0 0	33 117 201
9	0 0 0 1 0 0 1	34 118 202	37	0 1 0 0 1 0 1	35 119 203	65	1 0 0 0 0 0 1	36 120 204
10	0 0 0 1 0 1 0	37 121 205	38	0 1 0 0 1 1 0	38 122 206	66	1 0 0 0 0 1 0	39 123 207
11	0 0 0 1 0 1 1	40 124 208	39	0 1 0 0 1 1 1	41 125 209	67	1 0 0 0 0 1 1	42 126 210
12	0 0 0 1 1 0 0	43 127 211	40	0 1 0 1 0 0 0	44 128 212	68	1 0 0 0 1 0 0	45 129 213
13	0 0 0 1 1 0 1	46 130 214	41	0 1 0 1 0 0 1	47 131 215	69	1 0 0 0 1 0 1	48 132 216
14	0 0 0 1 1 1 0	49 133 217	42	0 1 0 1 0 1 0	50 134 218	70	1 0 0 0 1 1 0	51 135 219
15	0 0 0 1 1 1 1	52 136 220	43	0 1 0 1 0 1 1	53 137 221	71	1 0 0 0 1 1 1	54 138 222
16	0 0 1 0 0 0 0	55 139 223	44	0 1 0 1 1 0 0	56 140 224	72	1 0 0 1 0 0 0	57 141 225
17	0 0 1 0 0 0 1	58 142 226	45	0 1 0 1 1 0 1	59 143 227	73	1 0 0 1 0 0 1	60 144 228
18	0 0 1 0 0 1 0	61 145 229	46	0 1 0 1 1 1 0	62 146 230	74	1 0 0 1 0 1 0	63 147 231
19	0 0 1 0 0 1 1	64 148 232	47	0 1 0 1 1 1 1	65 149 233	75	1 0 0 1 0 1 1	66 150 234
20	0 0 1 0 1 0 0	67 151 235	48	0 1 1 0 0 0 0	68 152 236	76	1 0 0 1 1 0 0	69 153 237
21	0 0 1 0 1 0 1	70 154 238	49	0 1 1 0 0 0 1	71 155 239	77	1 0 0 1 1 0 1	72 156 240
22	0 0 1 0 1 1 0	73 157 241	50	0 1 1 0 0 1 0	74 158 242	78	1 0 0 1 1 1 0	75 159 243
23	0 0 1 0 1 1 1	76 160 244	51	0 1 1 0 0 1 1	77 161 245	79	1 0 0 1 1 1 1	78 162 246
24	0 0 1 1 0 0 0	79 163 247	52	0 1 1 0 1 0 0	80 164 248	80	1 0 1 0 0 0 0	81 165 249
25	0 0 1 1 0 0 1	82 166 250	53	0 1 1 0 1 0 1	83 167 251	81	1 0 1 0 0 0 1	84 168 252
26	0 0 1 1 0 1 0	85 169 253	54	0 1 1 0 1 1 0	86 170 254	82	1 0 1 0 0 1 0	87 171 255
27	0 0 1 1 0 1 1	89 172 256	55	0 1 1 0 1 1 1	89 173 257	83	1 0 1 0 0 1 1	90 174 258
28	0 0 1 1 1 0 0	91 175 259	56	0 1 1 1 0 0 0	92 176 260	84	0 0 1 0 1 0 0	93 177 261
	TUG-3 A			TUG-3 B			TUG-3 C	

PACKAGE INFORMATION

The ADMA-T1P is available in a 120-pin plastic quad flat package suitable for surface mounting, as illustrated in Figure 12.



Note: All dimensions are shown in millimeters and are nominal unless otherwise indicated.

Figure 12. ADMA-T1P TXC-04011 120-Pin Plastic Quad Flat Package

ORDERING INFORMATION

Part Number: TXC-04011-BIPQ 120-pin Plastic Quad Flat Package (PQFP)

RELATED PRODUCTS

TXC-02201, SM3 VLSI Device (SONET STS-3/STS-1 Mux/Demux). This device multiplexes/demultiplexes three STS-1s into/from an STS-3 signal, and interfaces with the SOT-1 device for the STS-1 signals.

TXC-02301B, SYN155 VLSI Device (155-Mbit/s Synchronizer, Data Output). Provides complete STS-3/STM-1 frame synchronization on incoming 155 Mbit/s signals in a single low power CMOS unit.

TXC-02302B, SYN155C VLSI Device (155-Mbit/s Synchronizer, Clock and Data Output). This device is similar to the SYN155. It has both clock and data outputs on the line side.

TXC-03001, SOT-1 VLSI Device (SONET STS-1 Overhead Terminator). In a single chip, it provides the SONET interface to any payload. Provides access to all of the transport and path overhead defined for an STS-1/STS-N SONET signal.

TXC-03003, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This device performs section, line, and path overhead processing for a STS-3/STS-3c/STM-1 signal. Compliant with ANSI and ITU-T standards.

TXC-04001B, ADMA-T1 VLSI Device (Dual T1 1.544 Mbit/s to VT1.5 or TU-11 Async Mapper-Desync). Interconnects two T1 signals with any two asynchronous mode VT1.5 or TU-11 tributaries carried in SONET STS-1 or SDH AU-3 rate payload interface. Similar to ADMA-T1P device but lacks add bus timing mode and is packaged in an 84-pin PLCC.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

IEEE (U.S.A.)

The Institute of Electrical and Electronics Engineers, Inc.
Customer Service Department
445 Hoes Lane
P. O. Box 1331
Piscataway, NJ 08855-1331

Tel: 800-7014333 (In U.S.A.)
Tel: 908-981-0060
Fax: 908-981-9667

ITU-TSS (International):

Publication Services of International Telecommunication Union (ITU)
Telecommunication Standardization Sector (TSS)
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

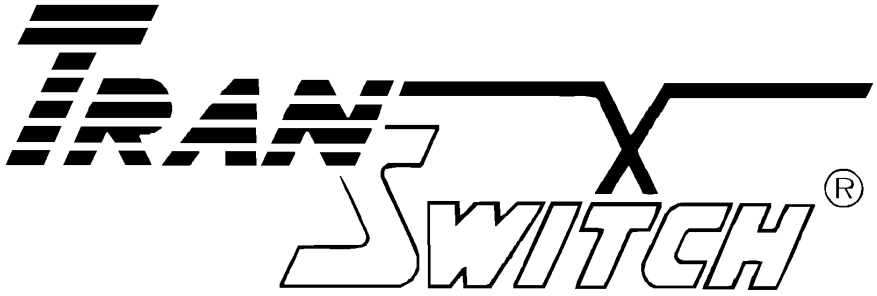
TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

- NOTES -

- NOTES -



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DOCUMENTATION UPDATE REGISTRATION FORM

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If located outside U.S.A., please add - Postal Code: _____ Country: _____

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