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SSI 32P3031
Pulse Detector and Servo Demodulator
Preliminary Data

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DESCRIPTION

The SSI 32P3031 is a low power pulse detector and servo demodulator designed for use in low power applications requiring +5V only power supplies. This device has a fully integrated bipolar circuit that detects and validates amplitude peaks in the output from a disk drive read amplifier, as well as detecting embedded servo information to provide position error signals used for read head positioning.

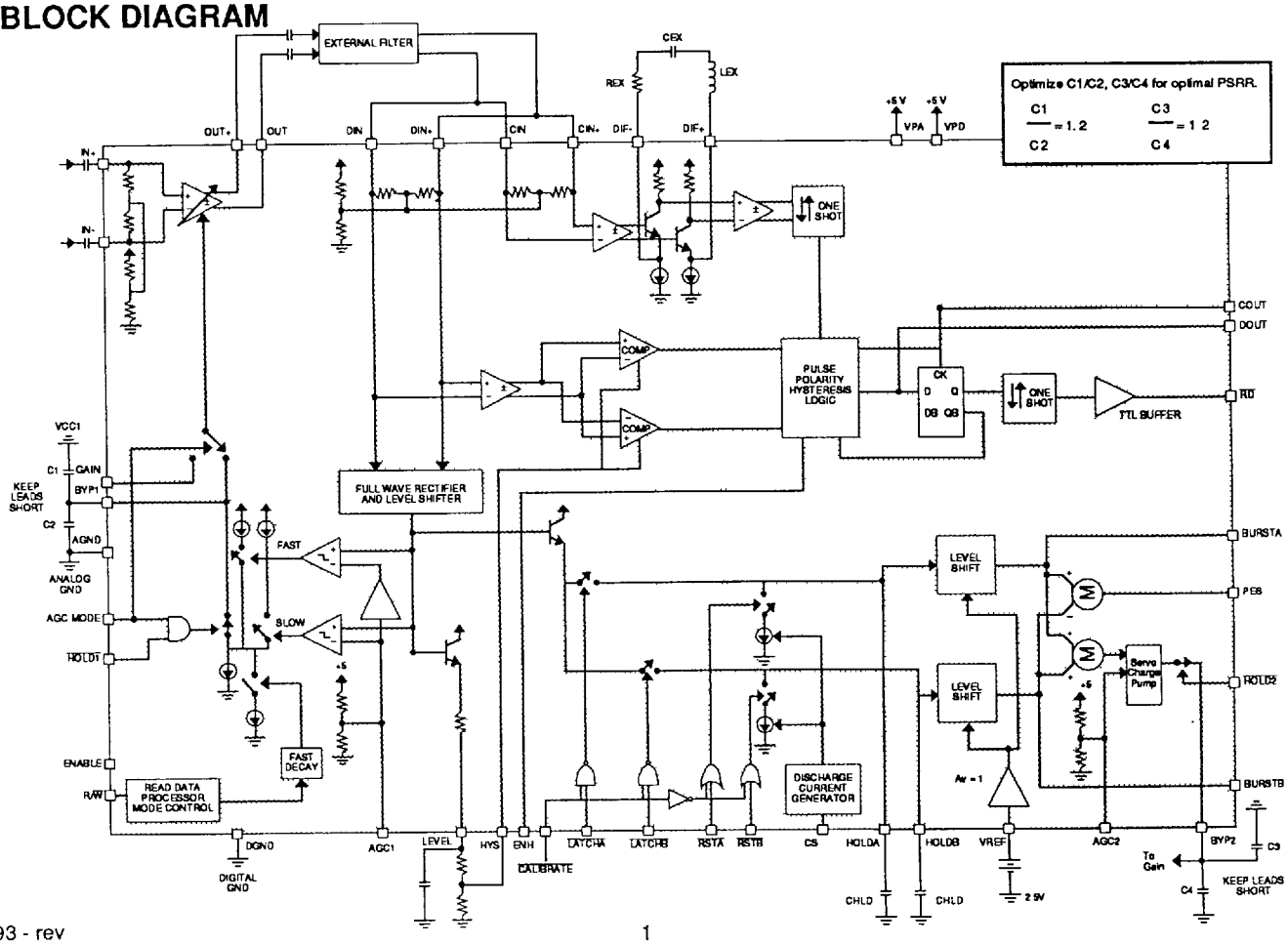
Time and amplitude qualification are used to provide a TTL compatible output that accurately duplicates the time position of input signal peaks. An AGC control loop, using a dual rate charge pump, provides a constant input amplitude for the level qualifier. Level qualification with or without hysteresis can be implemented as a fixed threshold or a constant percentage that tracks signal amplitude that enhances qualification during AGC loop transients.

(Continued)

FEATURES

- +5V only power supplies
- Wide bandwidth AGC input amplifier
- Fast and slow AGC attack and decay regions for fast transient recovery
- Embedded servo channel provides servo burst capture and difference circuits
- Local sampled servo AGC provided based on servo burst output amplitude sum
- Write to Read transient suppression
- Dual mode pulse qualification with/without pulse polarity hysteresis for read/servo data retrieval.
- 24 Mbit/s operation

BLOCK DIAGRAM



DESCRIPTION (Continued)

The Servo Demodulator consists of two peak detector channels that capture rectified servo data peaks. Buffered individual channel outputs are provided along with a difference output. Servo channel gain can be controlled by a sampled AGC signal based on maintaining the amplitude of the sum of both channels.

FUNCTIONAL DESCRIPTION

READ MODE (R/$\overline{W}$ pin high or open)

In Read Mode the SSI 32P3031 is used to process either data or servo signals. In the Data Read Mode the input signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks. In the Servo Read Mode the input signal is amplified and rectified and an error signal based on amplitude comparison is made available. Two servo burst channels are available that provide A & B burst levels.

DATA READ MODE (AGCMODE pin high or open)

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. Gain control is accomplished by full wave rectifying and amplifying the [(DIN+) - (DIN-)] voltage level and comparing it to a reference voltage level at the AGC1 pin.

The SSI 32P3031 contains a dual rate attack charge pump. The value of the attack current is dependent on the instantaneous level at DIN±. For signal levels above 125% of the desired level a fast attack mode is invoked that supplies a 1.4 mA charge current to the network on the BYP1 pin. Between 125% and 100% of the desired level the circuit enters a slow attack mode and supplies 0.18 mA of charge current to the BYP1 pin. This allows the AGC to rapidly recover during a write to read transition but reduces distortion once the AGC amplifier is within range.

Two decay modes are available and are automatically controlled within the device.

Upon a switch to write mode (R/$\overline{W}$ pin low), the device will hold the gain at its previous value, and the AGC input stage is switched into a low impedance state. When the device is then switched back to read mode the AGC holds the gain and stays in the low impedance state for 0.9 µs. It then switches into a fast/slow attack mode if the new gain required is less than the previously held gain or a fast decay mode if the gain required is more than its previous value. The fast decay current is 0.12 mA and stays on 0.9 µs. After the 0.9 µs time period the device stays in a steady state slow attack, slow decay mode. The slow decay discharge current is 4.5 µA.

The AGC1 pin is internally biased so that the target differential voltage input at DIN± is 1.0 Vpp at nominal conditions. The voltage on this pin can be modified by tying a resistor between AGC and AGND or VPA. A resistor to AGND decreases the voltage level, while a resistor to VPA increases it. The resulting AGC voltage level is shown in Figure 1.

Where:

V = Voltage at AGC1 with pin open (1.0V, nom.)

Rint = AGC1 pin input impedance (7.8 kΩ, typ.)

Rx = External resistor.

The new DIN± input target level is nominally

1.0 Vpp/V • V_{AGC}

The maximum AGC amplifier output swing is 2.6 Vp at OUT± which allows for up to 6 dB loss in any external filter between OUT± and DIN±.

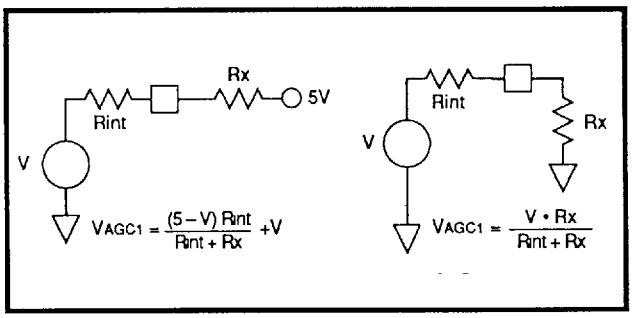


FIGURE 1: AGC Voltage

AGC gain is a linear function of the BYP1/Gain-pin voltage (VBYP1) as shown in Figure 2.

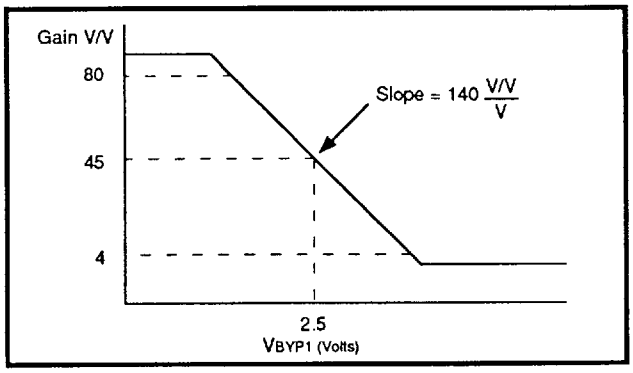


FIGURE 2: AGC Gain

The AGC amplifier has emitter follower outputs and can sink 4.0 mA.

One filter for both amplitude (DIN± input) and time (CIN± input) channels, or a separate filter for each may be used. If two filters are used, attention must be paid to time delays so that each channel is timed properly. A multi-pole Bessel filter is typically used for its linear phase or constant group delay characteristics.

In the amplitude channel the signal is sent to a hysteresis comparator. The hysteresis threshold level is set so that it will be tripped only by valid signal pulses and not by baseband noise. It can be a fixed level or a fraction of the DIN± voltage level.

The latter approach is accomplished by using an external filter/network between the LEVEL and HYS pins. This allows setting the AGC slow attack and decay times slow enough to minimize time channel distortion and setting a shorter time constant for the hysteresis level. The LEVEL pin output is a rectified and amplified version of DIN±, 1.0 Vpp at DIN± results in 1.0 Vop nominally, at the LEVEL pin. A voltage divider is used from LEVEL to ground to set the Hysteresis threshold at a percentage of the peak DIN± voltage. For example, if DIN± is 1.0 Vpp, then using an equal valued resistor divider will result in 0.5 Vop at the HYS pin. This will result in a nominal ±0.18V threshold or a 36% threshold of a ±0.5V DIN± input. The capacitor, from the LEVEL pin to GND, is chosen to set an appropriate time constant. This "feed forward" technique speeds up transient recovery by allowing qualification of the input pulses while the AGC is still settling. This helps in the two critical areas of write to read and head change recovery. Some care in the selection of the hysteresis level time constant must be exercised so as to not miss pattern (resolution) induced lower amplitude signals. Note that there is a built in 50mV threshold (ie., 10% of ±0.5V DIN± input) for level qualification even when the HYS pin is grounded. This is to prevent false triggering by baseband noise during a DC erase gap, (e.g., address mark). The output of the hysteresis comparator is the "D" input of a D-type flip-flop. The DOUT pin is a comparator output signal for testing purposes only. When testing, it requires an external 3-6 kΩ pull-down resistor to ground. If no testing is necessary, the DOUT pin can be pulled up to VPO (+5V) to save power.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes. It also requires an external 3-6 kΩ pull down resistor for testing.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from CIN± to the comparator input (not DIF±) is:

$$Av = \frac{-2000\,Cs}{LCs^2 + C(R+92)s + 1}$$

Where: C, L, R are external passive components
$20\ pF < C < 150\ pF$
$s = j\omega = j2\pi f$

OFF-CHIP DIFFERENTIATION

For constant desnity recording applications, a differentiation function with a low pass cut-off frequency tracking the data rate can maximize the signal-to-noise ratio performance. A time differentiated input can be applied at the CIN± pins, separated from the DIN1± pins. A 2 kΩ resistor should be placed across the DIF± pins in this case. This function can best be supported by the Silicon Systems programmable filters, such as the SSI 32F8020A and the SSI 32F8120A. The filters feature both a normal low pass output and a differentiated low pass output. The low pass cut-off frequency is programmable by the user to track the data rate. The signal delays of the two signal paths are well matched.

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the CIN± input. Two qualification modes exist to determine peaks. The first mode, qualification with pulse polarity hysteresis, (ENH = High), is exactly the same as the qualification on the SSI 32P541. In this mode, the D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak. In the second mode, qualification without pulse polarity hysteresis, (ENH = Low), the polarity of the peaks is ignored. In this mode, the D input to the flip-flop changes state whenever the DIN± input exceeds the threshold regardless of polarity. This is

FUNCTIONAL DESCRIPTION (Continued)

accomplished, (see Figure 3), by clocking the toggle flip-flop whenever the threshold is exceeded in either direction at the same time that the comparator detects a zero crossing. It may be advantageous to use this mode of pulse qualification for retrieving certain kinds of servo patterns.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched. The D flip-flop output triggers a one-shot that sets the $\overline{RD}$ output pulse width.

SERVO READ MODE

A position error signal (PES) is generated based on the relative amplitude of two servo signals, A and B. Rectified servo signal peaks are captured on hold capacitors at the HOLDA/B pins. This is accomplished by pulling $\overline{LATCHA}$ or $\overline{LATCHB}$ low for a sample period. Additionally, a default hold capacitor discharge current of 1.5 mA can be turned on by pulling $\overline{RSTA}$ or $\overline{RSTB}$ low. This default 1.5 mA discharge current can be modified by tying a resistor between CS and GND or VPA. A resistor to GND increases the discharge current, while a resistor to VPA decreases it. The equation for increasing the discharge current is:

$$Ics = 22.5V \cdot \left(\frac{15k + Rcs}{15k \cdot Rcs}\right), \quad Rcs \geq 15\ k\Omega$$

For decreasing the discharge current, the equation is:

$$Ics = 22.5V \cdot \left(\frac{Rcs - 22.5k}{15k \cdot Rcs}\right), \quad Rcs \geq 22.5\ k\Omega$$

Outputs BURSTA/B & PES are referenced to an external reference applied to the VREF pin.

In servo read mode (see Figure 4) the BYP2 pin is connected to the GAIN pin and the servo channel gain is determined by the read channel gain as controlled by the sum of the A and B amplitudes. In this case a current is sourced/sinked to/from the capacitor on the GAIN/BYP2 pin whenever the $\overline{HOLD2}$ pin is pulled high. The current magnitude and direction is determined by:

$$Ic = K_4[(K_5 \cdot V_{AGC2}) - Va(DIN)pp - Vb(DIN)pp]$$

Where:

V_{AGC2} = AGC2 pin voltage = 1.0V with pin open.

K_4 = 740 µA/Vpp

K_5 = 0.570 V/V

Va/b(DIN)pp = peak to peak A or B servo pattern signal voltages at DIN±

WRITE MODE

In Write Mode the SSI 32P3031 Pulse Detector section is disabled and preset for the following Read Mode. The digital circuitry is disabled, the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced to about 250Ω.

Holding the AGC amplifier gain and reducing input impedance shortens system Write to Read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 32P3031 and a head preamplifier such as the SSI 32R2020R. Write to read timing is controlled to maintain the reduced impedance for 0.9 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

MODE CONTROL

The device circuit mode is controlled by the ENABLE, R/W, AGCMODE, $\overline{HOLD1}$ and $\overline{HOLD2}$ pins a shown in Table 1.

Data Read Mode

AGC active and controlled by data, Digital section active.

Data Read Mode, Hold

AGC gain held constant, Digital section active. Gain will drift higher or lower at a rate determined by C_{BYP1} and Hold mode leakage current.

Servo Read Mode I (See Figures 4 & 5)

The BYP2 and GAIN pins are tied together. Read amplifier AGC control voltage developed from sum of Servo signal levels. $\overline{HOLD2}$ is toggled to update the control voltage after each Servo frame.

Calibrate Mode

A low level on $\overline{CALIBRATE}$ shall force $\overline{LATCHA}$ and $\overline{LATCHB}$ low and $\overline{RSTA}$ and $\overline{RSTB}$ high to measure the offset of the entire servo BURSTA, BURSTB, and PES channel.

Write

Read amplifier input impedance reduced. AGC gain held constant, $\overline{RD}$ stays high.

Power Down

Circuit switched to a low current disabled mode. Enable = TTL logic low.

Note: When AGCMODE is switched to a low state the voltage at the BYP1 pin will be held constant subject to Hold mode leakage current induced drift. So, when returning to Data Read Mode, the channel gain will be the same as it was prior to AGCMODE switching or slightly higher/lower.

TABLE 1: SSI 32P3031 Circuit Mode Control

ENABLE	R/$\overline{W}$	AGC MODE	$\overline{HOLD1}$	$\overline{HOLD2}$	READ PATH MODES
1	1	1	1	X	Data Read Mode
1	1	1	0	X	Data Read Mode Hold
1	1	0	X	1	Servo Read Mode - Sample
1	1	0	X	0	Servo Read Mode - Hold
1	0	X	X	X	Write
0	X	X	X	X	Power Down

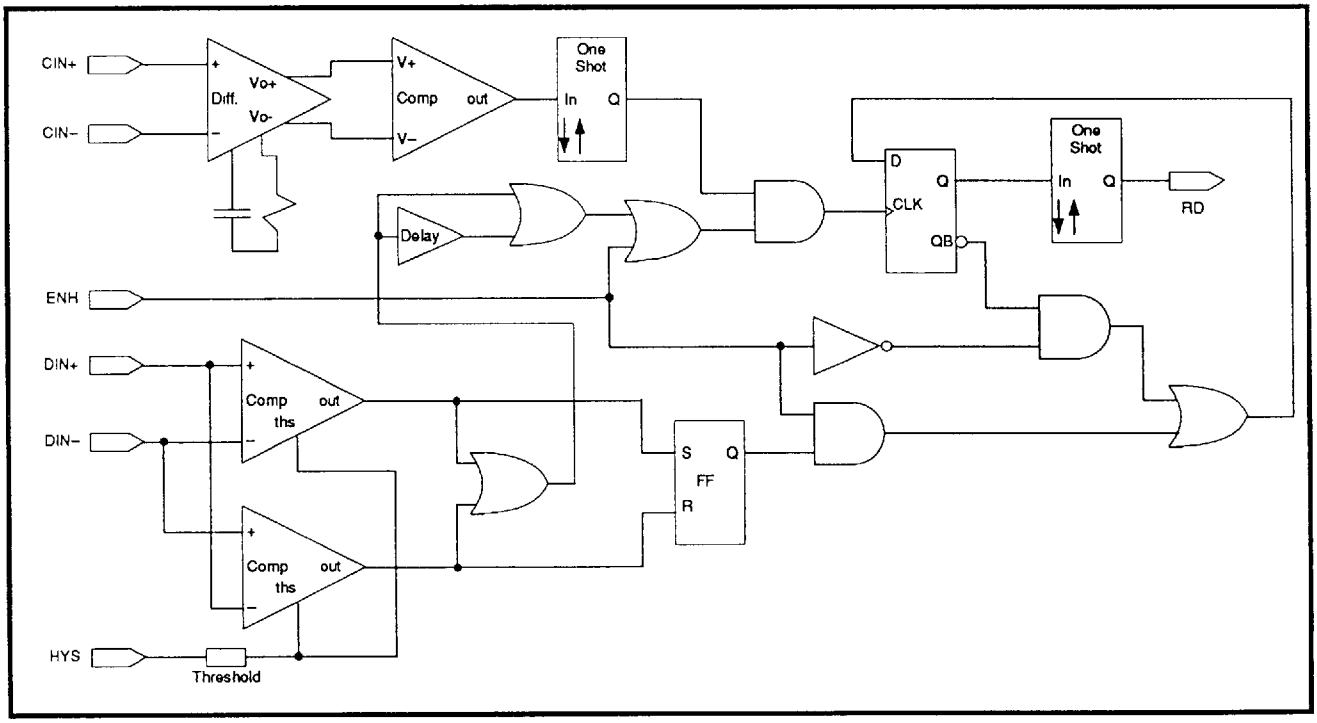


FIGURE 3: ENH Provides Two Pulse Qualification Modes.

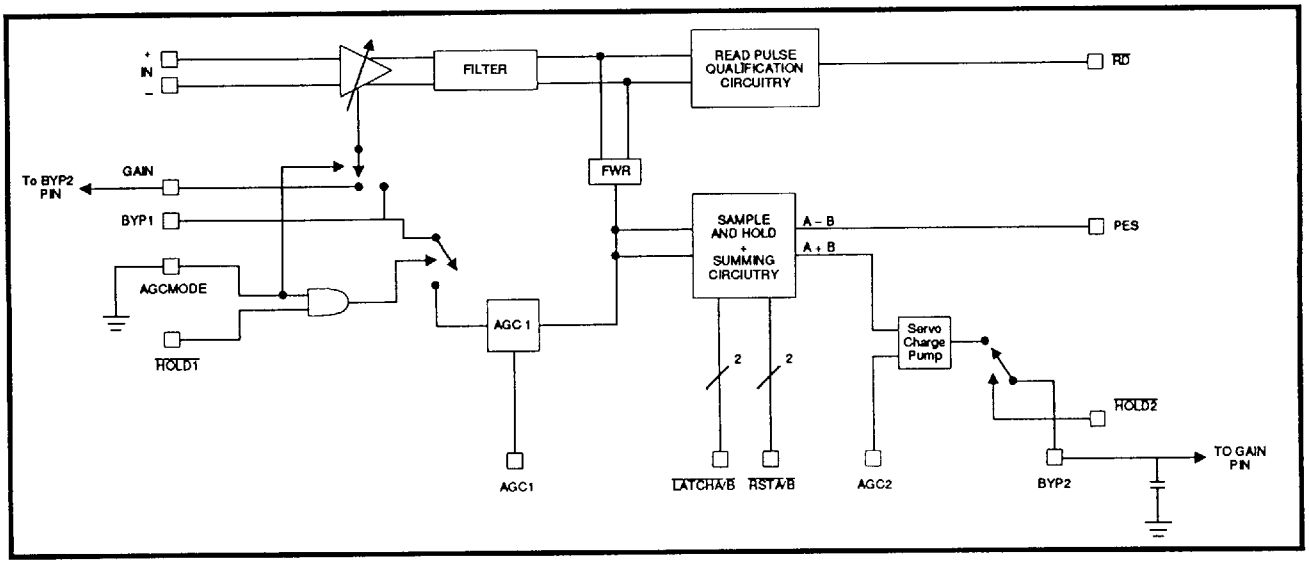


FIGURE 4: Servo Read Mode

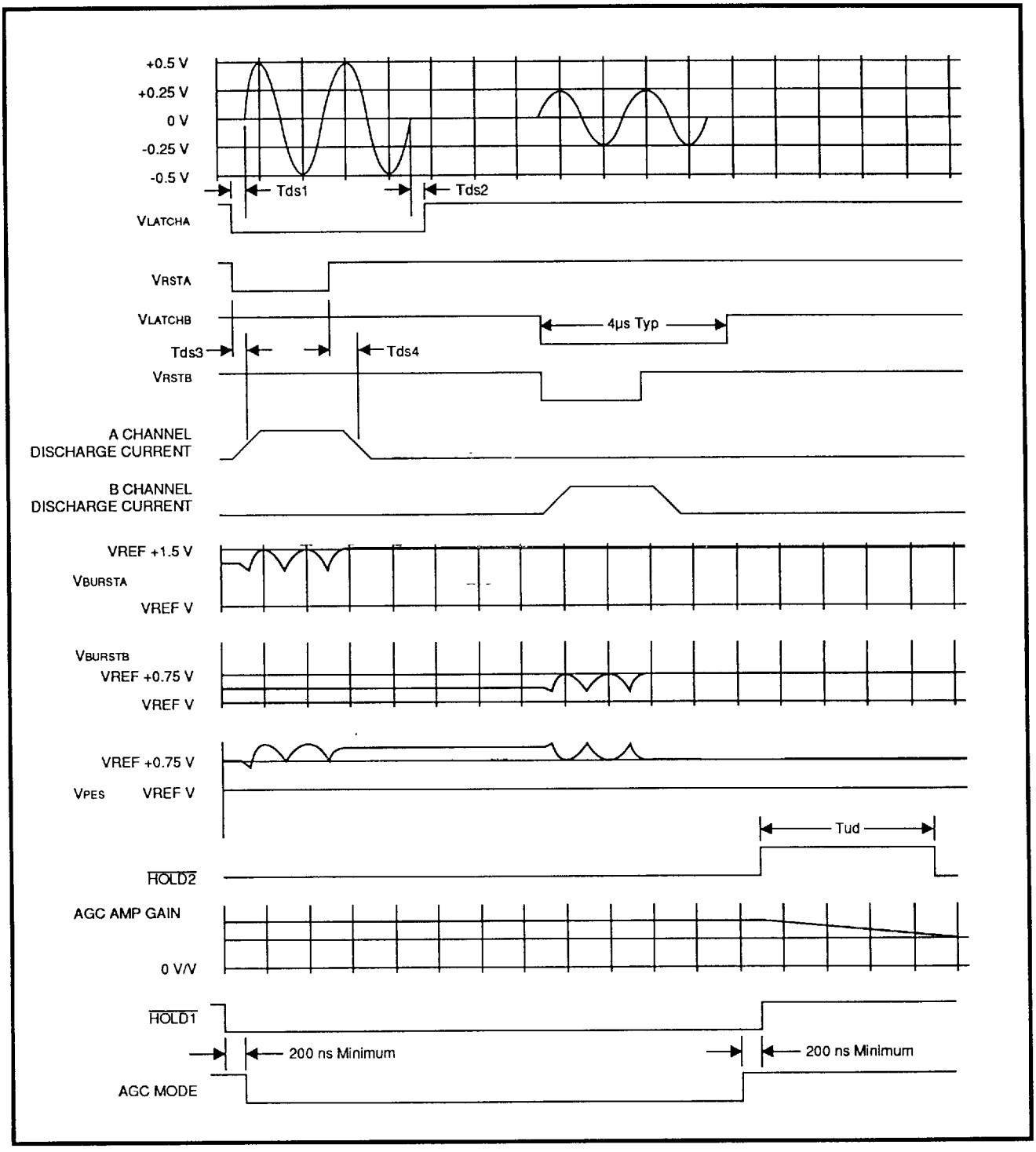


FIGURE 5: Servo Read Mode 1

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VPA	I	Analog (+5V) power supply for pulse detector.
AGND	I	Analog ground pin for pulse detector block.
VPD	I	Digital (+5V) supply pin for data synchronizer block.
DGND	I	Digital ground pin.
IN+, IN–	I	Analog signal input pins.
OUT+, OUT–	O	Read path AGC Amplifier output pins.
DIN+, DIN–	I	Analog input to the amplitude channel.
CIN+, CIN–	I	Analog input to the time channel.
DIF+, DIF–	I/O	Pins for external differentiating network. When off chip differentiation is used, a 2 kΩ resistor should be placed across DIF±.
COUT	O	Test point for monitoring the flip-flop clock input, pull-down resistor required. In normal operation, leave this pin open or tie to VPD to save power.
DOUT	O	Test point for monitoring the flip-flop D-input, pull-down resistor required. In normal operation, leave this pin open or tie to VPD to save power.
BYP1, BYP2	I/O	An AGC timing capacitor or network is tied between each pin and GND. BYP1 is for read data. BYP2 is for servo data.
AGC1, AGC2	I	Reference input voltage for the read data AGC loop (AGC1) and sampled servo AGC loop (AGC2).
LEVEL	O	Output from fullwave rectifier that may be used for input to the hysteresis comparator.
HYS	I	Hysteresis level setting input to the hysteresis comparator.
$\overline{\text{HOLD1}}$, $\overline{\text{HOLD2}}$	I	TTL compatible pin that holds the AGC gain when pulled low.
$\overline{\text{LATCHA}}$, $\overline{\text{LATCHB}}$	I	TTL compatible inputs that switch channel A or B into peak acquisition mode when low.
$\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$	I	TTL compatible input that enables the discharge of channels A & B hold capacitors when held low.
CS	I	Hold capacitor discharge current magnitude is controlled by a resistor from this pin to GND or VPA. If left open the default current is 1.5 mA.
HOLDA, HOLDB	I/O	Peak holding capacitors are tied from each of these pins to AGND.
VREF	O	Reference voltage for Servo outputs.
BURSTA, BURSTB	O	Buffered hold capacitor voltage outputs.
PES	O	Position error signal, A minus B output.
R/$\overline{\text{W}}$	I	TTL compatible Read/Write control pin. A low input selects write mode.
Enable	I	TTL compatible power up control. A low input selects a low power state.
AGCMODE	I	TTL compatible pin that selects the AGC loop control input. A high selects BYP1, a low selects GAIN.
Gain	I	A voltage at the pin may be used to control AGC gain.
$\overline{\text{RD}}$	O	TTL compatible read output, a falling edge corresponds to a detected peak.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{CALIBRATE}}$	I	Used to measure servo offset.
ENH	I	TTL compatible pulse qualification control pin. A low input selects modes which ignore polarity of peaks.

ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING
5V Supply Voltage, VPA, VPD	6.5V
Pin Voltage (Analog pins)	0.3 to VPA + 0.3V
Pin Voltage (Digital pins)	0.3 to VPD + 0.3V or +12 mA
Storage Temperature	-65 to 150°C
Lead Temperature (Soldering 10 sec.)	260°C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage (VPA, VPD)			4.5	5.0	5.5	V
Junction Temperature	Tj		-		135	°C
Ambient Temperature	Ta	ENABLE = High or Low	0		80	°C

POWER SUPPLY

IVCC1,2	Supply Current	Outputs unloaded; ENABLE = high or open		40	55	mA
Pd	Power dissipation	Ta = 25°C, outputs unloaded		200	300	mW
		ENABLE = Low		2.8		mW

LOGIC SIGNALS

VIL	Input Low Voltage		-0.3		0.8	V
VIH	Input High Voltage		2.0		VCC+0.3	V
IIL	Input Low Current	VIL = 0.4V	-0.4		-0.4	mA
IIH	Input High Current	VIH = 2.4V			100	µA
VOL	Output Low Voltage	IOL = 4.0 mA			0.5	V
VOH	Output High Voltage	IOH = -400 µA	2.4			V

ELECTRICAL SPECIFICATIONS (continued)

MODE CONTROL

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Enable off to on Transition Time	Settling time of external capacitors not included, ENABLE pin transitions from low to high		8	20	µs
Read to Write Transition Time	R/$\overline{W}$ pin transitions from high to low		0.12	1.0	µs
Write to Read Transition Time	R/W pin transitions from low to high AGC setting not included	0.4	0.9	1.6	µs
AGC mode off to on transition time	AGC mode pin transitions from low to high		0.3	2.0	µs
$\overline{HOLD1}$ ON to/from $\overline{HOLD1}$ OFF transition time	$\overline{HOLD1}$ pin transitions from low to high		0.12	1.0	µs
$\overline{HOLD2}$ ON to/from $\overline{HOLD2}$ OFF	$\overline{HOLD2}$ pin transitions from low to high		0.16	1.0	µs

READ MODE (R/W is High)

AGC Amplifier

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN±. OUT± are loaded differentially with 800Ω, and each side is loaded with < 10 pF to AGND, and AC coupled to DIN±. A 900 pF capacitor is connected between BYP1/BYP2 and AGND. An 1100 pF capacitor is connected between BYP1/BYP2 and VPA. AGC1/AGC2 pin is open.

Minimum Gain Range	1.0 Vp-p ≤ (OUT+) - (OUT-) ≤ 2.6 Vp-p	4		80	V/V
AGC Input Range		25		250	mVpp
Output Offset Voltage Variation	Over entire gain range	-500		+500	mV
Maximum Output	Set by BYP1 pin Voltage Swing	2.6	3.0		Vpp
Differential Input Resistance	(IN+) - (IN-) = 100 mVp-p @ 2.5 MHz	4	5.4	7.5	kΩ
Differential Input Capacitance	(IN+) - (IN-) = 100 mVp-p @ 2.5 MHz		4	10	pF
Single-Ended Input Impedance	R/$\overline{W}$ = high, IN+ or IN-	2	2.7	3.8	kΩ
	R/$\overline{W}$ = low, IN+ or IN-		160	250	Ω
Input Noise Voltage	Gain set to maximum, RS = 0, BW = 15 MHz		7	15	nV/√Hz
Bandwidth	-3 dB bandwidth at maximum gain	30	53		MHz

AGC Amplifier (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
OUT+ & OUT- Pin Current	No DC path to AGND	±2.5	±4.0		mA
CMRR (Input Referred)	IN± = 0 VDC + 100 mVp-p @ 5 MHz, gain set to max	40	75		dB
PSRR (Input Referred)	100 mVp-p on VPA, VPD @ 5 MHz gain set to max	30	55		dB
(DIN+) - (DIN-) Input Swing vs. AGC1 Input — Slope	25 mVp-p ≤ (IN+) - (IN-) ≤ 250 mVp-p, $\overline{HOLD}$ = high,		0.8		Vp-p/V
(DIN+) - (DIN-) Input Swing vs. AGC1 Input — Intercept	0.5 Vp-p ≤ (DIN+) - (DIN-) ≤ 1.5 Vp-p		0.163		V
(DIN+) - (DIN-) Input Voltage Swing Variation	25 mVp-p ≤ (IN+) - (IN-) ≤ 250 mVp-p			5.0	%
AGC1 Voltage	AGC1 open	0.8	1.0	1.2	V
AGC1 Pin Input Impedance		4.8	7.8	9.5	kΩ
Slow AGC Discharge Current	(DIN+) - (DIN-) = 0V	2.8	4.5	6.5	µA
Fast AGC Discharge Current	Starts at 0.9 µs after R/$\overline{W}$ goes high, stops at 1.8 µs	0.07	0.12	0.18	mA
BYP1 Leakage Current	$\overline{HOLD1}$ = low, 10 ≤ Gain ≤ 80	-0.2		+0.2	µA
Gain Pin Leakage Current	$\overline{HOLD2}$ = low, 10 ≤ Gain ≤ 80	-0.2		+0.2	µA
Slow AGC Charge Current	(DIN+) - (DIN-) = .563 VDC, V_{AGC1} = 2.3 V	-0.11	-0.18	-0.27	mA
Fast AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, V_{AGC1} = 2.3 V	-0.9	-1.4	-2.1	mA
Fast to Slow Attack Switchover Point	$\frac{[(DIN+) - (DIN-)]}{[(DIN+) - (DIN-)]\ FINAL}$	110		140	%
Gain Decay Time (Td)	(IN+) - (IN-) = 250 mVp-p to 125 mVp-p @ 2.5 MHz, (OUT+) - (OUT-) to 90% final value	12	20	36	µs
	(IN+) - (IN-) = 50 mVp-p to 25 mVp-p at 2.5 MHz (OUT+) - (OUT-) to 90% final value	38	60	110	ms
Gain Attack Time	R/$\overline{W}$ low to high (IN+) - (IN-) = 250 mVp-p @ 2.5 MHz, (OUT+) - (OUT-) to 110% final value	.8	2	3.6	µs

ELECTRICAL SPECIFICATIONS (continued)

READ MODE

Hysteresis Comparator

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC coupled, 1.0 Vp-p, 2.5 MHz sine wave. 0.5 VDC is applied to the HYS pin. R/W pin is high.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vp-p
Differential Input Resistance	(DIN+) - (DIN-) = 100 mVp-p @ 2.5 MHz	8	10	14	kΩ
Differential Input Capacitance	(DIN+) - (DIN-) = 100 mVp-p @ 2.5 MHz		3.0	5.0	pF
Single-Ended Input Impedance	DIN+ or DIN-	4	5	7	kΩ
Slope of Level Gain	Calculated from 0.6 < DIN± < 1.5 Vppd	0.70	0.85	1.0	V/Vp-p
Intercept of Level Gain	DIN± = 0 Vppd	0	0.30	0.50	V
Level Gain		Slope + (Intercept / DIN ppd)			
Level Pin Output Impedance	I_{LEVEL} = 0.2 mA	100	200	300	Ω
Level pin Maximum Output Current		1.5			mA
Slope of Hysteresis Gain	Calculated from 0.3V < HYS < 1.0V	0.32	0.36	0.44	V/V
Intercept of Hysteresis Gain	HYS = 0	-0.04	-0.025	0	V
Hysteresis Gain		Slope + (Intercept / HYS Voltage)			
HYS Pin Current	0.3V < HYS < 1.0V	0.0		-5	µA
Tracking Hysteresis Threshold Tolerance		-15		+15	%
DOUT Pin Output Low Voltage	5 kW from DOUT to GND	VCC -2.5	VCC -2.0	VCC -1.35	V
DOUT Pin Output High Voltage	5 kW from DOUT to GND	VCC -2.0	VCC -1.6	VCC -1.1	V

Active Differentiator

Unless otherwise specified, recommended operating conditions apply. Input (CIN+) - (CIN-) is an AC-coupled, 1.0 Vp-p, 2.5 MHz sine wave. 100W in series with 65 pF are tied from DIF+ to DIF-.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vp-p
Differential Input Resistance	(CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz	8	10	14	kΩ
Differential Input Capacitance	(CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz		3.0	5.0	pF
Single-Ended Input Impedance	CIN+ or CIN-	4	5	7	kΩ
Voltage Gain From CIN± to DIF±	2 kΩ across DIF+		1		V/V
DIF+ to DIF- Pin Current	Differentiator impedance must be set so as to not clip the signal for this current level	-0.7		+0.7	mA
COUT Pin Output Low Voltage	5 kΩ from COUT to GND	VCC -2.5	VCC -2.0	VCC -1.35	V
COUT Pin Output High Voltage	5 kΩ from COUT to GND	VCC -2.0	VCC -1.6	VCC -1.1	V
COUT Pin Output Pulse Width		22	35	52	ns

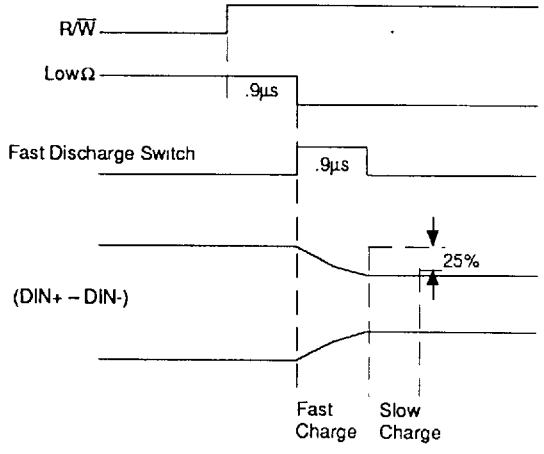


Figure A: AGC Attack Sequence

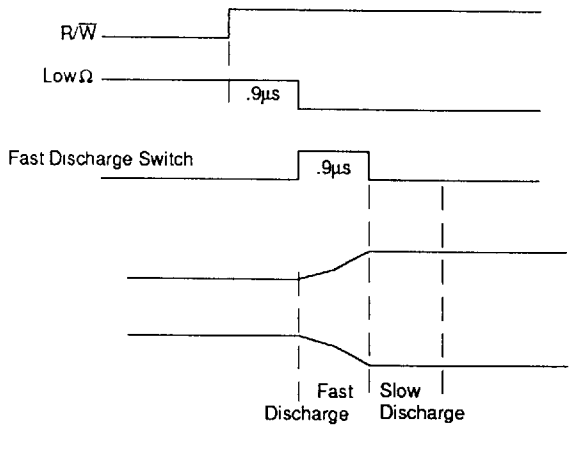


Figure B: AGC Decay Sequence

FIGURE 6: AGC Timing Diagram

ELECTRICAL SPECIFICATIONS (continued)

READ MODE (continued)

Output Data Characteristics (See Figure 7)

Unless otherwise specified, recommended operating conditions apply. Inputs (CIN+) - (CIN-) and (DIN+) - (DIN-) are in-place as an AC coupled, 1.0 Vp-p, 2.5 MHz sine wave. 100W in series with 65 pF are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin. $\overline{RD}$ is loaded with a 4 kΩ resistor to VCC and a 10 pF capacitor to DGND. ENABLE and R/$\overline{W}$ pins are high.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Td1	D Flip-Flop Set Up Time	Minimum allowable time delay from (DIN+) - (DIN-) exceeding hysteresis point to (DIF+) - (DIF-) hitting a peak value.	0			ns
Td3	Propagation Delay	From positive peak to $\overline{RD}$		13	40	ns
Td4	Propagation Delay	From negative peak to $\overline{RD}$		13	40	ns
|Td3-Td4|	Pulse Pairing	2.5 MHz sine wave input			1.5	ns
|Td3-Td4|	Pulse Pairing	4 MHz sine wave input			1.0	ns
Td5	Output Pulse Width		22	35	52	ns

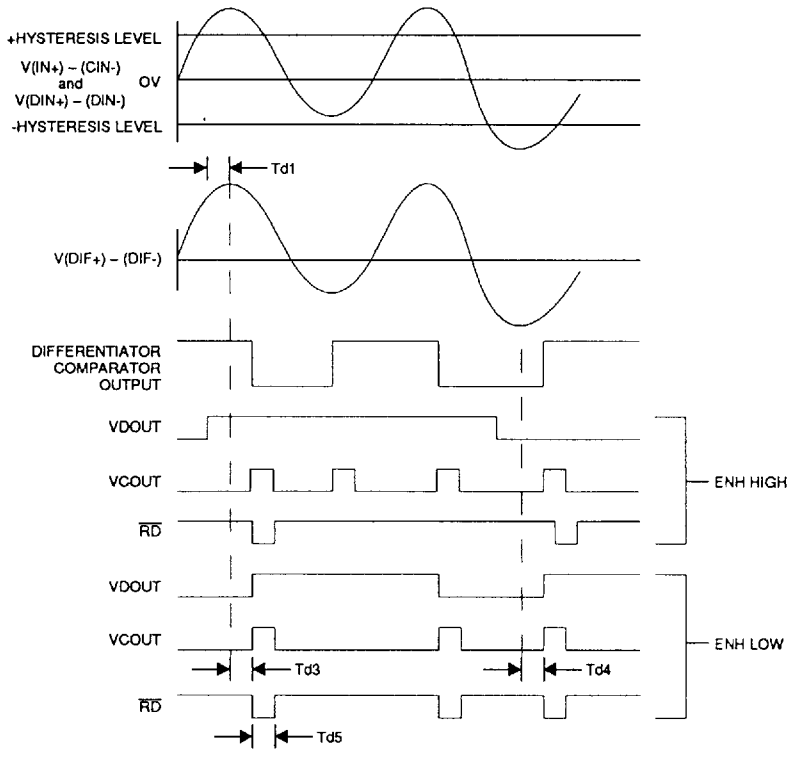


FIGURE 7: Read Mode Digital Section Timing Diagram

Servo Section
(Unless otherwise specified, recommended operating conditions apply.), LATCH A/B = Low, RST A/B = High, CS Pin Open

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VREF Voltage Range		2.25	2.5	2.75	V
VREF Pin Input Impedance		30			kΩ
AGC2 Pin Voltage	AGC2 Pin Open,	0.8	1.0	1.2	V
AGC2 Pin Input Impedance		4.8	6.5	9.5	kΩ
BURSTA/B pin Output Voltage vs (DIN+) – (DIN-)	$\overline{LATCHA/B}$ = Low	-20		+10	%
BURSTv A/B Output Offset Voltage V_{BURST} - VREF	I(HOLDA) = I(HOLDB) =-20 µA, $\overline{LATCHA}$, $\overline{B}$ = Low CS pin open (DIN+) = (DIN-)	-150		+150	mV
BURSTA - BURSTB Output Offset Match	$\overline{LATCHA/B}$ = low (DIN+) = (DIN-)	-15		+15	mV
Maximum PES Pin Output Voltage	Controlled by AGC2			VCC1-1.5	Vpp
PES Pin Output Offset Voltage	VPES - VREF, (DIN+) = (DIN-) $\overline{LATCHA/B}$ = Low	-15		+15	mV
Output Resistance, BURSTA/B & PES pins	ILOAD ± 500 µA			50	Ω
Hold A/B Charge Current	$\overline{LATCHA/B}$ = Low	8			mA
HOLDA/B Discharge Current Tolerance	$\overline{RSTA/B}$ = Low, CS pin open	0.8	1.5	2.2	mA
	$\overline{RSTA/B}$ = High, $\overline{LATCHA/B}$ = High	-0.2		+0.2	µA
Load Resistance BURSTA/B, PES pins	Resistors to GND	10.0			kΩ
Load Capacitance BURSTA/B, PES pins				20	pF
$\overline{LATCHA/B}$ pin set up time	(Tds1 in Figure 5)	150			ns
$\overline{LATCHA/B}$ pin Hold Time	(Tds2 in Figure 5)	150			ns
Channel A/B Discharge Current Turn On time	(Tds3 in Figure 5)			150	ns
Channel A/B discharge Current Turn Off time	(Tds4 in Figure 5)			150	ns
BYP2 Pin Leakage Current	$\overline{HOLD2}$ = Low	-0.2		+0.2	mA

ELECTRICAL SPECIFICATIONS (continued)

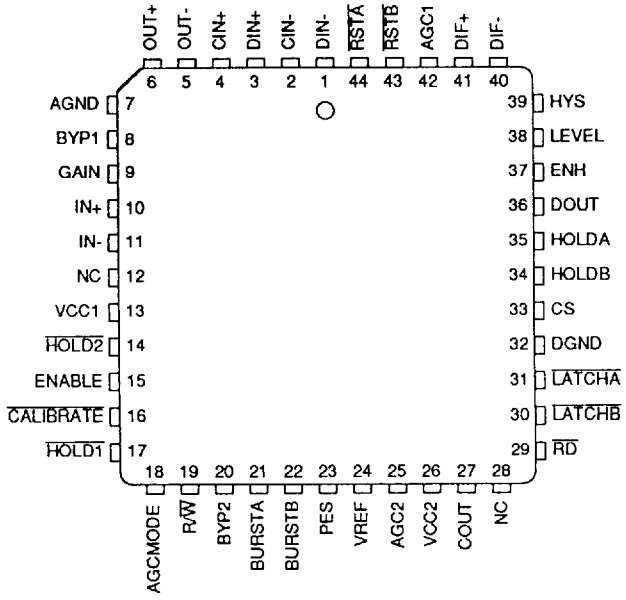
READ MODE (continued)

Servo Section (continued)

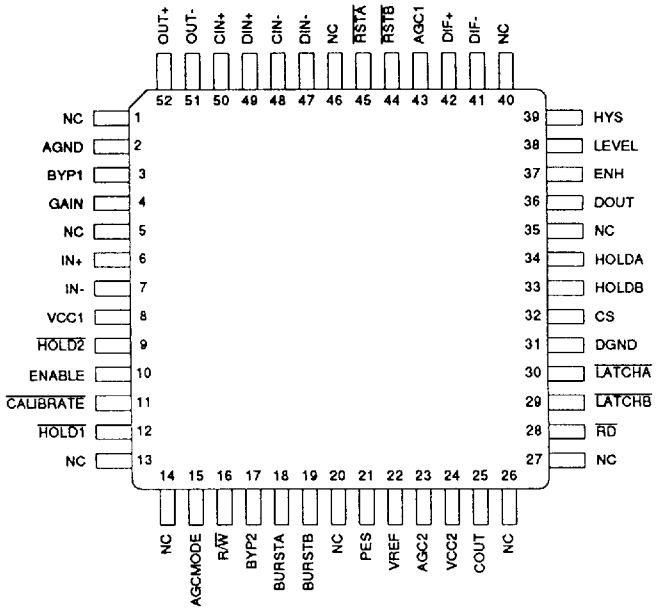
PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
BYP2 Pin Charge/Discharge Current	K4, $\overline{HOLD2}$ = High	570	735	900	µA/Vpp
Ic = K4[(K5 • VAGC2) – $V_{A(DIN)}$pp - $V_{B(DIN)}$pp]	K5, $\overline{HOLD2}$ = High	0.4	0.57	0.7	V/V
Maximum BYP2 pin charge/discharge current		190	300	450	µA
V_{PES} pp vs. V_{AGC2}	V_{PES} pp/V_{AGC2}	2.35	2.55	2.75	Vpp/V
	V_{PES} pp Swing AGC2 = Open	2.4	3	3.6	Vpp

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



44-Pin PLCC



52-Lead QFP

THERMAL CHARACTERISTICS: θja

44-Pin PLCC	60° C/W
52-Lead QFP	75° C/W

ORDERING INFORMATION

PART DESCRIPTION		ORDER NO.	PKG. MARK
SSI 32P3031	44-Pin PLCC	32P3031-CH	32P3031-CH
	52-Lead QFP	32P3031-CG	32P3031-CG

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714)573-6000, FAX (714) 573-6914