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SSI 32H6812
Servo & Spindle Driver with Shock Detection

Advance Information

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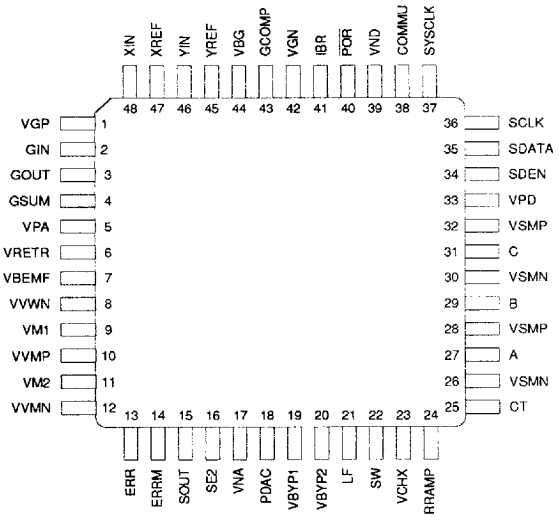
DESCRIPTION

The 32H6812 Servo/MSC Driver, a CMOS monolithic integrated circuit housed in a 48-lead TQFP package, operates from a single 5V supply. It provides a fully integrated servo driver and a spindle motor speed controller with internal power FETs. The servo driver is intended for use in disk drive head positioning systems employing linear or rotary voice coil motors. The spindle driver in conjunction with a microprocessor (μP) or digital signal processor (DSP), provides a complete spindle motor speed control system. It also includes one 10-bit D/A converter, a serial interface compatible with commonly used μP or DSP, and power fault circuitry. The device is ideal for use in 5V small form-factor disk drive applications and is available in a 48-Lead TQFP package.

FEATURES

- **48-lead TQPF package**
- **Internal 1A servo driver with no deadband, class-B output**
- **Power fault detection with built-in retract circuitry**
- **10-bit VCM D/A converter with 4 μs digital delay**
- **Internal precision voltage reference**
- **Programmable commutation delay for optimal motor efficiency**
- **Closed loop speed control at 5400 rpm**
- **Internal 1A spindle driver**
- **Serial interface compatible with Intel 80C196 and Motorola 68HC16**
- **Low power CMOS design with Sleep mode**
- **Internal shock detection circuitry**

PIN DIAGRAM



48-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

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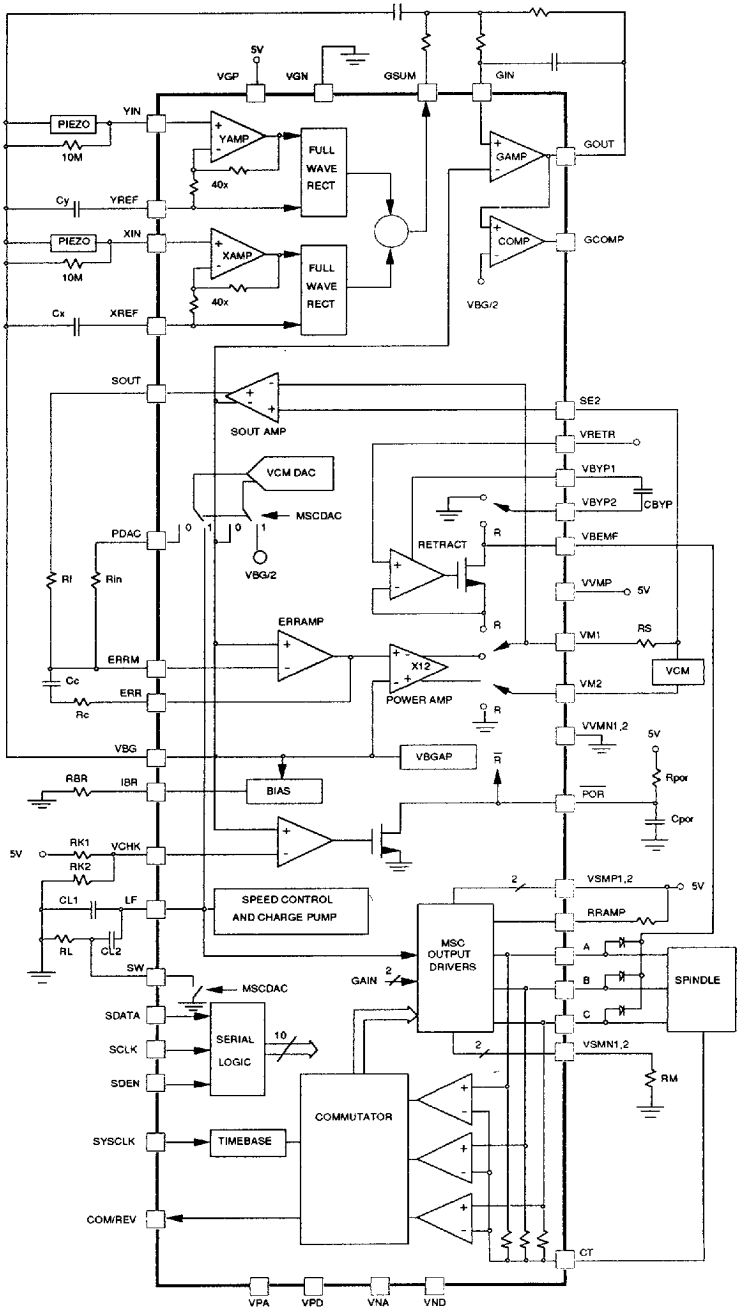
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

As shown in the block diagram, the 32H6812 can be divided into four major sections: servo positioner, spindle motor speed controller/driver, control circuitry and serial interface port.

SERVO POSITIONER

The servo positioner is a power transconductance amplifier for use in driving a voice coil servo motor (VCM). It has two primary modes of operation, normal (or linear) and retract. The retract mode is activated by a power supply failure or when $\overline{\text{RETR}}$ bit is asserted low with $\overline{\text{BRAKE}}$ (bit) being high. Otherwise the device operates in linear mode. The servo positioner consists of SOUT amplifier, ERR amplifier, retract amplifier, power amplifier and 10-bit VCM D/A converter.

SOUT Amplifier

The SOUT amplifier generates a voltage at SOUT proportional to positioner current, by sensing the voltage across an external resistor Rs, amplifying it and referencing it to VBG. Since the common mode voltage on Rs can range over the full power supply, while the differential voltage is in the order of millivolts, the SOUT amplifier is realized with high input common mode rejection and low input offset.

ERR Amplifier

The ERR amplifier is a high gain op amp. Due to the fixed gain of the power amp, ERR is proportional to the VCM voltage. The negative input of this amplifier is the system summing junction for the currents which are proportional to the desired VCM current, the measured VCM current, and the VCM voltage.

Power Amplifier

The power amplifier is a fixed gain voltage amplifier with differential inputs and outputs. Its input is the differential voltage between ERR and VBG. Its output drives the VCM directly through an internal NMOS bridge. An internal charge pump generates gate voltages higher than VVMP so the upper NMOS devices can drive VM1 and VM2 up to VVMP.

Retract Amplifier

When a voltage fault is sensed, or when $\overline{\text{RETR}}$ bit is asserted low while $\overline{\text{BRAKE}}$ bit is high, the servo positioner enters into Retract mode. In this mode, it is assumed that no current is available for VVMP. Thus power for this mode comes from VBEMF, the rectified spindle back emf voltage, and from VBYP1, a voltage generated from the external storage capacitor CBYP. The retract amplifier is powered by VBYP1. It senses the voltage at VRETR and, through a power NMOS source follower, raises VM1 to VRETR. The drain of the source follower is VBEMF.

VCM D/A Converter

Switched-capacitor circuitry is employed to implement the VCM D/A converter with two non-overlapped clock phases, one phase for auto-zeroing and another one for evaluation. These two phases run synchronously with an internal 500 KHz clock, which is derived directly from the system clock at SYSCLK.

The request of the VCM D/A converter is initiated by writing to the VCM D/A register (00) through the serial interface port. The input data word must be coded in two's complement form. Note that there would be a maximum of 2 µs of latency between a conversion request and the actual start of conversion. The conversion delay from the actual start of conversion to when the analog output begins to slew to a new value is 2 µs. Therefore a maximum of 4 µs is required for a conversion, in addition to the time needed for completion of a serial data transfer, which is equal to 16/SCLK.

When MSCDAC bit in the MSC_MODE register is low (default), VCM D/A converter output is provided at PDAC and is referenced to VBG. VBG also serves as a reference voltage for the error amplifier and the current sense amplifier. If MSCDAC bit is asserted high, D/A converter output will be switched to LF pin and referenced to VBG/2.

SPINDLE MOTOR SPEED CONTROLLER/DRIVER (CONTINUED)

The spindle motor speed controller in conjunction with a µP or DSP and external components provides the motor driving capability for starting, accelerating and rotational speed regulation for brushless DC motors without the need for Hall sensors.

SPINDLE MOTOR START-UP

Typical spindle motor start-up is accomplished with a companion µP. The commutation counter and the period counter can be initiated at power on or at START bit (MSC_MODE bit 6) rising edge. START bit should be held high during start-up to mask false commutation due to transient on the motor coils (A, B, C). STANDBY bit (CONT_MODE bit 2) can then be asserted to high along with $\overline{RETR}$ = $\overline{BRAKE}$ = 1 (this is Standby mode, see Table 2) to activate the spindle drivers and align the motor to start-up position (state 0). Each ADVANCE bit (MSC_MODE bit 0) rising edge will advance the motor to next commutation state (see Table 1).

When the motor achieves sufficient speed to generate adequate back EMF voltage, ADVANCE and START bits are reset by the µP. The motor will then continue to accelerate using the internal commutation delay selected by the DELAY bits (MSC_MODE bits 4 and 5).

To set the motor start-up current, MSCDAC bit (MSC_MODE bit 7) should be asserted to high. The transconductance amplifier input LF will then be provided from the VCM D/A converter. By programming VCM DAC and sense amplifier gain (GAIN0,1 bits in MSC_MODE), motor start-up current will be:

$$I_{Motor} = \frac{V_{LF}}{R_{Sense}} \cdot \text{Gain}$$

where voltage at LF pin will be precharged to the DAC output voltage. For fast precharging, external LF resistor (RL in Fig. 1) will also be shorted to ground through the SW pin.

Table 1: Commutation States

STATE	COMMU	PULLDOWNS			PULLUPS		
		A	B	C	A	B	C
0	0	OFF	ON	OFF	ON	OFF	OFF
1	1	OFF	OFF	ON	ON	OFF	OFF
2	0	OFF	OFF	ON	OFF	ON	OFF
3	1	ON	OFF	OFF	OFF	ON	OFF
4	0	ON	OFF	OFF	OFF	OFF	ON
5	1	OFF	ON	OFF	OFF	OFF	ON

SPINDLE MOTOR SPEED REGULATION

The motor speed regulation loop consists of a period counter, speed error detector, charge pump, loop filter and transconductance loop; as well as a commutator to determine the sequential switching of driver current to the motor winding.

Period Counter

A 500 kHz period counter starts with counts 5555 (5400.54 rpm) at the beginning of each revolution and counts down. Period resolution is therefore 2 µs. The counter resets at the end of each revolution.

Speed Error Detector

The speed error detector measures the difference between each motor revolution (8-pole or 12-pole selected by POLE in MSC_MODE bit 3) and the period counter and feeds this speed error to the charge pump circuit. When speed error is within ±32 µs (15.55 rpm) the motor is in "LOCK." The LOCK condition can be monitored on COM/REV pin by setting CRL0 = 0 and CRL1 = 1 (MSC_MODE bits 8 and 9). A logic HIGH on COM/REV pin then indicates motor speed is in LOCK.

If the speed error exceeds 1024 µs (497.66 rpm) too slow, the TOOSLOW condition can be monitored on COM/REV pin by setting CRL0 = 1 and CRL1 = 1. A logic HIGH on COM/REV pin will then indicate motor speed is too slow.

Charge Pump

A constant current source of 60 µA is used to charge or discharge for a 2 µs time multiple determined by the pulse-width modulation of the speed error. When the motor speed error exceeds 1024 µs too fast, the charge pump will discharge the LF pin for the whole period.

When the MSCDAC bit is asserted to high, the charge pump is disabled. LF voltage will then be provided from the VCM D/A converter. If the MSCDAC bit is low (default) and the speed regulation loop is activated, LF voltage will be limited to VBG to avoid excess current on the drivers. Since leakage current on LF pin can introduce speed error, leakage current on LF pin is limited to within 60 nA in order to achieve the highest speed accuracy.

Loop Filter

An external RC lowpass filter must be connected at the LF pin. LF also serves as the input to the transconductance amplifier. When the MSCDAC bit is asserted high during start-up and acceleration, external resistor RL is shorted to ground and the VCM D/A converter will be used to precharge the external capacitors at the LF pin, and thus set the motor start current.

Transconductance Loop

Input pin LF is the non-inverting input of a transconductance amplifier, which uses the lower driver transistor that is presently active per the commutation state, as the power driver element. An external resistor is used to sense the motor coil current. The voltage across the sense resistor is amplified by a gain stage (Gain = 5, 10, 20 or 30 selected by the GAIN bits in the MSC_MODE register) and fed to the inverting input of the transconductance amplifier.

The output pins A, B and C are intended to drive motor coils directly. The output drivers operate to reduce switching noise transients by limiting dv/dt during commutation. Each output consists of two N-channel MOSFET drivers, one for pullup to VSMP1 or VSMP2 and one for pulldown to VSMN1 or VSMN2. The pullup FET functions as a switch with voltage rise and fall times of about 25 microseconds. The pulldown FET is a part of the transconductance amplifier which converts the voltage LF into motor current (Imotor = VLF/(RSENSE • Gain)). When the pulldown output is commutating to the off state, dv/dt on the respective pin is controlled such that dv/dt is approximately 15/RRAMP volts per µs, where RRAMP is measured in kΩ.

SPINDLE MOTOR
SPEED REGULATION (CONTINUED)
Commutator

Motor armature position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back EMF from the coil, in conjunction with the state of the output drivers, indicates the armature position. The back EMF is compared with a reference at center tap and initiates commutation "events" when the appropriate comparison is made. Because the back EMF comparison event occurs prior to the time when optimum commutation should occur, it is preferred to delay commutation by a predetermined time after the comparison. There are two modes of commutation delay: adaptive and fixed delay. These are selected via the DELAY bits in the MSC_MODE register. In adaptive mode (default), the commutation delay is provided by a circuit which measures the interval between comparison events and delays commutation by a time equal to 3/7 of the prior measured interval. The circuit is adaptive and will provide the optimum delay for a wide range of motor speeds (-80% to 50% of the nominal value). Since the commutation of motor coils typically causes transients, the commutation delay circuit also provides a noise blanking function which prevents the circuit from responding to back EMF comparison events for a period of time equal to the greater of 5/7 of the interval between events or 64 µs after the comparison event. In fixed delay mode, a fixed delay and noise blank is provided. A longer fixed delay might be desirable during start-up to prevent the device from adapting to high frequency noise. The commutation table is shown in Table 1.

CONTROL CIRCUITRY

The control circuitry consists of a power fault detector, a shock detection circuit, and control logic.

The voltage fault detector monitors the system power supply VCC to prevent the VCM driver from responding to a false command during a power failure. The system power supply is applied at VCHK through an external resistor divider and compared with an internal voltage reference at VBG. Hysteresis is generated internally at the VCHK comparator. When a power fault is sensed, even for a brief power drop, $\overline{POR}$ pin will be pulled low regardless of the capacitance loading. Retract mode is activated during power fault.

Three power saving modes are provided, "Sleep," "Standby" and "Shockslp," along with three operating modes. All are selected with $\overline{RETR}$, $\overline{BRAKE}$, STANDBY, and SHOCKSLP bits per Table 2. With $\overline{RETR}$ and $\overline{BRAKE}$ low, both the VCM drivers and MSC drivers are in a high impedance state, and analog circuits are de-biased; this is the "Sleep" mode. With $\overline{RETR}$ and $\overline{BRAKE}$ high, and STANDBY high, MSC section is biased with spindle drivers activated; this is the "Standby" mode. With $\overline{RETR}$ low, $\overline{BRAKE}$ high, both VCM and MSC drivers are in a high impedance state, and the retract amplifier is activated and powered by the back EMF of a spinning motor for retracting heads. With $\overline{BRAKE}$ low, and $\overline{RETR}$ high, the VCM drivers are in a high impedance state, the MSC driver outputs are low impedance to ground (without current limiting), and the analog circuits are biased. Run mode occurs when $\overline{RETR}$ and $\overline{BRAKE}$ bits are high and STANDBY and SHOCKSLP bits are low.

A 2-axis shock detection circuitry is implemented to sense the shock signal at XIN and YIN pins. The shock signal across XIN, XREF pins (and YIN, YREF pins) is amplified and full-wave rectified and then summed with the other axis component at GSUM. This signal then goes through a lowpass filter and is compared to VBG/2. When SHOCKSLP is high, the shock detection circuitry is turned off; this is "SHOCKSLP" mode.

TABLE 2: Power Management/Operation Modes

MODE	$\overline{POR}$	$\overline{RETR}$	$\overline{BRAKE}$	STAND-BY	SHOCK-SLP	VCM ANALOG	SPM ANALOG	VCM DRIVER	SPM DRIVER	SHOCK DETECTION
FAULT	0	X	X	X	X	OFF	OFF	RETRACT	FLOAT	OFF
SLEEP	1	0	0	X	X	OFF	OFF	FLOAT	FLOAT	OFF
STANDBY	1	1	1	1	0/1	OFF	ON	FLOAT	ACTIVE	ON/OFF
RUN	1	1	1	0	0/1	ON	ON	ACTIVE	ACTIVE	ON/OFF
RETRACT	1	0	1	X	0/1	ON	ON	RETRACT	FLOAT	ON/OFF
BRAKE	1	1	0	X	0/1	ON	ON	FLOAT	LOW Z	ON/OFF

NOTE: During Power Fault and Sleep mode, all circuitry on chip will sleep, including the whole shock detection circuit. In modes other than Fault and Sleep, the shock detection circuit can be turned partially off (X, Y AMP will remain ON) with SHOCKSLP.

REGISTER DESCRIPTION

SERIAL INTERFACE DATA FORMAT AND DEFINITION

BIT	NAME	DESCRIPTION
0 (LSB)	R/W	Read/write control. It must be '0' for this device since all of its registers are write only.
1,2,3	DID0..2	Device ID. These three bits define the SSI device for which the serial communication is to be established. '111' is designated for this device.
4,5	ADDR0..1	Register address. These two bits define the internal register to which data is transferred. ADDR1 / ADDR0 / REGISTER 0 / 0 / VCM D/A 0 / 1 / CONT_MODE 1 / 0 / MSC_MODE 1 / 1 / Reserved

THE CONT_MODE REGISTER (ADDRESS 1)

0	$\overline{\text{RETR}}$	$\overline{\text{RETR}}$ select bit. See Table 2. Default is low.
1	$\overline{\text{BRAKE}}$	$\overline{\text{BRAKE}}$ select bit. See Table 2. Default is low.
2	STANDBY	STANDBY select bit. See Table 2. Default is low.
3	SHOCKSLP	SHOCKSLP select bit. See Table 2. Default is low.

THE MSC_MODE REGISTER (ADDRESS 2)

0	ADVANCE	ADVANCE is used by the µP to increment the commutation counter. The rising edge of ADVANCE will increment the counter by one. When held high, it inhibits the counter being incremented by the internal generated clock. When held low, it permits the normal operation of commutation from back EMF events. ADVANCE default is low. See also START, bit 6.
1,2	GAIN0, 1	Sense amplifier gain select. GAIN1 / GAIN0 / GAIN 0 / 0 / 30 (Default) 0 / 1 / 20 1 / 0 / 10 1 / 1 / 5
3	POLE	Select number of poles of spindle motor. POLE low indicates 8 pole motor while POLE high selects 12 poles.

THE MSC_MODE REGISTER (ADDRESS 2) (continued)

BIT	NAME	DESCRIPTION
4,5	DELAY	0,1 Delay mode select. DELAY1 / DELAY0 / DELAY MODE 0 / 0 / Adaptive(default) 0 / 1 / Fix delay = 150 µs 1 / 0 / Fix delay = 300 µs 1 / 1 / Fix delay = 500 µs
6	START	Start-up false commutation mask bit START should be held high along with ADVANCE bit during motor start up. Default is low.
7	MSCDAC	MSCDAC is used to select the input to LF pin. When MSCDAC is low (default), speed regulation loop and charge pump is activated and LF voltage is the loop filter output. When MSCDAC is high, LF voltage is connected to VCM D/A converter output and the charge pump is disabled. For fast precharging, MSCDAC will also short the external resistor on the SW pin to ground.
8,9	CRL0,1	COM/REV Pin mode select bits. CRL1 / CRL0 / COM/REV 0 / 0 / Commutation Clock 0 / 1 / Revolution Clock 1 / 0 / Lock Indicator 1 / 1 / Too Slow Indicator When CRL1 is high and CRL0 is low, a logic HIGH at COM/REV indicates a lock condition. If COM/REV is low, the motor speed is out of lock. When CRL1 = CRL0 = 1, a logic HIGH at COM/REV indicates the speed error exceeds 1024 µs too slow. CRL0 = CRL1 = 0 is the default.

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PIN DESCRIPTION

POWER SUPPLIES

NAME	TYPE	DESCRIPTION
VPA	-	Analog positive supply.
VNA	-	Analog ground.
VPD	-	Digital positive supply. It must be shorted externally with VPA.
VND	-	Digital ground. It must be shorted externally with VNA. VND is also the low side input to the current sense amplifier of the spindle motor and thus care should be taken to keep VND and the low side of the external resistor Rsense at the same potential.
VVMP[1]	-	Positive supply used for voice coil motor.
VVMN1,2	-	Negative supply used for voice coil motor.
VSMP1,2	-	Positive supply used for spindle motor.
VSMN1,2	-	Negative supply used for spindle motor. They are also the high side inputs to the current sense amplifier of the spindle motor.
VGP	-	Positive supply used for shock detection circuit.
VGN	-	Negative supply used for shock detection circuit.

SERVO POSITIONER

ERRM	I	The inverting input of the error amplifier. ERRM is referenced to VBG.
ERR	O	The error amplifier output. ERR is to provide compensation to the transconductance loop and is referenced to VBG.
SOUT	O	The current sense amplifier output. SOUT is referenced to VBG.
VRETR	I	The retract voltage must be provided externally.
VBYP1	I	The bypassed power supply. An external bypass capacitor is connected to this node to store charge for use by the retract circuitry. This pin is normally a diode drop below VCC, raised by VBEMF during retract.
VBYP2	I	The negative side of the bypass capacitor is connected to this pin. It is normally at ground, rising to VBEMF during retract.
VBEMF	I	Rectified spindle back emf voltage. This input provides current to the internal retract power amplifier.
VM1	O	One side of the voice coil motor sense resistor, and sense resistor combination.
VM2	O	The other side of the voice coil motor.
SE2	I	The voltage across the sense resistor for the voice motor current.
PDAC	O	The 10-bit VCM D/A converter output. It is referenced to VBG if MSCDAC is low, when MSCDAC bit is high, PDAC pin will be floated.

[1] The circuit board contacts for VVMP, VVMN1, VVMN2, VSMP1, VSMP2, VSMN1, and VSMN2 must be sized in accordance with anticipated motor currents. All pins must be connected with low resistance circuit board traces.

SPINDLE MOTOR COMMUTATOR/DRIVER

NAME	TYPE	DESCRIPTION
SYSCLK	I	System clock input at 1 MHz.
COM/REV	O	When the CRL0 bit and CRL1 bit in the MSC_MODE regsiter are low, this pin is defined as the LSB of the commutation counter. If CRL1 bit is low while CRL0 bit is high, it is defined as the revolution clock of the spindle motor. If CRL1 bit is high and CRL0 is low, COM/REV pin becomes lock indicator. A logic HIGH on this pin indicates motor speed is in lock condition. If CRL0 = CRL1 = 1, a logic HIGH on COM/REV pin then indicates speed is too slow by greater than 1024 µs.
LF	I	Control voltage input. The combination of the MOSFET drivers and the predriver circuit forms a transconductance amplifier which sets the motor current in relation to LF. In conjunction with R_{sense} connected at VSMN and the gain of the sense amplifier, the transconductance is defined by: Gm = Im/VIN = 1/(RSENSE x Gain), Gain = 5, 10, 20, 30 When MSCDAC bit is low, LF is provided from charge pump; When MSCDAC bit is high, LF is connected to VCM D/A converter output. An external RC loop filter must be connected at this pin.
SW	O	One side of the external resistor RL in the loop filter. When MSCDAC bit is asserted high, RL is shorted to ground through SW.
A,B,C	O	Spindle motor driver outputs.
CT	I	Back EMF input from spindle motor coil center tap.
RRAMP	I	Lower driver turn-off dv/dt setting resistor. External resistor from VPA to this pin sets the dv/dt slope of the motor coil voltage when the lower drivers are commutating to the off state. The dv/dt is approximately given by the relationship: dv/dt = 15/RRAMP, where dv/dt is expressed in volts/µs and RRAMP in kΩ.

CONTROL CIRCUITRY

VCHK	I	Comparator input for power supply monitoring. When VCHK is below VBG, an internal voltage fault is generated. Normally a resistor divider from VCC is connected at this pin. A capacitor can be connected at this pin to filter out noise transients.
VBG	O	Voltage reference, generated from the internal bandgap voltage, for use with the power supply monitor comparator.
IBR	O	A 21.5 kΩ ±1% resistor is tied from this pin to ground to establish a bias current for internal circuitry.
$\overline{POR}$	O/D	This pin serves the dual purpose of providing power-on-reset and of stretching short internal voltage fault pulses to a width suitable for the host micro controller. An external RC network sets the minimum width of any $\overline{POR}$ pulse. The circuit is designed so that even if a short power fault on VCHK is sensed, $\overline{POR}$ will be pulled low regardless of the capacitance loading.

CONTROL CIRCUITRY (continued)

NAME	TYPE	DESCRIPTION
XIN	I	X-axis shock detection input.
XREF	I	X-axis reference. XREF is ac-coupled externally to VBG.
YIN	I	Y-axis shock detection input.
YREF	I	Y-axis reference. YREF is ac-coupled externally to VBG.
GSUM	O	The summing node of full-wave rectified X-axis and Y-axis shock signals.
GIN	I	Negative input of GAMP. External RC components are connected between GIN and GOUT to have the required low pass filter response output at GOUT.
GOUT	O	Output of GAMP.
GCOMP	O	Output of GCOMP comparator. GCOMP is active low.

SERIAL INTERFACE PORT

SDATA	I	Serial data shifted into internal registers.
SCLK	I	Serial data timing reference. The rising edge of the SCLK shifts SDATA in while SDEN is asserted high.
SDEN	I	Serial data transfer enable. When active high, the serial data transfer is enabled.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

PARAMETER	RATING
Supply voltage @ VPA,VPD,VVMP,VSMP1,2 VGP	-0.3 to 7.0V
Motor current @ A,B,C,VM1,VM2	1.0A
Input voltage @ LF,RRAMP	-0.3 to VDD + 0.3V
Input voltage @	
A, B, C, VBEMF, VBYP1, VBYP2	-0.3 to 12.0V
VM1, VM2, SE2	-0.3 to 7.0V
All other pins	-0.3 to Vdd
Storage temperature	-65 to 50°C
Lead temperature (10 sec duration)	0 to 300°C

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside the recommended conditions.

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Supply voltage	Vdd		4.5		5.5	V
Supply current						
VPA,VPD	Idd				20	mA
VVMP	Ivmp				0.4	A
VSMP1, 2	Ismp				0.5	A
Standby mode	Istandby				15	mA
Sleep mode	Isleep				1.0	mA
VGP	Ivgp				4	mA
VGP Sleep	Igsleep				1	mA
Input voltage @ VBEMF			1.0		10	V
Input voltage @ LF			0		2.5	V
Ambient temperature	Ta		0		70	°C
Capacitive load on digital outputs	Cl				100	pF

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RECOMMENDED OPERATING CONDITIONS (continued)
The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside the recommended conditions.

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Analog output load	Cl				40	pF
	Rl				10	kΩ
System clock fc = 1 MHz						
Freq. tolerance	fc		-0.1		0.1	%
Pulse width	Twh,Twl		0.4		0.6	µs
Biasing resistor Rbias = 21.5 kΩ	Rbias		-1		1	%
External resistors	Rf, Rc		10			kΩ

PERFORMANCE SPECIFICATIONS

Digital I/O

Digital input @ SDATA, SCLK, SDEN, SYSCLK	Vil				0.8	V
	Vih		2.0			V
	Iil,Iih				±1	µA
Digital O/D output @ $\overline{POR}$	Ioh	Voh = Vdd			1	µA
	Iol	Vol = 0.4V	4.0			mA
	Vol	Iol = 4 mA			0.4	V
Digital Output @ COM/REV	Vol	Iol = 2.0 mA			0.4	V
	Voh	Ioh = -100 µA	2.4			V

Servo Positioner

VBYP1 current	Normal mode				100	µA
	Retract mode	Power off, VBYP1 = 3V			20	µA
BEMF current	Normal mode	VBEMF = 4V			300	µA
	Retract mode	Imotor = 0, VBEMF = 3V, Power off, VRETR = 0.5V			20	µA

Servo Positioner (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
SOUT amplifier Gain		3.9		4.1	V/V
Input offset	SOUT = VBG	-3		3	mV
Output swing	RL = 10 kΩ to VBG	0.15		Vdd-1	V
CMRR		60			dB
ERRAMP amplifier Gain		60			dB
Unit gain bandwidth			1		MHz
Input offset	ERR = ERRM	-10		10	mV
Output swing		0.15		Vdd-1.25	V
Power amplifier (VCM Driver)	Gain (VM2-VM1)/(ERR-VBG)	11		13	V/V
Total voltage drop across Power FET's(PFET)	Imotor = 200 mA			1.0	V
Bridge crossover time	Ivcm = 10 mA, pp step input, RL = 16Ω			10	µs
VCM output THD	Ivcm = 100 mA, pp @ 100 Hz, RL = 16Ω			2	%
Retract amplifier (normal)	VRETR leakage	-1		1	µA
Retract amplifier (retract)	VRETR = 0.5V, VBEMF ≥ 1V, RL = 16Ω				
Offset		-100		0	mV
Maximum output current	VRETR = 0.5V, VBYP1 = 4.5V, VM1 = VM2 VBEMF = 1.0V	40			mA
	VBEMF = 1.5V	60			mA

Spindle Motor Speed Controller/Driver

Charge pump current		48		72	µA
Leakage current @ LF	0 < VIN < 2.5V	-25		25	nA
Total voltage drop across	I = 200 mA			0.4	V
power FETs(SFET)	I = 500 mA			1.0	V
Outputs impedance @ A,B,C Rin while not driving	-0.3V < Vin < 7V	10			kΩ
Output impedance @ CT Rin	-0.3V < Vin < 7V	3			kΩ

RECOMMENDED OPERATING CONDITIONS (continued)
The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside the recommended conditions.

Control Circuitry

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
On resistance at $\overline{POR}$				200	Ω
VBG	Iout < ±0.2 mA	2.16		2.30	V
VCHK comparator offset w.r.t. VBG Hysteresis		-15 40		15 120	mV mV

Shock Detection Circuitry

XAMP,YAMP	Gain,XIN or YIN to GSUM 0.5 mV,peak < V(IN) < 20 mV,peak 1KHz < V(IN) < 5 KHz	36		44	V/V
	Differential input resistance	2850			Ω
	Input leakage current	-50		50	nA
GAMP	Input referred offset	-15		15	mV
	Output swing	0.75		VBG + 0.1	V
	Bandwidth		1		MHz
GCOMP Comparator Threshold w.r.t. VBG		-1.05		1.2	V

D/A Converter

Full-scale voltage			VBG		V
Resolution			10		bits
Digital Delay				4	µs
LSB voltage			VBG/1024		V
Differential nonlinearity				1	LSB

Serial Interface Port

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
SDEN setup time prior to SCLK	Tsens	3 5			ns
SDEN hold time after SCLK	Tsenh	50			ns
SDATA setup time prior to SCLK rise	Tds	15			ns
SDATA hold time after SCLK rise	Tdh	15			ns
SCLK pulse width	Tpw	100			ns

APPLICATIONS INFORMATION

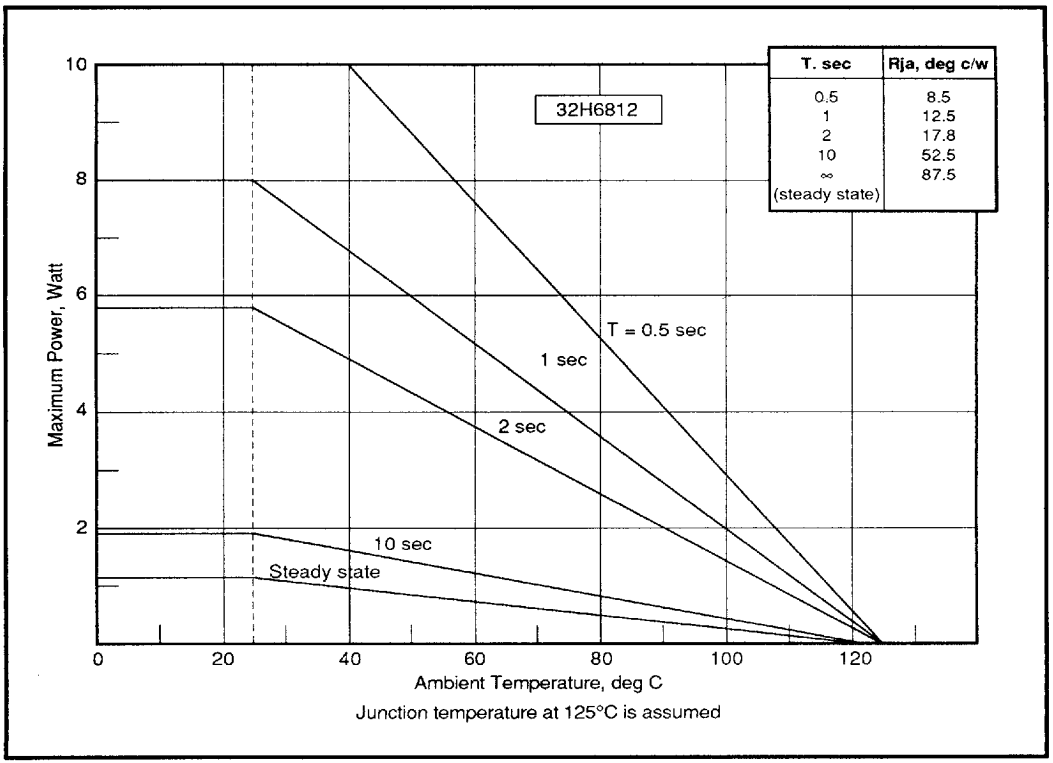
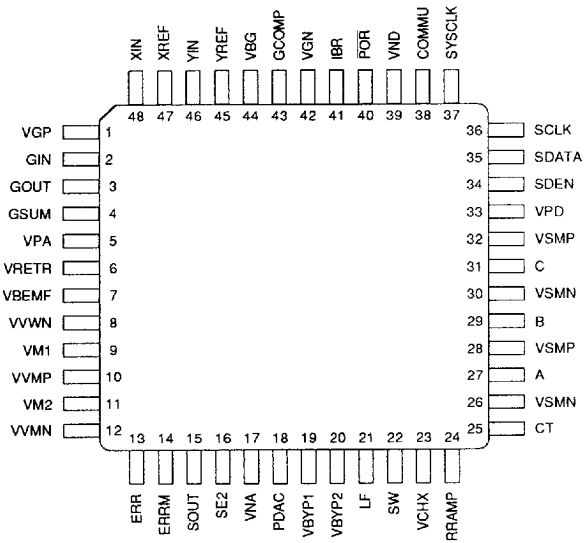


FIGURE 1: Power Dissipation Derating

SSI 32H6812
Servo & Spindle Driver with Shock Detection

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



48-Lead TQFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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