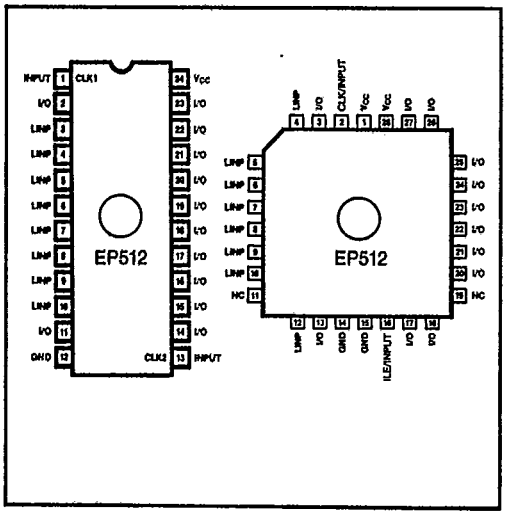
ALTERA 12 MACROCELL EPLD EP512

FEATURES

- High Performance logic replacement for TTL and 74HC or 74HCT SSI and MSI logic.
- High Speed, tpd = 25ns, and 40MHz operating frequency.
- "Zero Power" (150 μA Standby Current).
- Twelve Macrocells with configurable I/O architecture allowing up to 22 inputs (10 dedicated, 12 I/O) and 12 outputs.
- Eight configurable inputs which can implement latch, register, or flow-through mode; synchronous or asynchronous operation.
- Programmable product term allocation allowing up to 16 product terms for a single Macrocell.
- Programmable registers providing D, T, SR or JK flip-flops with Clear, Preset, and Clock control.
- Two product terms for all Macrocell control signals (OE, Preset, Clear and Clock).
- Dual feedback on all Macrocells for buried register implementation and input usage.
- A+PLUS software support featuring Schematic Capture, Netlist, Boolean Equation and State Machine design entry.
- Space saving 24 pin DIP, 300 mil, and 28 pin JLCC/PLCC packages.

CONNECTION DIAGRAM



GENERAL DESCRIPTION

The Altera EP512 provides a User-Configurable, High-Performance solution for general purpose logic and custom control (state machine) functions. The EP512 features an enhanced PLD architecture to easily integrate 74ALS and HC (HCT) SSI and MSI logic. In addition, a single EP512 can also replace multiple programmable logic devices (22V10, 20RA10, 20L10, 20R10).

The EP512 uses sum-of-products logic providing a configurable AND-OR structure. The device can implement combinatorial, latched, and registered logic functions, active high or low. The EP512 contains a total of 12 I/O Macrocells, 8 user-configurable input structures (latch, register or flow-through operation) and 2 inputs that can be programmed to serve as either combinatorial inputs or clock inputs for the input and output register functions.

A unique feature of the EP512 is the ability to re-allocate product terms between adjacent macrocells allowing a single macrocell to have 8, 12 or 16 product terms. In addition, each macrocell contains two dedicated product terms for each control signal: Output Enable, Preset, Clear, and Asynchronous Clock. Each macrocell also contains dual feedback allowing the logic to be buried while reserving the I/O pin as an additional input.

The EP512 uses advanced CMOS EPROM cells as logic control elements. This technology allows the EP512 to operate in high performance applications while significantly reducing the power consumption. Other advantages include: 100% generic testing (all devices are 100% tested at the factory). The device can be erased with ultraviolet light. Design changes are no longer costly, nor is there a need for testing after programming.

Programming the EP512 is accomplished with the use of Altera's A+PLUS development software which supports four different design entry methods. Once the circuit has been tested, the A+PLUS software performs automatic translation into logical equations, Boolean minimization, and design fitting directly into an EP512.

PRELIMINARY DATA

NOTICE: THIS IS NOT A FINAL SPECIFICATION. SOME PARAMETRIC LIMITS ARE SUBJECT TO CHANGE.

REV. 2.0

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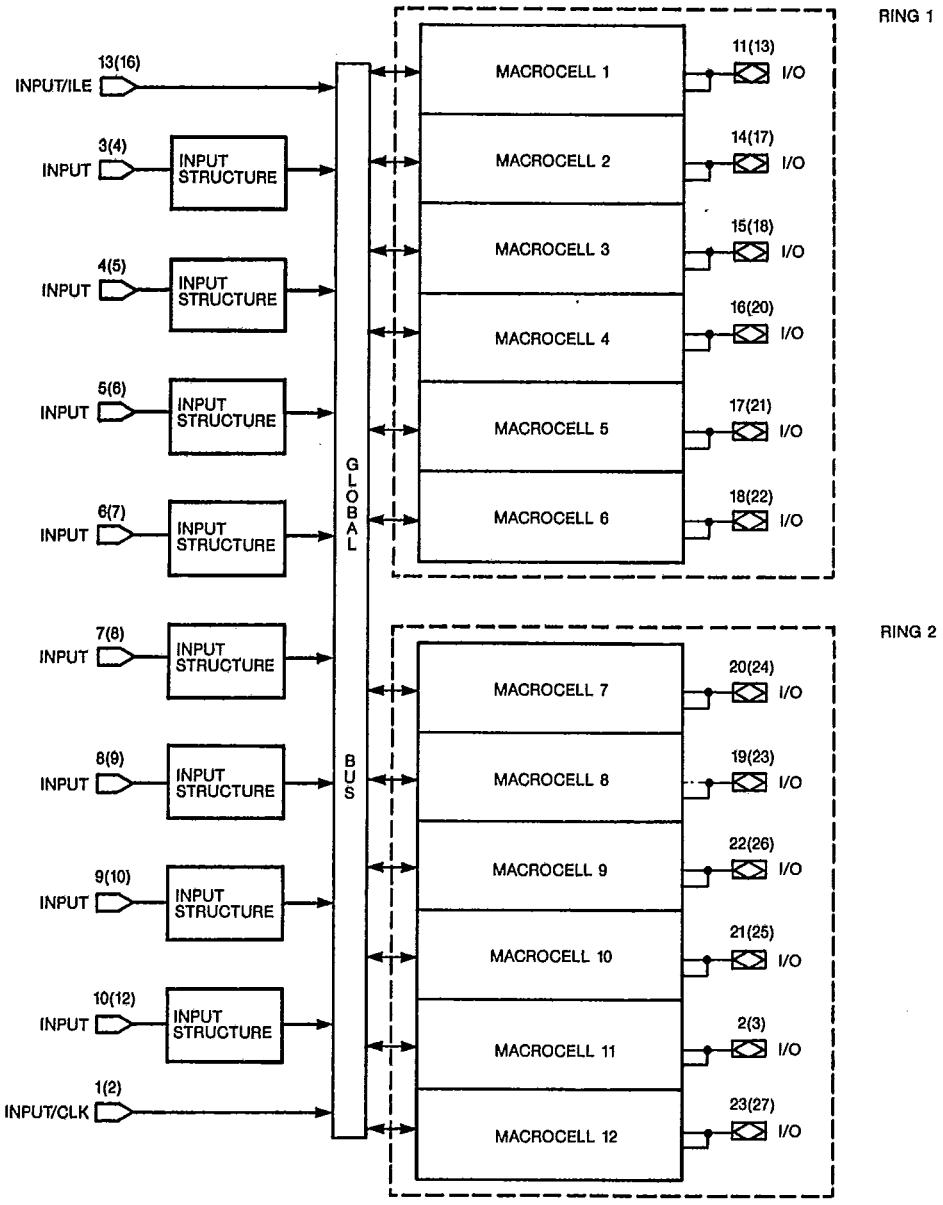
Figure 1. EP512 Block Diagram



Pin #'s in () pertain to 28 pin JLCC/PLCC package.

FUNCTIONAL DESCRIPTION

The EP512 is an Erasable Programmable Logic Device (EPLD) which uses a CMOS EPROM technology to configure connections in a programmable AND logic array. The EP512's innovative architecture allows it to integrate many standard TTL functions. The device also contains an enhanced I/O architecture which provides advanced functional capability for user-configurable logic.

Figure 1 shows the EP512 Block Diagram. Externally, the EP512 provides 10 dedicated inputs and 12 I/O pins programmed for input, output, or bi-directional operation. The device contains 12 macrocells which can be independently configured.

Figure 2 shows an EP512 Macrocell. The internal architecture uses a sum-of-products (AND-OR) structure. Inputs to the programmable AND array come from the true and complement forms of the 10 dedicated inputs, 12 macrocell feedback signals and 12 I/O pins. Each EP512 Macrocell contains 16 product terms. Eight product terms are dedicated to control signals (OE, CLK, Preset and Clear), while eight product terms are used for the general data array. Each EP512 product term represents a 68 input AND gate.

At the intersection point between an AND array input and a product term is an EPROM control cell. In the erased state, all cell connections are made. This means both the true and complement of all array inputs are connected to each product term. During the programming process, selected connections are opened. Therefore, any product term may be connected to the true or complement of any array input signal. When both the true and complement of an array input signal are left connected, a logical false results on the output of the AND gate. If both the true and complement of any array input signal are programmed open, then a logical "don't care" results for that input. If all 68 inputs for a given product term are programmed open, then a logical true results on the output of the corresponding AND gate.

The EP512 contains 10 dedicated inputs, 8 data inputs and 2 programmable system clock inputs (ILE and CLK). ILE (pin 13) provides synchronous clocking to the input structures while CLK (pin 1) provides synchronous clocking to the macrocell registers. These system clocks are connected directly from the EP512 external pins. When using these system clocks, ILE is negative edge triggered (data transitions occur on the falling edge of ILE)

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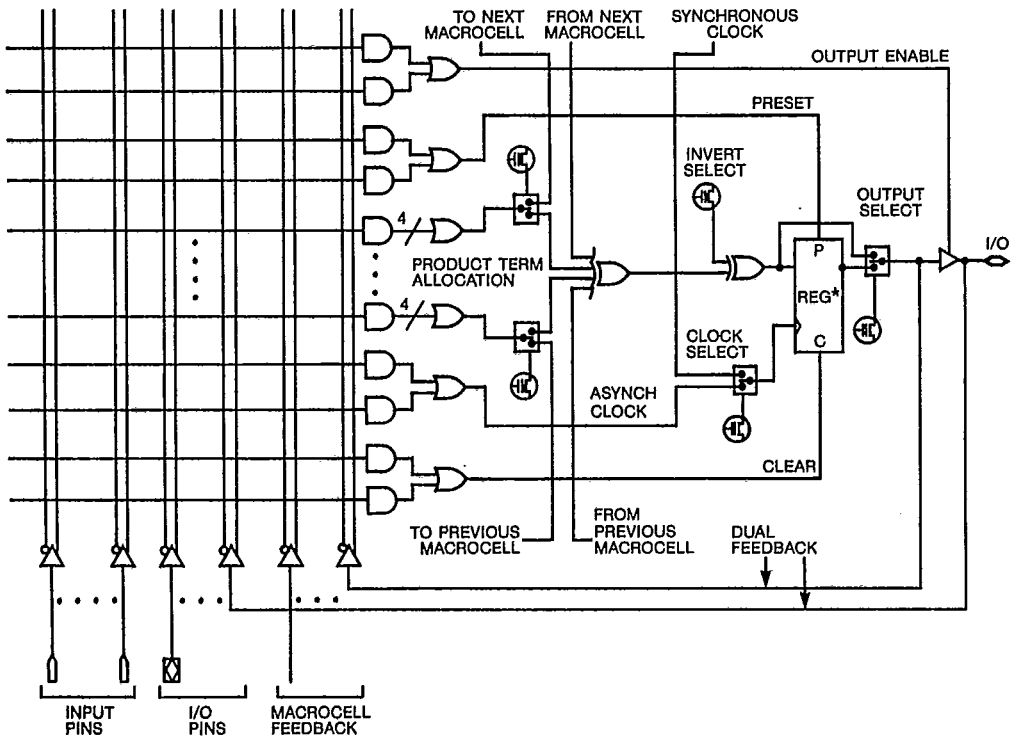
Figure 2. Logic Array Macrocell



* REGISTER CAN BE D, T, JK, OR RS FLIP-FLOP

and CLK is positive edge triggered (data transitions occur on the rising edge of CLK). ILE and CLK may also be used as general purpose inputs.

For asynchronous clocking of the input structure, the clock signal is derived from a dedicated product term (see Figure 3). For asynchronous clocking of the macrocell registers, the clock signal is derived from two dedicated product terms (see Figure 2). Each input structure and macrocell register is individually configurable allowing a mixture of synchronous and asynchronous clocking on both the input structures and the macrocell registers.

INPUT STRUCTURE

Figure 3 shows a functional block diagram of the input structure of the EP512. The EP512 contains 8 programmable input structures that may be individually configured as one of the following:

—Synchronous D-type register
—Asynchronous D-type register
—Synchronous input latch
—Asynchronous input latch
—Flow through latch

The dedicated ILE input (pin 13) serves as a synchronous clock for both synchronous input latch and synchronous input register modes. For asynchronous clocking, a dedicated product term is available and provides clocking for the Asynchronous Register and Asynchronous Latch modes. The ILE Select Mux, shown in Figure 3, determines whether the input clocking will be provided by the dedicated ILE input (synchronous mode) or the dedicated Product term (asynchronous mode). Table 1 shows the Input Structure Function Table using the ILE (pin 13) input for control. Note, when using synchronous clocks (ILE), the input register is negative edge triggered. Positive edge triggered operation can be achieved by using the ILE product term (asynchronous mode) for clocking control. Flow through input operation can be achieved by connecting the Flow Through Select Mux to Vcc (see Figure 3).

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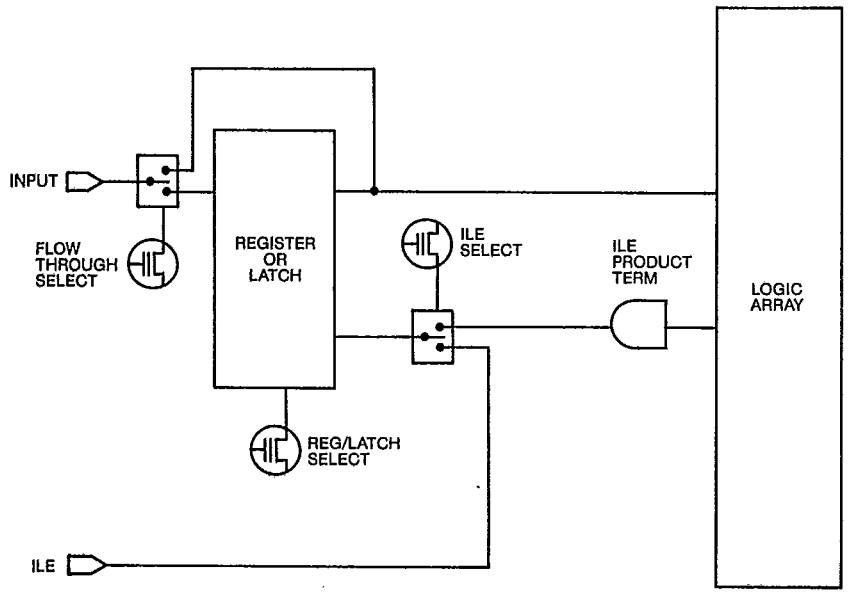
TABLE 1 EP512 INPUT FUNCTIONS

Input Type	ILE	D	Q
Latch	H	H	H
Latch	H	L	L
Latch	L	X	Qn
Register	↓	H	H
Register	↓	L	L
Flow-Through	X	H	H
Flow-Through	X	L	L

Figure 3. Input Structure



PRODUCT TERM ALLOCATION

The EP512 supports Product Term Allocation, allowing unused product terms from one macrocell to be placed into another macrocell. In the EP512, this allocation is done between adjacent macrocells in groups of 4 product terms. Thus, each macrocell has two adjacent macrocells to share product terms. The EP512 macrocells are grouped into two "rings" (Ring 1 and Ring 2) with 6 macrocells per ring. Table 2 shows the structure of the two rings and defines each macrocell's adjacent partners. By using Product Term Allocation, each macrocell can implement logic requiring up to 16 product terms.

For example, if Macrocell 4 requires 16 product terms, Altera's A+PLUS Design Software will allocate four product terms from Macrocell 3 and four product terms from Macrocell 5 to give Macrocell 4 a total of 16 product terms. Macrocells 3 and 5 each have four product terms remaining which may be kept or used by other macrocells. This example is illustrated in Figure 4. Even if a macrocell has allocated all of its product terms to adjacent macrocells, its register and associated control functions are still usable. In this case the input to the I/O register is tied to GND (VCC if the invert select EPROM bit is programmed). For example, the register preset and clear may used to implement an asynchronous S-R latch.

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I/O ARCHITECTURE

The EP512 Input/Output Architecture provides each macrocell with over 50 possible I/O configurations. Each I/O can be individually configured for combinatorial or registered output, with programmable output polarity. Four different types of registers (D, T, JK, SR), can be implemented into every I/O without any additional logic requirements. Each macrocell contains two dedicated product terms (see Figure 2) for every control

Figure 4. Product Term Allocation Example

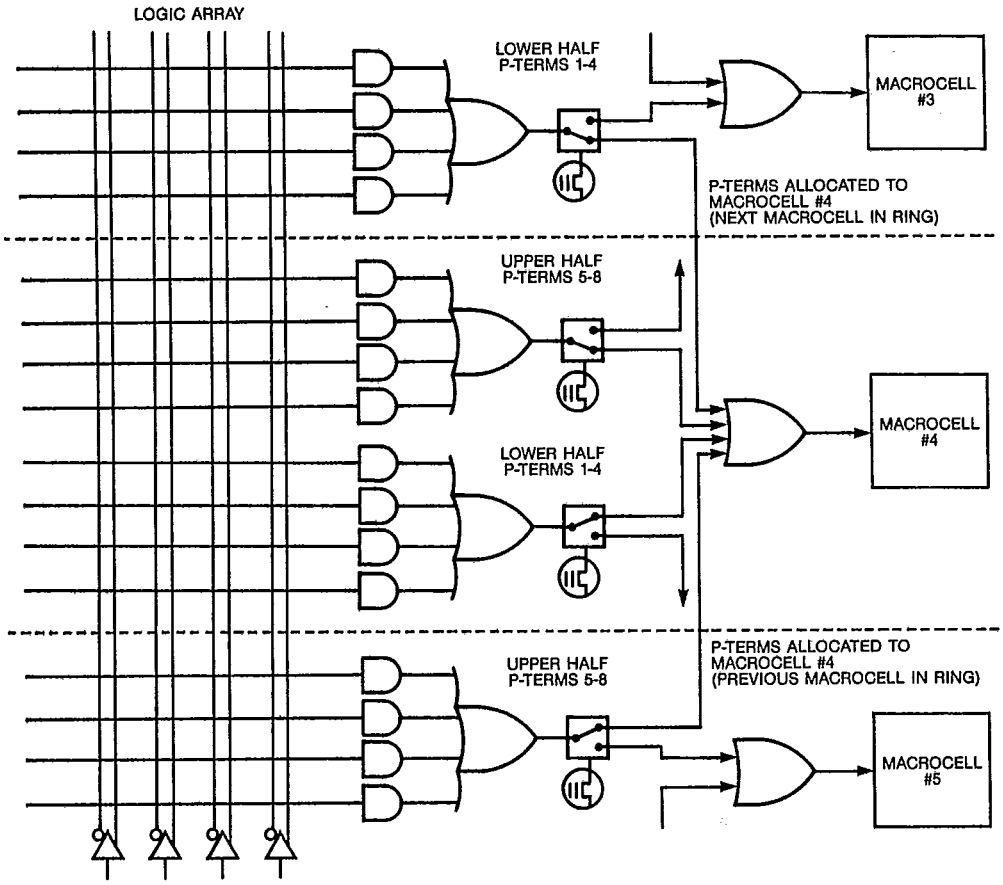

TABLE 2 PRODUCT TERM ALLOCATION

Ring 1			Ring 2		
Current Macrocell	Next Macrocell	Previous Macrocell	Current Macrocell	Next Macrocell	Previous Macrocell
1	2	6	7	8	12
2	3	1	8	9	7
3	4	2	9	10	8
4	5	3	10	11	9
5	6	4	11	12	10
6	1	5	12	7	11

function (Asynchronous Preset, Asynchronous Clear, Asynchronous Clock, and Output Enable).

Each macrocell register may be individually configured to function in either a synchronous or asynchronous clock mode. Synchronous clocking is provided by the dedicated clock pin (pin 1) while asynchronous clocking is provided by the two dedicated asynchronous clock product terms (see Figure 1).

Product Term Allocation is controlled by Altera's A+PLUS Design Software and implemented using the Product Term Allocation Control Muxes shown in Figure 2. The product terms are ORed together to generate the logic signal for the Macrocell Combinatorial output or Macrocell Register input. This scheme allows a more efficient utilization of product terms and greater flexibility in design architecture.

Output polarity is controlled by the Invert Select EPROM bit. This feature allows active high or active low output and also permits DeMorgan's inversion for improved minimization of logic.

OUTPUT/FEEDBACK

Every macrocell in the EP512 has Dual Feedback. This architectural feature enables the designer to use the macrocell for buried logic and also use the macrocell's I/O pin as a dedicated input, increasing design flexibility. Dual Feedback is implemented in the EP512 by providing a feedback path from both the input pin and the macrocell register (see Figure 2). These paths are separated by the tri-state buffer controlled by the Output Enable control signal. When the tri-state buffer is disabled (Output Enable grounded), the register uses the internal feedback path, while allowing the second feedback path to function as a dedicated input path. This second feedback path allows the I/O pin to connect directly into the logic array.

In the erased state, the I/O is configured for combinatorial active low output with input (pin) feedback.

FUNCTIONAL TESTING

The EP512 is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield. As a result, traditional problems associated with fuse-programmed circuits are eliminated. The erasable nature of the EP512 allows test program patterns to be used and then erased. This facility to use application-independent, general purpose tests is called generic testing and is unique for EPLDs among user-defined LSI logic devices.

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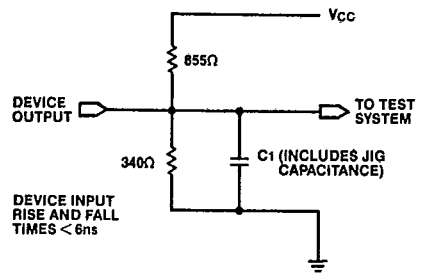
Figure 5. AC Test Conditions



Power supply transients can affect AC measurements, simultaneous transitions of multiple outputs should be avoided for accurate measurement. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

DESIGN SECURITY

The EP512 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied nor retrieved. This enables a high level of design protection, since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

TURBO-BIT

The EP512 contains a programmable option to control the automatic power down feature that enables the low standby power mode of the device. This option is controlled by a TURBO-BIT which can be set using A+PLUS. When the TURBO-BIT is programmed (Turbo = ON), the low standby power mode (Icc1) is disabled. This renders the circuit less sensitive to Vcc noise transients which can be created by the power-up/power-down cycle when operating in the low power mode. The typical Icc vs frequency data for both Turbo and Non-Turbo (low power) mode is shown in each EPLD data sheet. All AC values are tested with the TURBO-BIT programmed. If the design requires low power operation then the TURBO-BIT should be disabled (Turbo = OFF). When operating in this mode, some AC parameters are subject to increase. Values given in the AC specifications section under "Non-Turbo Adder" must be added to the respective AC parameter to determine worst-case timing.

Figure 6. I_{CC} Vs. F_{max}

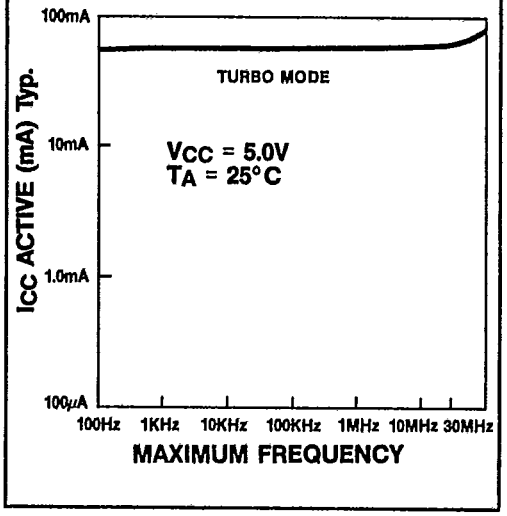
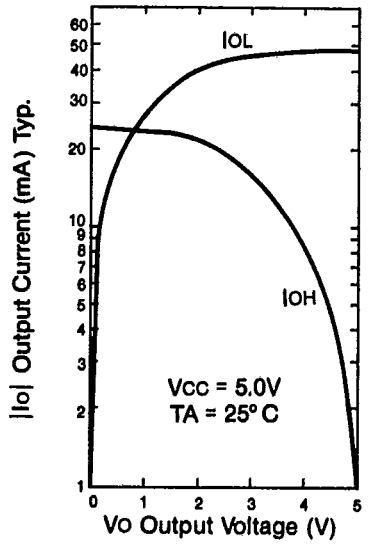


Figure 7. Output Drive Currents



ABSOLUTE MAXIMUM RATINGS

COMMERCIAL OPERATING RANGE

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Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	With respect to GND note (3)	-2.0	7.0	V
V_{PP}	Programming supply voltage		-2.0	13.5	V
V_I	DC INPUT voltage		-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		-150	150	mA
I_{OUT}	DC OUTPUT current, per pin		-25	25	mA
P_D	Power dissipation			750	mW
T_{STG}	Storage temperature	No bias	-65	+150	°C
T_{AMB}	Ambient temperature	Under bias	-65	+135	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage		4.75	5.25	V
V_I	INPUT voltage		0	V_{CC}	V
V_O	OUTPUT voltage		0	V_{CC}	V
T_A	Operating temperature	For Commercial	0	70	°C
T_R	INPUT rise time	note (8)		100	ns
T_F	INPUT fall time	note (8)		100	ns

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = 0°C for Commercial)
Note (1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3		0.8	V
V_{OH}	HIGH level TTL output voltage	I_{OH} = -4mA DC	2.4			V
V_{OH}	HIGH level CMOS output voltage	I_{OH} = -2mA DC	3.84			V
V_{OL}	LOW level TTL output voltage	I_{OL} = 4mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	-10		+10	μA
I_{OZ}	3-state output off-state current	V_O = V_{CC} or GND	-10		+10	μA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND No load note (7)			150	μA
I_{CC2}	V_{CC} supply current (non-turbo)	V_I = V_{CC} or GND No load, f = 1.0 MHz note (6)			50	mA
I_{CC3}	V_{CC} supply current (turbo)	V_I = V_{CC} or GND No load, f = 1.k0 MHz note (6)			100	mA

CAPACITANCE

Note (4)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1.0 MHz		20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1.0 MHz		20	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V f = 1.0 MHz		20	pF

AC CHARACTERISTICS

EP512-25, EP512-30, EP512-35

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(V_{CC} = 5V ±5%, T_A = 0°C to 70°C for Commercial)

			EP512-25		EP512-30		EP512-35		NON-TURBO ADDER	
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	note (5)	UNITS
t_{PD1}	Input to non-registered output	C_1 = 50pF		25		30		35	10	ns
t_{PD2}	I/O input to non-registered output			25		30		35	10	ns
t_{PZX}	Input or I/O input to output enable			25		30		35	10	ns
t_{PXZ}	Input or I/O input to output disable	C_1 = 5pF note (2)		25		30		35	10	ns
t_{CLR}	Asynchronous output clear time	C_1 = 50pF		25		30		35	10	ns
t_{SET}	Asynchronous output preset time			25		30		35	10	ns

SYNCHRONOUS CLOCK MODE

			EP512-25		EP512-30		EP512-35		NON-TURBO ADDER	
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	note (5)	UNITS
f_{MAX}	Maximum frequency	note (9)	50		40		40		0	MHz
t_{SU}	Input or I/O input setup time		20		25		25		10	ns
t_H	Input or I/O input hold time		0		0		0		0	ns
t_{CH}	Clock high time		10		12.5		12.5		10	ns
t_{CL}	Clock low time		10		12.5		12.5		10	ns
t_{CO1}	Clock to output delay			15		20		20	10	ns
t_{CNT}	Minimum clock period (register output feedback to register input—internal path)			30		35		40	10	ns
f_{CNT}	Internal maximum frequency ($1/t_{CNT}$)	note (6)	33		30		25		0	MHz

SYNCHRONOUS CLOCK MODE—INPUT STRUCTURE

			EP512-25		EP612-30		EP512-35		NON-TURBO ADDER	
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	note (5)	UNITS
f_{IMAX}	Maximum input frequency ($1/t_{ICP}$)		40		33		28.5		0	MHz
f_{ISU}	Input register setup time		5		5		5		0	ns
t_{IH}	Input hold time		5		5		5		0	ns
t_{ICH}	Input clock high time		10		12.5		12.5		10	ns
t_{ICL}	Input clock low time		10		12.5		12.5		10	ns
t_{ICO1}	Input clock to output			30		35		40	10	ns
t_{ICP}	Input clock period minimum			25		30		35	10	ns
t_{ILO1}	Input latch to output	note (6)		35		40		40	10	ns

ASYNCHRONOUS CLOCK MODE

EP512-25, EP512-30, EP512-35

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SYMBOL	PARAMETER	CONDITIONS	EP512-25		EP512-30		EP512-35		NON-TURBO ADDER	UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	note (5)	
f_{AMAX}	Maximum frequency $1/(t_{ACL} + t_{ACH})$	note (9)	20		16.5		16.5		0	MHz
t_{ASU}	Input or I/O input setup time		7		10		10		10	ns
t_{AH}	Input or I/O input hold time		23		27		30		10	ns
t_{ACH}	Clock high time		25		30		30		10	ns
t_{ACL}	Clock low time		25		30		30		10	ns
t_{ACO1}	Clock to output delay			35		45		50	10	ns
t_{ACNT}	Minimum clock period (register output feedback to register input—internal path)			55		65		70	10	ns
f_{ACNT}	Internal maximum frequency $(1/t_{ACNT})$		18		15		14.2		0	MHz

ASYNCHRONOUS CLOCK MODE—INPUT STRUCTURE

SYMBOL	PARAMETER	CONDITIONS	EP512-25		EP512-30		EP512-35		NON-TURBO ADDER	UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	note (5)	
t_{AIMAX}	Max. freq. input reg.			20		16.5		16.5	0	MHz
t_{AISU}	Input setup to asynch clk.		0		0		0		10	ns
t_{AIH}	Input hold after asynch clk.		23		26		30		10	ns
t_{AICH}	Asynch input high time		25		30		30		10	ns
t_{AICL}	Asynch input low time		25		30		30		10	ns
t_{AICO1}	Asynch input clk. to output			48		55		60	10	ns
t_{AILO1}	Asynch input latch to output			53		60		65	10	ns

INPUT-CLOCK-TO-MACROCELL-CLOCK A.C. CHARACTERISTICS

SYMBOL	PARAMETER	EP512-25		EP512-30		EP512-35		NON-TURBO ADDER	UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	note (5)	
t_{ILMC}	Synchronous ILE Synchronous Macrocell CLK	25		30		35		10	ns
	Synchronous ILE Asynchronous Macrocell CLK	5		8		10		10	ns
	Asynchronous ILE Synchronous Macrocell CLK	48		55		65		10	ns
	Asynchronous ILE Asynchronous Macrocell CLK	20		35		50		10	ns

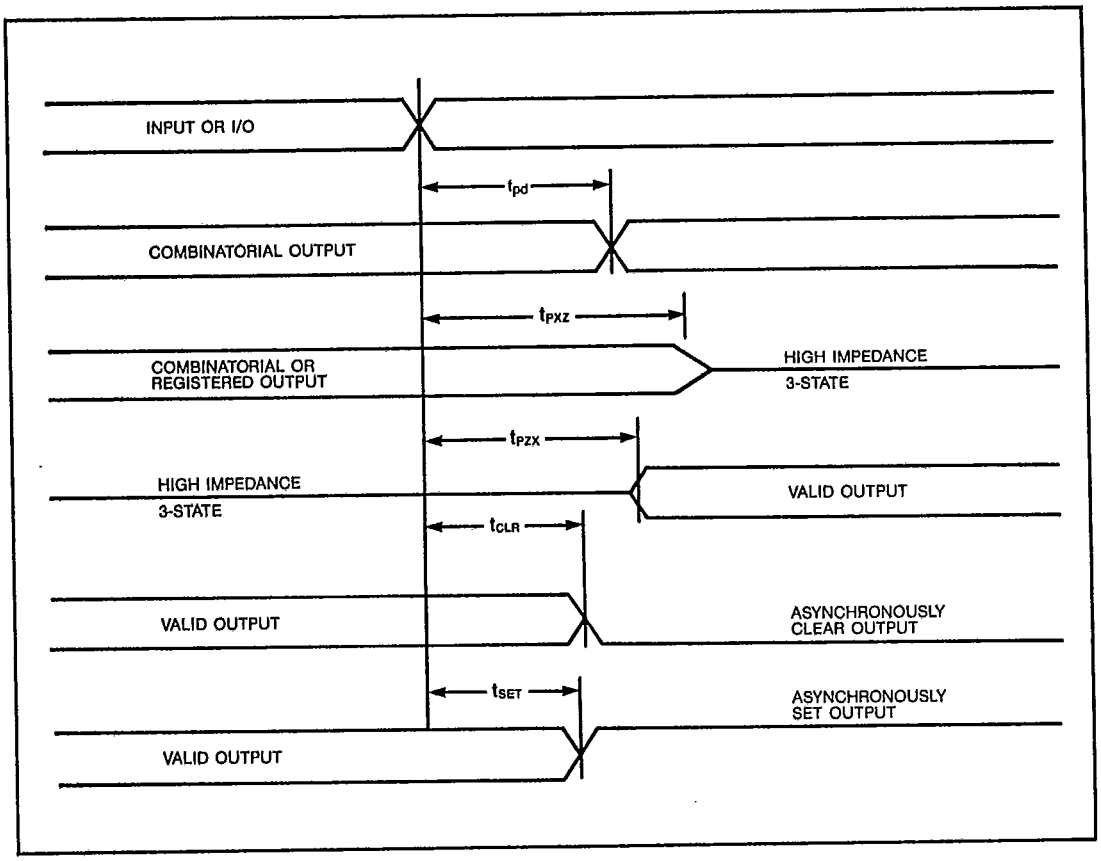
Notes:
1. Typical values are for T_A = 25°C, V_{CC} = 5V
2. Sample tested only for an output change of 500mV.
3. Minimum DC input is -0.3V. During transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
4. Capacitance measured at 25°C. Sample tested only. Clock pin capacitance for dedicated clock inputs only. Pin 1 (high voltage pin during programming), has capacitance of 50pF max.
5. See TURBO-BIT™, page 56.
6. Measured with device programmed as a 12 bit counter.
7. EPLD automatically goes into standby mode if logic transitions do not occur when in non-turbo mode (approximately 100ns after last transition). This feature may not be available on initial production units. Check factory for status.
8. Clock t_R, t_F = 100ns.
9. The f_{MAX} values shown represent the highest frequency for pipelined data.

Note: The recommended erase procedure for this device is to expose it to a standard UV lamp for a minimum of one hour.

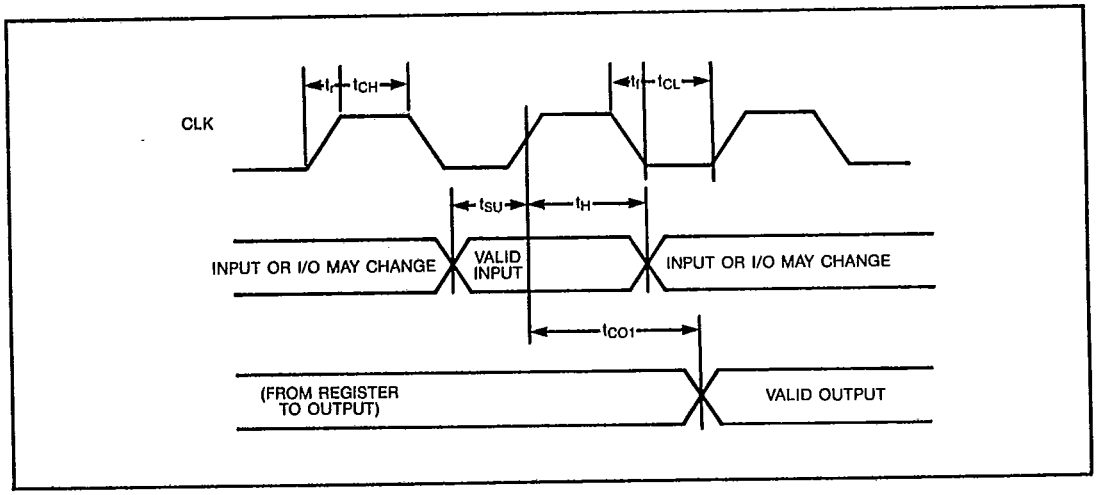
GRADE	AVAILABILITY
Commercial (0°C to 70°C)	EP512-25 EP512-30 EP512-35

Figure 8. Switching Waveforms

COMBINATORIAL MODE

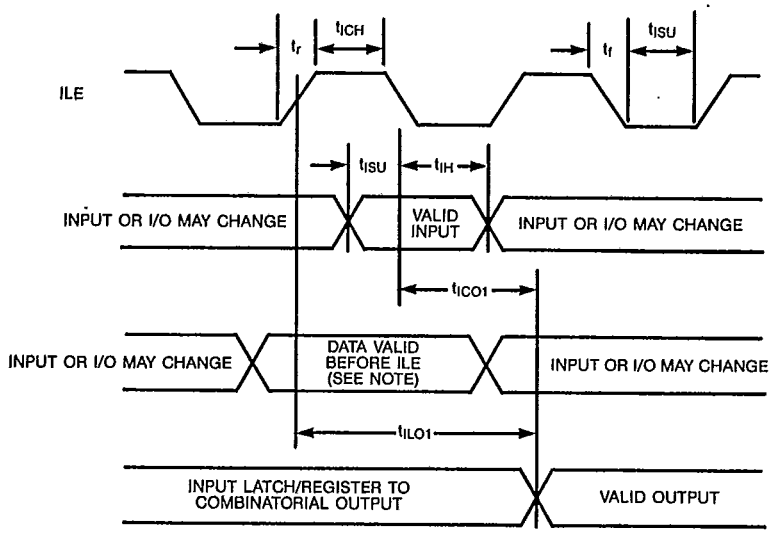


SYNCHRONOUS CLOCK MODE (MACROCELLS)



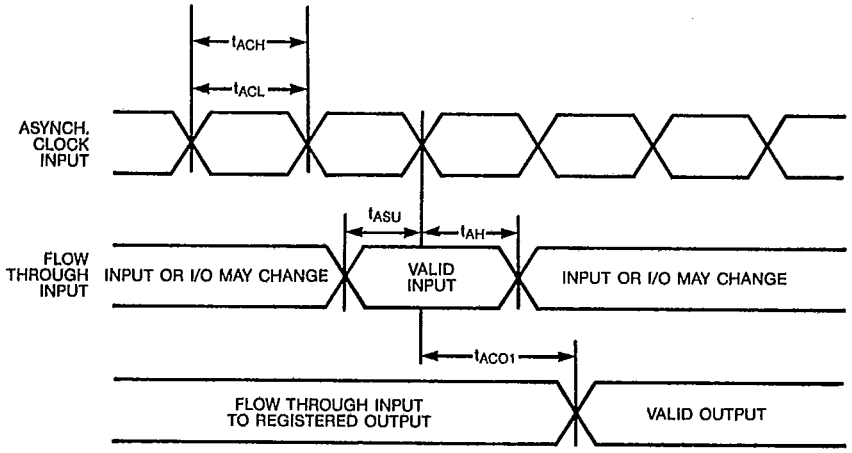
Switching Waveforms (Continued)

SYNCHRONOUS CLOCK MODE (INPUT STRUCTURE)



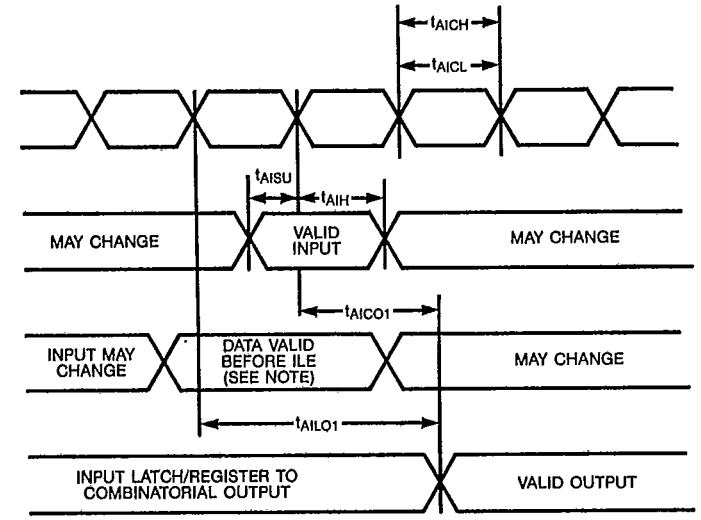
NOTE: WHEN ILE GOES HIGH BEFORE DATA IS VALID, USE t_{PD} INSTEAD OF t_{ILO1}

ASYNCHRONOUS CLOCK MODE (MACROCELLS)



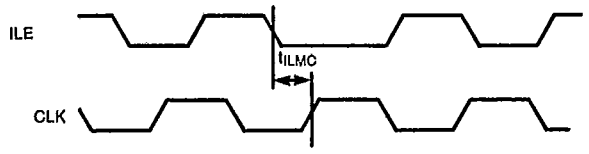
Switching Waveforms (Continued)

ASYNCHRONOUS CLOCK MODE (INPUT STRUCTURE)



NOTE: WHEN ILE GOES HIGH BEFORE DATA IS VALID, USE t_{PD} INSTEAD OF t_{AILO1}

INPUT CLOCK-TO-MACROCELL CLOCK TIMING



NOTES: t_r AND t_f < 6ns
t_{CL} and t_{CH} MEASURED AT 0.3V AND 2.7V
ALL OTHER TIMING AT 1.5V
INPUT VOLTAGE LEVELS AT 0V AND 3V