Preliminary

CS-7100

CS-7100

5V, 250mA Voice Coil Motor Driver with H-bridge and Head Retraction Circuitry

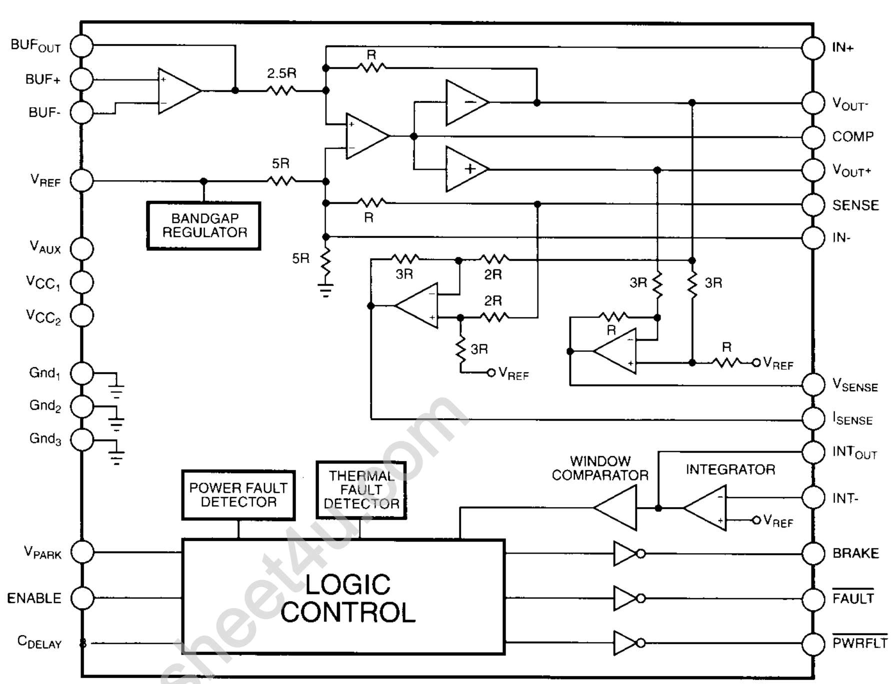
Description

The CS-7100 is a voice coil power driver intended for use in 5V 2.5 inch hard disk servo systems. The CS-7100 contains the complete H-Bridge power amplifier, including the 4 power transistors, and all control functions. Head retraction circuitry is provided to allow for a controlled shutdown of the drive. Power Fault, Over Velocity Fault, and Thermal Fault Detection are also included.

Absolute Maximum Ratings

V_{CC_1}, V_{CC_2}	10V
Auxiliary Supply, V_{AUX}	17V
Logic Input Voltage	-0.3V to V_{AUX}
Logic Output Voltage	-0.3V to 17V
Maximum Junction Temperature	150°C
Maximum Power Dissipation	700mW
H-Bridge Output Current	350mA
Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to +70°C

Block Diagram

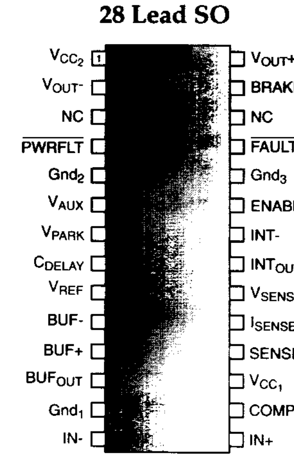


Features

- **Single 5 Volt Power Supply**
- **Full 250mA H-Bridge**
- **On Chip Transient Protection**
- **Low System Offset Current (<1mA)**
- **Low Supply Current (6mA)**
- **Low Current Standby Mode**
- **All Amplifiers Internally Compensated**
- **No Crossover Distortion**
- **Timed Stop/Retract/Brake Sequence**
- **Programmable Retract Voltage**
- **Programmable System Bandwidth**
- **Bandgap-based Power Fault Detector**
- **Over Velocity Detection**
- **On Chip Thermal Protection**

Package Options

28 Lead SO



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Electrical Characteristics: V_{CC} = 4.5V to 5.5V, T_A = 0 to 70°C, Unless otherwise specified					
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Power Supply					
Supply Voltage Range V_{CC_1} and V_{CC_2}		4.5	5.0	5.5	V
Total Supply Current (I_{CC}+ I_{AUX}) V_{ENABLE} = 2.0V (Track Following)			6.0	15.0	mA
V_{ENABLE} = 0.8V				2.0	mA
Auxiliary Voltage, V_{AUX}		2.0		15	V
Auxiliary Current, I_{AUX} V_{CC} = 0, V_{AUX} = 5.0V				15	mA
■ Logic I/O					
Logic HI Input Current	V_{IN} = 2.0V			100	μA
Logic LOW Input Current	V_{IN} = 0.8V			-100	μA
Logic HI Input Voltage			1.5	2.0	V
Logic LOW Input Voltage		0.8	1.5		V
$\overline{BRAKE}$	I_{OUT} = 100μA			0.4	V
$\overline{FAULT}$	I_{OUT} = 100μA			0.4	V
$\overline{PWRFAULT}$	I_{OUT} = 100μA			0.4	V
■ Voltage Reference					
V_{REF}		2.40	2.50	2.60	V
Output Current		2.0			mA
PSRR		40			dB
■ Closed Loop System (R_{SENSE} = 2Ω)					
Transconductance (Buffer amplifier set for Gain = 1.0) (T_A = 25°C) I_{OUT} = 200mA		190	200	210	mA/V
(T_A = 0 to 70°C) I_{OUT} = 200mA		186	200	214	mA/V
Output Offset Current	T_A = 25°C			1.0	mA
Output Offset Current	T_A = 0 to 70°C			1.25	mA
Input Voltage Range		0.00		3.50	V
Frequency Response		30			kHz
■ H-Bridge Amplifier					
Voltage Gain			14		V/V
Frequency Response		60			kHz
Bridge Output Current		250			mA
Quiescent Bias Current (per Side)			2		mA
Bridge Saturation Voltage, I_{OUT} = 100mA, T_A = 25°C				0.25	V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics: continued					
■ **H-Bridge Amplifier (continued)**					
Bridge Saturation Voltage, I_{OUT} =200mA, (T_A= 0 to 70°C)				0.60	V
Thermal Shutdown Temp.			150		°C
■ **Buffer Amplifier**					
Open Loop Gain		60			dB
Input Offset Voltage				5	mV
Input Bias Current				5.0	µA
Unity Gain Bandwidth		300	500		kH_Z
PSRR		50			dB
Input Common Mode Range		0.0		3.5	V
Output Voltage Range		0.1		3.5	V
■ **Current Sensing Amplifier**					
Closed Loop Gain	V_{IN} = (V_{OUT}-) - (SENSE)	1.45	1.50	1.55	V/V
Input Offset Voltage				5	mV
■ **Voltage Sensing Amplifier**					
Closed Loop Gain	V_{IN} = (V_{OUT}-) - (SENSE)	0.322	0.333	0.344	V/V
Input Offset Voltage				5	mV
■ **Sum/Integrator Amplifier**					
Open Loop Gain		60			dB
Unity Gain Bandwidth		300	500		kH_Z
Input Offset Voltage				5	mV
Common Mode Range		0.5		4.0	V
■ **Fault Comparator**					
Upper Threshold V_{UPPER} - V_{REF}	T_A = 25°C	0.63	0.70	0.77	V
Lower Threshold V_{REF} - V_{LOWER}	T_A = 25°C	0.63	0.70	0.77	V
Temperature Coefficient			-0.33		%/C
■ **Power Fault Level**					
V_{PWRFLT}		3.75	4.00	4.25	V
Hysteresis			100	200	mV
■ **Power Fault Timer**					
Charging Current		0.6	1.0	1.4	µA
Park Voltage Threshold			0.55		V
Brake Voltage Threshold			1.10		V

Electrical Characteristics: continued

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Head Park					
V_{PARK}	$R_{PARK} = 5k\Omega$	0.4	0.5	0.6	V
Output Current		10			mA
■ Head Brake					
$V_{OUT}+$	$I_{OUT} = 50mA$			0.3	V
$V_{OUT}-$	$I_{OUT} = 50mA$			0.3	V

Package Pin Description

PACKAGE PIN #	PIN SYMBOL	FUNCTION
28 Lead SO		
17	V_{CC_1}	Positive power supply, 4.5V to 5.5V.
13	Gnd_1	Analog ground.
6	V_{AUX}	Auxiliary power supply for head park during supply line failure.
1	V_{CC_2}	Positive power supply for the H-Bridge driver.
5	Gnd_2	Ground for the H-Bridge driver.
24	Gnd_3	Ground for the H-Bridge driver.
9	V_{REF}	Internal voltage reference for external DAC.
7	V_{PARK}	Voltage that is programmed by an external resistor and is applied across the VCM during park.
12	BUF_{OUT}	Output of the buffer amplifier and input to the transconductance amplifier.
10	BUF-	Negative input to the buffer amplifier.
11	BUF+	Positive input to the buffer amplifier.
23	ENABLE	Digital input to select standby of full power mode.
8	C_{DELAY}	A timing pin where an external capacitor sets the park and spin brake intervals.
25	$\overline{FAULT}$	Open collector NPN output. A digital output signaling an over velocity or a thermal fault condition. Reset by the ENABLE pin.
27	BRAKE	Open collector NPN output. A digital output to brake the spin motor. High indicates brake.
4	$\overline{PWRFAULT}$	Open Collector NPN output. Low indicates power fault.
21	INT_{OUT}	Output of the velocity integration amplifier.
22	INT-	Negative input of the velocity integration amplifier.
20	V_{SENSE}	Output of the amplifier sensing the total bridge voltage.
19	I_{SENSE}	Output of the amplifier sensing the VCM current.
14	IN-	Negative input of the transconductance amplifier.
15	IN+	Positive input of the transconductance amplifier.
2	$V_{OUT}-$	Negative output of H-Bridge.
28	$V_{OUT}+$	Positive output of H-Bridge.
18	SENSE	Current sense input from the current sense resistor.
16	COMP	Compensation node for the transconductance amplifier.
3, 26	NC	No connection.

Circuit Description

Power Supply

Power supply pins V_{CC_1} and V_{CC_2} must be connected together externally. V_{AUX} can be connected to V_{CC} or to a Park voltage source. During normal operation where the Park source is not active, the V_{AUX} is internally powered from the V_{CC} line. Gnd_1, Gnd_2, and Gnd_3 must all be connected to system ground.

Over Velocity Control

The over velocity control loop consists of three operational amplifiers and a dual level detector with internally controlled thresholds. One amplifier provides a voltage which tracks the VCM current, one amplifier provides a voltage which tracks the H-Bridge output voltage. The third amplifier is configured as a summer or an integrator. The output of the integrator is compared to preset limits, and when an over velocity condition occurs, a latched state is set that shuts down the power amplifier and initiates a head brake. This latched condition can be reset by toggling the ENABLE pin low then high.

The current sensing amplifier provides a voltage which is 1.5 times the voltage across R_{SENSE} and is referenced to V_{REF}. The gain of this amplifier is set by internal resistors.

The voltage sensing amplifier provides a voltage which is one third the voltage across the H-Bridge and is referenced to V_{REF}. The gain of this amplifier is set by internal resistors.

The integrator amplifier is configured to sum and integrate the voltages from the voltage and current sensing amplifiers and provide an output to the comparators. External components control the gain and time constant of the integrator.

The fault comparator is used to compare the output of the integrator amplifier to a pair of voltages that represent over velocity. If either limit is exceeded, the fault latch is set and a head brake is initiated. The comparator threshold voltage is set internally.

Transconductance Loop

The transconductance loop consists of a full H-Bridge output stage, a low offset error amplifier, precision internal gain setting resistors, and an input buffer amplifier. A single current sense resistor is used to set the transconductance.

The buffer amplifier is a low offset operational amplifier which can be configured as a gain stage or as a second order low pass filter.

The error amplifier is a low offset operational amplifier. Access is provided to all three terminals to allow programming of the overall system response.

The power amplifier is a full H-Bridge with 250mA capability, and built in transient protection diodes. The differential voltage gain is 14. Class AB bias is used to eliminate crossover distortion.

The power amplifier is protected from overload by thermal shutdown circuitry. Should a thermal overload occur, the H-Bridge amplifier will turn off until the ENABLE line is toggled low then high.

Power Fault Detector

The power fault detector monitors the V_{CC} line. Should an under voltage condition occur, the $\overline{PWRFAULT}$ will switch low and a timed sequence will begin. First a head brake will occur, then a head park will occur and finally the BRAKE will switch high initiating a spin brake. If the power recovers during the sequence, the head brake and park will complete their cycles, but the spin brake will be cancelled.

Power Fault Timer

The power fault timer uses an internally generated charge current and an external capacitor to control the timing of the head brake, park and spin brake sequence. Two threshold levels are used to create three time sequences. While the capacitor is charging to the first level, a head brake is initiated by turning on both H-Bridge NPN power transistors. While the capacitor voltage is between the first and second levels, a head park is initiated by turning on one H-Bridge NPN power transistor and applying a controlled voltage to the other side of the VCM. When the capacitor voltage exceeds the second threshold, a spin brake is initiated by turning off the BRAKE output. The timer will remain in this state until the V_{CC} line recovers to a level above V_{FAULT}.

Should the power recover while the timer is in the head brake or head park sequence, the timer will complete the head brake and park, but the spin brake will be cancelled. If the power recovers while the timer is in a spin brake mode, the brake will be released.

Head park can only occur due to a power fault. During head park, one side of the H-Bridge is pulled low and a voltage that is set at the V_{PARK} pin is applied across the VCM.

The head brake is implemented by turning on both H-Bridge NPN power transistors. The head brake is turned on by a power fault, an over velocity fault or a thermal shutdown fault. In the case of a thermal shutdown fault, the brake turns on after the chip has cooled below the thermal shutdown temperature.

Logic

The ENABLE pin is used to select full power mode or standby mode. When ENABLE is high, the circuit is in the full power mode. When ENABLE is low, the circuit is in a standby mode with only the logic powered.

The BRAKE output is an open collector NPN transistor which is intended to drive an external FET spin brake circuit.

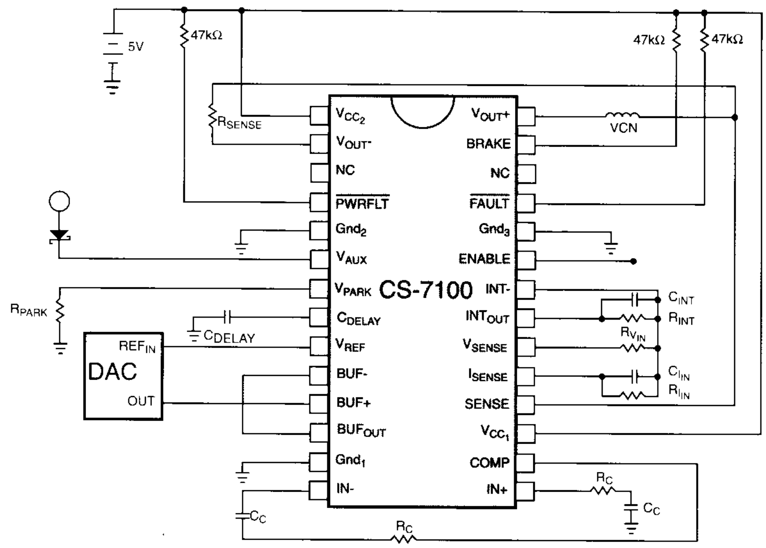
The $\overline{FAULT}$ line is an open collector NPN transistor which is intended to provide a system reset.

The PWRFAULT line is an open collector NPN transistor which indicates a low power condition.

Voltage Reference

A bandgap voltage source is used to provide the reference for the power fault detector and for the 2.5V transconductance reference voltage.

Application Diagram



Package Specification

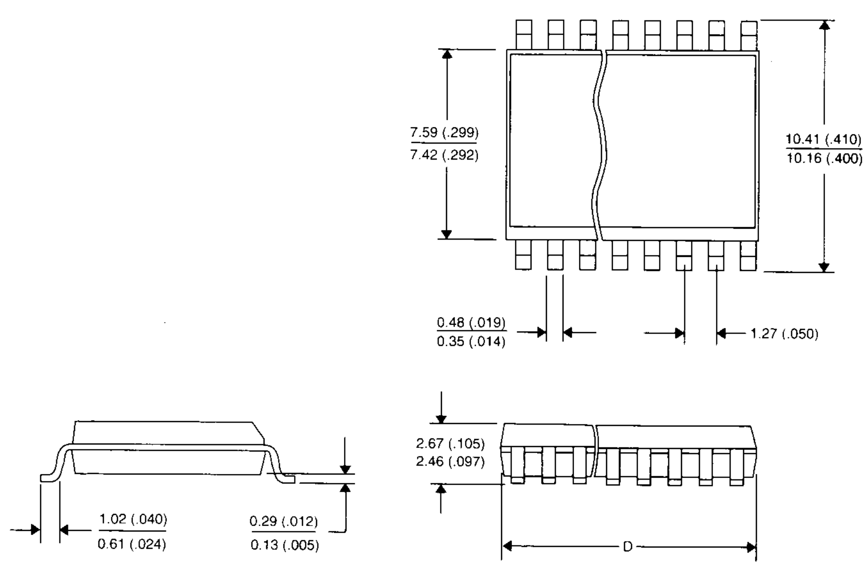
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D Metric Max	D Metric Min	D English Max	D English Min
28 Lead SO	18.06	17.81	.711	.701

PACKAGE THERMAL DATA

Thermal Data		28 Lead SODW	
$R\Theta_{JC}$	typ	15	°C/W
$R\Theta_{JA}$	typ	75	°C/W

28 Lead SO



Ordering Information

Part Number	Description
CS-7100DW28	SO Wide

Preliminary

This product is in the preproduction stages of the design process. The data sheet contains preliminary data. CSC reserves the right to make changes to the specifications without notice. Please contact CSC for the latest available information.

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