CS-511/511R

4, 6, 8-Channel Ferrite Read/Write Circuit with Enhanced System Write to Read Recovery Time

Description

The CS-511 is a bipolar monolithic integrated circuit designed for use with a center-tapped ferrite recording head. It provides a low noise read path, write current control, and data protection circuitry for as many as 8 channels. The CS-511 requires +5V and +12V power supplies and is available in a variety of packages.

The CS-511R performs the same function as the CS-511 with the addition of internal 750 Ω damping resistors.

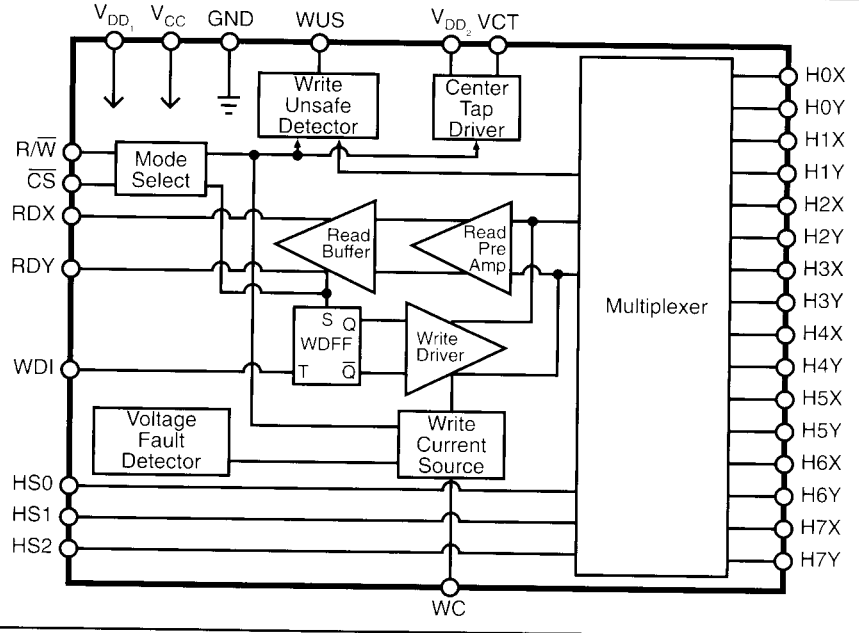
Features

- **High Performance:**
  Read Mode Gain = 100V/V
  Input Noise = 1.5nV/√Hz Maximum
  Write Current Range = 10mA to 40mA
- **Enhanced System Write to Read Recovery Time**
- **Power Supply Fault Protection**
- **Programmable Write Current Source**
- **Write Unsafe Detection**
- **+5V, +12V Power Supplies**

Absolute Maximum Ratings (All voltages referenced to GND). Currents into device are positive.

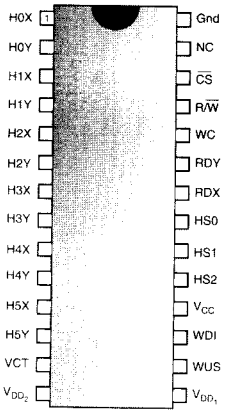
DC Supply Voltage (V_{DD_1})	-0.3 to +14V_{DC}
(V_{DD_2})	-0.3 to +14V_{DC}
(V_{CC})	-0.3 to +6 V_{DC}
Digital Input Voltage Range (V_{IN})	-0.3 to V_{CC} +0.3V_{DC}
Head Port Voltage Range (VH)	-0.3 to V_{DD_1} +0.3V_{DC}
WUS Pin Voltage Range (V_{WUS})	-0.3 to +14V_{DC}
Write Current (IW) Zero Peak	60mA
Output Current RDX, RDY (I_O)	-10mA
VCT	-60mA
WUS	+12mA
Storage Temperature Range(T_S)	-65 to 150°C
Lead Temperature PDIP (10 sec. Soldering)	260°C
Package Temperature PLCC, SO (20 Sec Reflow)	215°C

Block Diagram

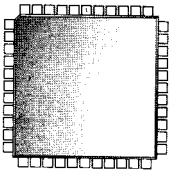


Package Options

28, 32, 34 Lead SO Wide



44 Lead PLCC



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Recommended Operating Conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Supply Voltage (V_{DD_1})		10.8	12.0	13.2	VDC
(V_{CC})		4.5	5.0	5.5	VDC
Head Inductance (Lh)		5		15	µH
Damping Resistor (RD)	(511 only)	500		2000	Ω
RCT Resistor (RCT)*	Iw = 40mA	114	120	126	Ω
Write Current (IW)		10		40	mA
Junction Temperature Range (T_J)		+25		+135	°C

*For Iw = 40mA, At other Iw levels refer to Applications Information that follows this specification.

DC Characteristics: Unless otherwise specified, recommended operating conditions apply.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Power Supply					
V_{CC} Supply Current					
Read/Idle	Read/Idle Mode			35	mA
Write	Write Mode			30	mA
V_{DD} Supply Current					
Idle	Idle Mode			20	mA
(sum of V_{DD_1} and V_{DD_2})					
Read	Read Mode			35	mA
Write	Write Mode			20+Iw	mA
Power Dissipation	T_J = +125°C				
Idle	Idle Mode			400	mW
Read	Read Mode			600	mW
Write	Write Mode, IW = 40mA, RCT = 0Ω			800	mW
	Write Mode, IW = 40mA, RCT = 120Ω			610	mW
■ Digital I/O					
VIL, Input Low Voltage				0.8	VDC
VIH, Input High Voltage		2.0		VCC +0.3	VDC
IIL, Input Low Current	VIL = 0.8V	-0.4			mA
IIH, Input High Current	VIH=2.0V			100	µA
VOL, WUS Output, Low Voltage	IOL = 8mA			0.5	VDC
IOH, WUS Output High Current	VOH = 5.0V			100	µA
■ Write Mode					
Center Tap Voltage (VCT)	Write Mode		6.0		VDC
Head Current (per side)	Write Mode, $0 \le V_{CC} \le 3.7V$, $0 \le V_{DD_1} \le 8.7V$	-200		200	µA
Write Current Range		10		40	mA
Write Current Constant "K"		2.375		2.625	
Iwc to Head Current Gain			0.99		mA/mA
Unselected Head Leakage Current				85	µA
RDX, RDY Output Offset Voltage	Write/Idle Mode	-20		+20	mV

DC Characteristics: continued

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Write Mode (continued)					
RDX, RDY Common Mode Output Voltage	Write/Idle Mode		5.3		VDC
RDX, RDY Leakage	RDX, RDY = 6V Write/Idle Mode	-100		100	µA
■ Read Mode					
Center Tap Voltage	Read Mode		4.0		VDC
Head Current (per side)	Read or Idle Mode $0 \le V_{CC} \le 5.5V$ $0 \le V_{DD_1} \le 13.2V$	-200		200	µA
Input Bias Current (per side)				45	µA
Input Offset Voltage	Read Mode	-4		+4	mV
Common Mode Output Voltage	Read Mode	4.5		6.5	VDC

Dynamic Characteristics and Timing: Unless otherwise specified, recommended operating conditions apply and IW = 35mA, Lh = 10µH, Rd = 750Ω CS-511 only, f(WDI) = 5MHz, CL (RDX, RDY) ≥ 20pF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Write Mode					
Differential Head Voltage Swing		7.0			V(pk)
Unselected Head Transient Current				2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	511 511R	10 600		 960	kΩ Ω
WDI Transition Frequency	WUS = low	250			kHz
■ Read Mode					
Differential Voltage Gain	V_{IN} = 1mV_{pp} @ 300 kHz RL (RDX), RL (RDY) = 1kΩ	85		115	V/V
Dynamic Range	DC Input Voltage, V_I, Where Gain Falls by 10%. $V_{IN} = V_I$+0.5mV_{pp} @ 300kHz	-3		+3	mV
Bandwidth (-3db)	$\|Zs\| < 5\Omega$, V_{IN} = 1mV_{pp}	30			MHz
Input Noise Voltage	BW = 15MHz, Lh = 0, Rh = 0			1.5	nV/√Hz
Differential Input Capacitance	f = 5MHz			20	pF
Differential Input Resistance	f = 5MHz 511 511R	2 460		 860	kΩ Ω
Common Mode Rejection Ratio	V_{CM} = VCT + 100mV_{pp} @ 5MHz	50			db
Power Supply Rejection Ratio	100mV_{pp} @ 5MHz on V_{DD_1}, V_{DD_2}, or V_{CC}	45			db
Channel Separation	Unselected Channels: V_{IN} = 100mV_{pp} @ 5MHz & Selected Channel: V_{IN} = 0mV_{pp}	45			db
Single Ended Output Resistance	f = 5MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	±2.1			mA

Dynamic Characteristics and Timing: continued

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Switching Characteristics					
R/$\overline{W}$ to Write	Delay to 90% of Write Current			1.0	µs
R/$\overline{W}$ to Read	Delay to 90% of 100mV 10MHz Read Signal Envelope or to 90% Decay of Write Current			1.0	µs
$\overline{CS}$: $\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100mV 10MHz Read Signal Envelop			1.0	µs
$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current			1.0	µs
HS0 HS1 to any Head HS2	Delay to 90% of 100mV 10MHz Read Signal Envelope			1.0	µs
WUS: Safe to Unsafe - TD1	Iw = 35mA	1.6		8.0	µs
Unsafe to Safe - TD2				1.0	µs
Head Current:	Lh = 0µH, Rh = 0Ω			25	ns
Prop. Delay - TD3	From 50% Points				
Asymmetry	WDI has 50% Duty Cycle and 1ns Rise/Fall Time			2	ns
Rise/Fall Time	10% - 90% Points			20	ns

Package Pin Description

SO Wide 28L	SO Wide 32L	SO Wide 34L	PLCC 44L	Pin Name	Description
1	1	1	1	HOX	X, Y head connections
2	2	2	2	HOY	X, Y head connections
3	3	3	5	H1X	X, Y head connections
4	4	4	6	H1Y	X, Y head connections
5	5	5	7	H2X	X, Y head connections
6	6	6	8	H2Y	X, Y head connections
7	7	7	9	H3X	X, Y head connections
8	8	8	10	H3Y	X, Y head connections
9	9	9	11	H4X	X, Y head connections
10	10	10	12	H4Y	X, Y head connections
11	11	11	13	H5X	X, Y head connections
12	12	12	14	H5Y	X, Y head connections
	13	13	15	H6X	X, Y head connections
	14	14	16	H6Y	X, Y head connections
	15	15	19	H7X	X, Y head connections
	16	16	20	H7Y	X, Y head connections
13	17	17	21	VCT	Voltage Center Tap: voltage source for head center tap
14	18	18	22	V_{DD_2}	Positive power supply for the center-tap voltage source
15	19	19	23	V_{DD_1}	+12V
16	20	21	29	WUS	Write Unsafe: a high level indicates an unsafe writing condition
17	21	22	30	WDI	Write Data In: negative transition toggles direction of head current
18	22	23	31	V_{CC}	+5V
19	23	24	32	HS2	Head Select
20	24	25	33	HS1	Head Select
21	25	26	34	HS0	Head Select
22	26	27	35	RDX	X, Y Read Data: differential read signal out

Package Pin Description: continued

SO Wide 28L	SO Wide 32L	SO Wide 34L	PLCC 44L	Pin Name	Description
23	27	28	36	RDY	X, Y Read Data: differential read signal out
24	28	29	37	WC	Write Current: used to set the magnitude of the write current
25	29	30	38	R/$\overline{W}$	Read/Write: a high level selects read mode
26	30	31	42	$\overline{CS}$	Chip Select: a low level enables device
28	32	34	44	Gnd	Ground

Circuit Description

The CS-511 gives the user the ability to address up to 8 center-tapped ferrite heads and provide write drive or read amplification. Head selection and mode control are accomplished using the HSn, $\overline{CS}$, & R/$\overline{W}$ inputs as in tables 1 & 2. Internal pullups are provided for the $\overline{CS}$ & R/$\overline{W}$ inputs to force the device into a non-writing condition if either control line is opened accidentally.

Table 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

Table 2: Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

0=Low Level 1=High level

Write Mode

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the CS-511 as a current switch and activates the Write Unsafe (WUS) Detector circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding read mode selection initializes the Write Data Flip-Flop, WDFF, to pass write current through the "X" side of the head. The zero-peak write current magnitude is programmed by an external resistor Rwc connected from pin WC to Gnd and is given by:

Iw = K/Rwc, where K = Write Current Constant

The Write Unsafe Detection circuitry monitors voltage transitions at the selected head connections and flags any of the following conditions as a high level on the Write Unsafe open collector output:

- Head open
- Head center tap open
- WDI frequency too low
- Device in read mode
- Device not selected
- No write current

Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

To further ensure data security, a voltage fault detection circuit prevents application of write current during power loss or power sequencing.

To enhance Write to Read recovery time the change in RDX, RDY common mode voltage is minimized by biasing these outputs to a level within the read mode range when in write mode.

Power dissipation in write mode may be reduced by placing a resistor (RCT) between V_{DD_1} and V_{DD_2}. Optimum resistor value is 120Ω x 40/Iw (Iw in mA). At low write currents, (<15mA) read mode dissipation is higher than write mode and RCT, though recommended, may not be considered necessary. In this case V_{DD_2} is connected directly to V_{DD_1}.

Read Mode

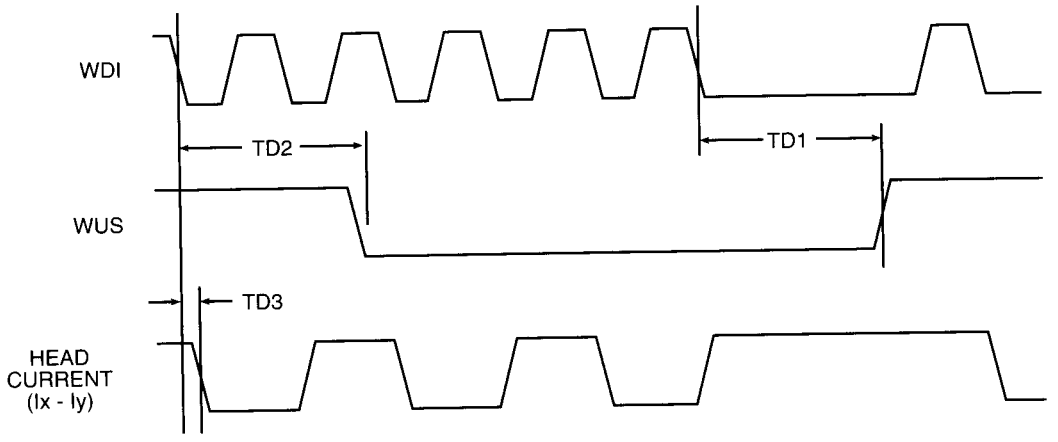
Taking $\overline{CS}$ low and R/$\overline{W}$ high selects read mode which configures the CS-511 as a low noise differential amplifier for the selected head. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The internal write current source is gated off in read mode eliminating the need for any external gating.

Read mode selection also initializes the Write Data Flip-Flop (WDFF) to pass write current through the "X" side of the head at a subsequent write mode selection.

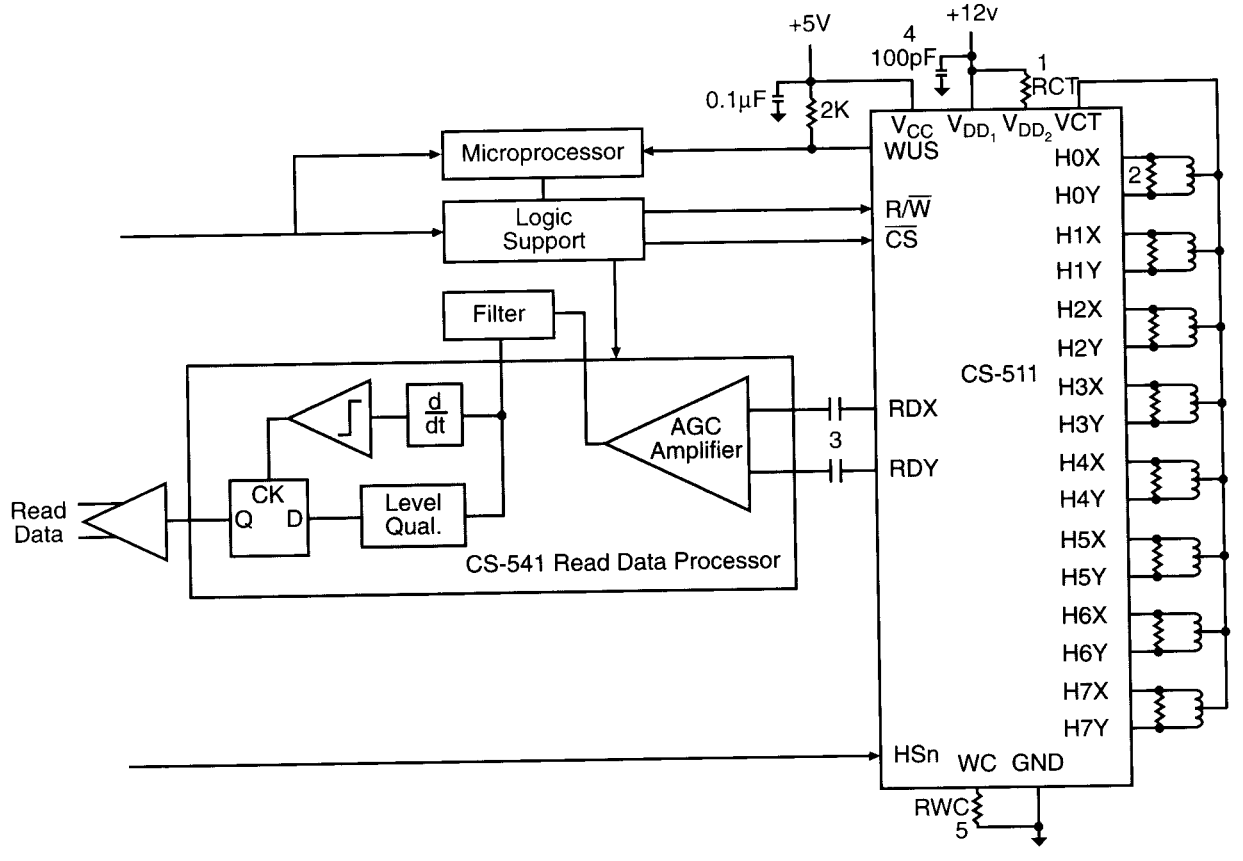
Idle Mode

Taking $\overline{CS}$ high selects the idle mode which switches the RDX, RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wired OR'ed and the Write Current programming resistor to be common to all devices.

Write Mode Timing Diagram



Application Diagram



Notes:

1. An external resistor, RCT, given by; RCT = 120 (40/Iw) where Iw is the zero peak write current in mA, can be used to limit internal power dissipation. Otherwise connect V_{DD_2} to V_{DD_1}.
2. Damping resistors not required on 511R versions.
3. Limit DC current from RDX and RDY to 100µA and load capacitance to 20pF. In multi-chip application these outputs can be wire-OR'ed.
4. The power bypassing capacitor must be located close to the 511 with its ground returned directly to device ground, with as short a path as possible.
5. To reduce ringing due to stray capacitance this resistor should be located close to the 511. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

Package Specification

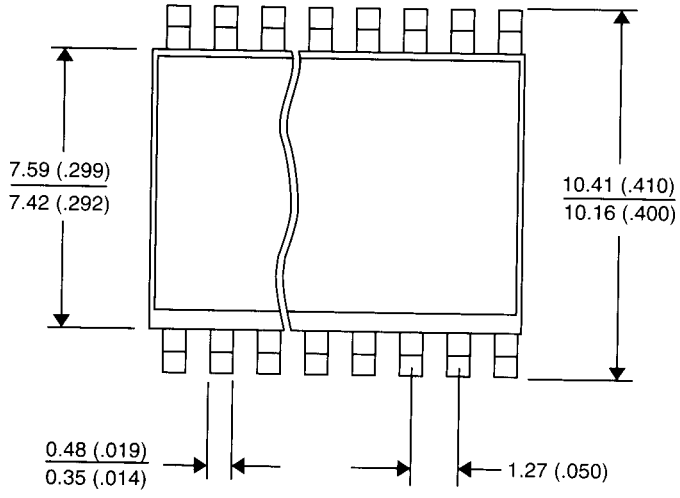
PACKAGE DIMENSIONS IN mm (INCHES)

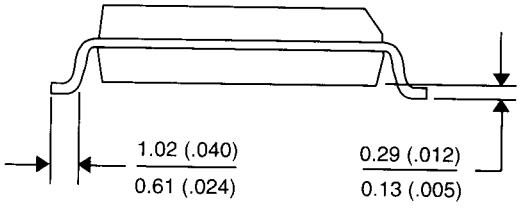
Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
28L SO Wide	18.06	17.81	.711	.701
32L SO Wide	21.04	20.53	.828	.808
34L SO Wide				
44L PLCC (A)	17.65	17.40	.695	.685
44L PLCC (B)	16.61	16.51	.654	.650

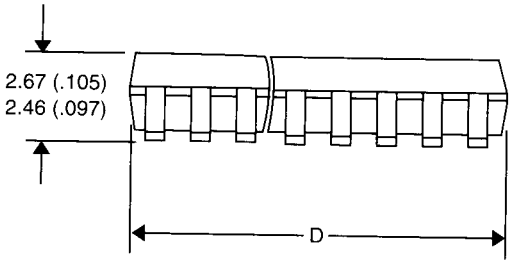
PACKAGE THERMAL DATA

Thermal Data	$R\Theta_{JC}$ typ	$R\Theta_{JA}$ typ	
28L SO	15	75	°C/W
32L SO	15	75	°C/W
34L SO			°C/W
44L PLCC	16	55	°C/W

SO Wide

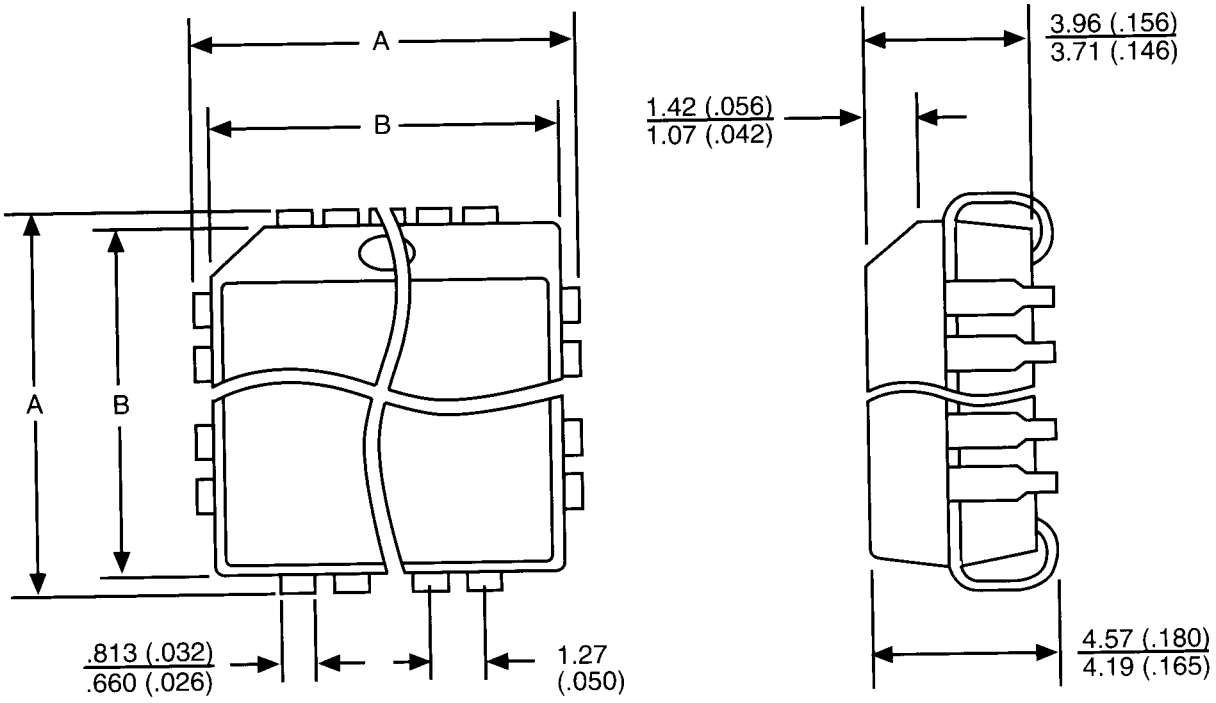






Package Specification: continued

PLCC



Ordering Information

Part Number	Description
CS-511-8MRDW34	34 Lead SO
CS-511-6RDW28	28 Lead SO
CS-511-8RDW32	32 Lead SO
CS-511-8RFN44	44 Lead PLCC

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