AmPAL*22V10-15/22V10-20

T-46-13-47

24-Pin IMOX III™ Programmable Array Logic (PAL)

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- 15-ns performance
- Increased logic power — up to 22 inputs and 10 outputs
- Increased product terms — average 12 per output
- Variable product-term distribution improves ease of use
- Each output user-programmable for registered or combinatorial operation
- Individually user-programmable output polarity
- Extra terms provide logical synchronous-PRESET and asynchronous-RESET capability
- TTL-level PRELOAD for improved testability
- Packaged in 24-pin Slim DIP and 28-pin chip-carrier packages
- Platinum-Silicide fuses ensure high programming yield, fast programming, and unsurpassed reliability
- AC and DC testing done at the factory utilizing special designed-in test features
- 3000-V Input ESD Protection on all pins

GENERAL DESCRIPTION

The AmPAL22V10 is a second-generation Programmable Array Logic (PAL) device. It utilizes the familiar sum-of-products (AND-OR) logic structure, allowing users to program custom logic functions. The AmPAL22V10 is an extension of the PAL concept. First-generation devices were largely limited to TTL-replacement applications. The AmPAL22V10 permits the development of custom LSI functions of 500 to 800 equivalent gate complexity.

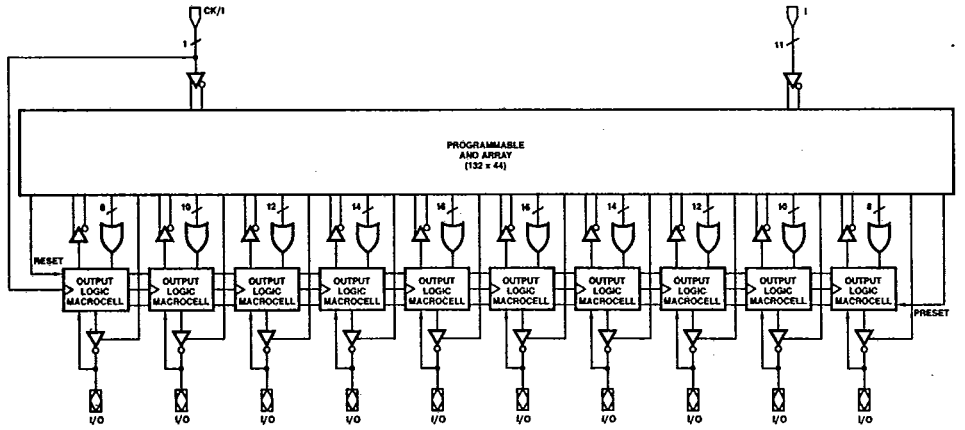
The AmPAL22V10 contains up to 22 inputs and 10 outputs. It incorporates the unique capability of defining and programming the architecture of each output on an individual basis. Each output is user-programmable for either registered or combinatorial operation. This allows the designer to optimize the device design by having only as many registers as needed. In addition, each output has user-programmable output polarity, further simplifying design and contributing to the precise application requirements.

Increased logic power has been built into the AmPAL22V10 by increasing the number of product terms from 8-per-output to an average of 12-per-output. Further innovation can be seen in the introduction of variable product-term distribution. This technique allocates from 8 to 16 logical product terms to each output (please refer to the Block Diagram for distribution details). This variable allocation of terms allows far more complex functions to be implemented than in previous devices.

System operation has been enhanced by the addition of a synchronous-PRESET and an asynchronous-RESET product term. These terms are common to all output registers.

The AmPAL22V10 also incorporates power-up RESET and the unique capability to PRELOAD the output registers to any desired state during testing. PRELOAD is essential to permit full logical verification during test.

BLOCK DIAGRAM



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IMOX is a trademark of Advanced Micro Devices, Inc.

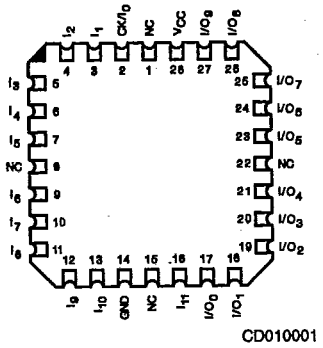
Publication #	Rev.	Amendment
08601	B	/0

Issue Date: September 1987

CONNECTION DIAGRAM
Top View

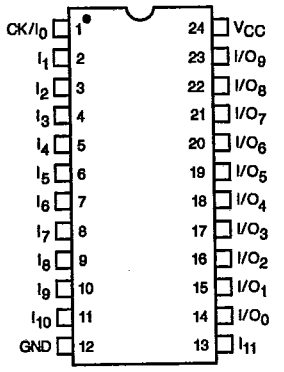
T-46-13-47

LCC*



CD010001

DIPs**



CD010011

*Also available in PLCC. Pinouts identical to LCC.
**Also available in Flatpack. Pinouts identical to DIPs.

Pin Designations: I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
GND = Ground
CK = Clock
NC = No Connection

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed/Power Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AMPAL22V10 -15 P C -

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +75°C)
E = Extended Commercial (–55 to +125°C)

c. PACKAGE TYPE
P = 24-Pin Slim Plastic DIP (PD3024)
D = 24-Pin Slim Ceramic DIP (CD3024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

b. SPEED/POWER OPTION
–15 = 15 ns (Full Power)

a. DEVICE NUMBER/DESCRIPTION
AmPAL22V10-15
24-Pin IMOX III Programmable Array Logic

Valid Combinations	
AMPAL22V10-15	PC, DC, DCB, DE, JC, LC, LE

Valid Combinations

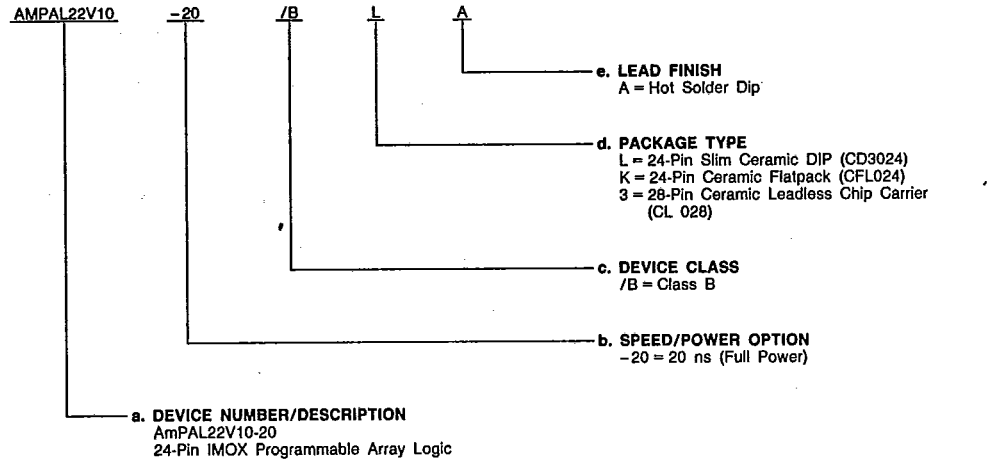
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

T-46-13-47

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed/Power Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AMPAL22V10-20	/BLA/B3A/BKA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, and 11.

FUNCTIONAL DESCRIPTION

The AmPAL22V10 is a second-generation Programmable Array Logic device. It contains a programmable fuse array organized in the familiar sum-of-products (AND-OR) structure.

The block diagram below shows the basic architecture of the AmPAL22V10. There are up to 22 inputs and 10 outputs available. The inputs are connected to a programmable-AND array which contains 120 logical product terms. Initially the AND gates are connected, via fuses, to both the TRUE and COMPLEMENT of every input. By selective programming of fuses, the AND gates may be "connected" to only the TRUE input (by blowing the COMPLEMENT fuse), to only the COMPLEMENT input (by blowing the TRUE fuse), or to neither type of input (by blowing both fuses), establishing a logical "don't care." When both the TRUE and COMPLEMENT fuses are left intact, a logical FALSE results on the output of the AND gate. An AND gate with all fuses blown will assume the logical-TRUE state. The outputs of the AND gates are connected to fixed-OR gates. There is an average of 12 product terms per OR gate (output), and as the Block Diagram shows, variable product term distribution has been implemented. This technique allocates different quantities of logical product terms to different outputs, allowing more complex logical functions to be performed than were previously possible. Up to 16 logical terms can be evaluated in one output in a single clock cycle (no feedback necessary).

Output Logic Macrocells (OLMs) T-46-13-47

A dramatic innovation in logic design is the implementation on the AmPAL22V10 of variable output architecture. This allows the user to program, on an output-by-output basis, the function of the outputs. As shown in the Output Logic Macrocell (OLM) diagram below, each output cell contains two additional fuses, S_0 and S_1. S_1 controls whether the output will be registered or combinatorial. S_0 controls the output polarity (active HIGH or active LOW). Depending on the states of these two fuses, an individual output will operate in one of four modes (see the logic diagrams on the next page): Registered/Active LOW, Registered/Active HIGH, Combinatorial/Active LOW, and Combinatorial/Active HIGH (note that the feedback path also changes with output mode). This innovation gives the designer more flexibility and enables optimization of the device for precise application requirements. It also allows for better device utilization — programming only as many registers as are needed.

PRESET/RESET

To improve in-system functionality, the AmPAL22V10 has additional PRESET and RESET product terms. These terms are connected to all registered outputs. When the synchronous-PRESET product term is asserted (HIGH), the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the asynchronous-RESET product term is asserted (HIGH), the output registers will be immediately loaded with a LOW (independent of the clock). These functions are particularly useful for applications such as system power-on and reset.

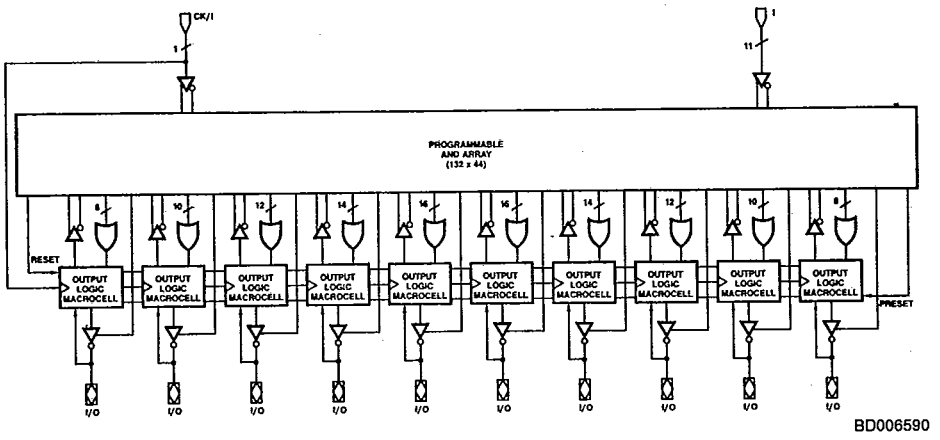
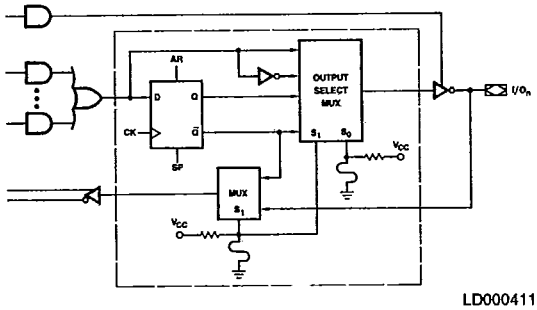


Figure 1. Block Diagram



S_1	S_0	Output Configuration
0	0	Registered/Active LOW
0	1	Registered/Active HIGH
1	0	Combinatorial/Active LOW
1	1	Combinatorial/Active HIGH

0 = Unblown Fuse
1 = Blown Fuse

Figure 2. Output Logic Macrocell Diagram

PRELOAD

To simplify testing, the AmPAL22V10 is designed with unique PRELOAD circuitry that provides an easy method of testing registered devices for logical functionality. PRELOAD allows any arbitrary state value to be loaded into the output registers.

A typical functional test sequence would be to verify all possible state transitions for the device being tested. To verify these transitions requires the ability to set the state registers into an arbitrary "present state" value, and to set the device inputs to any arbitrary "present input" value. Once this is done, the state machine is then clocked into a new state, or "next state." The next state is then checked to validate the transition from the present state. In this way any state transition can be checked.

Without PRELOAD, it is difficult and in some cases impossible to load an arbitrary present state value. This can lead to logic verification sequences that are either incomplete or excessively long. Long test sequences result when the feedback from the state register "interferes" with the inputs, forcing the state machine to go through many state transitions before it can reach an arbitrary state value. Therefore the test sequence will be mostly state initialization and not actual testing. The test sequence becomes excessively long when a state must be re-entered many times to test a wide variety of input combinations.

In addition, complete logic verification may become impossible when states that need to be tested cannot be entered with normal state transitions. For example, the state which the machine powers-up into cannot be tested because it cannot be entered from the main sequence. Similarly, "forbidden" or don't care states that are not normally entered need to be tested to ensure that they return to the main sequence.

PRELOAD eliminates these problems by providing the capability to go directly to any desired arbitrary state. Thus test sequences may be greatly shortened, and all possible states can be tested, greatly reducing test time and development costs, and guaranteeing proper in-system operation.

Fabrication

T-46-13-47

The AmPAL22V10-15 is manufactured using Advanced Micro Devices' IMOX III slot-isolation process. This advanced process is an extension of the IMOX II process. It uses slot isolation between transistors to permit an increase in density and a decrease in internal capacitance, resulting in the fastest possible programmable-logic devices.

These devices are fabricated with AMD's fast programming, highly reliable Platinum-Silicide Fuse technology. Utilizing an easily implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Extra test words are preprogrammed during manufacturing to ensure extremely high field programming yields (> 98.5%), and to provide extra test paths to achieve excellent parametric correlation.

Platinum Silicide was selected as the fuse-link material to achieve a well-controlled melt rate resulting in large nonconductive gaps that ensure very stable, long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible-link programmable logic.

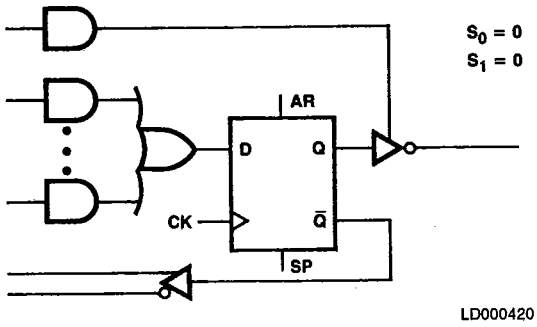


Figure 3-1. Registered/Active LOW

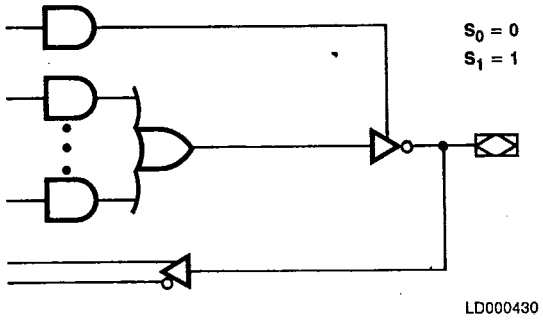


Figure 3-3. Combinatorial/Active LOW

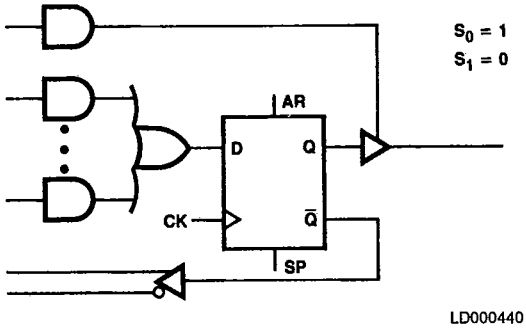


Figure 3-2. Registered/Active HIGH

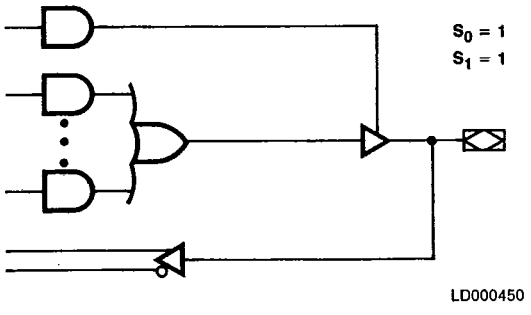


Figure 3-4 Combinatorial/Active HIGH

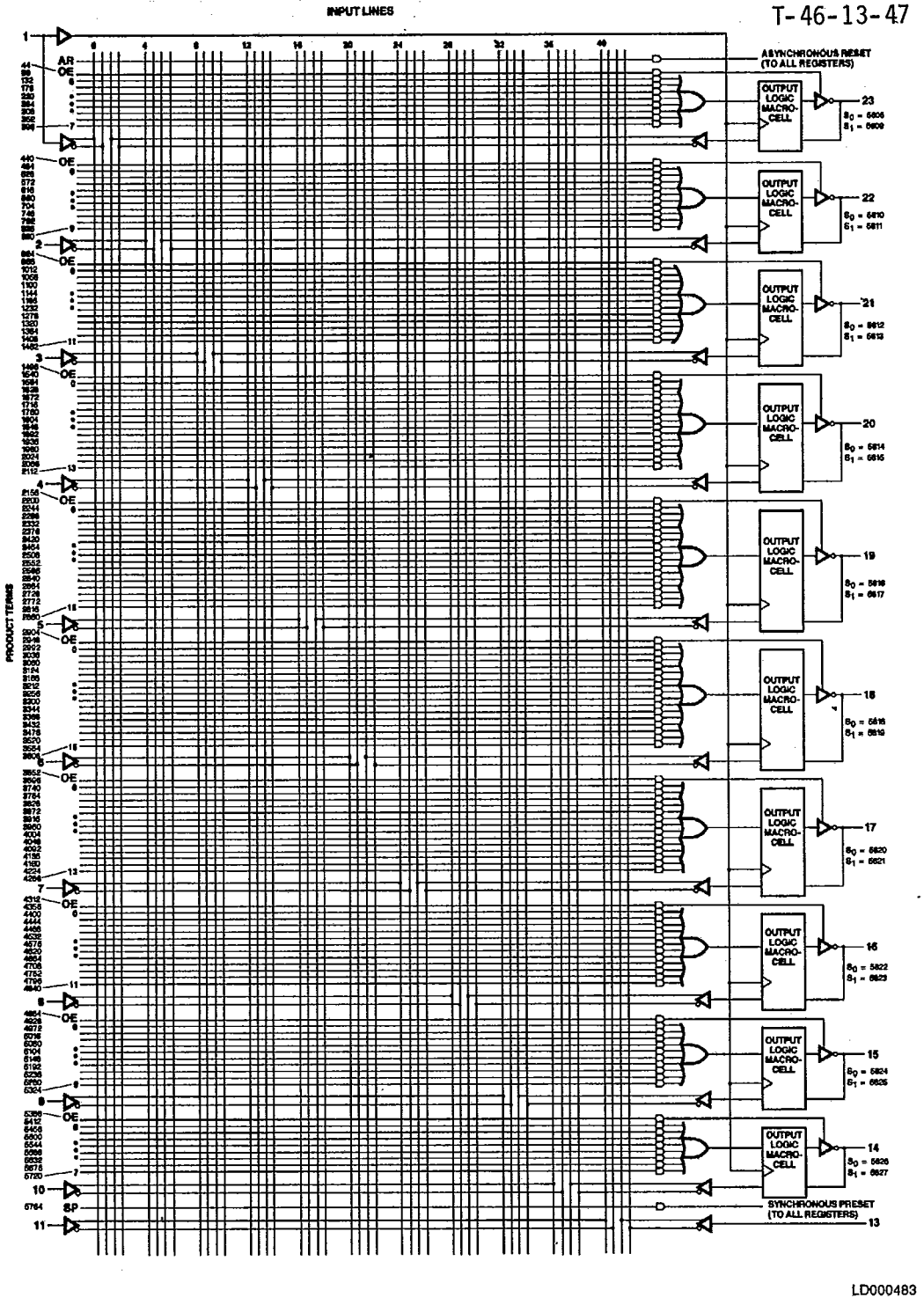


Figure 4. Logic Diagram — JEDEC Fuse Numbering

ABSOLUTE MAXIMUM RATINGS T-46-13-47

Storage Temperature ..... −65 to +150°C
Supply Voltage to Ground Potential
(Pin 24 to Pin 12) Continuous ..... −0.5 to +7 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 16 V
Output Current into Outputs During Programming
(Max. Duration of 1 sec) ..... 200 mA
DC Input Voltage ..... −0.5 to +5.5 V
DC Input Current ..... −30 to +5 mA
Ambient Temperature with Power Applied ..... +125°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) Operating Free Air ..... 0°C to +75°C
Supply Voltage (V_{CC}) ..... +4.75 to +5.25 V

Extended Commercial (E) Devices
Temperature (T_A) ..... −55°C Min.
Temperature (T_C) ..... +125°C Max.
Supply Voltage (V_{CC}) ..... +4.50 to +5.50 V

Military (M) Devices*
Temperature (T_A) ..... −55°C Min.
Temperature (T_C) Operating Case ..... +125°C Max.
Supply Voltage (V_{CC}) ..... +4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military Product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions				Min.	Typ. (Note 1)	Max.	Unit
			COM'L	MIL & E-COM'L					
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	I_{OH} = −2 mA		2.4	3.5		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	I_{OL} = 12 mA				0.50	V
V_{IH} (Note 2)	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for all Inputs				2.0			V
V_{IL} (Note 2)	Input LOW Level	Guaranteed Input Logical LOW Voltage for all Inputs						0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V					−20	−100	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V						25	μA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = 5.5 V						1.0	mA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.5 V (Note 3)				−30	−50	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max.			B		150	180	mA
					AL		75	90	
					Q		40	55	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA					−0.9	−1.2	V
I_{OZH}	Output Leakage Current (Note 4)	V_{CC} = Max., V_{IN} = V_{IL} or V_{IH}	V_O = 2.7 V					100	μA
I_{OZL}			V_O = 0.4 V					−100	

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.
4. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).
5. Pinout for DIPs only.

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Unit
C_{IN} †	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz (Note 5)	Pins 1, 13		9		pF
			Others		6		
C_{OUT} †	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz			9		

† Not included in Group A tests.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Note 1)

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No.	Parameter Symbol	Parameter Description	22V10-15						Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{PD}	Input or Feedback to Non-Registered Output		15					ns
2	t_{EA}	Input to Output Enable		15					ns
3	t_{ER}	Input to Output Disable		15					ns
4	t_{CO1}	Clock to Output		12					ns
5	t_{CO2}	Register Feedback through Array to Combinatorial Output, Relative to External Clock		22					ns
6	t_S	Input or Feedback Setup Time	13						ns
7	t_H	Hold Time	0						ns
8	t_P	Clock Period ($t_S + t_{CO1}$)	25						ns
9	t_{WH}	Clock Width – HIGH Level	10						ns
10	t_{WL}	Clock Width – LOW Level	10						ns
11	f_{MAX}	Maximum Frequency		40					ns
12	t_{AW}	Asynchronous – RESET Width	15						ns
13	t_{AR}	Asynchronous – RESET Recovery Time	15						ns
14	t_{AP}	Asynchronous – RESET to Registered Output		20					ns

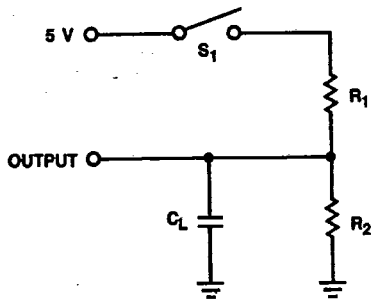
SWITCHING CHARACTERISTICS over MILITARY and EXTENDED-COMMERCIAL operating ranges (for APL Products, Group A, Subgroups 7, 8, 9, 10, 11 are tested unless otherwise noted) (Note 2)

No.	Parameter Symbol	Parameter Description	22V10-20						Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{PD}	Input or Feedback to Non-Registered Output		20					ns
2	t_{EA}	Input to Output Enable		20					ns
3	t_{ER}	Input to Output Disable		20					ns
4	t_{CO1}	Clock to Output		15					ns
5	t_{CO2}	Register Feedback through Array to Combinatorial Output, Relative to External Clock		30					ns
6	t_S	Input or Feedback Setup Time	17						ns
7	t_H	Hold Time	0						ns
8	t_P	Clock Period ($t_S + t_{CO1}$)	32						ns
9	t_{WH}	Clock Width – HIGH Level	15						ns
10	t_{WL}	Clock Width – LOW Level	15						ns
11	f_{MAX}	Maximum Frequency		31					ns
12	t_{AW}	Asynchronous – RESET Width	20						ns
13	t_{AR}	Asynchronous – RESET Recovery Time	20						ns
14	t_{AP}	Asynchronous – RESET to Registered Output		25					ns

Notes: 1. Commercial Test Conditions: $R_1 = 300$, $R_2 = 390$.
2. Military/Extended-Commercial Test Conditions: $R_1 = 390$, $R_2 = 750$.
3. t_{PD} is tested with switch S_1 closed and $C_L = 50$ pF.
4. For three-state outputs, output enable times are tested with $C_L = 50$ pF to the 1.5 V level; S_1 is open for high-impedance to HIGH tests and closed for high-impedance to LOW tests. Output disable times are tested with $C_L = 5$ pF. HIGH to high-impedance tests are made to an output voltage of $V_{OH} - 0.5$ V with S_1 open; LOW to high-impedance tests are made to the $V_{OL} + 0.5$ V level with S_1 closed.

SWITCHING TEST CIRCUIT

T-46-13-47



TC001190

SWITCHING WAVEFORMS

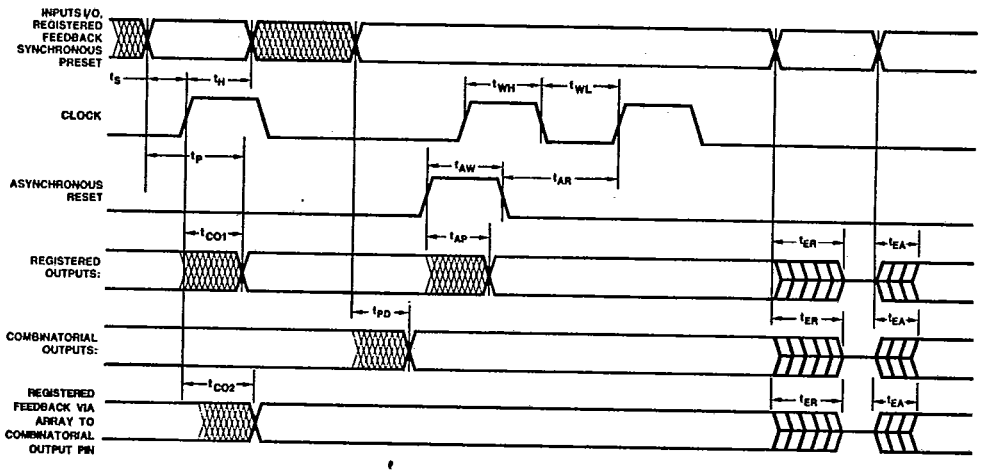
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
———		
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

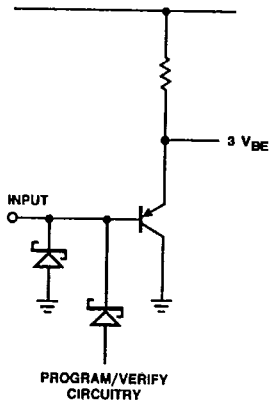
SWITCHING WAVEFORMS (Cont'd.)

T-46-13-47



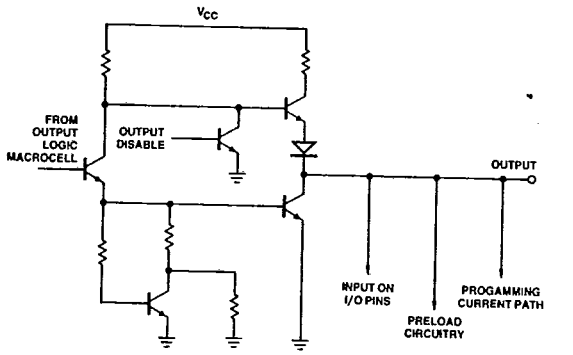
WF022287

INPUT/OUTPUT CIRCUIT DIAGRAM



IC000893

Input Circuitry



IC000900

Output Circuitry

PRELOAD of Registered Outputs

The AmPAL22V10 registered outputs are provided with circuitry to allow loading each register synchronously with either a HIGH or LOW. This feature will simplify testing since any state can be loaded into the registers to control test sequencing.

The pin levels and timing necessary to perform the PRELOAD function are detailed below. Parameters are listed in the Programming Parameters table (page 12).

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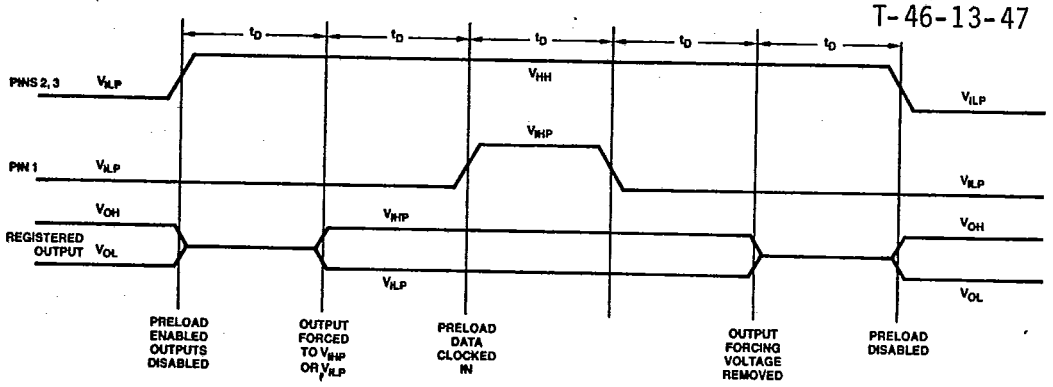


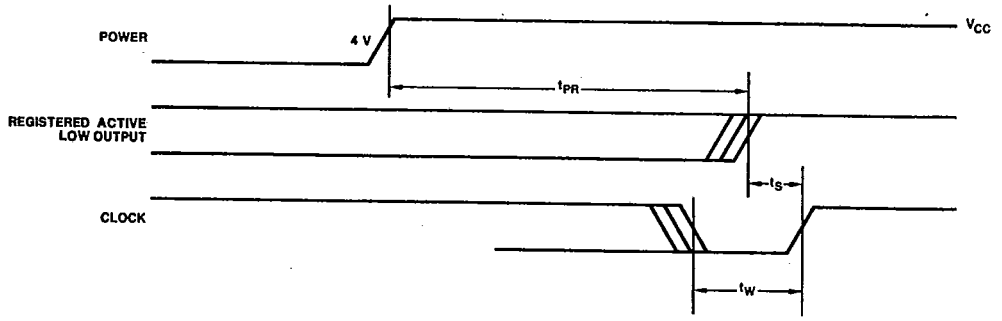
WF022293

Level forced on registered output pin during PRELOAD cycle	Register Q output state after cycle
V_{IHP}	HIGH
V_{ILP}	LOW

Power-Up RESET

The registered devices in the AMD PAL Family have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to LOW. The output state will depend on the polarity of the output buffer. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the asynchronous operation of the power-up reset, and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.



WF022301

Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Unit
t_{PR}	Power-Up Reset Time		600	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics			
t_W	Clock Width				

PROGRAMMING

Programming and Verification

The AmPAL22V10 is programmed and verified using AMD's standard programmable logic programming algorithm. The fuse to be programmed is selected by input line number (array row), product term (array column), and by output (one at a time). The fuse is then programmed and verified by applying a simple sequence of voltages to two control pins (1 and 13).

Input line numbers (0 – 43) are addressed using a full decode scheme via TTL levels on pins 6 – 11 where 6 is the LSB and 11 is the MSB. Even-numbered input lines represent the TRUE version of a signal and odd-numbered lines represent the complement. Input line addressing is shown in Table 1. Note that input lines 44 – 62 are reserved for further expansion, and input line 63 is utilized for selecting the fuses used for programming output polarity and whether the output is registered or combinatorial.

Product terms are addressed using a 1-of-24 addressing scheme on pins 2 – 5 where pin 2 is the LSB and 5 is the MSB. Product term addressing is shown in Table 2. Logical product terms (0 – 15) are selected via TTL levels on the four addressing pins. Note that outputs with fewer than 16 product terms will decode blank space for decoding values greater than the number of product terms on that output. Architectural product terms are selected by placing a zener voltage level (V_{HH}) on the MSB (pin 5) and using pins 2 – 4 for an additional eight decoding states (only five are used). The specific decoding of architectural features is best shown in Table 2.

Fuse selection by output must be done one output at a time (following control pin 1 going to V_{HH}) as shown in the Programming Waveform diagram.

Once fuses have been selected, the simple programming and verification sequence may be completed as shown in the Programming Waveform diagram. AC and DC requirements for programming are shown in the Programming Parameters table.

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Security Fuse Programming

A single fuse is provided on each AmPAL22V10 part to prevent unauthorized copying of PAL fuse patterns. Once blown, the circuitry enabling fuse verification and registered output PRELOAD is permanently disabled.

Programming of the security fuse is the same as an array fuse. Verification of a blown security fuse is accomplished by verifying the whole fuse array as if every fuse were blown.

Programming Yield

AMD PAL devices have been designed to ensure extremely high programming yields (> 98%). To help ensure that a part was correctly programmed, once programming is completed, the entire fuse array should be reverified at both LOW and HIGH V_{CC}. Reverification can be accomplished by reading all ten outputs in parallel rather than one at a time. This verification cycle checks that the array fuses have been blown and can be sensed by the outputs under varying conditions. Programming yield losses are most likely due to poor programming socket contact, programming equipment out of calibration, or improper usage of said equipment.

Post-Programming Functional Yield (PPFY)

AMD PAL devices contain many internal test features, including circuitry and extra fuses which allow AMD to test the ability of each part to perform programming before shipping, to assure high programming yields, and to ensure correct logical operation for a correctly programmed part. This designed-in testability enables AMD's programmable logic devices to yield 99.9% PPFY (see Section 2.3 of the AMD Programmable Logic Handbook for further details).

PROGRAMMING PARAMETERS (T_A = 25°C)

Parameter Symbol	Parameter Description		Min.	Typ.	Max.	Unit
V_{HH}	Control Pin Extra HIGH Level (Note 1)	Pin 1 @ 10 – 40 mA	10	11	12	V
		Pin 13 @ 10 – 40 mA	10	11	12	
V_{OP}	Program Voltage Pins 14 – 23 @ 15 – 200 mA (Note 1)		14	15	16	V
V_{IHP}	Input HIGH Level During Programming and Verify		2.4	5	5.5	V
V_{ILP}	Input LOW Level During Programming and Verify		0.0	0.3	0.5	V
V_{CCP}	V_{CC} During Programming @ I_{CC} = 50 – 200 mA		5	5.2	5.5	V
V_{CCL}	V_{CC} During First-Pass Verification @ I_{CC} = 50 – 200 mA		4.4	4.5	4.6	V
V_{CCH}	V_{CC} During Second-Pass Verification @ I_{CC} = 50 – 200 mA		5.4	5.5	5.6	V
V_{Blown}	Successful Blown Fuse Sense Level @ Output			0.3	0.5	V
V_{OP}/dt	Rate of Output Voltage Change		20		250	V/μs
V_{13}/dt	Rate of Fusing Enable Voltage Change (Pin 13 Rising Edge) (Note 1)		100		1000	V/μs
t_P	Fusing Time, First Attempt		10	50	100	μs
	Subsequent Attempts (Maximum of 8)		4	5	10	ms
t_D	Delays Between Various Level Changes		100	200	15,000	ns
t_V	Period During which Output is Sensed for V_{Blown} Level				500	ns
V_{ONP}	Pull-Up Voltage on Outputs Not Being Programmed		V_{CCP} – 0.3	V_{CCP}	V_{CCP} + 0.3	V
R	Pull-Up Resistor on Outputs Not Being Programmed		1.9	2	2.1	kΩ

Notes: 1. Pinout for DIPs only.

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TABLE 1. INPUT ADDRESSING

Input Line Number	Input Line Number Address Pin States						Input Line Number	Input Line Number Address Pin States					
	11	10	9	8	7	6		11	10	9	8	7	6
0	L	L	L	L	L	L	32	H	L	L	L	L	L
1	L	L	L	L	L	H	33	H	L	L	L	L	H
2	L	L	L	L	H	L	34	H	L	L	L	H	L
3	L	L	L	L	H	H	35	H	L	L	L	H	H
4	L	L	L	H	L	L	36	H	L	L	H	L	L
5	L	L	L	H	L	H	37	H	L	L	H	L	H
6	L	L	L	H	H	L	38	H	L	L	H	H	L
7	L	L	L	H	H	H	39	H	L	L	H	H	H
8	L	L	H	L	L	L	40	H	L	H	L	L	L
9	L	L	H	L	L	H	41	H	L	H	L	L	H
10	L	L	H	L	H	L	42	H	L	H	L	H	L
11	L	L	H	L	H	H	43	H	L	H	L	H	H
12	L	L	H	H	L	L		•					
13	L	L	H	H	L	H		•					
14	L	L	H	H	H	L		•					
15	L	L	H	H	H	H		•					
16	L	H	L	L	L	L		•					
17	L	H	L	L	L	H		•					
18	L	H	L	L	H	L		•					
19	L	H	L	L	H	H		•					
20	L	H	L	H	L	L		•					
21	L	H	L	H	L	H		RESERVED					
22	L	H	L	H	H	L		•					
23	L	H	L	H	H	H		•					
24	L	H	H	L	L	L		•					
25	L	H	H	L	L	H		•					
26	L	H	H	L	H	L		•					
27	L	H	H	L	H	H		•					
28	L	H	H	H	L	L		•					
29	L	H	H	H	L	H		•					
30	L	H	H	H	H	L		•					
31	L	H	H	H	H	H	63*	H	H	H	H	H	H

*Architecture row

TABLE 2. COLUMN NUMBER ADDRESSING

Column Number										Column Number Select Address Pin States				Description
										5	4	3	2	
0	0	0	0	0	0	0	0	0	0	L	L	L	L	Logical PTs
1	1	1	1	1	1	1	1	1	1	L	L	L	H	Logical PTs
2	2	2	2	2	2	2	2	2	2	L	L	H	L	Logical PTs
3	3	3	3	3	3	3	3	3	3	L	L	H	H	Logical PTs
4	4	4	4	4	4	4	4	4	4	L	H	L	L	Logical PTs
5	5	5	5	5	5	5	5	5	5	L	H	L	H	Logical PTs
6	6	6	6	6	6	6	6	6	6	L	H	H	L	Logical PTs
7	7	7	7	7	7	7	7	7	7	L	H	H	H	Logical PTs
-	8	8	8	8	8	8	8	8	-	H	L	L	L	Logical PTs
-	9	9	9	9	9	9	9	9	-	H	L	L	H	Logical PTs
-	-	10	10	10	10	10	10	-	-	H	L	H	L	Logical PTs
-	-	11	11	11	11	11	11	-	-	H	L	H	H	Logical PTs
-	-	-	12	12	12	12	-	-	-	H	H	L	L	Logical PTs
-	-	-	13	13	13	13	-	-	-	H	H	L	H	Logical PTs
-	-	-	-	14	14	-	-	-	-	H	H	H	L	Logical PTs
-	-	-	-	15	15	-	-	-	-	H	H	H	H	Logical PTs
OE	OE	OE	OE	OE	OE	OE	OE	OE	OE	HH	L	L	L	Output Enable
P	P	P	P	P	P	P	P	P	P	HH	L	L	H	Output Polarity
R	R	R	R	R	R	R	R	R	R	HH	L	H	L	Register/Non-Register Output
-	AR*	-	-	-	-	-	-	SP**	-	HH	L	H	H	*Asynchronous RESET **Synchronous PRESET
-	SF	-	-	-	-	-	-	-	-	HH	H	L	H	Security Fuse (Special Verify Required)
Pin 23	Pin 22	Pin 21	Pin 20	Pin 19	Pin 18	Pin 17	Pin 17	Pin 15	Pin 14					
Programming Access and Verify Pin														

Legend: L = V_{ILP}
H = V_{IHP}
HH = V_{HH}

PROGRAMMING WAVEFORMS

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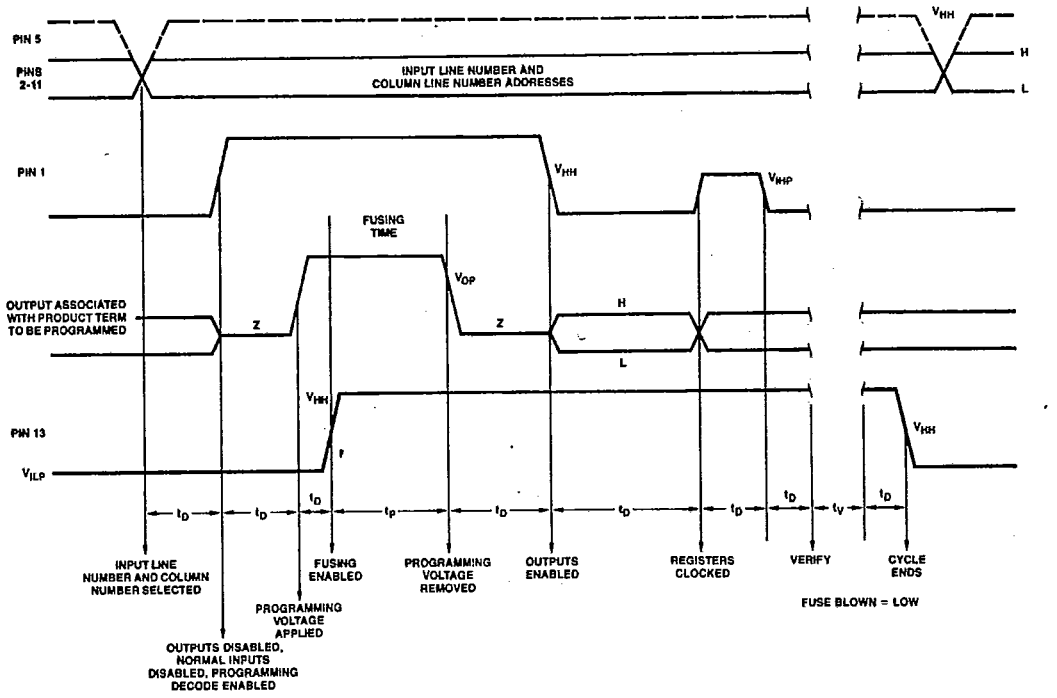

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AmPAL22V10 PROGRAMMING EQUIPMENT INFORMATION T-46-13-47

Vendor	Programmer Model (s)	Personality Module	Socket Adapter
Data I/O 10525 Willow Road N.E. Redmond, WA 98052 (206) 881-6464	System 19, 29 or 100	Logicpak 715-1983-003 (Rev 4 or Newer)	303A-004 (Rev 3 or Newer) 303A-011A (Rev 1 or Newer) 303A-011B (Rev 1 or Newer)
	Model 60A or 60H	360A-001 (Rev 4 or Newer)	On-Board
JMC PROMAC Division 2999 Monterey/Salinas Highway Monterey, CA 93940 (408) 373-3622	PROMAC P3 (Rev 2.0 or Newer)	On-Board	On-Board
Stag Microsystems 528-5 Weddell Drive Sunnyvale, CA 94086 (408) 745-1991 or (800) 227-8836	Model PPZ	Zm2200 (Rev 10 or Newer)	On-Board (Rev 10 or Newer)
	Model ZL30, ZL30A, ZL32	On-Board (Rev 38 or Newer)	On-Board (Rev 38 or Newer)
Structured Design 988 Bryant Way Sunnyvale, CA 94087 (408) 988-0725	SD 1040 PAL Burner (Rev V1.02A or Newer)	On-Board	On-Board
Valley Data Sciences 2426 Charleston Road Mt. View, CA 94043 (415) 968-2900	VDS 160 Series	On-Board (Rev 1.03 or Newer)	On-Board
Varix Corporation 122 Spanish Village Suite 608 Dallas, TX 75248 (214) 437-0777	Omni-Programmer SP0-300	Under Development	Under Development
DIGELEC 1602 Lawrence Ave., Suite 113 Ocean,NJ 07712 (210) 493-2424	803 Series	FAM52 (Rev 5.4 or Newer)	DA55 (Rev B3 or Newer) (Rev V1.02A or Newer)
	860 Series (Rev A 1.0 or Newer)	On-Board	On-Board
KONTRON Electronics 1230 Charleston Rd Mountain View, CA 94039 (415) 965-7020 (800) 227-8834	EPP-80	On-Board	On-Board
	MPP-80S	UPM/B Module (Version 1.45 or Newer)	On-Board
		UPM/C Module (Version 1.45 or Newer)	

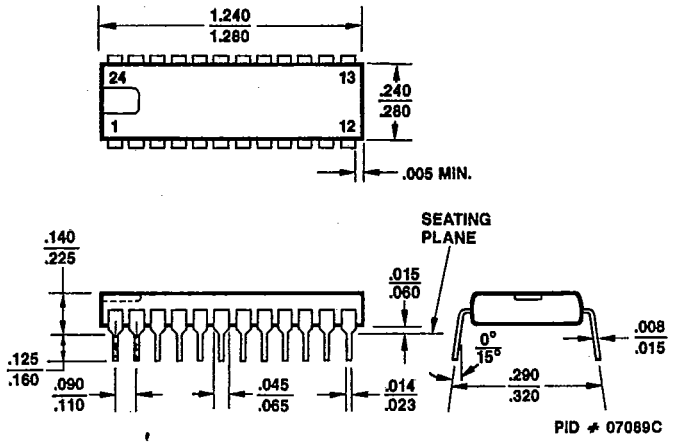
The machines noted above have been qualified by AMD to ensure high programming yields. Check with the factory to determine the current status of vendors noted under development, or other available models.

Design Aid Software for AmPAL22V10

Software Vendor	Software Package	Comments
P-CAD Systems (408) 971-1300	CUPL	
Advanced Micro Devices (408) 732-2400	AmCUPL	Developed and supported by P-CAD Systems
Data I/O (206) 881-6444	ABEL	

PHYSICAL DIMENSIONS* T-46-13-47

PD3024



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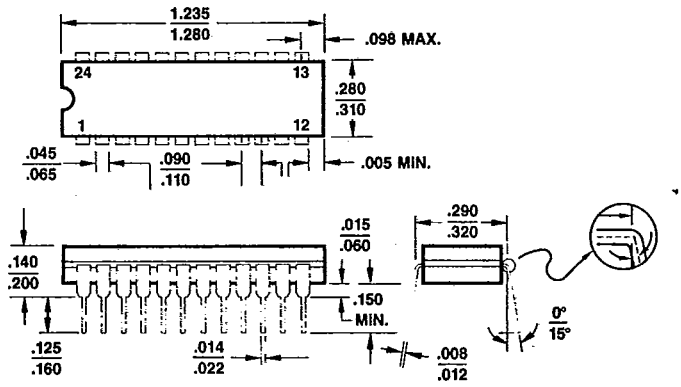

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*For reference only.

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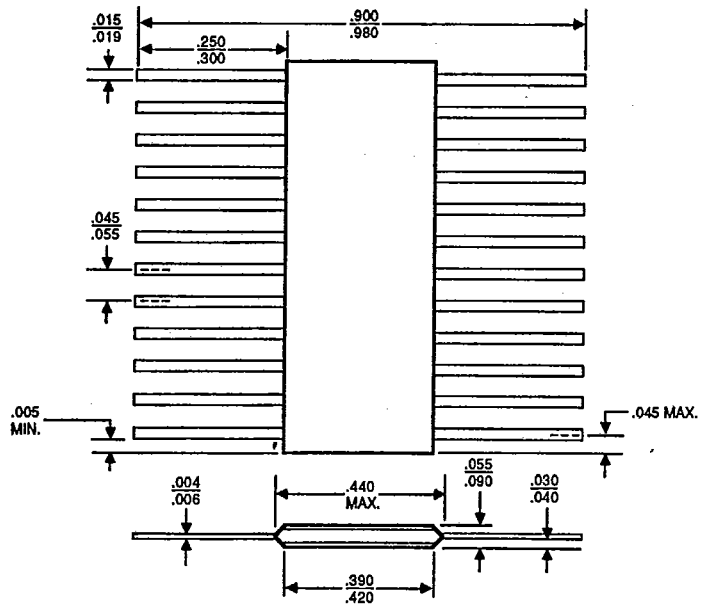

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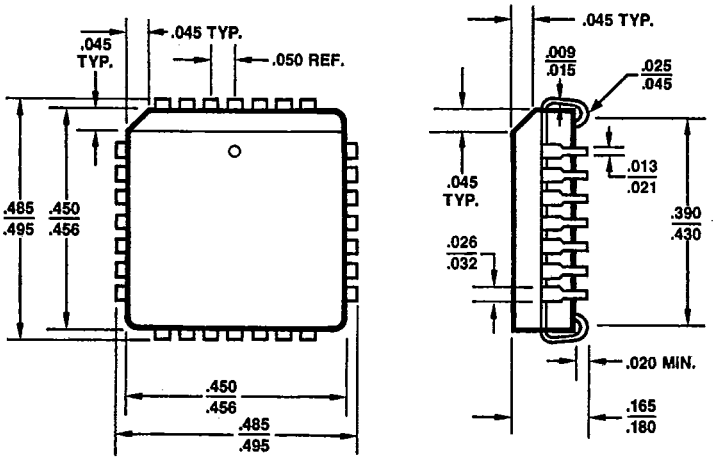

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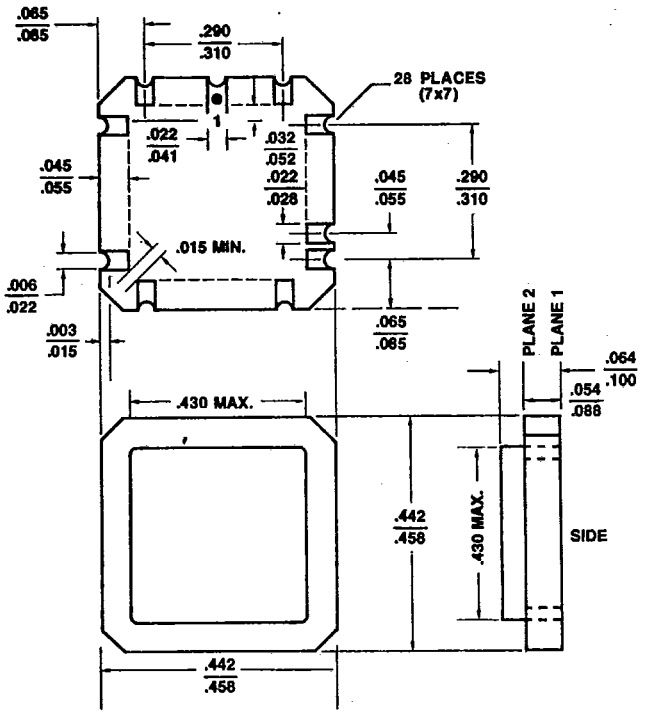

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