Trident

Omega 82C128™

Product Brief

Scalable ZV Serial IRQ/PWR

Features

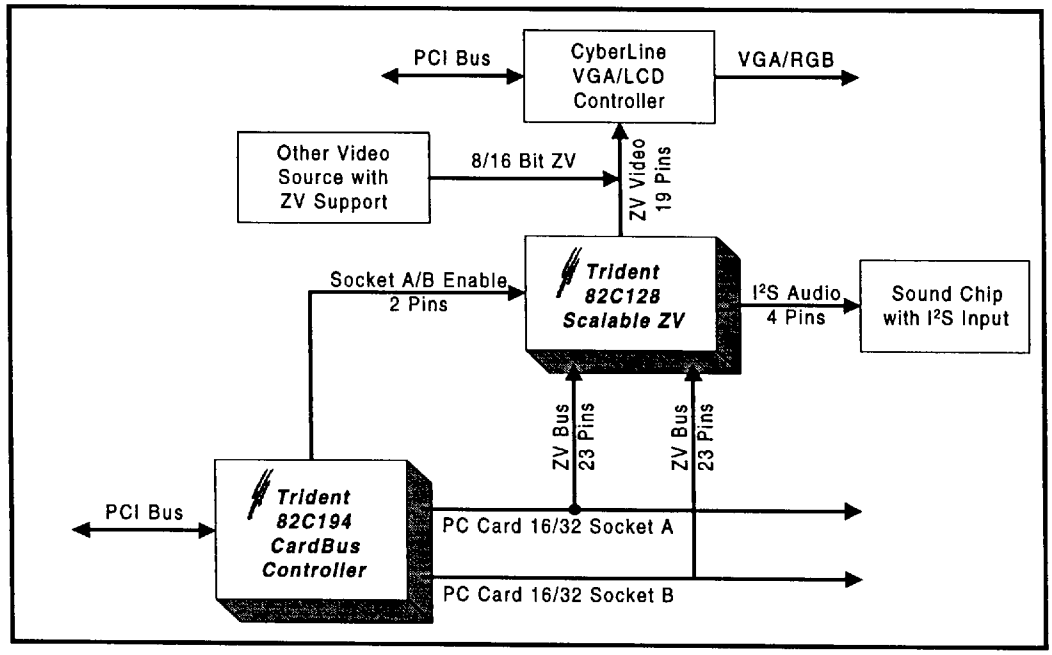
Scalable ZV Port Solution

- Companion chip to Omega 82C194 CardBus host controller to allow dual-socket ZV port input to LCD graphics controllers
- Tri-state control on ZV port buffers to allow other sources of video chip input (e.g., TV tuner or MPEG decoder) to a video port or an LCD graphics controller
- Directly controlled by the Omega 82C128 to replace 7 TTL's for a socket A or a socket B ZV port input selection to an LCD graphics controller chip
- Supports dual-clock edge 8 bit ZV port (16-to-8 conversion) for next generation LCD graphics controllers
- Packaged in a 100 pin TQFP or PQFP

Interrupt and Power Control

- Integrates the 82C28 chip for Legacy Interrupt and Power Control
- Converts serial IRQ control data into ISA bus required IRQ signals
- Converts serial power chip control data into a parallel format required by major PCMCIA power switch chips
- Replaces a 9 TTL glue logic providing reduced cost and board space
- Designed to work with parallel power control chips such as Micrel 2560/2563 or TI 2201/2202
- Operate at 33 MHz clock speed

Omega 82C128 Scalable Zoom Video™ System Block Diagram



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Scalable ZV Serial IRQ/PWR

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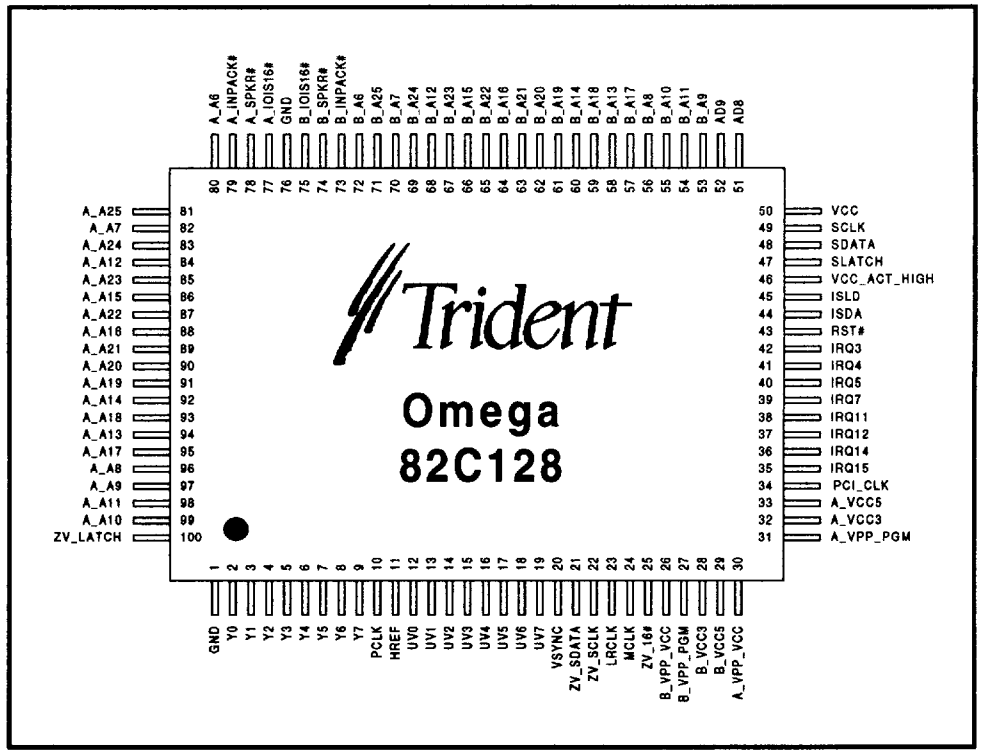
Overview

The Omega 82C128 is a companion chip to the Omega 82C194 CardBus host controller capable of providing ZV port buffers into LCD graphics controller in the notebook design. It replaces at least 7 TTL's for ZV port buffering to reduce board layout space and minimize the cost for dual-socket ZV port support. The 82C128 supports tri-state ZV buffer to make the feature-rich notebook easy to design. It allows other video chips, e.g. TV tuner or MPEG decoder, to share or use the same video port of the LCD controller, such as a ZV port input, and maximize its usage.

The Omega 82C128 supports additional video formats for next generation(s) LCD graphics controllers. It converts the 16 bit ZV port video input into an 8 bit video format and permits an VMI 1.4 type of format to be converted inside the LCD graphics controller. This will reduce the pin requirement for multiple video format support in an LCD graphics controller.

The Omega 82C128 integrates its predecessor 82C28 chip which replaces 9 TTL's to become a companion chip to the Omega 82C194 (PCI-to-PCMCIA) host controller. Its interrupt function converts the serial IRQ control data into eight Legacy IRQ's (3, 4, 5, 7, 11, 12, 14, and 15) for transfer to the ISA bus. The IRQ serial data latch input signal latches parallel IRQ data every 16 bits and operates from a 33 MHz PCI clock input.

The power control function of the Omega 82C128 similarly converts a single socket A or B serial chip power control data input (SDATA) into an 8 bit parallel format required by major parallel power switch control chips. Latching is performed by the SLATCH input; a separate SCLK input is required. VCC5 and VCC3 control output can be configured to be active high or low by hardwiring the VCC_AT_HIGH pin to the appropriate voltage level.



Omega 82C128 Pinout Diagram

Contact your local Trident representative for an *Omega 82C128 Technical Reference Manual.*

Trident Microsystems, Inc., 189 North Bernardo Avenue, Mountain View, CA 94043-5203. Specifications subject to change without notice.
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