NEC

MOS INTEGRATED CIRCUIT
μPD424800-L

4M BIT DYNAMIC RAM
(FAST PAGE MODE)

DESCRIPTION

The NEC μPD424800-L is a 524288-word by 8 bits dynamic CMOS RAM with optional fast page mode. CMOS sense amplifier, peripheral circuits and 1 transistor memory cell technique realize high speed access, cycle time and low power dissipation. Refresh is accomplished by performing $\overline{RAS}$ only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 1024 address combinations of A_0 to A_9, during a 128 ms period.

The μPD424800-L is packaged in 28-pin plastic SOJ, 28-pin plastic ZIP and 28-pin plastic TSOP. ★

FEATURES

- 524288 words by 8 bits organization

DEVICE	ACCESS TIME (MAX.)	R/W CYCLE (MIN.)	PAGE MODE CYCLE (MIN.)
μPD424800-70L	70 ns	140 ns	45 ns
μPD424800-80L	80 ns	160 ns	50 ns
μPD424800-10L	100 ns	190 ns	60 ns

- Low power dissipation
  - Active . . . . . 577.5 mW MAX. (μPD424800-70L)
    522.5 mW MAX. (μPD424800-80L)
    440.0 mW MAX. (μPD424800-10L)
  - Standby . . . . . 1.1 mW MAX. (CMOS level)
- Single +5V ± 10% power supply
- On-chip substrate bias generator
- Multiplexed address inputs . . . . . Row Address: A0 to A9, Column Address: A0 to A8
- Non latched I/O, TTL-compatible
- Read-modify-write, Fast Page Mode capability
- 1024 refresh cycles/128 ms
- $\overline{RAS}$ only refresh, hidden refresh and $\overline{CAS}$ before $\overline{RAS}$ internal address refresh

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The mark ★ shows revised points.

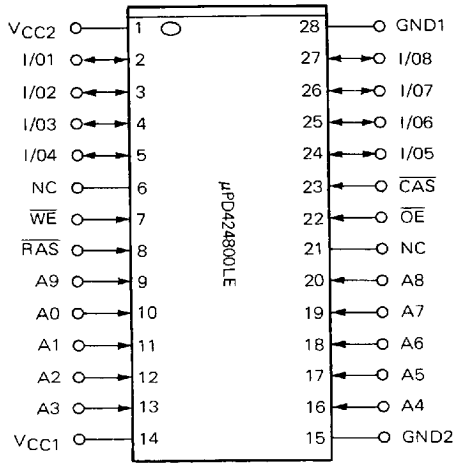
ORDERING INFORMATION★

PART NUMBER	PACKAGE	ACCESS TIME (MAX.)	QUALITY GRADE
μPD424800LE-70L	28-Pin Plastic SOJ	70 ns	Standard
μPD424800LE-80L	28-Pin Plastic SOJ	80 ns	Standard
μPD424800LE-10L	28-Pin Plastic SOJ	100 ns	Standard
μPD424800V-70L	28-Pin Plastic ZIP	70 ns	Standard
μPD424800V-80L	28-Pin Plastic ZIP	80 ns	Standard
μPD424800V-10L	28-Pin Plastic ZIP	100 ns	Standard
μPD424800G5-70L-7JD	28-Pin Plastic TSOP	70 ns	Standard
μPD424800G5-80L-7JD	28-Pin Plastic TSOP	80 ns	Standard
μPD424800G5-10L-7JD	28-Pin Plastic TSOP	100 ns	Standard
μPD424800G5-70L-7KD	28-Pin Plastic TSOP(Reverse bent)	70 ns	Standard
μPD424800G5-80L-7KD	28-Pin Plastic TSOP(Reverse bent)	80 ns	Standard
μPD424800G5-10L-7KD	28-Pin Plastic TSOP(Reverse bent)	100 ns	Standard

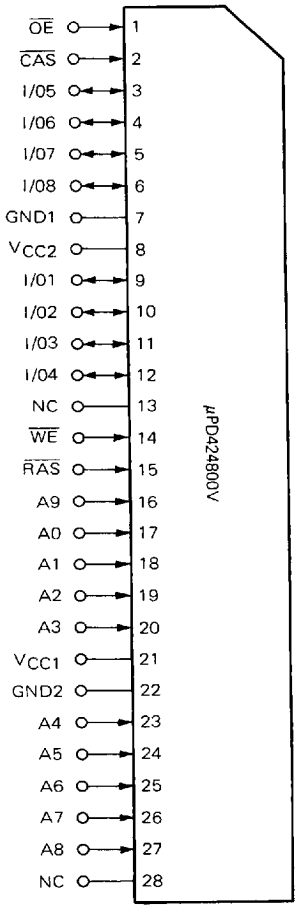
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

PIN CONFIGURATION*

28-pin Plastic SOJ
(Top View)

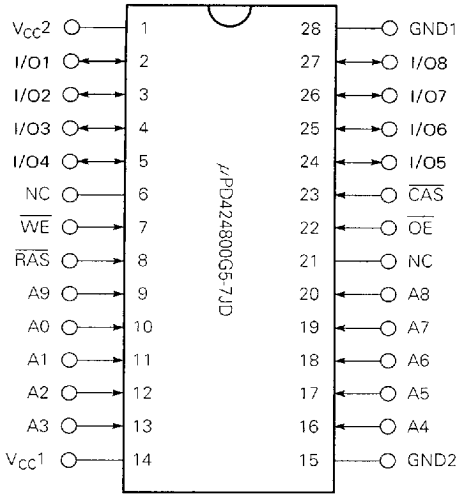


28-pin Plastic ZIP
(Front View)

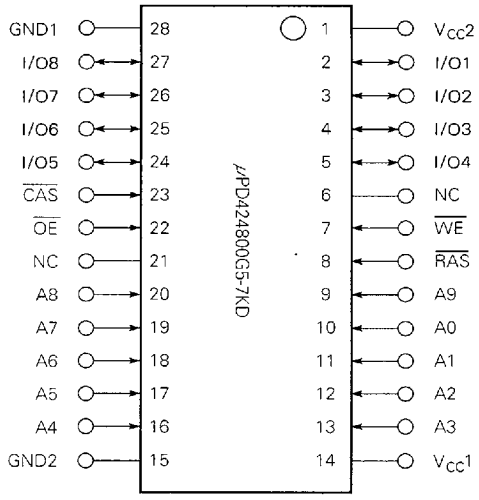


A0 to A9	Addresses Inputs
I/01 to I/08	Data Inputs/Outputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC1, 2	Supply Voltage
GND1, 2	Ground
NC	No Connection

28-Pin Plastic TSOP
(Top View)



28-Pin Plastic TSOP(Reverse bent)
(Top View)



A0 to A9	Addresses Inputs
I/01 to I/08	Data Inputs/Outputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$V_{CC1, 2}$	Supply Voltage
GND1, 2	Ground
NC	No Connection

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to GND	V_T	−1.0 to +7.0 V
Supply Voltage	Vcc	−1.0 to +7.0 V
Short Circuit Output Current	Io	50 mA
Power Dissipation	P_D	1 W
Operating Temperature	Topt	0 to +70 °C
Storage Temperature	Tstg	−55 to +125 °C

***COMMENT:** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS[Notes 1, 2]

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP	MAX.	UNIT
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		V_{CC}+1.0	V
Low Level Input Voltage	V_{IL}		−1.0		0.8	V
Ambient Temperature	Ta		0		70	°C

DC CHARACTERISTICS (Recommended Operating Conditions unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP	MAX	UNIT	NOTE
Operating Current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC}=t_{RC(MIN.)}$, I_O=0 mA	μPD424800-70L			105	mA	3
			μPD424800-80L			95		
			μPD424800-10L			80		
Standby Current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}\geqq V_{IH(MIN.)}$, I_O=0 mA				2	mA	
		$\overline{RAS}$, $\overline{CAS}\geqq V_{CC}$−0.2 V, I_O=0 mA				0.2	mA	★
Refresh Current	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS}\geqq V_{IH(MIN.)}$ $t_{RC}=t_{RC(MIN.)}$, I_O=0 mA	μPD424800-70L			105	mA	3
			μPD424800-80L			95		
			μPD424800-10L			80		
Operating Current (Page Mode)	I_{CC4}	$\overline{RAS}\leqq V_{IL(MAX.)}$, $\overline{CAS}$ Cycling $t_{PC}=t_{PC(MIN.)}$, I_O=0 mA	μPD424800-70L			80	mA	3
			μPD424800-80L			70		
			μPD424800-10L			60		
Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC5}	$\overline{RAS}$ Cycling, $t_{RC}=t_{RC(MIN.)}$, I_O=0 mA	μPD424800-70L			105	mA	3
			μPD424800-80L			95		
			μPD424800-10L			80		
Battery Back up current (Standby with $\overline{CAS}$ Before $\overline{RAS}$ Refresh)	I_{CC6}	Stand-by: V_{CC}−0.2V$\leqq\overline{RAS}$ $\overline{CAS}\leqq V_{IH}$ MAX. $\overline{CAS}$ Before $\overline{RAS}$ Refresh: $t_{RAS}\leqq$200ns 1024 cycle/128ms $\overline{OE}=V_{IH}$ A0−A9, $\overline{WE}=V_{IH}$ OR V_{IL} else input: V_{CC}−0.2V$\leqq V_{IH}\leqq V_{IH}$ MAX. 0V$\leqq V_{IL}\leqq$0.2V output: Hi-z				300	μA	
Input Leakage Current	$I_{I(L)}$	V_I=0 to 5.5 V all other pins not under test=0 V		−10		10	μA	
Output Leakage Current	$I_{O(L)}$	D_{OUT} is disabled V_O=0 to 5.5 V		−10		10	μA	
Output High Voltage	V_{OH}	I_O=5 mA		2.4			V	
Output Low Voltage	V_{OL}	I_O=4.2 mA				0.4	V	

CAPACITANCE (Ta=25°C, f=1 MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Input Capacitance	C_{I1}	A0 to A9			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	pF
Data Input/Output Capacitance	C_D	I/01 to I/08			7	pF

AC CHARACTERISTICS (Recommended Operating Conditions unless Otherwise Noted) Notes 2, 4, 5

PARAMETER	SYMBOL	μPD424800-70L		μPD424800-80L		μPD424800-10L		UNIT	NOTE
		MIN	MAX	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t_{RC}	140		160		190		ns	6
Read Write Cycle Time	t_{RWC}	185		210		250		ns	6
Fast Page Mode Cycle Time (Read or Write)	t_{PC}	45		50		60		ns	6
Fast Page Mode Cycle Time (Read Modify Write)	t_{PRWC}	90		100		120		ns	6
Access Time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	4,5,7
Access Time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	4,5,7
Access Time from Column Address	t_{AA}		35		40		50	ns	4,5,7
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		40		45		55	ns	4,5,7
Access Time from $\overline{OE}$	t_{OEA}		20		20		25	ns	4,5,7
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	17	40	17	50	ns	7
$\overline{CAS}$ → Data Setup Time	t_{CLZ}	0		0		0		ns	
$\overline{OE}$ → Data Setup Time	t_{OLZ}	0		0		0		ns	
Output Buffer Turn-off Delay ($\overline{CAS}$)	t_{OFF}	0	15	0	15	0	20	ns	8
OE Data Delay Time	t_{OED}	15		15		20		ns	
Output Buffer Turn-off Delay ($\overline{OE}$)	t_{OEZ}	0	15	0	15	0	20	ns	8
$\overline{OE}$ Command Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive Setup Time	t_{OES}	0		0		0		ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge time	t_{RP}	60		70		80		ns	
$\overline{RAS}$ Pulse Width (Random Read, Write)	t_{RAS}	70	10000	80	10000	100	10000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	70	125000	80	125000	100	125000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20		20		25		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40		45		55		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	70		80		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	25	60	25	75	ns	7
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		12		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		20		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	35		40		50		ns	
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Write Command Hold Time Referenced to $\overline{CAS}$	t_{WCH}	10		15		20		ns	10
Write Command Pulse Width	t_{WP}			15		20		ns	10
Data-in Setup Time	t_{DS}	0		0		0		ns	11
Data-in Hold Time	t_{DH}	15		15		20		ns	11
Write Command Setup Time	t_{WCS}	0		0		0		ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	90		105		130		ns	12
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	40		45		55		ns	12
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	55		65		80		ns	12
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20		20		25		ns	

PARAMETER	SYMBOL	μPD424800-70L		μPD424800-80L		μPD424800-10L		UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX.		
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15		15		20		ns	
$\overline{CAS}$ Setup Time for CBR Refresh	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time for CBR Refresh	t_{CHR}	15		15		20		ns	
Refresh Period	t_{REF}		128		128		128	ms	

NOTE

(1) All voltages referenced to GND

(2) An initial pause of 100 μs is required after power-on followed by 8 refresh ($\overline{RAS}$ only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) cycles before proper device operation is achieved.

(3) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC3} is measured on condition that Column addresses in $\overline{RAS}$ only cycle are held high or Low level and I_{CC4} is measured on condition that column addresses are charged only one time during t_{PC} (MIN.).

(4) AC measurements assume t_T=5 ns

(5) V_{IH}(MIN.) and V_{IL}(MAX.) are reference levels for measuring timing of input signals.
Transition times are measured between V_{IH} and V_{IL}
Access times are measured at V_{OH}(MIN.) and V_{OL}(MAX.) and loading condition is 2TTL + 100 pF

(6) The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (Ta=0 to 70° C) is assured.

(7) If $t_{RCD} \leq t_{RCD}$(MAX.) and $t_{RAD} \leq t_{RAD}$(MAX.), access time is defined by t_{RAC}(MAX.)
If $t_{RCD} \geq t_{RCD}$(MAX.), access time is defined by t_{CAC}(MAX.) and if $t_{RAD} \geq t_{RAD}$(MAX.), access time is defined by t_{AA}(MAX.)

(8) t_{OFF}(MAX.) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}

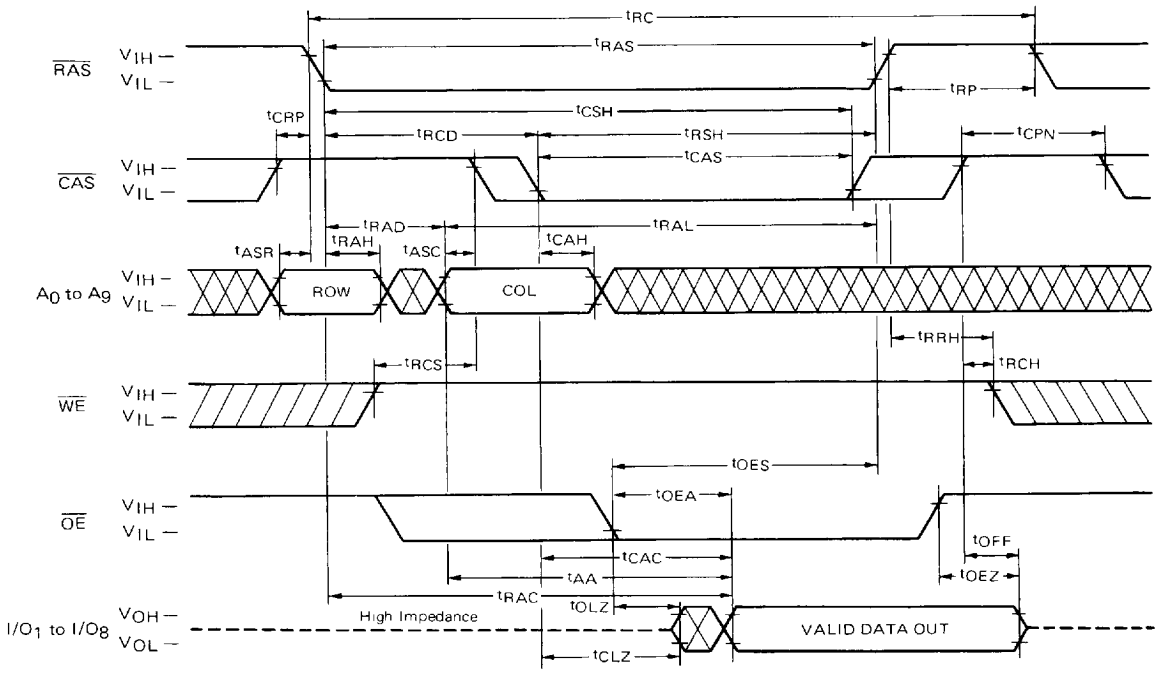
(9) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle

(10) t_{WP} is applicable for late write cycle or read-modify-write cycle. In early write cycle, t_{WCH}(MIN.) should be satisfied.

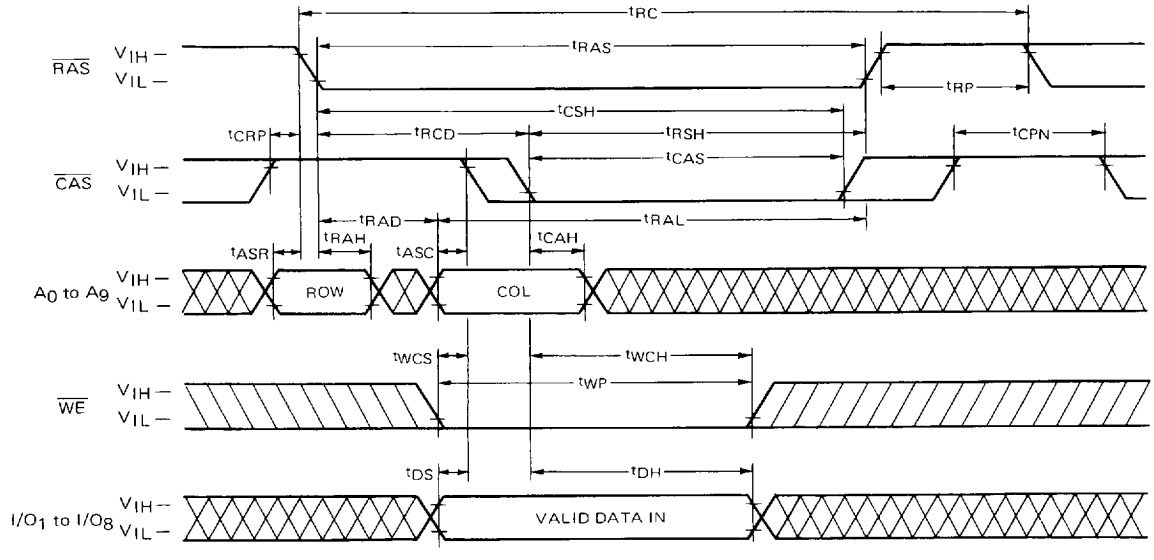
(11) These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in late write or read-modify-write cycles.

(12) These parameters are the condition defining read-modify-write cycle.

READ CYCLE

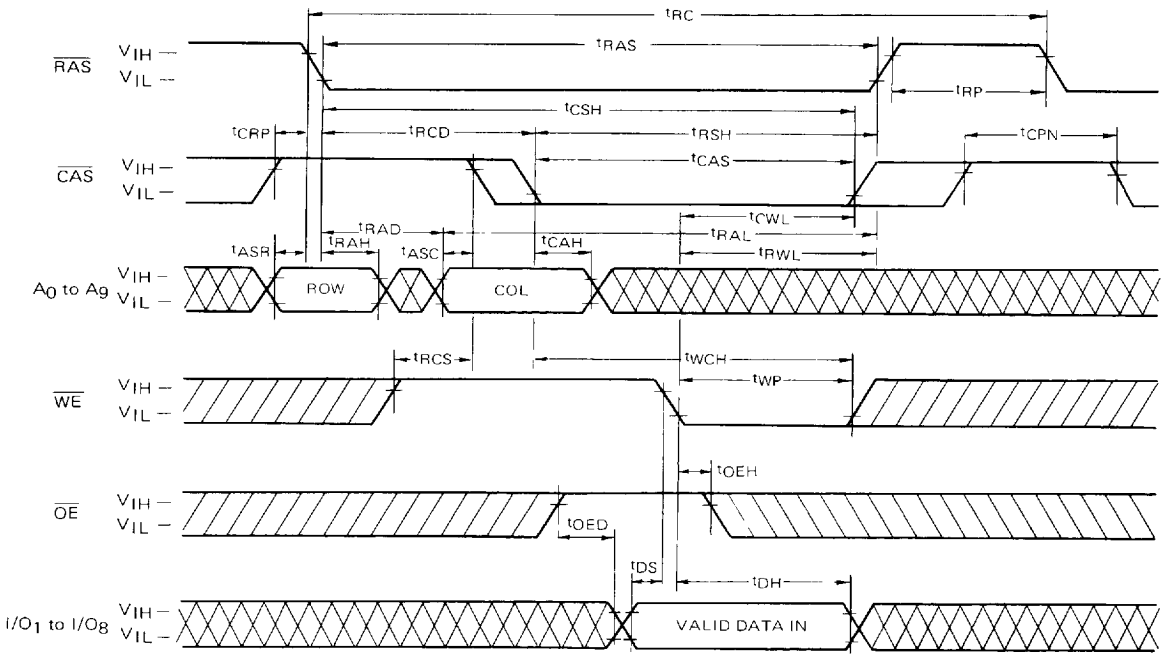


EARLY WRITE CYCLE

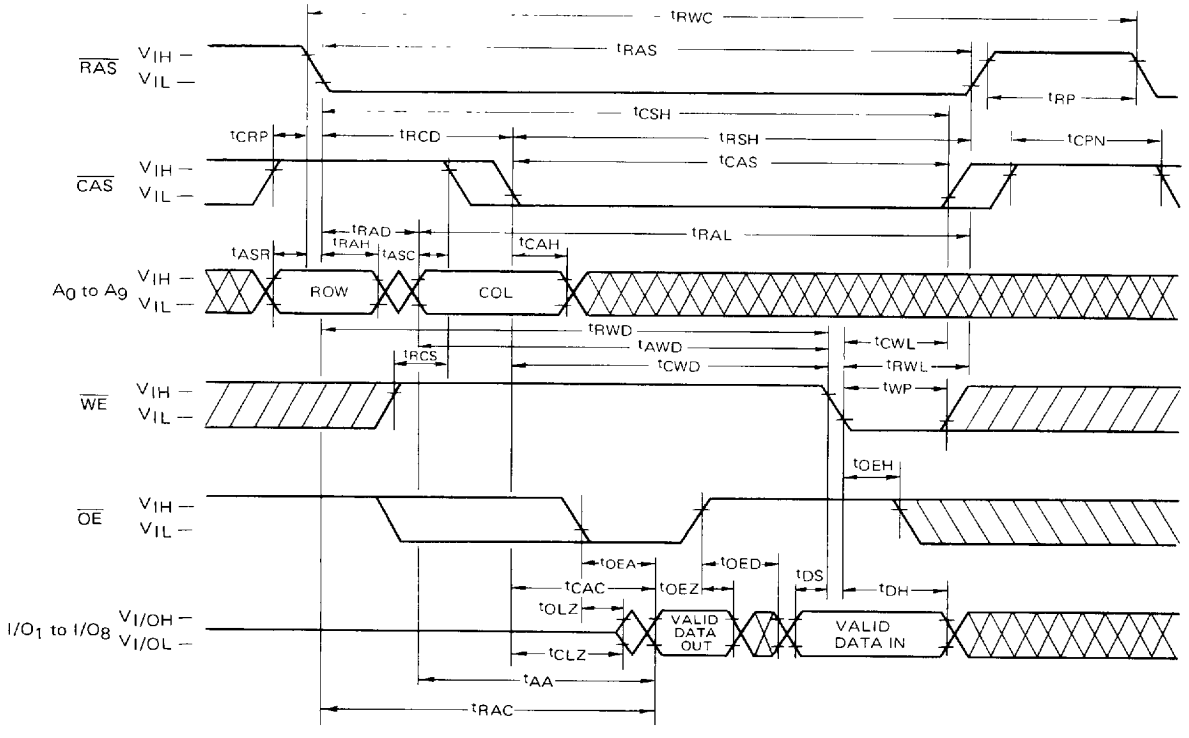


* $\overline{OE}$ Don't care

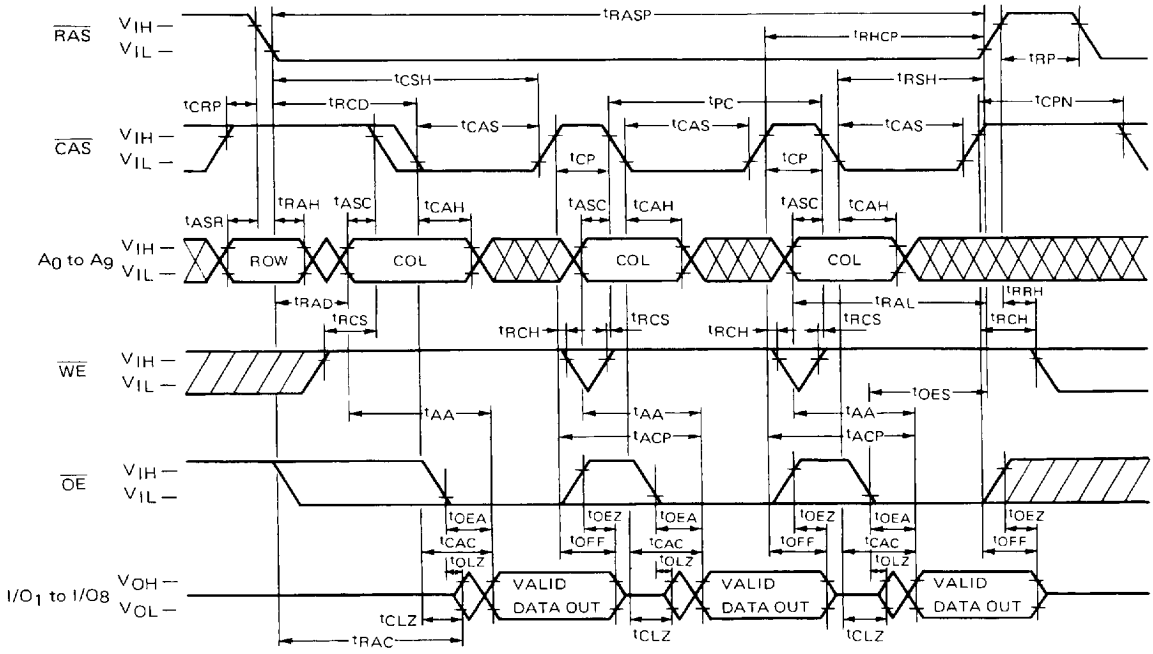
LATE WRITE CYCLE



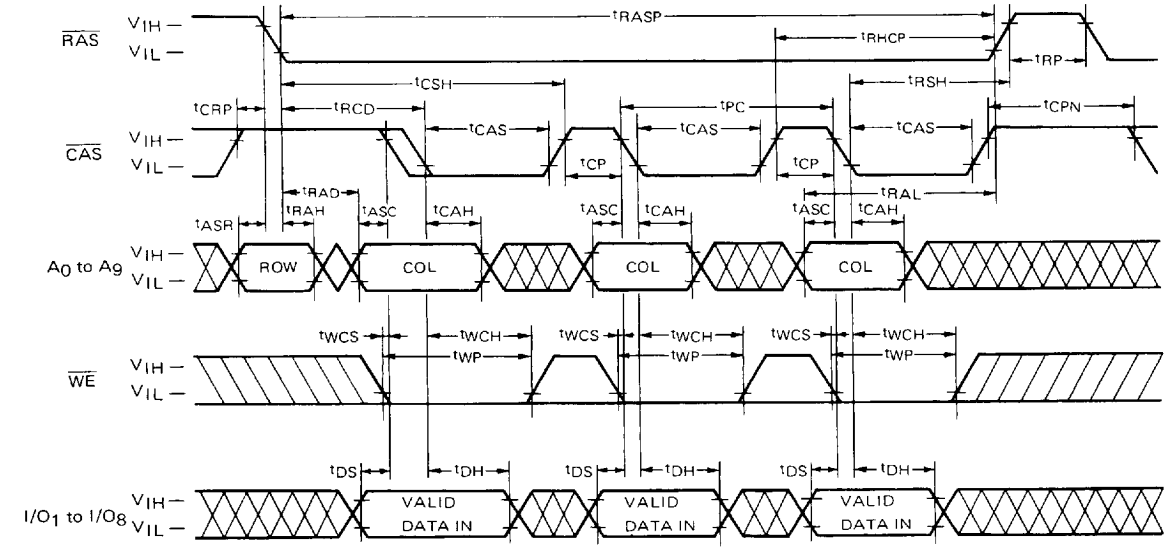
READ-MODIFY-WRITE CYCLE



PAGE MODE READ CYCLE

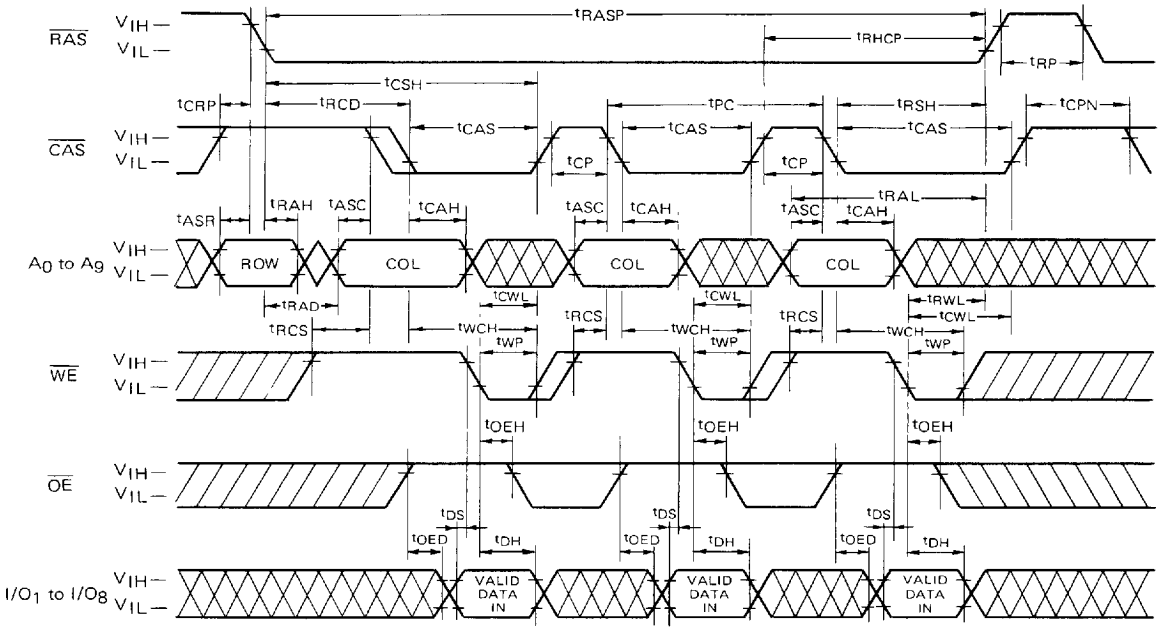


PAGE MODE EARLY WRITE CYCLE

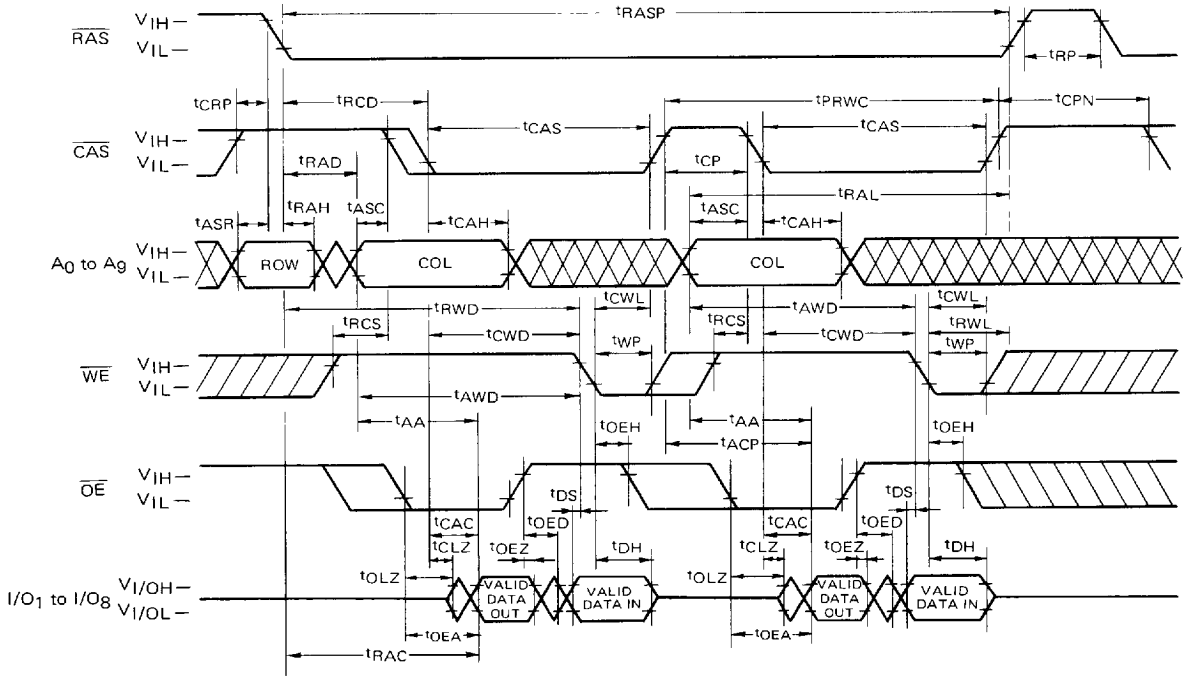


* $\overline{OE}$ Don't care

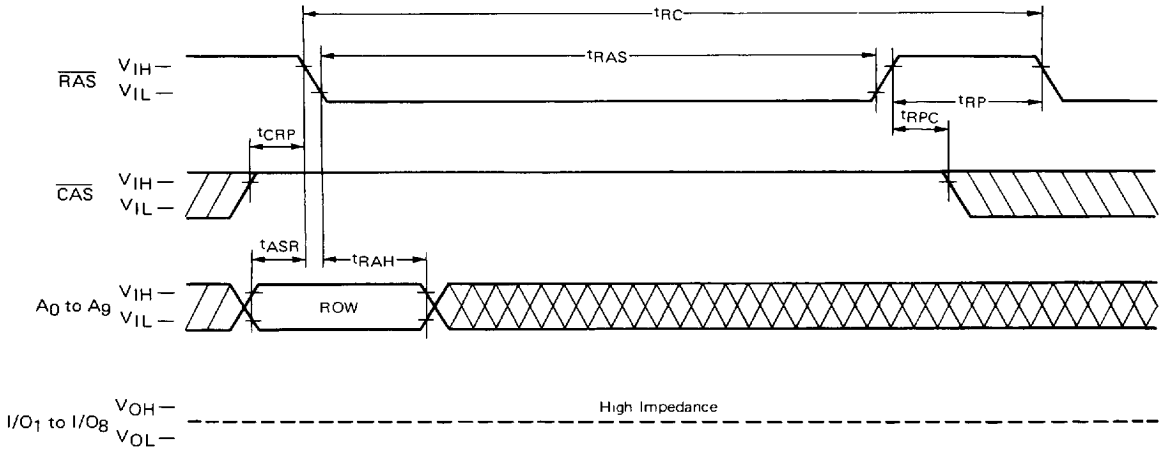
PAGE MODE LATE WRITE CYCLE



PAGE MODE READ-MODIFY-WRITE CYCLE

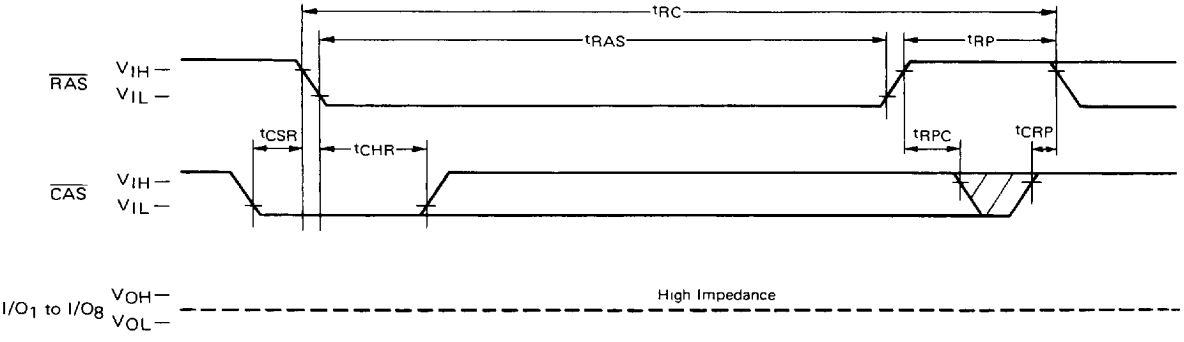


$\overline{RAS}$ ONLY REFRESH CYCLE



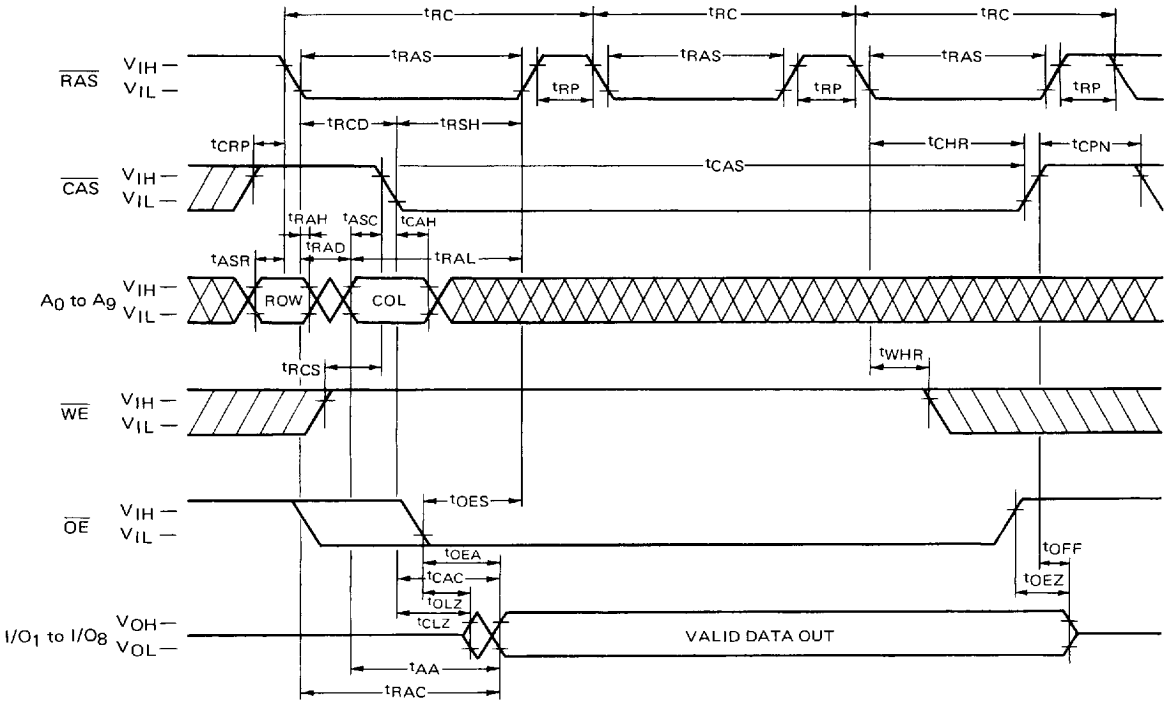
* $\overline{WE}$, $\overline{OE}$: Don't care

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH



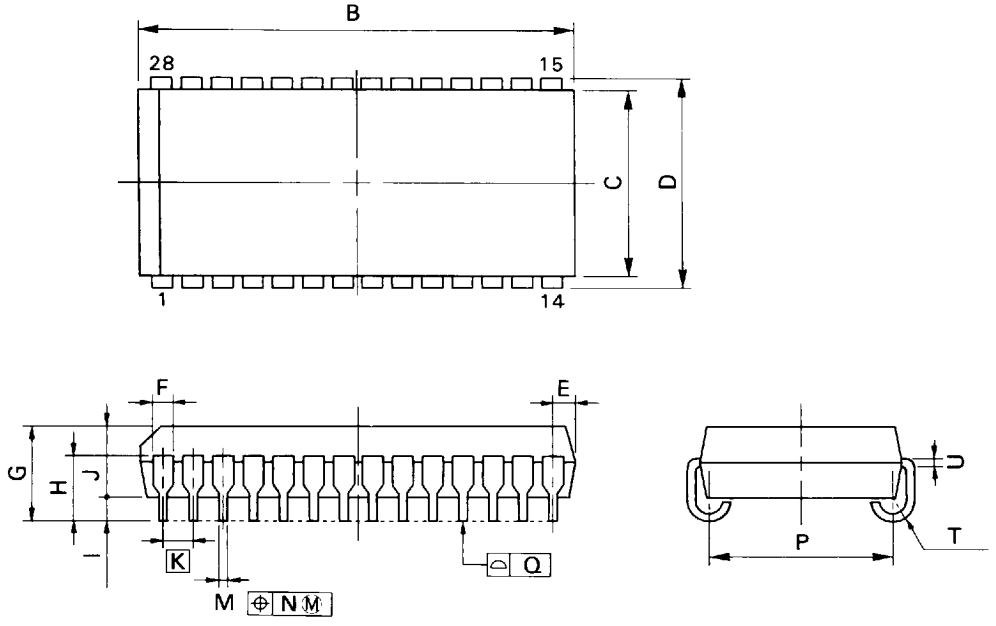
* $\overline{WE}$, $\overline{OE}$: Don't care

$\overline{CAS}$ BEFORE $\overline{RAS}$ HIDDEN REFRESH CYCLE



PACKAGE INFORMATION*

28PIN PLASTIC SOJ (400 mil)



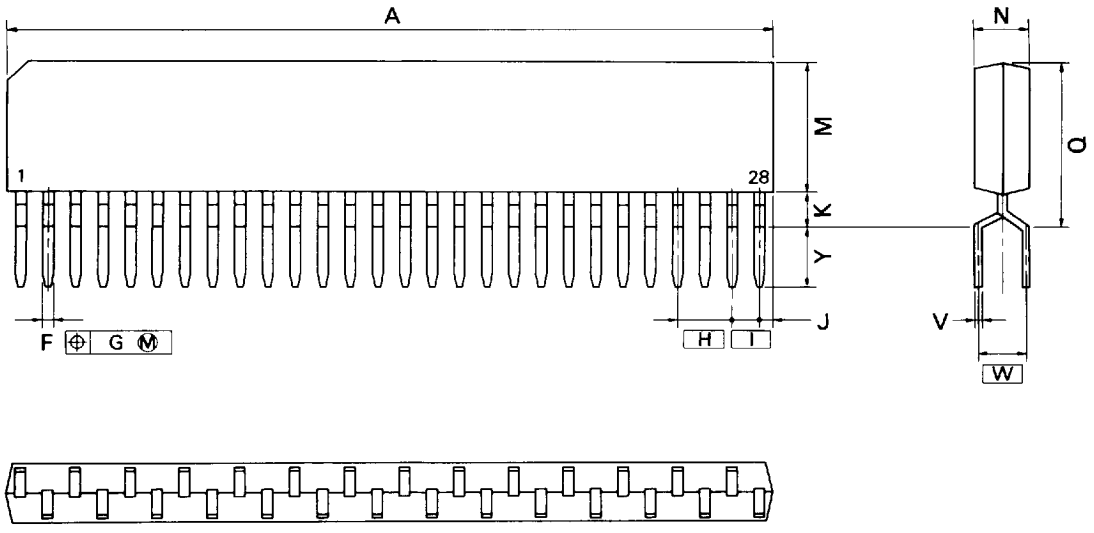
P28LA-400A-1

NOTE

Each lead centerline is located within 0.12 mm (0 005 inch) of its true position (T P) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$18.67^{+0.2}_{-0.35}$	$0.735^{+0.008}_{-0.013}$
C	10.16	0.400
D	$11.18^{\pm 0.2}$	$0.440^{+0.008}_{-0.007}$
E	$1.08^{\pm 0.15}$	$0.043^{+0.006}_{-0.007}$
F	0.6	0.024
G	$3.5^{\pm 0.2}$	$0.138^{+0.008}_{-0.007}$
H	$2.4^{\pm 0.2}$	$0.094^{+0.008}_{-0.007}$
I	0.8 MIN	0.031 MIN
J	2.6	0.102
K	1.27 (T P)	0.050 (T P)
M	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	$9.40^{\pm 0.20}$	$0.370^{+0.008}_{-0.007}$
Q	0.15	0.006
T	R0.85	R0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

28PIN PLASTIC ZIP (400mil)

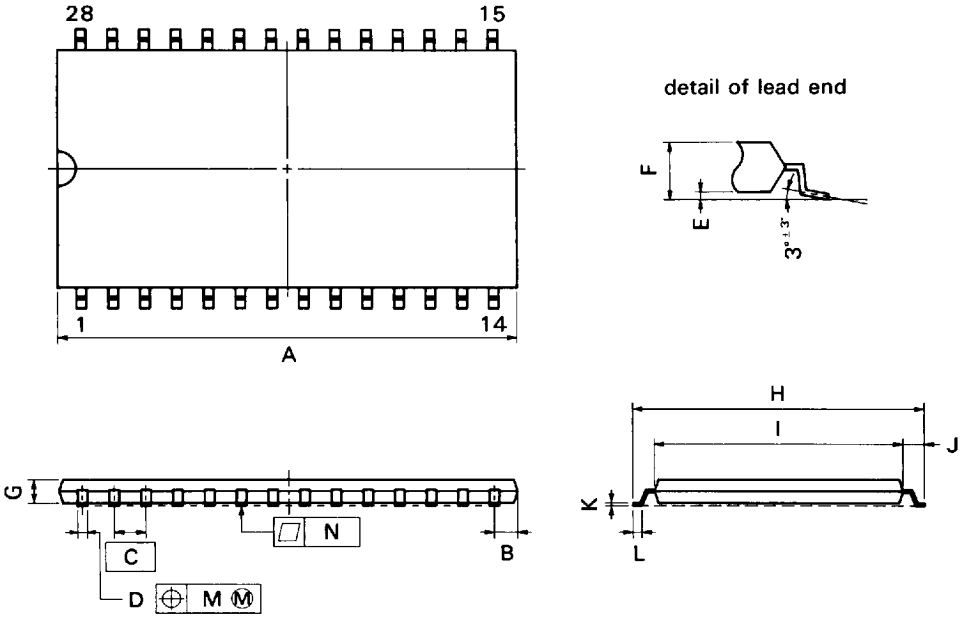


P28V-254-400A

NOTE
Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	36 83 MAX	1.450 MAX.
F	$0.5^{\pm 0\ 1}$	$0.020^{+0\ 004}_{-0\ 005}$
G	ϕ0.25	ϕ0.010
H	2 54	0.100
I	1.27	0.050
J	1.27 MAX.	0.050 MAX.
K	1.0 MIN	0.039 MIN.
M	8.9 MAX.	0.350 MAX.
N	$2.8^{\pm 0\ 2}$	$0.110^{+0\ 009}_{-0\ 008}$
Q	10 16 MAX	0.400 MAX.
V	$0.25^{+0\ 10}_{-0\ 05}$	$0.010^{+0\ 004}_{-0\ 003}$
W	2.54	0.100
Y	$3.3^{\pm 0\ 5}$	$0.130^{\pm 0\ 02}$

28 PIN PLASTIC TSOP (400mil)



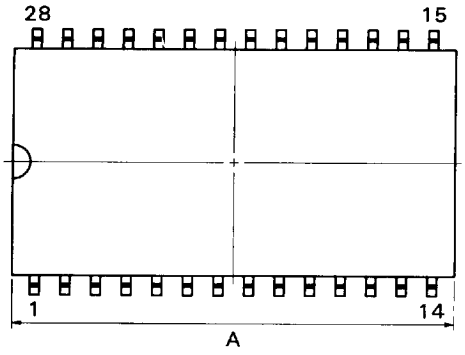
S28G5-50-7JD

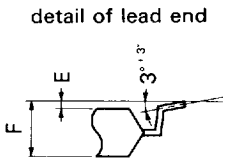
NOTE

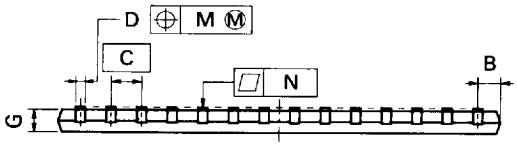
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

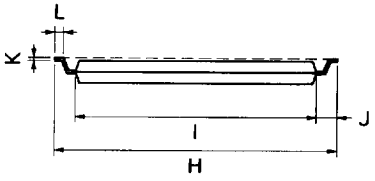
ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX.	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
E	$0.05^{\pm 0.05}$	$0.002^{\pm 0.002}$
F	1.1 MAX	0.044 MAX.
G	0.97	0.038
H	$11.76^{\pm 0.2}$	$0.463^{\pm 0.008}$
I	$10.16^{\pm 0.1}$	$0.400^{\pm 0.004}$
J	$0.8^{\pm 0.2}$	$0.031^{+0.008}_{-0.008}$
K	$0.14^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
L	$0.5^{\pm 0.1}$	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004

28 PIN PLASTIC TSOP (400mil)









S28G5-50-7KD

NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.81 MAX.	0.741 MAX.
B	1.15 MAX	0.046 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
E	$0.05^{\pm 0.05}$	$0.002^{\pm 0.002}$
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	$11.76^{\pm 0.2}$	$0.463^{\pm 0.008}$
I	$10.16^{\pm 0.1}$	$0.400^{\pm 0.004}$
J	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
K	$0.14^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
L	$0.5^{\pm 0.1}$	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004

RECOMMENDED SOLDERING CONDITIONS★

The following conditions (see table below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document "SMT MANUAL" (IEI-1207).

μPD424800LE

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature . 230° C or below, Reflow time 30 seconds below (210°C or higher), Number of reflow process : 1, Exposure limit* · 7 days (10 hours pre-baking is required at 125°C afterwards).	IR30-107
VPS	Peak package's surface temperature . 215°C or below, Reflow time : 40 seconds below (200°C or higher), Number of reflow process : 1, Exposure limit* . 7 days (10 hours pre-baking is required at 125°C afterwards).	VP15-107
Partial heating method	Terminal temperature : 300°C or below, Flow time · 10 seconds or below, Exposure limit* : None	

* : Exposure limit before soldering after dry-package is opened.
Storage conditions : 25°C and relative humidity at 65% or less.

NOTE : Do not apply more than a single process at once,except for "Partial heating method".

μPD424800G5

Undecided: Please consult with our sales offices.

TYPE OF THROUGH HOLE MOUNT DEVICE

μPD424800V

Soldering process	Soldering conditions
Wave soldering	Solder temperature : 260°C or below, Flow time : 10 seconds or below.