SY0002

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• INTRODUCTION

The SY0002 is a crystal-based PLL synchronizer designed as a module level subsystem for easy incorporation into telecommunication equipment.

• FEATURES

- Low jitter output from intrinsically low jitter VCXO;
- Four selectable references inputs: 8, 16, 32 and 64KHz;
- Alarms and status;
- Buffered reference output;
- Tristate (high impedance) reference and oscillators outputs;
- Provides free running clock output;
- The unit changes timing modes in response to external events;
- J-TAG service port for re-programming and servicing;

• APPLICATIONS

- ATM
- SDH
- PDH
- SONET
- other telecommunication equipment.

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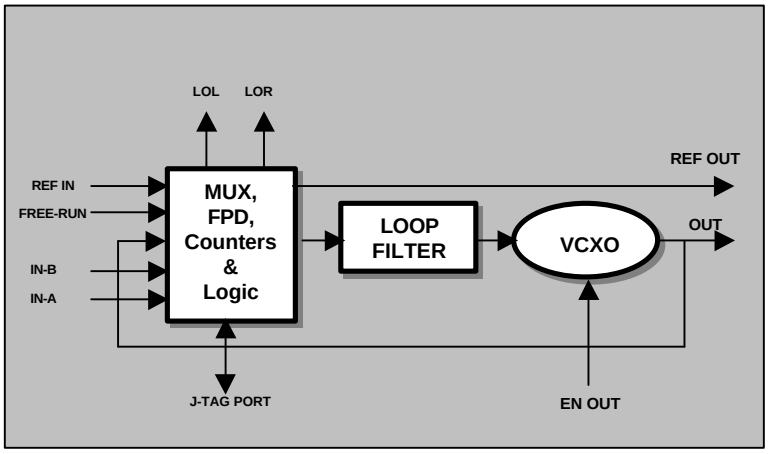

• DESCRIPTION

The SY0002 is a Phase Lock Loop has been designed as a module level subsystem for easy incorporation into telecommunication equipment. The module generates the output from a low jitter VCXO. The SY0002 can lock to one of four reference frequencies from 8 to 64kHz that can be selected using to external select pins. The counters, phase detector and other logic are implemented in programmable logic. The loop bandwidth is optimized according to used VCXO and wanted output performance. The two output signals monitor the status of the phase loop LOL (Loss of Lock) and LOR (Loss of Reference). The two control inputs provides module to go into free-run regardless of the reference (FREE_RUN) and to the tristate high impedance output (OUT EN). The SMD package dimensions are 19.4 x 20.3 mm and power supply is 3.3V.

- INPUT REFERENCE SELECTION

IN-A	IN-B	REFERENCE SELECTED
0	0	8KHz (default)
1	0	16KHz
0	1	32KHz
1	1	64KHz

- OUTPUT PROGRAMMING

EN OUT	FREE-RUN	OUTPUT
0	0	Locked to Reference
1	X	Hi-Z Tri-State
0	1	Free-Run

- ALARM STATES

LOL	LOR	ALARM
0	0	No alarm
1	0	Loss of Lock
0	1	Loss of Reference

• PIN DESCRIPTION

Pin #	Name	Description
1	REF OUT	Reference Output -> The buffered signal from REFERENCE IN pin.
2	TCK	J-TAG port for factory usage – TCK
3	TMS	J-TAG port for factory usage – TMS
4	GND	Ground
5	FREE-RUN	Free-Run -> Control input to force unit to run as free running oscillator
6	LOR	Loss of Reference -> Output signal shows presence of the reference
7	LOL	Loss of Lock -> Output signal shows status of the PLL
8	REF IN	Reference Input -> Reference input signal
9	OUT	Oscillator Output -> Output of the module
10	OUT EN	Output Enable -> Control input to enable/disable the module output
11	Vcc	Positive supply voltage
12	TDO	J-TAG port for factory usage – TDO
13	IN-B	External Reference 1 Input -> Select input from reference 1
14	IN-A	External Reference 2 Input -> the input from reference 2

• ORDERING INFORMATION

SY0002-19.44	*Output frequency 19.44MHz*
SY0002-38.88	*Output frequency 38.88MHz*
SY0002-77.76	*Output frequency 77.76MHz*

- *For other frequencies contact the factory!*

• SPECIFICATION

General Specifications	Mechanical	19.4 x 20.3 mm	SMT Module FR4 14pins dual-in-line
	Power Environment Internal Oscillators	3.3VDC, <100mA Operating Temperature Storage Temperature Humidity Voltage Controlled Crystal Oscillator (VCXO)	Regulated 0°C to 70°C -40° to 85°C 5% to 95% non-condensing
Input Signals	Number of Reference Inputs	1	
	Input reference frequency Signal Level	8, 16, 32 and 64kHz HCMOS/TTL Compatible	Select by external pins
Output Signals	Number of Outputs	2	
	Output 1	19.44, 38.88, 77.76MHz	User defined
	Output 1 Signal Level	HCMOS	
	Output 2	Buffered REF IN	
	Output 2 Signal Level	HCMOS	
	Tracking/Capture Range	±25ppm min	
Signal Quality Performance	Jitter generation	<0.001UI	
	Jitter tolerance	2 µs, 10 Hz (0.05 UI @ 8KHz)	
Frequency Output Performance	Free run accuracy	±20ppm max. @ 25°C	No reference signal

- **OUTLINE DRAWING**