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A TDK Group Company

SSI 75T981/982
Precise Call Progress Tone Detector

July 1990

4

DESCRIPTION

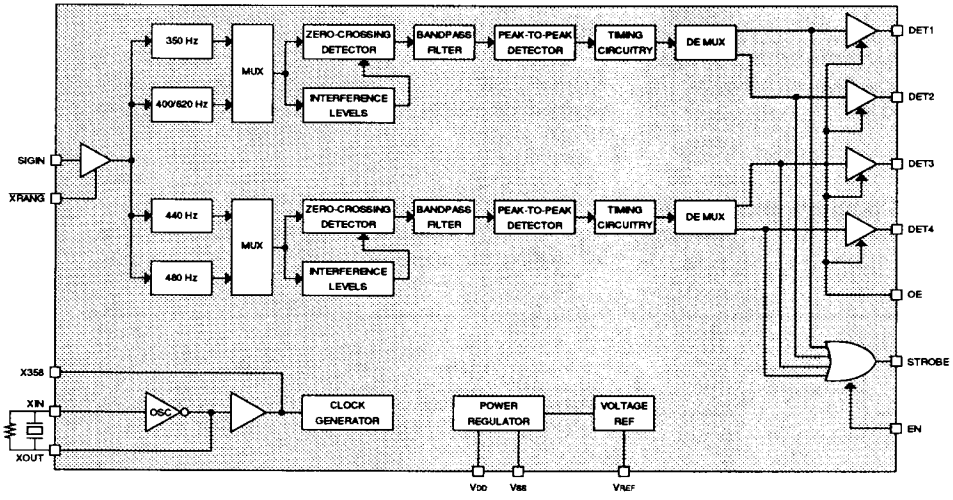
The SSI 75T981 and SSI 75T982 Precise Call Progress Tone Detector circuits enable automatic monitoring of tones in dial telephone systems for the purpose of routing calls. Built using CMOS switched capacitor technology, each has four independent channels for detecting precise tones in the 305 to 640 Hz range. The outputs of the channels have a response related to the respective tone durations.

The SSI 75T981 and SSI 75T982 are identical except for the tones detected. The SSI 75T981 will decode 350Hz, 400Hz, 440Hz and 480Hz. The SSI 75T982 will decode 350Hz, 440Hz, 480Hz and 620Hz tones.

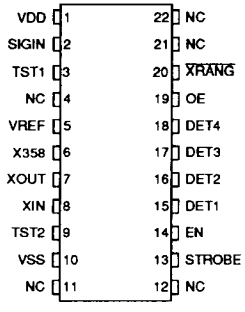
FEATURES

- **Detects & decodes precise tones throughout 305-640 Hz telephone progress band**
- **35 dB dynamic range**
- **Single supply CMOS (low power)**
- **Adjustable gain sensitivity**
- **Supply range 4.75 to 5.5 VDC**
- **Uses 3.58 MHz crystal**
- **Three-state outputs**
- **Standard 22-pin DIP**
- **Second source to Teltone M981 and M982**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The functional block diagram is shown on page 1. Channels 1 and 2, and 3 and 4 are multiplexed, respectively as shown. Each channel starts with a 4-pole band-pass filter that reduces the amplitude of the out-of-band signals. The output of the front-end filter is fed into two circuits, one being a zero-crossing detector which functions as a limiter-AGC, and the other being a circuit that controls the level of the interference floor based on the level of the incoming signal. The output of the ZCD, and energy-limited signal, is fed into a peak-to-peak detector that determines if the precise frequency is present by checking the amplitude of the signal from the back-end filter. Pulses from the peak-to-peak detector, which indicate the presence of the precise tone, are counted to time the duration of the input pulsed-tone. If the criteria of the specifications are met, the appropiate detect output goes to the high state. As shown in the block diagram, all circuitry after the front-end filters is multiplexed. A digital demultiplexer follows the P-P detector to provide the four distinct outputs.

SIGIN

The input signal is applied to the SIGIN pin and is AC-coupled into the front-end filters. The SSI 75T981 and SSI 75T982 can amplify a low level signal by 10 dB when the $\overline{\text{XRANG}}$ pin is held low.

DET OUTPUTS & OE

Outputs DET1-4 are CMOS push-pull when enabled (OE="1") and high impedance when disabled (OE="0"). A "1" on a DET pin indicates that the appropriate valid tone pulse was detected (see Table 1). Detect timing is shown in Figure 1.

STROBE & EN

The STROBE pin is the logical OR of the DETn outputs and will indicate when any one of the four call progress tones has been detected. STROBE is unaffected by OE but goes to a high impedance state when EN="0".

XIN, XOUT & X358

Internal timing and clocks are derived form the 3.58 MHz clock. The SSI 75T981 and SSI 75T982 contain an on-board inverter with sufficient gain to provide oscillation when connected to a low cost "colorburst" crystal. The crystal is connected between XIN and XOUT. A 1MΩ 10% resistor is also connected between these pins. In this mode, X358 is a clock frequency output available to drive other parts requiring the same frequency.

The part will also operate with an external digital clock (duty cycle 40% to 60%).

VREF

Internal analog signal reference voltage. Noise or interference coupled onto this pin may degrade chip functionality.

TST1 & TST2

Manufacturer's special test pins. These pins should be left floating, not grounded.

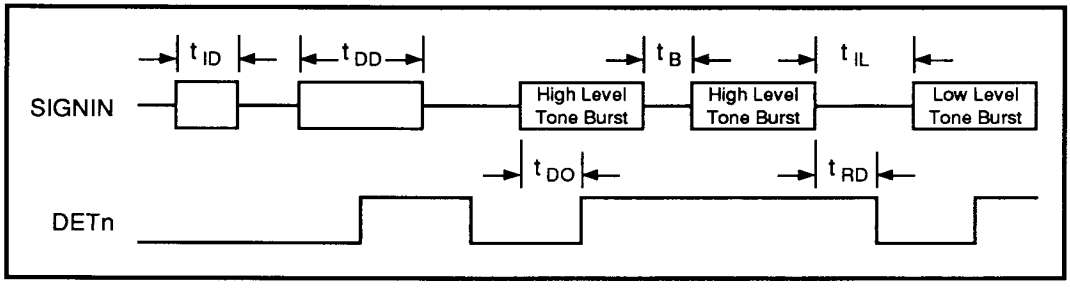


FIGURE 1: Timing Diagram

TIMING CHARACTERISTICS
(Ta = 25°C, V_{DD}-Vss = 4.75V to 5.5V)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
t_{DD}	Signal Duration for Detection	In band, see Electrical Char.	200	-	ms
t_{DO}	Time to Output	In band, see Electrical Char.	-	200	ms
t_B	Bridge Time	In band, see Electrical Char.	-	30	ms
t_{ID}	Signal Duration for Rejection	Noise at SIGIN: –50 dBm, 0.2-3.4 kHz	-	160	ms
t_{RD}	Time to Release	Noise at SIGIN: –50 dBm, 0.2-3.4 kHz	-	200	ms
t_{IL}	Interval Duration for Detection of Both Signals	High to Low; High = 0 dBm, Low = –25 dBm	1	-	sec
t_{EN}	DETn Pin Enable Time, Z to Low or High	C_L = 50 pF, R_L = 100 kΩ	-	450	ns
t_{DS}	DETn pin Disable Time, Low or High to Z	C_L = 50 pF, R_L = 100 kΩ	-	450	ns

4

TABLE 1: Frequency Detection

SIGNAL PRESENT (fo)		DET1	DET2	DET3	DET4	OE	STROBE	EN
75T981	75T982							
350 Hz	350 Hz	1	X	X	X	1	1	1
400 Hz	620 Hz	X	1	X	X	1	1	1
440 Hz	440 Hz	X	X	1	X	1	1	1
480 Hz	480 Hz	X	X	X	1	1	1	1
Other In-Band		0	0	0	0	1	0	1
Any		High Impedance				0	0	0

Note: Out-of-band tones may cause short detect pulses if at sufficient amplitude and pulsed duration.

ELECTRICAL CHARACTERISTICS
(0°C ≤ Ta ≤ 70°C)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
VDD		4.75	5.5	V
Oscillator Frequency Deviation	At XOUT from 3.57959 MHz	–0.01	+0.01	%
Power Supply Noise	0.1 - 5 kHz	-	20	mVpp
Current Drain	VDD=5.5V, Ta = 0°C	-	30	mA
Must Detect Signal				
Frequency Range		–1.0	+1.0	% of *fo*
Level (see Note 2)	$\overline{\text{XRANG}}$=0; In-Band, see Table 1	–35	–10	dBm
	$\overline{\text{XRANG}}$=1; In-Band, see Table 1	–25	0	dBm
Must Reject Signal Level	$\overline{\text{XRANG}}$=0; Noise at SIGIN: -50dBm, 0.2 - 3.4 kHz	-	–60	dBm
	$\overline{\text{XRANG}}$=1; Noise at SIGIN: -50dBm, 0.2 - 3.4 kHz	-	–50	dBm
Level Skew Between Adjacent In-Band Signals for Detection of both	see Note 4	-	6	dB
Steady State Response Must Reject Level	$f < fo - 5\%$ or $f > fo + 5\%$ see Timing Characteristics & Note 3	-	0	dBm
SIGIN Pin				
Voltage Range		VDD - 10	VDD	V
Input Impedance	Resistance; f = 500 Hz	80	-	kΩ
	Capacitance	-	15	pF
Gain	$\overline{\text{XRANG}}$=0	9.9	10.1	dB
$\overline{\text{XRANG}}$ Pin				
VIL		-	0.5	V
VIH		VDD - 2.0	-	V
Pullup Current	$\overline{\text{XRANG}}$=VSS	-	–10	µA
Detect Pins, DETn				
VOL	ISINK = –1mA	-	0.5	V
VOH	ISOURCE = 1mA	VDD - 0.5	-	V
IOZ	VO = VDD, VSS	-	1	µA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
STROBE Pin				
VOL	ISINK = –1 mA	-	0.5	V
VOH	ISOURCE = 1 mA	VDD - 0.5	-	V
OE, EN Pins				
VIL		-	0.5	V
VIH		VDD - 2.0	-	V
Pullup Current	OE, EN = VSS	-	–10	µA
External Clock				
VIL	XOUT Open	-	0.2	V
VIH	XOUT Open	VDD - 0.2	-	V
Duty Cycle	XOUT Open	40	60	%
XIN, XOUT Loading				
Capacitance	Crystal oscillator active	-	10	pF
Resistance	Crystal oscillator active	20	-	MΩ
X358 Pin (CL = 20 pF)				
VOL	ISINK = –10 µA	-	0.2	V
VOH	ISOURCE = 10 µA	VDD - 0.2	-	V
Duty Cycle		40	60	%

Notes:

1. All parameters are specified at VDD = 5 volts and $\overline{\text{XRANG}}$ at a logical "high" state, which implies unity front-end gain. Power levels in dBm are referenced to 600Ω.

2. A post-filter AGC is employed to enhance end-of-tone detection for high-level signals. A drop in amplitude of the input tone may cause an end-of-tone (interval) indication.

3. Large input voltage transients may cause excessive ringing in the highly selective filter, causing spurious detection. The detects are not considered as incorrect circuit operation.

4. Any tone 40 Hz – 1% from fo must adhere to this specification, where fo is defined in Table 1.

ABSOLUTE MAXIMUM RATINGS
(Operation above absolute maximum ratings may damage the device.)

PARAMETER	CONDITIONS	RATING
DC Supply Voltage	V_{DD} – Vss	+7V
Input Voltage	All inputs except SIGIN	Vss – 0.3V to V_{DD} + 0.3V
SIGIN Voltage		V_{DD} – 18V to V_{DD} + 0.3V
Storage Temperature		–65°C to 150°C
Operating Temperature		0°C to 70°C
Lead Temperature	Soldering, 10 sec.	260°C

NORMAL CALL PROGRESS TONES AND SEQUENCE (Refer to Figure 2.)

TONE	FREQUENCY (Hz)	CADENCE
Precision Dial Tone	350 + 440	Continuous
Old Dial Tones	600 + 120 or 133 and other combinations	Continuous
Precision Busy	480 +620	0.5 s on 0.5 s off
Old Busy	600 +120	0.5 s on 0.5 s off
Precision Reorder	480 +620	0.3 s on local 0.2 s off reorder
Old Reorder	600 +120	0.2 s on toll 0.3 s off reorder 0.25 s on toll 0.25 s off local
Precision Audible Ringback	440 +480	2 s on 4 s off
Old Audible Ringback	420 +40 and other combinations	2 s on 4 s off

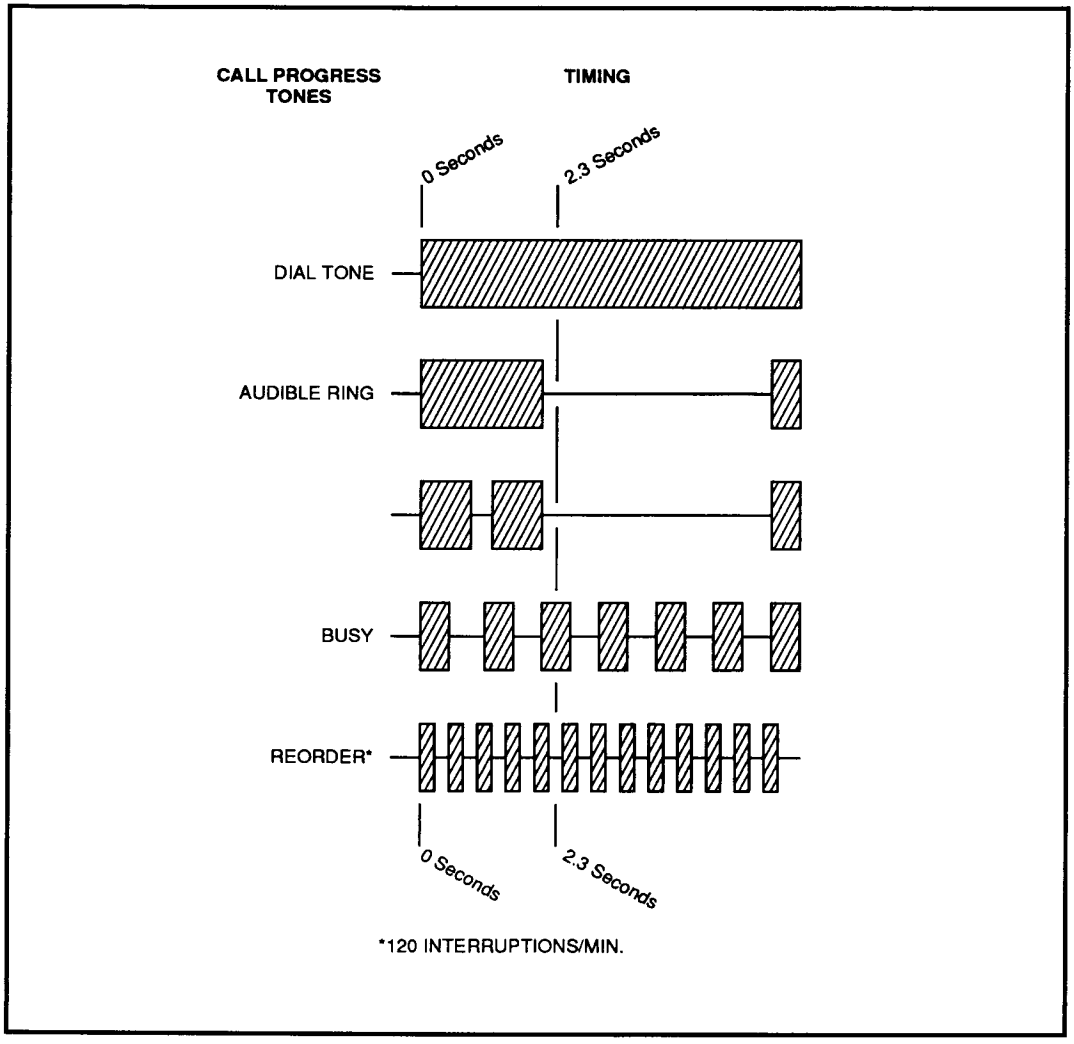


FIGURE 2: Normal Call Progress Tones and Sequence

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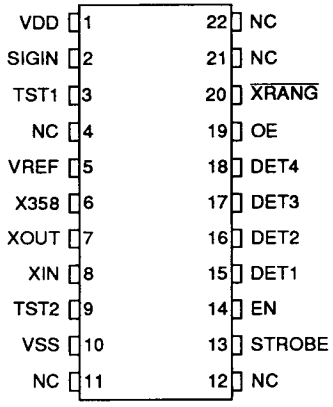
PACKAGE PIN DESIGNATIONS
(TOP VIEW)



22 - PIN DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T981 22-Pin Plastic DIP	75T981-CP	75T981-CP
SSI 75T982 22-Pin Plastic DIP	75T982-CP	75T982-CP

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