

April 1994

DESCRIPTION

The SSI 32P3041 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of encoded read signals. The circuit will handle a data rate of 32 Mbit/s.

In Read mode the SSI 32P3041 provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

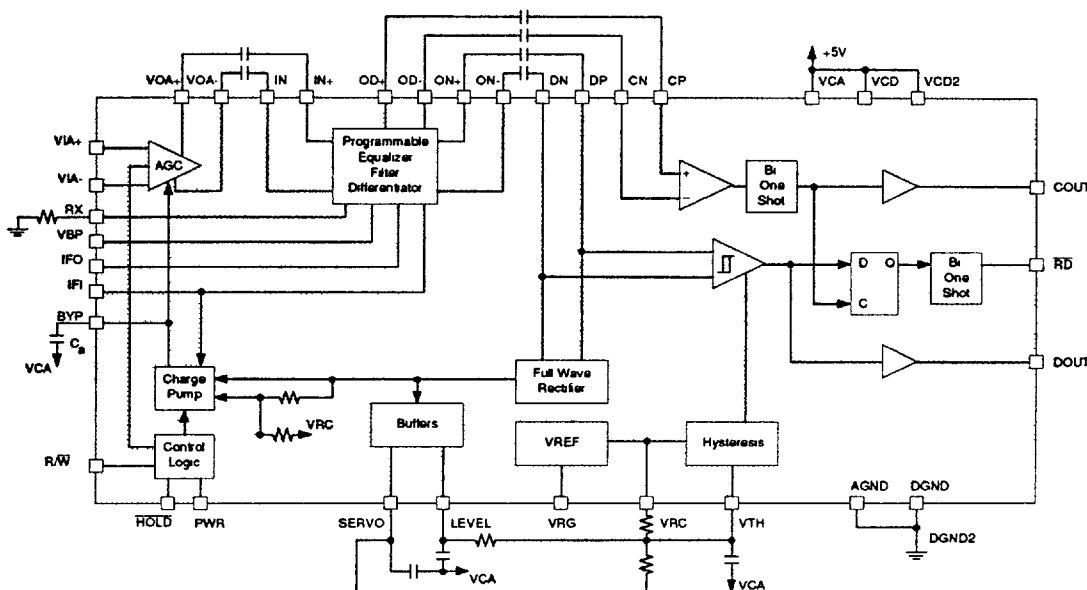
Write to read transient recovery is enhanced by providing AGC input impedance switching and a selectable Fast Recovery mode that provides a higher decay current.

Additionally, the SSI 32P3041 contains an integrated programmable electronic filter with cutoff frequencies between 2.5 and 13 MHz. High frequency boost (for pulse slimming) of up to 9.5 dB is also provided. The SSI 32P3041 requires only a +5V power supply and is available in 36-lead SOM and 32-lead TQFP packages.

FEATURES

- Compatible with 32 Mbit/s data rate operation
- Fast Attack/Decay modes for rapid AGC recovery
- Dual rate charge pump for fast transient recovery charge pump currents track programmable channel bandwidth
- Low drift AGC hold, fast AGC recovery, and low AGC input impedance control signals. Circuitry supports programmable gain non-AGC operation
- Temperature compensated, exponential control AGC
- Precision wide bandwidth fullwave rectifier
- Supports programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components
- $\pm 2\%$ Filter group delay variation from 0.3 FC to FC
- Servo burst output available
- Differential hysteresis qualifier comparator to ease clock channel timing
- Accurate feed forward or fixed threshold set

BLOCK DIAGRAM



0494 - rev.

SSI 32P3041

Pulse Detector with Programmable Filter

FEATURES (continued)

- 1 ns max pulse pairing with sine wave input
- 5 mW low power Idle mode
- TTL read data output
- +5V only operation
- 36-pin SOM and 32-pin TQFP packages

FUNCTIONAL DESCRIPTION

The SSI 32P3041 Pulse Detector is designed to support a 32 Mbit/s data rate. The signal processing circuits include a wide band variable gain amplifier, a programmable electronic filter, differentiator and pulse slimming equalizer, a precision wide bandwidth fullwave rectifier, and a dual rate charge pump. A fully differential filter, differentiator, equalizer, and fullwave rectifier are provided to minimize external noise pick-up. To optimize recovery for constant density recording, the AGC charge pump current tracks the programmable filter current IFI. The differentiator zero tracks the programmable filter cutoff frequency. Thus in constant density recording applications, an approximately constant differentiated signal amplitude is maintained. The desired filter response and equalization are easily programmed with the SSI 32D4661, Time Base Generator DACs. A dual rate attack charge pump and a Fast Decay mode are included for fast transient recovery. At maximum IFI current, the normal AGC attack current is 0.28 mA. When the signal exceeds 125% of the nominal signal level, the attack current is increased by a factor of 5. The nominal decay current at max IFI is 5.6 μ A. The decay current is increased 20 times when in the Fast Decay mode. In this mode, transients that produce low gain will recover more rapidly with the fast decay current, while transients that produce high gain will put the circuit in the Fast Attack Recovery mode. The Decay modes are automatically controlled within the device. When R/W is low, the AGC is in its Hold mode and its input impedance is switched low. When R/W is switched high, the AGC remains in the hold and low input impedance state for 2.3 μ s and then switches to the Fast Decay mode for 0.7 μ s. The AGC amplifier input impedance is reduced to allow quick recovery of the AGC amplifier input AC coupling capacitors. When the HOLD input is low, the AGC action is stopped and the AGC amplifier gain is set by the voltage at the BYP pin. In most applications, the BYP pin voltage is stored on an external capacitor when HOLD

goes low. In applications where AGC action is not desired, the BYP voltage can be set by a resistor divider network connected from VCC to VRC. If a programmable gain is desired, the resistor network could be driven by a current DAC. The precision fullwave rectifier produces an accurate Level and Servo output signal. These outputs are referenced to the reference voltage VRC. SERVO and LEVEL are buffered open emitter outputs with 100 ohm series current limiting resistors. These outputs could be further filtered with external capacitors.

LEVEL has an internal 50 μ A discharge current source. An optional Servo output capacitor discharge circuit can be included. An external resistor connected to the RX pin sets the electronic filter reference current which is the source from pin IFO. If a programmable frequency response is desired, a portion of the current from IFO, which is proportional to absolute temperature, must be injected into pin IFI. This could be accomplished by a current DAC. Some frequency response programming may be accomplished by connecting IFO to IFI and switching different resistors to pin RX. Frequency boost is accomplished by varying the voltage at VBP. VBP has a nominal 100 mV built-in offset so that the circuit has 0 dB boost for VBP below 100 mV. The voltage at VBP should be proportional to the reference voltage at pin VRG.

A differential comparator with floating hysteresis threshold allows differential signal qualification for noise rejection. An accurate feed forward qualification level is generated by comparing the difference between LEVEL and VRC. VRC is referenced to VCA. Thus with the VTH resistor network connected from VCA to VRC, an accurate fixed threshold can be established. The threshold is clamped to a minimum value of 50 mV. Thus a qualified signal must exceed this minimum level even when the VTH-VRC voltage is zero. A qualified signal zero crossing triggers the output one shot. The one shot period is set internally. Low level differential outputs are provided for high speed operation and to minimize noise generation.

SSI 32P3041 Pulse Detector with Programmable Filter

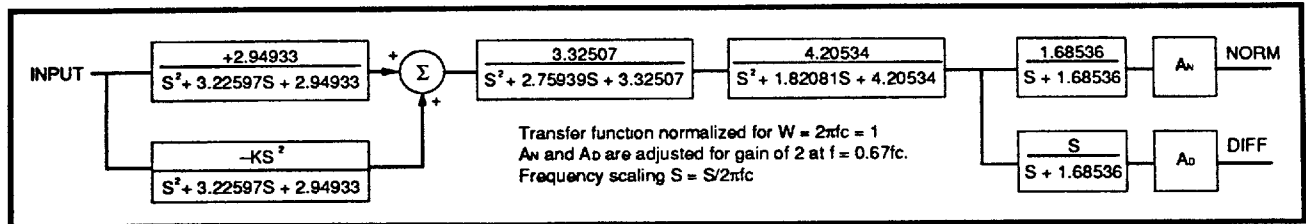


FIGURE 1: Bessel Filter Transfer Function

$$K = 2.94933 \left(10^{\frac{\text{BOOST (dB)}}{20}} - 1 \right)$$

TABLE 1: Typical Change Inf - 3 dB Point with Boost

Boost (dB)	Gain@ f_c (dB)	Gain@peak (dB)	f_{Peak}/f_c	$f_{-3\text{dB}}/f_c$	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.20	0.36
2	-1	0.00	no peak	1.47	0.76
3	0	0.15	0.62	1.74	1.22
4	1	1.00	1.08	1.96	1.73
5	2	2.12	1.24	2.13	2.30
6	3	3.35	1.24	2.28	2.94
7	4	4.56	1.39	2.42	3.65
8	5	5.82	1.39	2.54	4.46
9	6	7.04	1.39	2.66	5.36
10	7	8.24	1.39	2.77	6.38
11	8	9.41	1.39	2.88	7.52
12	9	10.55	1.39	2.98	8.79
13	10	11.70	1.55	3.08	10.22

- Notes: 1. f_c is the original programmed cutoff frequency with no boost.
 2. $f_{-3\text{dB}}$ is the new -3 dB value with boost implemented.
 3. f_{peak} is the frequency where the magnitude peaks with boost implemented.

e.g., $f_c = 13\text{ MHz}$ when boost = 0 dB
 if boost is programmed to 5 dB, then $f_{-3\text{dB}} = 27.69\text{ MHz}$
 $f_{\text{peak}} = 16.12\text{ MHz}$

SSI 32P3041

Pulse Detector with

Programmable Filter

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
VIA+, VIA-	I	AGC Amplifier input pins.
IN+, IN-	I	Equalizer/filter input pins.
DP, DN	I	Data inputs to data comparators and fullwave rectifier.
CP, CN	I	Differentiated data inputs to the clock comparator.
VTH	I	Threshold level setting input for the data comparators.
R/W	I	TTL compatible input when high puts the charge pump in the normal mode.
PWR	I	TTL compatible input when high puts the circuit in its normal operating mode.
HOLD	I	TTL compatible input when low disables the AGC action by turning off the charge pump

OUTPUT PINS

VOA+, VOA-	O	AGC amplifier output pins.
ON+, ON-	O	Equalizer/filter normal output pins.
OD+, OD-	O	Equalizer/filter differentiated output pins.
DOUT	O	Test point for monitoring the data F/F D-input. Usage requires an external 2.4 k Ω resistor from DOUT to GND. (Not available in 32-pin TQFP package.)
COUT	O	Test points for monitoring the data F/F clock inputs. Usage requires an external 2.4 k Ω resistor from COUT to GND.
		(Not available in 32-pin TQFP package.)
RD	O	TTL compatible read data output pins.
LEVEL	O	Open NPN emitter output that provides a fullwave rectified signal for the VTH input. The signal is referenced to VRC.
SERVO	O	Open NPN emitter output that provides a fullwave rectified servo signal. The signal is referenced to VRC.

ANALOG PINS

VRC	-	Reference voltage pin for SERVO and LEVEL. VRC is referenced to VCA.
VRG	-	Reference voltage pin for the programmable filter. VRG is referenced to ground.
VBP	-	The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND.
RX	-	Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO.
IFO		Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin.

SSI 32P3041

Pulse Detector with Programmable Filter

PIN DESCRIPTION (continued)

ANALOG PINS (continued)

NAME	TYPE	DESCRIPTION
IFI		Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency.
BYP		The AGC integrating capacitor C_A is connected between BYP and VCA.
VCA, VCD, VCD2		Analog and Digital +5 volts.
AGND, DGND, DGND2		Analog and Digital grounds.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, $4.5V < VCC < 5.5V$, $0^\circ C < T_a < 70^\circ C$

ABSOLUTE MAXIMUM RATINGS (Operation above maximum ratings may damage the device.)

PARAMETER	RATING
Storage Temperature	-65 to +150°C
Junction Operating Temperature, T_j	+130°C
Supply Voltage, VCA, VCD	-0.7 to 7V
Voltage Applied to Inputs	-0.5 to VCA, VCD +0.5V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING
Supply Voltage $VCA = VCD = VCC$	$4.5V < VCC < 5.5V$
Ambient Temperature, T_a	$0^\circ C < T_a < 70^\circ C$

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ISS Supply Voltage Current	Active mode		75	90	mA
	Low-Power mode		1	1.5	mA
PD Power Dissipation	Active mode		400	500	mW
	Low-Power mode		5	8	mW

SSI 32P3041

Pulse Detector with Programmable Filter

ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified, $4.5V < V_{CC} < 5.5V$, $0^{\circ}C < T_a < 70^{\circ}C$

LOGIC SIGNALS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VIL TTL Input Low Voltage		-0.3		0.8	V
VIH TTL Input High Voltage		2.0		$V_{CC} + 0.3$	V
IIL TTL Input Low Current	$V_{IL} = 0.4V$	-0.4			mA
IIH TTL Input High Current	$V_{IH} = 2.7V$			0.1	mA
VOH TTL Output High Voltage	$I_{OH} = -400\mu A$	2.4			V
VOL TTL Output Low Voltage	$I_{OL} = 3\text{ mA}$			0.5	V
TRDRF Output Rise and Fall Time	$CL = 15\text{ pF}$			7	ns
TH Hold Input Switching Times				0.3	μs

AGC AMPLIFIER

The input signals are AC coupled to V_{IA+} and V_{IA-} , V_{OA+} and V_{OA-} are AC coupled to I_{N+} and I_{N-} , O_{N+} and O_{N-} are AC coupled to DP and DN, $C_a = 1000\text{ pF}$, $F_{in} = 4\text{ MHz}$. Unless otherwise specified, the output is measured differentially at V_{OA+} and V_{OA-} , $F_{in} = 4\text{ MHz}$ and filter boost at $F_c = 0\text{ dB}$.

VIR	Input Range	Filter boost at $FC = 0\text{ dB}$	24		240	mVppd
		Filter boost at $FC = 9\text{ dB}$	20		120	mVppd
VDPN	DP-DN voltage	$V_{IA\pm} = 0.1\text{ Vpp}$	0.85		1.05	Vppd
VDPNV	DP-DN Voltage Variation	$24\text{ mV} < V_{IA\pm} < 240\text{ mV}$			8.0	%
AV	Gain Range		1.9		22	V/V
AVPV	Gain Sensitivity			38		dB/V
VOADR	V_{OA+} , V_{OA-} Dynamic Range	THD = 1% max	0.75			Vpp
ZIN	Input Impedance	$R/\bar{W} = \text{high}$	3.0		7.5	k Ω
ZCMIN	Common Mode Input Impedance	$R/\bar{W} = \text{high}$		1.5		k Ω
		$R/\bar{W} = \text{low}$		200		Ω
VOS	Output Offset Voltage Variation	Over gain range	-200		+200	mV
VINO	Input Noise Voltage	gain = max, filter not connected to $V_{OA\pm}$, $R_s = 0\Omega$, $B_w = 15\text{ MHz}$		5	10	nV/ $\sqrt{\text{Hz}}$
BW	Bandwidth	No AGC action	55	75		MHz
CMRR	Common-mode Rejection Ratio	gain = max, $V_{in} = 0\text{ VDC} + 100\text{ mVpp}$ @ 5 MHz	40	65		dB
PSRR	Power Supply Rejection Ratio	gain = max, 100 mVpp @ 5 MHz on VCA, VCD, VCD2	45	67		dB
TGD	Gain Decay Time	$V_{IA\pm} = 240\text{ mV}$ to 120 mV $V_{OA\pm} > 0.9$ Final Value BYP \leq , 1000 pF, IFI = max		34	44	μs
TGA	Gain Attack Time	$V_{IA\pm} = 120\text{ mV}$ to 240 mV $V_{OA\pm} < 1.1$ Final Value BYP \leq , 1000 pF, IFI = max		1.5	2	μs

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Pulse Detector with Programmable Filter

EQUALIZER/FILTER (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TLZ Low Impedance Mode Time	R/ \bar{W} transitions from low to high	1.5		3.0	μ s

AGC CONTROL

The input signals are AC coupled to DP and DN. $C_a = 1000$ pF, LEVEL load = 50 μ A, SERVO load = 100 μ A.

VDI DP-DN Signal Input Range				1.4	V _{pp}
ALO Level (Servo) Output Gain	DP-DN = 0.25 to 0.5 VDC LG = (V _{LEVEL} - V _{RC})/2 (DP-DN)	0.73		0.81	V/V
BWL Level (Servo) Output Bandwidth	1 dB	15			MHz
VLO Level Offset Voltage	Output-V _{RC} , IL = 50 μ A			30	mV
VSO Servo Offset Voltage	Output - V _{RC} , IL = 100 μ A			30	mV
ZLS Level (Servo) Output Impedance	IL = 100 μ A		200	300	Ω
ID Discharge Current			0.008 x IFI		mA
IDF Fast Discharge Current	2.3 to 3.0 μ s after R/ \bar{W} goes high		20 x ID		mA
ICH Charge Pump Attack Current			50 x ID		mA
ICHF Charge Pump Fast Attack Current	DP-DN = 1.35 V _{pp}		5 x ICH		mA
IBYP Pin Leakage Current	HOLD = low, V _{BYP} = V _{CC} -1.5V	-0.1		0.1	μ A
VRC Reference Voltage		V _{CC} -2.52		V _{CC} -2.15	V
IVRC Output Drive		-0.75		0.75	mA
VRG Reference		2.15		2.5	V
IVRG Source Current		1			mA
VAGC Pin Voltage			V _{RC} +1.0		V

EQUALIZER/FILTER The input signals are AC coupled to IN+ and IN-.

f _c Filter Cutoff Frequency	f _c = 19.14(IFI/IFO)(1/R _x)	2.5		13.5	MHz
VRX PTAT Reference Current Set Output Voltage	TA = 25°C I _{Rx} = 0 - 0.7 mA R _x > 1.21 k Ω		850		mV
IFOR PTAT Reference Current Output Current Range	TA = 25°C 1.21 k Ω < R _x < 7.73 k Ω IFO = V _{Rx} /R _x	0.11		0.7	mA

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Pulse Detector with Programmable Filter

EQUALIZER/FILTER (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
IFIR PTAT Programming Current Range	TA = 25°C, VRX = 850 mV	0.11		0.7	mA
VBPR Input Voltage Range		0		VRG	V
IBP Input Bias Current				3	μA
FCA Filter FC Accuracy	FC = 5 to 13.5 MHz	-12		+12	%
AO $[(ON\pm)]/[(IN\pm)]$ Normal Gain	F = 0.67 FC	1.4		2.2	V/V
AD $[(OD\pm)]/[(IN\pm)]$ Diff Gain	F = 0.67 FC	1.0AO		1.3AO	V/V
FB Frequency Boost at FC	FB = 20 log [1.884(VBP-0.1) / VRG+1] VBP -0.1>0	0		9.5	dB
FBA Frequency Boost Accuracy	FB = max	-1		+1	dB
TGD Group Delay Variation	0.3 FC to FC = 13.5 MHz FB = 0 to max	-2		+2	%
VOO Output Offset Voltage	Variation over entire frequency range	-200		+200	mV
VOF Filter Output Dynamic Range	THD = 1.5% max	1.0			Vpp
	THD = 3.0% max F = 0.67 FC	1.25			Vpp
RINF Filter Input Resistance		4.0	6.0	8.0	kΩ
CINF Filter Input Capacitance				7	pF
RO Filter Output Resistance	IO = 0.5 mA		70	85	Ω
IFOD Filter Output Drive Current		-1		+1	mA
VNN Eout Output Noise Voltage ON±	BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = 0		2.2	3.0	mVRMS
	BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = VRG		3.0	4.5	mVRMS
VND Eout Output Noise Voltage OD±	BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = 0		5.4	6.4	mVRMS
	BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = VRG		9.6	10.6	mVRMS

SSI 32P3041

Pulse Detector with Programmable Filter

DATA COMPARATOR

The input signals are AC coupled to DP and DN.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
RINDC Differential Input Resistnace		7		14	k Ω
CINDC Differential Input Capacitance				5	pF
ATH Threshold Voltage Gain, Kth	$0.3 < V_{TH-VRC} < 0.75$	0.42		0.49	V/V
VIAMIN Minimum Threshold Voltage	$V_{TH-VRC} \leq 0.11V$.05		V
TPDDC Propagation Delay	To DOUT		10		ns
ITH VTH Input Bias Current				2	μA
DOUTSS DOUT Signal Swing	2.4 k Ω from DOUT to GND		0.5		V

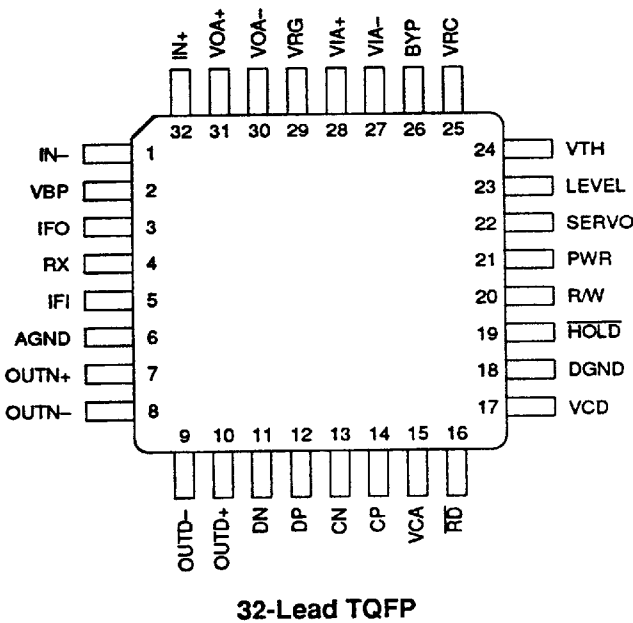
CLOCKING

The input signals are AC coupled to CP and CN.

RINCL Differential Input Resistance		7		14	k Ω
CINCL Differential Input Capacitance				5	pF
TDS D F/F Set Up Time	DP-DN threshold to CP-CN zero cross	0			ns
TPP Pulse Pairing	$V_s = 1V_{pp}$, $F = 2.5$ MHz			1	ns
TPDCL Propagation Delay to RD	$V_s = 20$ mVpp sq wave		14	20	ns
RDPW Output Pulse Width	Measured at 1.4V level	10		20	ns
COUTS Signal Swing	2.4 k Ω from COUT to GND		0.5		V

SSI 32P3041
Pulse Detector with
Programmable Filter

PACKAGE PIN DESIGNATIONS
(Top View)

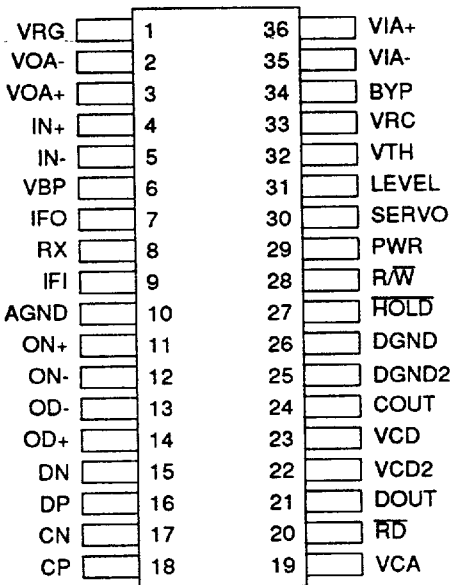


32-Lead TQFP

CAUTION: Use handling procedures necessary
for a static sensitive component.

THERMAL CHARACTERISTICS: θ_{ja}

32-Lead TQFP	124° C/W
36-Lead SOM	75° C/W



36-Lead SOM

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32P3041 32-Lead Thin Quad Flatpack	32P3041-CGT	32P3041-CGT
36-Lead Small Outline	32P3041-CM	32P3041-CM

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