National Semiconductor

December 1992

NGA Series
ASPECT™ III ECL Gate Arrays

General Description

The NGA Series of gate arrays feature the highest possible performance for designs requiring the speed and complexity of the ECL process. This series of gate arrays is based on National's High Performance 0.8 micron ASPECT III ECL process, thus providing both high performance and a low speed-power product of <50 fJ.

The NGA Series of arrays will be offered in sizes ranging from 10,000 gates and 72 I/O up to 80,000 gates and 256 I/O. The internal ECL logic of the NGA Series arrays will consist of two types of ECL internal cells: standard and low power cells with typical gate delays of 110 ps and 140 ps respectively. All NGA Series gate arrays will feature CAD-programmable speed/power options for the internal ECL cells that allows the designer to maximize the performance by individually assigning the switching speed output drive currents for each internal macro. All I/O locations may be programmed to either 100K, 10K or TTL on all arrays in the family (except the NGA095T which has only ECL I/O).

Features

- ASPECT III technology provides 0.8 micron high performance ECL
- High performance ECL (std. power cells): typical delay = 110 ps (FO = 1, L = 0mm)
- High performance ECL (low power cells): typical delay = 140 ps (FO = 1, L = 0mm)
- I/O interfaces: ECL (100K), ECL (10K) or TTL
- CAD-programmable speed/power options on internal ECL cells
- ECL input frequencies in excess of 2 GHz
- High Density: up to 80,000 equivalent gates
- Common cell library with all NGx Series gate arrays
- Four-layer metallization ensures over 85% utilization of internal logic
- Menu-driven design tools, DA4™, uses industry standard software

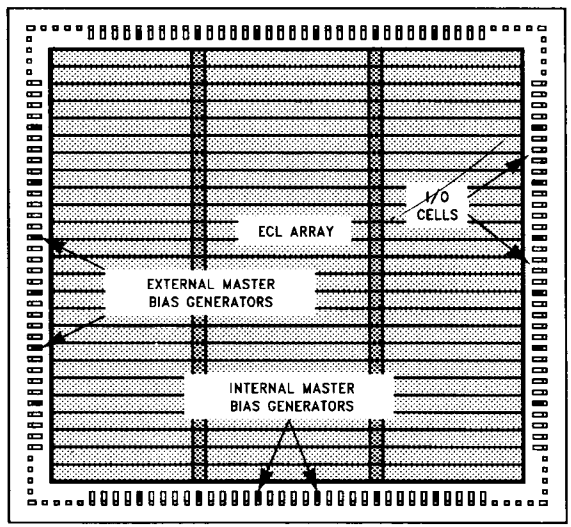

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FIGURE 1. NGA Series Gate Arrays

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RRD-B20M112/Printed in U. S. A.

ASPECT III Process

The NGA Series arrays use a proprietary National process called ASPECT III, an ECL process that provides 0.8 micron ECL devices. This new revolutionary process allows designs to operate in excess of 2 GHz with low power consumption and is the first bipolar process to use poly-silicon for emitter and base structures. Poly-silicide serves as a source of impurities for both the emitter and base. This permits the fabrication of extremely shallow emitter and base regions. The combination of shallow emitter and base regions leads to transistors with a very high switching speed. ASPECT also uses poly-silicon resistors which exhibit low junction capacitance, making them ideal passive elements for high-speed logic circuits.

This same layer of poly-silicon is silicided and used for local interconnection, thus increasing design flexibility and packing density. Contacts for the base, collector are made through poly-silicide, leading to a contactless process. The ASPECT technology is a self-aligning process which is high yielding and scalable to smaller geometries.

Array Organization

Electrical components (transistors, resistors, diodes and capacitors) are organized into repeating structures called internal cells. Macros, which are the building blocks of gate array logic design, are built by interconnecting the components in one or more internal cells.

The NGA Series arrays utilize an internal core of cells arranged in a sea of gate fashion, continuous rows of cells without channels between them. Each row of cells contain slave bias generators to power the entire row, if the cells powered by the generator are not used, then the bias generator is powered down (see *Figure 1*). The I/O and pads are located around the periphery of the internal core. The I/O may be directly interfaced by the internal ECL levels without the need for level shifting or the need of special I/O drivers, all signals must be buffered through the I/O before entering or leaving the internal core.

All NGA Series arrays utilize four-layer metallization for signal and power bussing. One layer of metal is reserved only for power bussing, and the other layers are for interconnect routing.

NGA Series ECL Gate Arrays

TABLE I. The NGA Gate Array Series

Description	NGA005T	NGA010T	NGA095T
ECL Gates	10,240	26,500	80,080
Standard Power Cells	1,024	2,652	0
Low Power Cells	1,024	2,652	16,016
Typical Internal Delays (ps) (1)			
Standard Power Cells	110–300	110–300	
Low Power Cells	140–440	140–440	140–440
Speed, Power Options			
Macro Attributes	Yes	Yes	Yes
Standard/Low Power Cells(2)	Both	Both	All Low Power
Typical Power			
Standard Power (mW)	0.3–1.0	0.3–1.0	
Low Power Cells (mW)	0.1–0.3	0.1–0.3	0.1–0.3
I/O			
100K/10K/10KH	Yes	Yes	Yes
ECL I/O only	0	0	256
ECL/TTL	72	128	0
Power/GND	40	48	83
Packages			
MQUAD(3)	100	160	
LDCC	116	132/172	
CPGA	75/109	99/173	323

Note 1: F.O. = 1, L = 0mm

Note 2: Alternate rows of standard and low power cells

Note 3: Contact NSC sales for availability

Internal Cell Capabilities

The internal core of the NGA series is comprised of two types of internal cells, standard power and low power cells, these internal cells are made up of components (transistors, resistors) that macros overlays are placed on to form logic functions. Both the standard and low power ECL cells provide for speed/power programming, that is to say that the switching speed and output drive currents may be individually set to one of three possible levels. In this way, the speed may be maximized and the power minimized for critical paths.

One internal ECL cell consists of 10 switching transistors, 3 current source transistors, 2 output emitter followers and 22 resistors. It is equivalent to 5 gates.

I/O Capabilities

I/O cells in the NGA Series are capable of performing input, output, transceiver logic, and conversion functions (ECL/TTL). The array's I/O organization is flexible, with each signal pad supported by a dedicated I/O cell. All external signals must enter the internal array to perform logic through any I/O cell, likewise, all internal signals must exit the internal core through any I/O.

The ECL I/O are designed to drive 50Ω loads and may be paired to drive 25Ω loads. Each I/O cell offers a choice of signal termination options. For short signal paths, a series terminated load may be used, thus simplifying designs in systems where external termination on the board is not practical. To minimize noise, internal pull-down resistors are provided to keep unused inputs from floating.

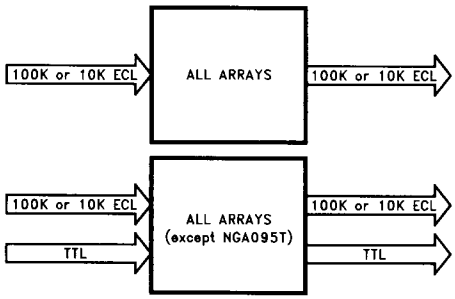

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FIGURE 2. Interface Capabilities

Either 100K, 10K, or 10KH interface capability is available on all NGA Series arrays. All input threshold and logic levels must uniformly belong to the same ECL family. Likewise, the output interface must be the same type as that used for input. The I/O may also be independently configured as either ECL or TTL available on all configurations except the NGA095T The TTL outputs are capable of totem-pole, open-collector, or TRI-STATE® configurations. *Figure 2* illustrates the acceptable interface options for the NGA Series arrays.

Speed/Power Options

Speed/power options are a feature of all NGA Series gate arrays. This feature allows the designer to minimize overall chip power consumption while maintaining speed critical paths.

Two sets of macros are available for each ECL logic function in the NGA macro library, the standard macros and paired macros (see Table II). The paired macros use two times as much current as the standard macros, and are designed for use in the critical circuitry to ensure high speed operation. These two macro types can be used interchangeably on both the high and low power internal cells within the same chip.

TABLE II. Current Setting of Internal ECL Gates (Speed/Power Options)

Power Setting	Low	Medium	High
Low Power Macros			
Current Source (μA)	50	100	200
OEF Current (μA)	50	100	200
Low Power Paired Macros			
Current Source (μA)	100	200	400
OEF Current (μA)	100	200	400
Standard Macros			
Current Source (μA)	150	300	600
OEF Current (μA)	200	400	800
Standard Paired Macros			
Current Source (μA)	300	600	1200
OEF Current (μA)	400	600	1600

Essentially, speed/power options are used to assign the current setting (HIGH = 0.60 mA, MEDIUM = 0.30 mA, LOW = 0.15 mA) for standard power cells, and (HIGH = 0.20 mA, MEDIUM = 0.10 mA, LOW = 0.05 mA) for low power cells, to the current source that controls switching speed; and one of three settings (HIGH = 0.80 mA, MEDIUM = 0.40 mA, LOW = 0.20 mA), for standard power, and (HIGH = 0.20 mA, MEDIUM = 0.10 mA, LOW = 0.05 mA) for low power to the true and complement output emitter followers. The latter setting permits zero power consumption for unused outputs. *Figure 3* illustrates circuit options for each of the three settings.

Speed/Power Options (Continued)

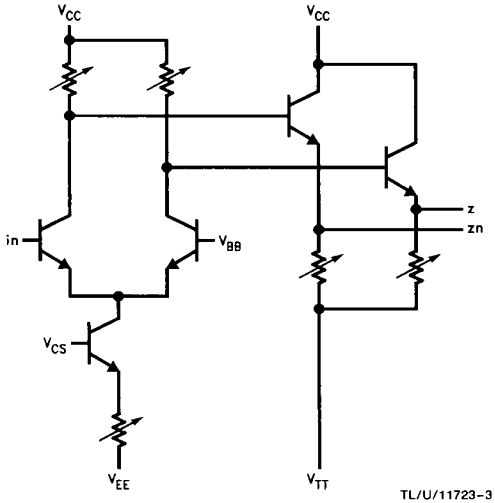


FIGURE 3. Speed/Power Options

The speed/power options are assigned during schematic capture. Default values for each setting may be specified during schematic capture as well. Designers may use the speed/power options to fine tune the design after place and routing simply by returning to schematic capture and reassigning the previously set values without having to repeat placement and routing.

The examples in Table III illustrate how speed/power options can affect propagation delays vs power consumption at the macro level.

TABLE III. Macro Speed/Power Trade-Off

Macro	I_{CS}	I_{OEF}	Speed (ps)	Power (mW)
2-Input NOR (eor2)	High	High	230	8.6
	Medium	High	300	6.7
	Low	Medium	550	3.4
D-Flip-Flop (efd)	High	High	340	23.8
	Medium	High	480	15.3
	Low	Medium	810	11.0

NGA Series Macro Library

The NGA Macro Library contains gates and complex functions designed and constructed to minimize area and maximize performance. The following list of functions are available in the *"NGx Macro Library"* for use on NGA Series gate arrays, for complete specifications, refer to the *NGx Macro Library.*

NGA Series Macro Library (Continued)

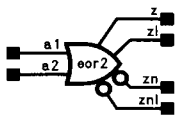
Name	Description
Input/Output Macros	
ied	Differential ECL Input Buffer
ieda	Differential ECL Input Buffer (High-Speed)
iem	ECL Input Buffer w. True/False Outputs
iema	ECL Input Buffer w/ True/False Outputs (High-Fanout)
ited	TTL-to-ECL Input Buffer
ye50m	50Ω ECL Output Buffer (100K)
yed2	Differential ECL Output Buffer (100K)
yetd	ECL-to-TTL Output Buffer (20 mA)
yvbb	V_{BB} Reference Output
betd	Transceiver, ECL-to-TTL Output, TTL-to-ECL Input
ECL Macros (Standard Power)	
eadf1	1-Bit Full Adder w/ Gated Inputs
eadh1	1-Bit Half Adder
eadl1	1-Bit Carry Lookahead Adder
ean2	2-Input AND/NAND Gate
edc4c	2:4 Decoder w/ Enable-Bar
edlr	D-Type Latch w/ Gated Enable-Bar and Reset
edr	Buffer/Inverter
edra	Differential Buffer
efd	D-Flip-Flop
efdr	D-Flip-Flop w/ Reset
efdra	D-Flip-Flop w/Clock Enable-Bar and Reset
efdrd	2:1 Mux D-Flip-Flop w/ Clock Enable-Bar and Reset
efdre	4:1 Mux D-Flip-Flop w/ Clock Enable-Bar and Reset
efdrf	D-Flip-Flop w/ 0R2 Data Input and Sync Reset (High-Speed)
efdrs	D-Flip-Flop w/ Gated Data, Clock and Async Set and Reset
efjrs	JK Flip-Flop w/ Async Set and Reset
efm	D-Flip-Flop w/ 2:1 Multiplexed Data Inputs
ehl2	High/Low Level Generator
emx2	2:1 Multiplexor
emx2a	Differential 2:1 Multiplexor
emx2b	2:1 Multiplexor w/ Enable-Bar
emx4	4:1 Multiplexor
emx4a	4:1 Multiplexor w/ Differential S0 Input
emx802	8:1 Multiplexor w/ Enable
eoa23	2-Wide, 3-Input OAI
eoa2302	2-Wide, 3-Input OAI (High-Drive)
eoa24	2-Wide, 4-Input OAI
eoa44	4-Wide, 4/3/33-Input OAI
eoa46	4-Wide, 5/4/5/6-Input OAI
eoa66	6-Wide, 6/6/4/4/2/2-Input OAI
eoa88	2-Wide, 8-Input OAI
eor2	2-Input OR/NOR Gate
eor202	2-Input OR/NOR Gate (High-Drive)
eor5	5-Input OR/NOR Gate
eor502	5-Input OR/NOR Gate (High-Drive)
eor8	8-Input OR/NOR Gate
eor12	12-Input OR/NOR Gate
exn4	4-Input XNOR Gate
exn402	4-Input XNOR Gate (High-Drive)
exo2	2-Input XOR/XNOR Gate
exo4	4-Input XOR/XNOR Gate
exo9	9-Input XOR/XNOR Gate

NGA Series Macro Library (Continued)

Name	Description
ECL Macros (Low Power)	
ean2t	2-Input AND/NAND Gate
edrat	Differential Buffer
edrt	Buffer/Inverter
efdrt	D-Flip-Flop w/ Reset
efdrat	D-Flip-Flop w/ Clock Enable-Bar and Reset
efdrdt	2:1 Mux D-Flip-Flop w/ Clock Enable-Bar and Reset
efdret	4:1 Mux D-Flip-Flop w/ Clock Enable-Bar and Reset
efdrst	D-Flip-Flop w/ Gated Data, Clock and Async Set and Reset
efmt	D-Flip-Flop w/ 2:1 Multiplexed Data Inputs
emx2t	2:1 Multiplexor
emx4t	4:1 Multiplexor
emx4a	4:1 Multiplexor w/ Differential S0 Input
emx802t	8:1 Multiplexor w/ Enable
eoa23t	2-Wide, 3-Input OAI
eoa24t	2-Wide, 4-Input OAI
eoa88t	2-Wide, 8-Input OAI
eor2t	2-Input OR/NOR Gate
eor5t	5-Input OR/NOR Gate
eor8t	8-Input OR/NOR Gate
exo2t	2-Input XOR/XNOR Gate
exo4t	4-Input XOR/XNOR Gate

Selected Macro AC Performance

eor2



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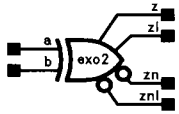
2-Input OR/NOR Gate (STD. Power Version)

Parameter	Min (ps)	Typ (ps)	Max (ps)
t_{pLH}	100	160	230
t_{pHL}	80	110	160

exo2

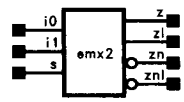


TL/U/11723–5

2-Input XOR Gate (STD. Power Version)

Parameter	Min (ps)	Typ (ps)	Max (ps)
t_{pLH}	130	220	320
t_{pHL}	130	190	270

emx2



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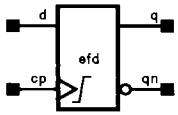
2:1 Multiplexor (STD. Power Version)

Parameter	Min (ps)	Typ (ps)	Max (ps)
$t_{pLH\ (data)}$	110	170	240
$t_{pHL\ (data)}$	80	120	160
$t_{pLH(s)}$	130	220	320
$t_{pHL(s)}$	130	190	270

Selected Macro AC Performance (Continued)

efd



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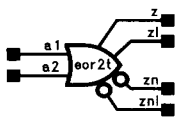
D-Flip-Flop (STD. Power Version)

Parameter	Min (ps)	Typ (ps)	Max (ps)
t_{pLH} (cp-q)	150	240	340
t_{pHL} (cp-q)	140	210	300
t_{pLH} (cp-qb)	150	240	340
t_{pHL} (cp-qb)	140	210	300
setup (d-cp)	100		
hold (d-cp)	0		

eor2t



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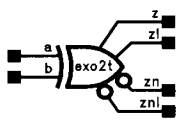
2-input OR/NOR Gate (LOW Power Version)

Parameter	Min (ps)	Typ (ps)	Max (ps)
t_{pLH}	100	160	240
t_{pHL}	110	150	240

exo2t



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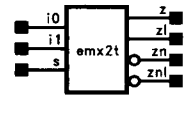
2-input XOR Gate (LOW Power Version)

Parameter	Min (ps)	Typ (ps)	Max (ps)
t_{pLH}	150	230	340
t_{pHL}	170	240	400

emx2t



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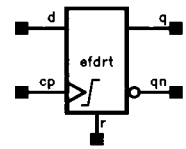
2:1 Multiplexor

Parameter	Min (ps)	Typ (ps)	Max (ps)
t_{pLH} (data)	110	170	250
t_{pHL} (data)	110	160	240
t_{pLH} (s)	150	220	330
t_{pHL}(s)	160	240	390

efdrt



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D-Flip-Flop w/ Reset (LOW Power Version)

Parameter	Min (ps)	Typ (ps)	Max (ps)
t_{pLH} (cp-q)	210	340	520
t_{pHL} (cp-q)	220	330	520
t_{pLH} (cp-qb)	190	290	430
t_{pHL} (cp-qb)	200	300	460
t_{pLH} (r-qb)	220	330	510
t_{pHL} (r-q)	250	360	570
setup (d-cp)	150		
hold (d-cp)	0		

AC Specifications

The NGA Series macro propagation delays are specified as MIN, TYP, and MAX values, with variations due to process, power supply and temperature, as shown in the "AC Performance Variations" table.

AC PERFORMANCE VARIATIONS

	Variation Type					
	Temperature		Voltage		Process	
	Min (Note 1)	Max (Note 3)	Min (Note 1)	Max (Note 3)	Min (Note 1)	Max (Note 3)
Derating Form Typical (%) (Note 2)	−4	15	−2	5	−15	15
Total	−21%	35%				

Note 1: Minimum: T_j = 0°C, V_{EE} = −4.8V, Best Case Process.

Note 2: Typical: T_j = +25°C, V_{EE} = −4.5V, Normal Process.

Note 3: Maximum: T_j = +125°C, V_{EE} = −4.2V, Worst Case Process.

INTERCONNECT AND FANOUT DELAYS

Type	Worst Case Δ Delay/mm (ps)		Conditions		Worst Case Δ Delay/FO (ps)	
	t_{PLH}	t_{PHL}	I_{CS}	I_{OEF}	t_{PLH}	t_{PHL}
ECL (Standard Power)	47	198	150 μA	200 μA	3.25	2.70
	43	98	300 μA	400 μA	3.25	2.70
	37	42	600 μA	800 μA	3.25	2.70
ECL (Low Power)	89	562	50 μA	50 μA	3.50	3.0
	68	277	100 μA	100 μA	3.50	3.0
	56	121	200 μA	200 μA	3.50	3.0

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	−55°C to +125°C
V_{EE} Pin Potential to V_{CC} Pins (V_{MAX})	−7.0V to +0.5V
Input Voltage (DC) (V_I)	V_{EE} to (V_{CC} + 0.5V)
Output Current (DC Output HIGH) (I_O)	−50 mA
Operating Range ECL (V_{EE})	−5.7V to −4.2V
Operating Range TTL (V_{TTL})	4.75V to 5.25V

Note 1: Unless otherwise specified contractually.

Note: *Stresses greater than those in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only operation of the device at any point above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device relability.*

DC Specifications

All NGA Series gate arrays operate from a standard ECL power supply. With F100K I/O, the NGA Series is designed to operate from a standard 100K power supply, although a standard 10K power supply may be used instead. When mixed ECL/TTL I/Os are used, an additional power supply is required. The following tables provide the power requirements for each allowable interface configuration.

Power Supply Requirements

I/O	V_{CC} (V)	V_{EE} (V)	V_{TTL} (V)	V_{TT} (V)	Arrays
F100K	GND	−4.2 to −5.7		−1.9 to −2.1	All
F10K	GND	−4.7 to −5.7		−1.9 to −2.1	
F100K/TTL	GND	−4.2 to −5.7	4.75 to 5.25	−1.9 to −2.1	All except NGA095T
F10K/TTL	GND	−4.7 to −5.7	4.75 to 5.25	−1.9 to −2.1	
Pseudo ECL (PECL)	V_{TTL}	GND	4.75 to 5.25	2.85 to 3.15	

F100K ECL DC Characteristics

V_{EE} = −4.5V; V_{CC} = V_{CCA} = GND; T_J = −10°C to +125°C (Note 1)

Symbol	Parameter	Conditions (Note 2)		Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	V_{IN} = $V_{IH(Max)}$ or $V_{OL(Min)}$	50Ω to −2.0V	−1035	−955	−870	mV
V_{OL}	Output LOW Voltage			−1830	−1705	−1605	mV
V_{IH} (Note 3)	Input HIGH Voltage	Guaranteed HIGH Signal for All Inputs		−1126		−880	mV
V_{IL} (Note 3)	Input LOW Voltage	Guaranteed LOW Signal for All Inputs		−1810		−1520	mV

Note 1: Equilibrium temperature.

Note 2: Conditions for testing are chosen to guarantee operation under worst case conditions.

Note 3: Forcing one input at a time. Apply $V_{IH(Max)}$ or $V_{IL(Min)}$ to all other inputs.

F100K ECL DC Characteristics

V_{EE} = −5.2V; V_{CC} = V_{CCA} = GND; T_J = −10°C to +125°C (Note 1)

Symbol	Parameter	Conditions (Note 2)		Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	V_{IN} = $V_{IH(Max)}$ or $V_{OL(Min)}$	50Ω to −2.0V	−1055	−955	−870	mV
V_{OL}	Output LOW Voltage			−1850	−1705	−1605	mV
V_{IH} (Note 3)	Input HIGH Voltage	Guaranteed HIGH Signal for All Inputs		−1126		−880	mV
V_{IL} (Note 3)	Input LOW Voltage	Guaranteed LOW Signal for All Inputs		−1810		−1520	mV

Note 1: Equilibrium temperature.

Note 2: Conditions for testing are chosen to guarantee operation under worst case conditions.

Note 3: Forcing one input at a time. Apply $V_{IH(Max)}$ or $V_{IL(Min)}$ to all other inputs.

F10K ECL DC Characteristics

V_{EE} = −5.2V; V_{CC} = V_{CCA} = GND

Parameter	Conditions	Junction Temperature				
		0°C	+25°C	+65°C	+125°C	Units
$V_{OH(Max)}$	V_{IH} = $V_{IH(Max)}$	−897	−862	−810	−732	mV
$V_{OH(Min)}$	V_{IL} = $V_{IL(Min)}$	−1112	−1077	−1025	−947	mV
$V_{OL(Max)}$		−1656	−1644	−1620	−1584	rnV
$V_{OL(Min)}$		−1920	−1920	−1920	−1920	mV
$V_{IH(Max)}$ (Note 1)		−888	−858	−810	−728	mV
$V_{IL(Min)}$ (Note 1)		−1920	−1920	−1920	−1920	mV
$V_{IHA(Min)}$ (Note 1)		−1209	−1172	−1125	−1045	mV
$V_{ILA(Max)}$ (Note 1)		−1604	−1567	−1520	−1440	mV

Note 1: Forcing one input at a time. Apply $V_{IH(Max)}$ or $V_{IL(Min)}$ to all other inputs.

TTL DC Characteristics over Operating Temperature Range

V_{CC} = 5.0V ±5%; T_J = −10°C to +125°C (Note 1)

Symbol	Parameter	Condition		Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −400 μA	V_{CC} = 4.75V	2.7	3.0		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA/20 mA	V_{CC} = 4.75V		0.25	0.5	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.80	V
I_{IH}	Input HIGH Current (Note 2)	V_{CC} = 5.25V	V_{IN} = 2.4V			40	μA
I_{IL}	Input LOW Current (Note 2)	V_{CC} = 5.25V	V_{IN} = 0.4V			−400	μA
I_{OZH}	Output OFF Current HIGH	V_{CC} = 5.25V	V_{OUT} = 2.4V			40	μA
I_{OZL}	Output OFF Current LOW	V_{CC} = 5.25V	V_{OUT} = 0.4V			−40	μA
I_{OS}	Output OFF Short Circuit Current (Note 3)	V_{CC} = 5.25V 8 mA/20 mA Driver	V_{OUT} = 0V	−15		−130	mA

Note 1: Forcing one input at a time. Apply $V_{IH(Max)}$ or $V_{IL(Min)}$ to all other inputs.

Note 2: Current per input.

Note 3: Not more than one output should be shorted at a time. Output should not be shorted for more than one second.

Packaging

National offers a wide variety of ceramic packages with low thermal resistance and a wide range of pin counts. These packages are designed to reduce delay loading, cross-talk and power supply noise. All the packages provide an internal ground plane for shielding and good heat transfer properties as well as minimal pin-to-bonding pad delay. Some of the packages allow for direct on-package mounting of decoupling capacitors. To check on availability of the NGA Series gate arrays in packages other than the ones listed in Table I please contact National Semiconductor ASIC Marketing.

Design Automation Support

National Semiconductor's design automation tools, DA4, gives users convenient access to the NGA ASPECT III gate array series. The state-of-the-art proprietary and flexible generic tools are integrated under a rule-based design flow manager in an open system, that allows existing hardware and software to be integrated into the design environment, reducing the costs of ownership and user training. The open architecture of National's Design Automation System allows the transfer of the design from the user's workstation to National's system through the EDIF backplane. National uses the EDIF standard for netlists and symbols when transmitting and receiving data between CAE tools. By plugging tools in and out of the EDIF backplane, you can tailor an environment to suit your design needs.

Design Automation Support (Continued)

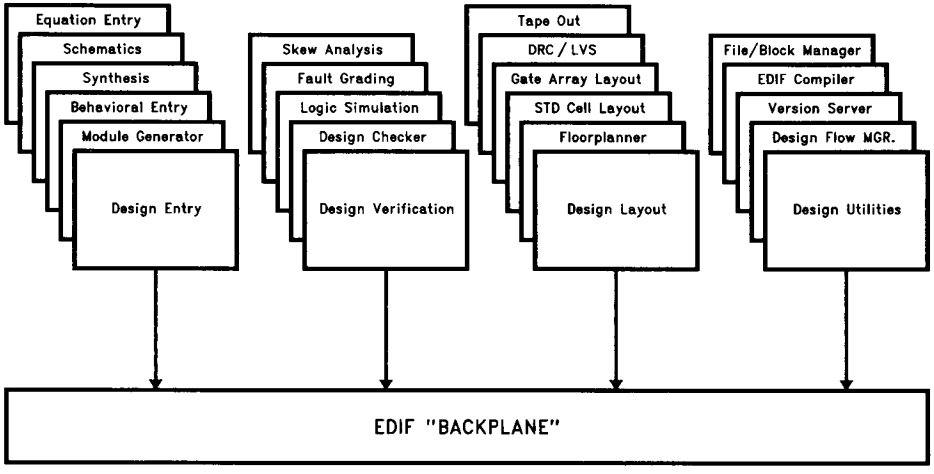

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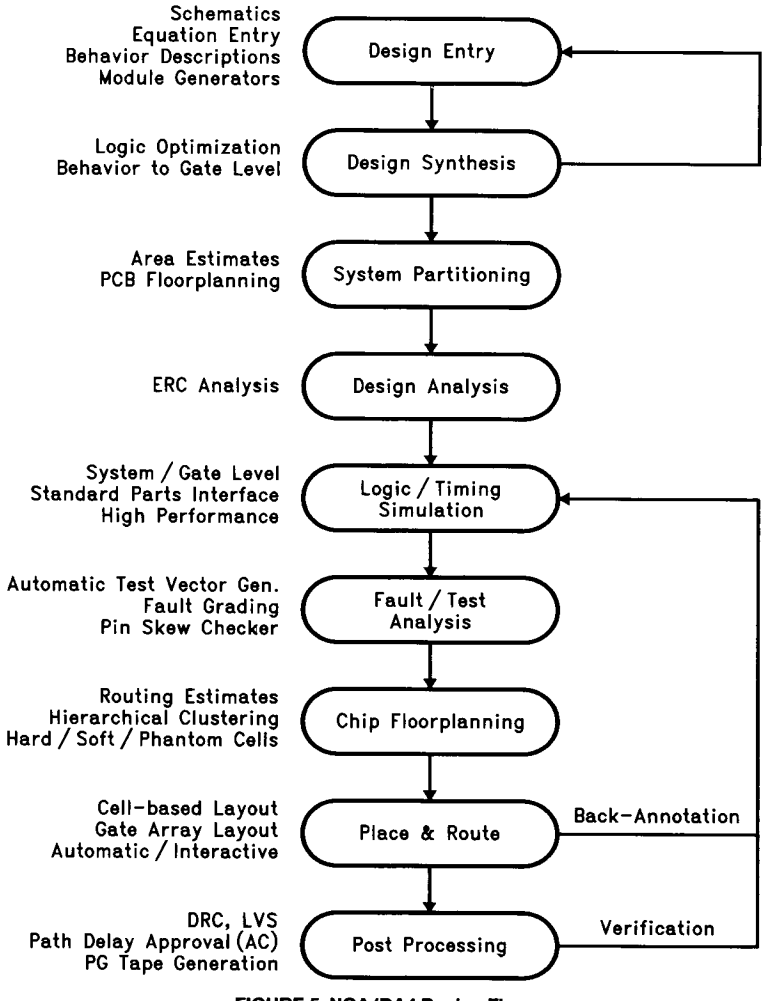
FIGURE 4. Open Architecture through EDIF

Design Automation Support (Continued)



TL/U/11723–13

FIGURE 5. NGA/DA4 Design Flow

ASIC Design Centers

Lit. # 111820-001

North American Design Centers

Santa Clara
National Semiconductor
1120 Kifer
Sunnyvale, CA 94086
Tel: 408-721-7714

Los Angeles
National Semiconductor
15641 Red Hill Avenue
Suite 120
Tustin, CA 92680
Tel: 714-566-9049

Boston
National Semiconductor
20 Blanchard Road
Suite 1
Burlington, MA 01803
Tel: 617-221-4500

Arlington
National Semiconductor
1111 East Bardin Road
Arlington, TX 76017
Tel: 817-468-6306

Canada
National Semiconductor
5925 Airport Road
Suite 112
Mississauga, ON L4V1W1
Tel: 416-678-2597

International Design Centers

Japan
Sansei-doh Shinjuku Bldg. 5f
4-15, Nishishinjuku, Shinjuku-ku,
Tokyo 160
Tel: 011-81-3-299-7020

West Germany
National Semiconductor GmbH
Industriestrasse 10
D-8080 Fuerstenfeldbruck
West Germany
Tel: 011-49-81-41-103-0

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Industriestrasse 10
D-8080 Furstenfeldbruck
West Germany
Tel: (0-81-41) 103-0
Telex: 527-649
Fax: (08141) 103554

National Semiconductor Japan Ltd.
Sanseido Bldg. 5F
4-15 Nishi Shinjuku
Shinjuku-Ku,
Tokyo 160, Japan
Tel: 3-3299-7001
FAX: 3-3299-7000

National Semiconductor Hong Kong Ltd.
Suite 513, 5th Floor
Chinachem Golden Plaza,
77 Mody Road, Tsimshatsui East,
Kowloon, Hong Kong
Tel: 3-7231290
Telex: 52996 NSSEA HX
Fax: 3-3112536

National Semiconductores Do Brasil Ltda.
Av. Brig. Faria Lima, 1383
6.0 Andor-Conj. 62
01451 Sao
Tel: (55/
Fax: (55/

National Semiconductor (Australia) PTY, Ltd.
1st Floor, 441 St. Kilda Rd.
Melbourne, 3004

034754