2M x 72 DRAM MODULE

Features

- 168 Pin JEDEC Standard, 8 Byte Dual In-line Memory Module
- 2Mx72 Dual Bank Fast Page Mode DIMM
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{AA}	Access Time From Address	35ns	40ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- All inputs and outputs are fully TTL compatible
- Single 5V, ± 0.5V Power Supply
- Au contacts
- Optimized for byte-write parity applications
- System Performance Benefits:
  - Buffered inputs (except $\overline{RAS}$, Data)
  - Reduced Noise (32 V_{SS}/V_{CC} pins)
  - 4 Byte Interleave enabled
  - Byte write, byte read accesses
  - Buffered PDs
- Fast Page Mode, Read-Modify-Write Cycles
- Refresh Modes: $\overline{RAS}$-Only, CBR and Hidden Refresh
- 1024 refresh cycles distributed across 16ms
- 10/10 addressing (Row/Column)
- Card size:
  - 5.25" x 1.0" x 0.354" (TSOP/SOJ)
  - 5.25" x 1.25" x 0.354" (SOJ)
- DRAMS in TSOP/SOJ Packages

Description

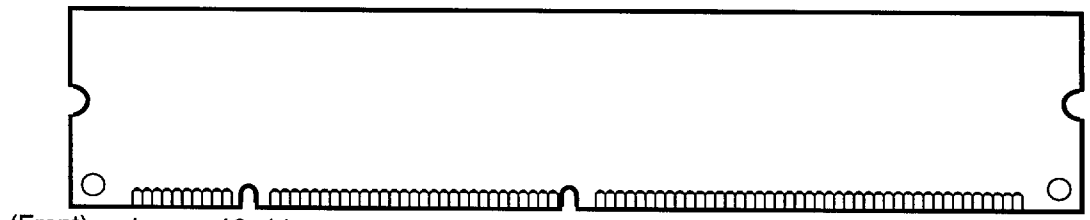
IBM11M2720Q is an industry standard 168-pin 8-byte Dual In-line Memory Module (DIMM) which is organized as a 2Mx72 high speed memory array and is configured as two 1Mx72 banks. The DIMM uses eight 1Mx16 DRAMs in TSOP or SOJ packages, and four 1Mx4 Quad CAS DRAMs in SOJ packages. This DIMM is intended for parity applications.

Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net and skew delays, which simplifies the memory subsystem design analysis. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density, addressing, performance and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ($\overline{PDE}$) signal. ID bits also allow detection of card features, and may be dot-or'd at the system level to provide information for the entire DIMM bank. For example, if a x64 or x72 (ECC) DIMM were inserted into a bank of x72 parity DIMMs, IDO (grounded) would indicate that at least one DIMM in that memory bank will not function properly. PD8 would indicate what positions, if any, contained an ECC DIMM.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x64 non-parity (5V) and ECC DIMMs (5V and 3.3V).

Card Outline (SOJ Version)



50H4348
SA14-4608-02
Revised 5/96

Pin Description

$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe (Buffered)
$\overline{WE0}$, $\overline{WE2}$	Read/write Input (Buffered)
$\overline{OE0}$, $\overline{OE2}$	Output Enable (Buffered)
A0, B0, A1 - A9	Address Inputs (Buffered)
DQx	Data Input/output
PQx	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD8	Presence Detects (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID0 - ID1	ID Bits

Pinout

Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	43	V_{SS}	127	V_{SS}
2	DQ0	86	DQ36	44	OE2	128	NC
3	DQ1	87	DQ37	45	RAS2	129	RAS3
4	DQ2	88	DQ38	46	CAS4	130	CAS5
5	DQ3	89	DQ39	47	CAS6	131	CAS7
6	V_{CC}	90	V_{CC}	48	$\overline{WE2}$	132	$\overline{PDE}$
7	DQ4	91	DQ40	49	V_{CC}	133	V_{CC}
8	DQ5	92	DQ41	50	NC	134	NC
9	DQ6	93	DQ42	51	NC	135	NC
10	DQ7	94	DQ43	52	DQ18	136	DQ54
11	PQ8	95	PQ44	53	DQ19	137	DQ55
12	V_{SS}	96	V_{SS}	54	V_{SS}	138	V_{SS}
13	DQ9	97	DQ45	55	DQ20	139	DQ56
14	DQ10	98	DQ46	56	DQ21	140	DQ57
15	DQ11	99	DQ47	57	DQ22	141	DQ58
16	DQ12	100	DQ48	58	DQ23	142	DQ59
17	DQ13	101	DQ49	59	V_{CC}	143	V_{CC}
18	V_{CC}	102	V_{CC}	60	DQ24	144	DQ60
19	DQ14	103	DQ50	61	NC	145	NC
20	DQ15	104	DQ51	62	NC	146	NC
21	DQ16	105	DQ52	63	NC	147	NC
22	PQ17	106	PQ53	64	NC	148	NC
23	V_{SS}	107	V_{SS}	65	DQ25	149	DQ61
24	NC	108	NC	66	PQ26	150	PQ62
25	NC	109	NC	67	DQ27	151	DQ63
26	V_{CC}	110	V_{CC}	68	V_{SS}	152	V_{SS}
27	WE0	111	NC	69	DQ28	153	DQ64
28	CAS0	112	CAS1	70	DQ29	154	DQ65
29	CAS2	113	CAS3	71	DQ30	155	DQ66
30	RAS0	114	RAS1	72	DQ31	156	DQ67
31	OE0	115	NC	73	V_{CC}	157	V_{CC}
32	V_{SS}	116	V_{SS}	74	DQ32	158	DQ68
33	A0	117	A1	75	DQ33	159	DQ69
34	A2	118	A3	76	DQ34	160	DQ70
35	A4	119	A5	77	PQ35	161	PQ71
36	A6	120	A7	78	V_{SS}	162	V_{SS}
37	A8	121	A9	79	PD1	163	PD2
38	NC	122	NC	80	PD3	164	PD4
39	NC	123	NC	81	PD5	165	PD6
40	V_{CC}	124	V_{CC}	82	PD7	166	PD8
41	NC	125	NC	83	ID0	167	ID1
42	NC	126	B0	84	V_{CC}	168	V_{CC}

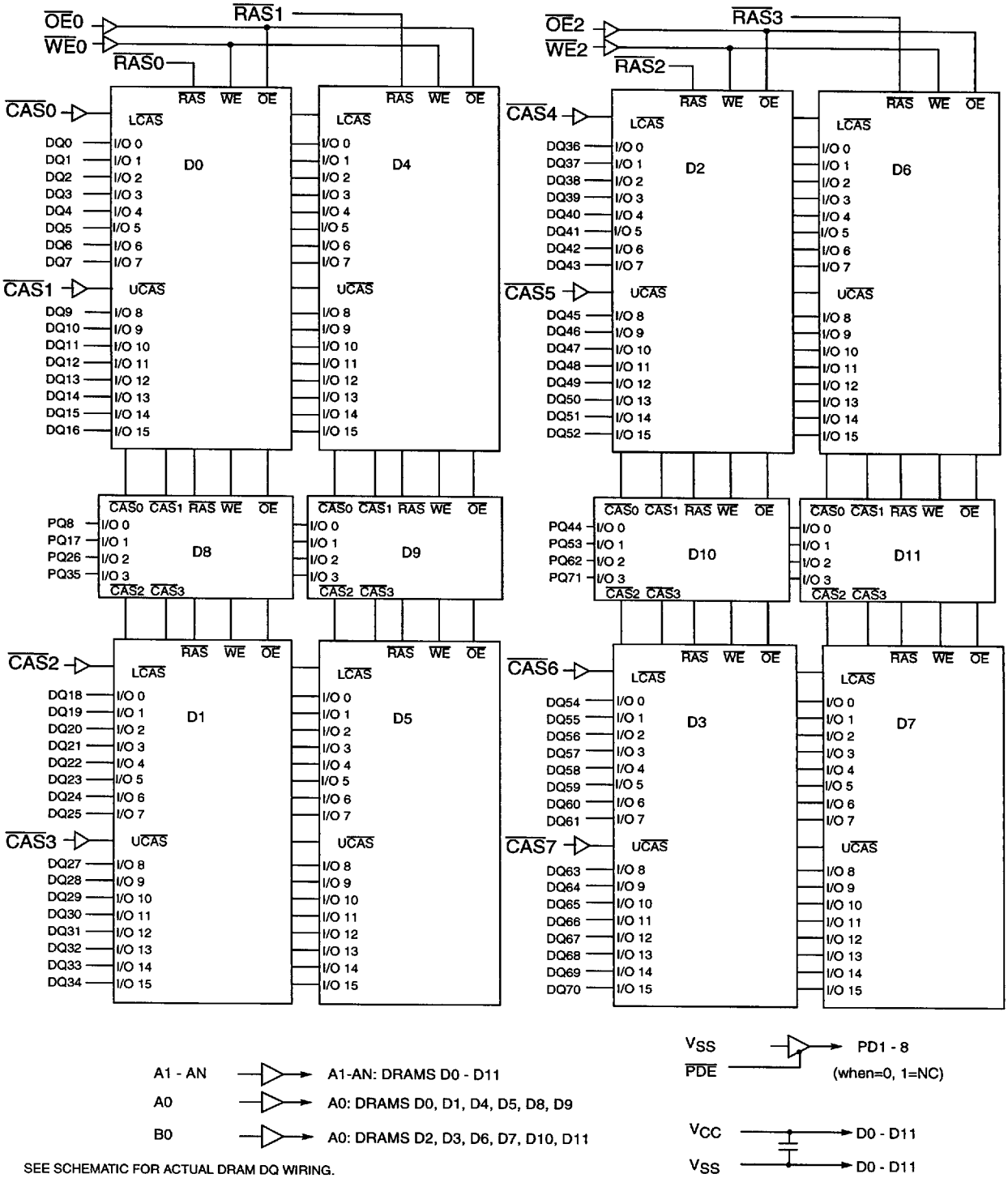
Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Speed	Addr.	Leads	Dimension	Notes
IBM11M2720Q-60	2Mx72	60ns	10/10	Au	5.25"x1.0"x0.354"	
IBM11M2720Q-70		70ns				
IBM11M2720Q-60J		60ns			5.25"x1.25"x0.354"	1
IBM11M2720Q-70J		70ns				1

1. DRAM package designator appended to speed portion of part number on assemblies beginning with DRAM die rev E.

Block Diagram



SEE SCHEMATIC FOR ACTUAL DRAM DQ WIRING.

Truth Table

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	$\overline{PDE}$	DQx
Standby		H	H→X	X	X	X	X	X	High Impedance
Read		L	L	H	L	Row	Col	X	Valid Data Out
Early-Write		L	L	L	X	Row	Col	X	Valid Data In
Late-Write / RMW		L	L	H→L	L→H	Row	Col	X	Valid Data Out, Valid Data In
Fast Page Mode - Read 1st Cycle		L	H→L	H	L	Row	Col	X	Valid Data Out
Subsequent Cycles		L	H→L	H	L	N/A	Col	X	Valid Data Out
Fast Page Mode - Write 1st Cycle		L	H→L	L	X	Row	Col	X	Valid Data In
Subsequent Cycles		L	H→L	L	X	N/A	Col	X	Valid Data In
Fast Page Mode - RMW 1st Cycle		L	H→L	H→L	L→H	Row	Col	X	Valid Data Out, Valid Data In
Subsequent Cycles		L	H→L	H→L	L→H	N/A	Col	X	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh		L	H	X	X	Row	N/A	X	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh		H→L	L	H	X	X	X	X	High Impedance
Hidden Refresh	Read	L→H→L	L	H	L	Row	Col	X	Data Out
	Write	L→H→L	L	H	X	Row	Col	X	Data In
Read Presence Detects		X	X	X	X	X	X	L	Not Affected (PD Bits Valid)

Presence Detect

Pin	-60	-70
PD1 (PD1 - PD4: Addressing/Density)	1	1
PD2	0	0
PD3	1	1
PD4	0	0
PD5 (EDO Detection)	0	0
PD6 (PD6 - PD7: Speed)	1	0
PD7	1	1
PD8 (Parity/ECC Designator)	1	1
ID0 (DIMM Type/Width)	1	1
ID1 (Refresh Mode)	0	0

1. PD1-8 are buffered outputs (0 = driven to V_{OL}, 1 = open)
2. ID0-1 are unbuffered outputs (0 = V_{SS}, 1 = open)
3. $\overline{PDE}$ should be tied high or low at system level if not used

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +6.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} +0.5, 6.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} +0.5, 6.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	9.1	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1
I_{OUTPD}	Short Circuit Output Current (PD)	60	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} +0.5	V	1, 2
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1, 2

1. All voltages referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 2.0V for pulse widths of ≤ 4.0ns (or V_{CC} + 1.0V for ≤ 8.0ns). Additionally, V_{IL} may undershoot to -2.0V for pulse widths ≤ 4.0ns (or -1.0V for ≤ 8.0ns). Pulse widths measured at 50% points with amplitude measured peak to DC reference.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0V ± 0.5V)

Symbol	Parameter	Max	Units
C_{I1}	Input Capacitance (A0, B0, A1-A9)	13	pF
C_{I2}	Input Capacitance ($\overline{RAS}$)	30	pF
C_{I3}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	13	pF
C_{I4}	Input Capacitance ($\overline{PDE}$)	18	pF
C_{IO1}	Input/Output Capacitance (DQx)	22	pF
C_{IO2}	Input/Output Capacitance (PQx)	22	pF
C_{O1}	Output Capacitance (PD)	15	pF
C_{O2}	Output Capacitance (ID)	5	pF

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0V ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	842	mA	1, 2, 3
		-70	—	712		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	24	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	842	mA	1, 3, 4
		-70	—	712		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ ≤ V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	492	mA	1, 2, 3
		-70	—	452		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	12	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	842	mA	1, 3, 4
		-70	—	712		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any Input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)), All Other Pins Not Under Test = 0V	All but $\overline{RAS}$	-10	+10	µA	
		$\overline{RAS}$	-30	+30		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1},I_{CC3},I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1},I_{CC4} depend on output loading. Specified values are obtained with output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.
4. Refresh current is specified for 1 bank.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5.0V ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns maximum delay, no pulse shrinkage to the DRAM device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.
4. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	1
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10K	20	10K	ns	2
t_{ASR}	Row Address Setup Time	5	—	5	—	ns	
t_{RAH}	Row Address Hold Time	8	—	8	—	ns	
t_{ASC}	Column Address Setup Time	2	—	2	—	ns	
t_{CAH}	Column Address Hold Time	10	—	10	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	18	40	18	45	ns	3
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	25	13	30	ns	4
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	58	—	68	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	25	—	ns	5
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	-2	—	-2	—	ns	6
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	-2	—	-2	—	ns	6
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	57	—	62	—	—	
t_{CLCH}	Hold Time from $\overline{CAS}$ Low to $\overline{CAS}$ High	10	—	10	—	ns	7
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	

1. Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
2. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 15ns plus a minimum t_{OH} of 2ns would result in turning data out of the DIMM at 17ns (3ns before max t_{CAC} of 20ns).
3. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
4. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
5. Either t_{CDD} or t_{ODD} must be satisfied.
6. Either t_{DZC} or t_{DZO} must be satisfied.
7. Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.

Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Setup Time	2	—	2	—	ns	1
t_{WCH}	Write Command Hold Time	17	—	17	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	17	—	22	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	47	—	57	—	ns	
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	
t_{DS}	D_{IN} Setup Time	-2	—	-2	—	ns	2
t_{DH}	D_{IN} Hold Time	20	—	20	—	ns	2

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1,2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	ns	1,2
t_{AA}	Access Time from Address	—	35	—	40	ns	1,2
t_{OEA}	Access Time from $\overline{OE}$	—	20	—	25	ns	1,2
t_{RCS}	Read Command Setup Time	2	—	2	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	2	—	2	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	—	40	—	ns	
t_{CAL}	Column Access to $\overline{CAS}$ Lead Time	35	—	40	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	2	—	2	—	ns	
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	5	—	5	—	ns	
t_{OH}	Output Data Hold time	2	—	2	—	ns	
t_{OHO}	Output Data Hold from $\overline{OE}$	2	—	2	—	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	2	20	2	20	ns	4
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	25	—	ns	5
t_{OFF}	Output Buffer Turn-off Delay	2	20	2	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
5. Either t_{CDD} or t_{ODD} must be satisfied.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	45	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	ns	1,2

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	158	—	188	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	83	—	98	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	55	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	58	—	68	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	15	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	83	—	98	—	ns	
t_{CPW}	$\overline{WE}$ Delay time from $\overline{CAS}$ Precharge	63	—	73	—	ns	1

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Refresh Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	14	—	14	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	15	—	15	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	8	—	8	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	3	—	3	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

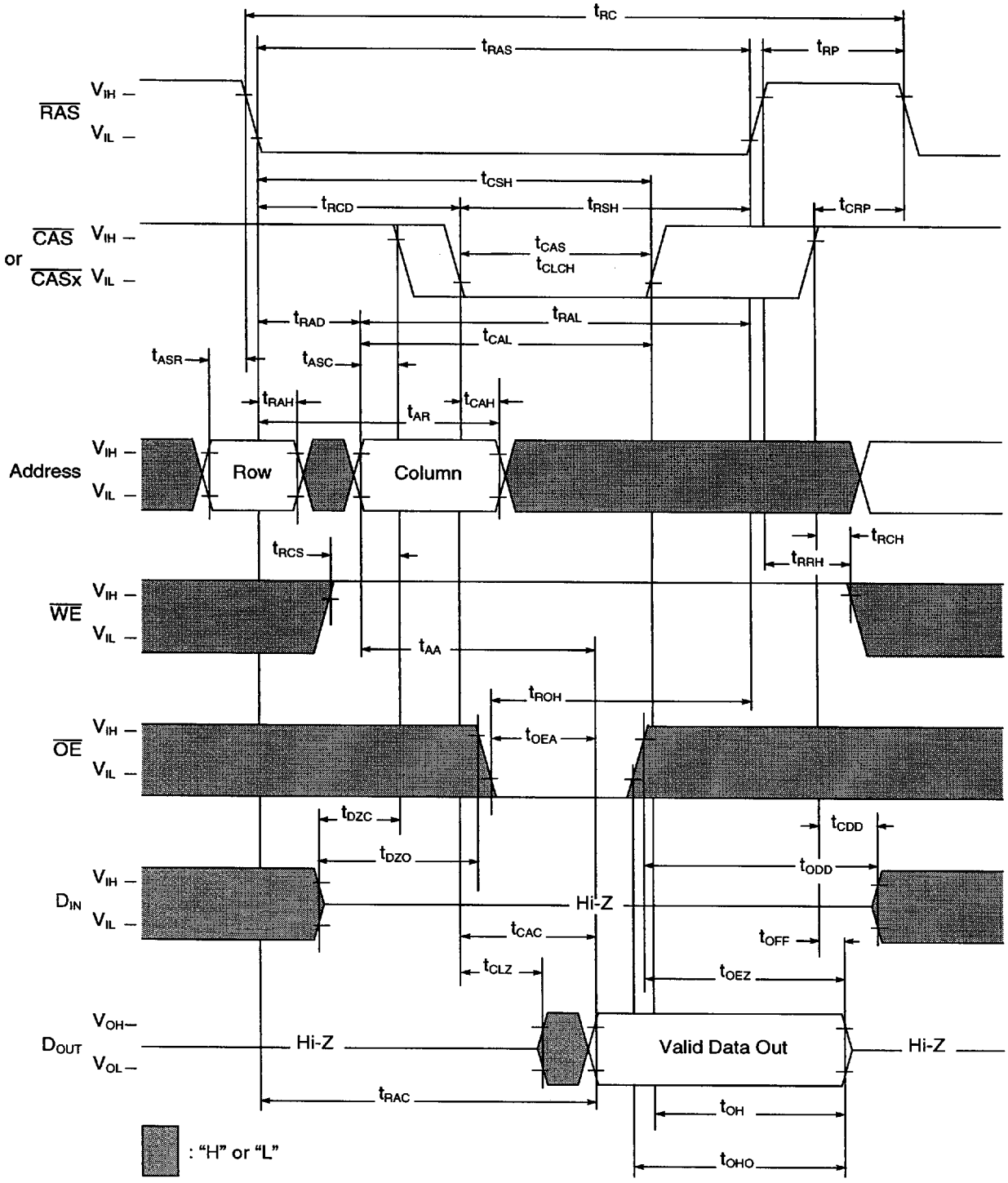
1. 1024 refreshes are required every 16ms.

Presence Detect Read Cycle

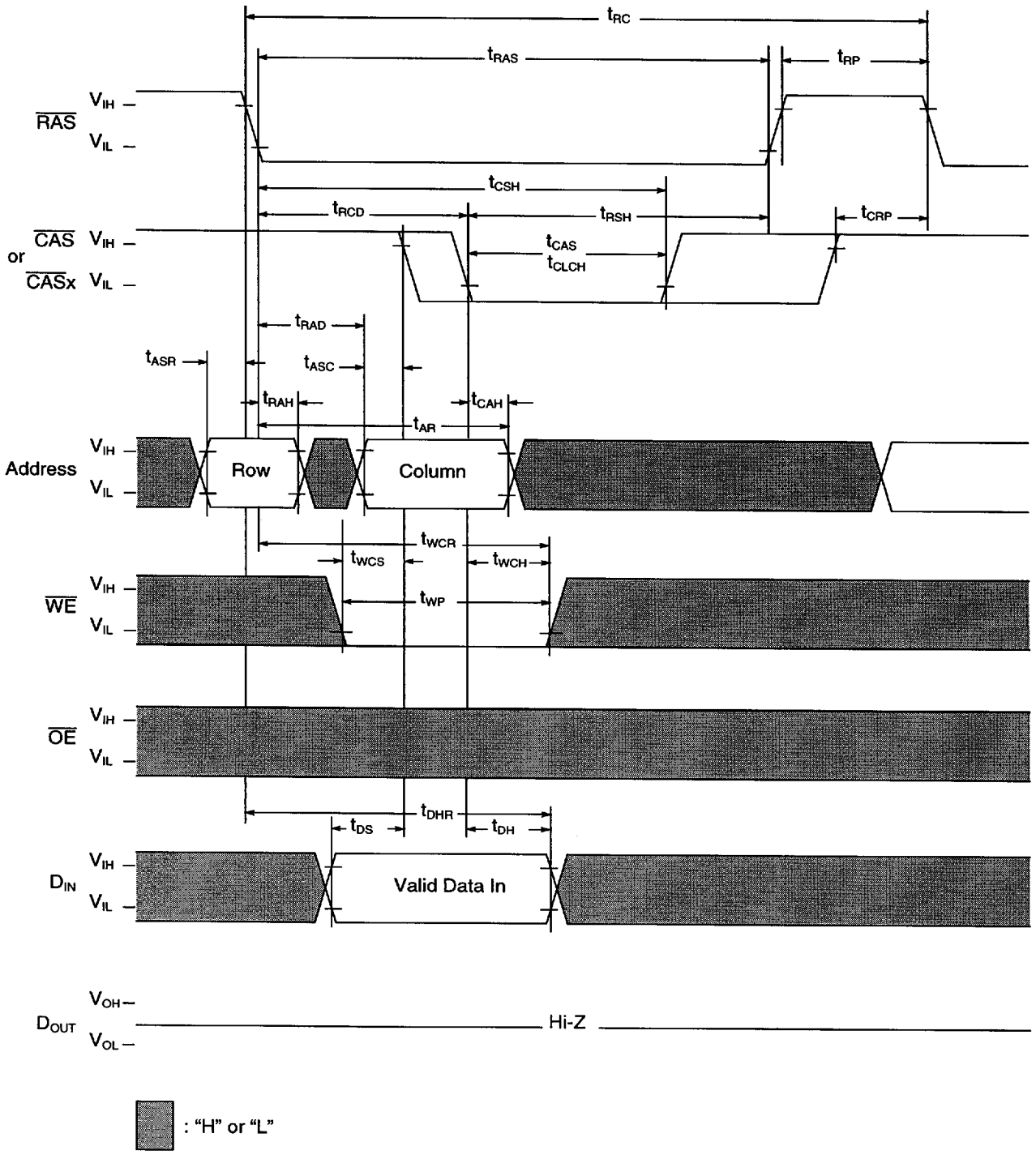
Symbol	Parameter	-60		-70		Unit	Notes
		Min	Max	Min	Max		
t_{PD}	$\overline{PDE}$ to Valid Presence Detect Data	—	10	—	10	ns	1
t_{PDOFF}	$\overline{PDE}$ Inactive to Presence Detects Inactive	0	10	0	10	ns	2

1. Measured with the specified current load and 100pF.
2. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

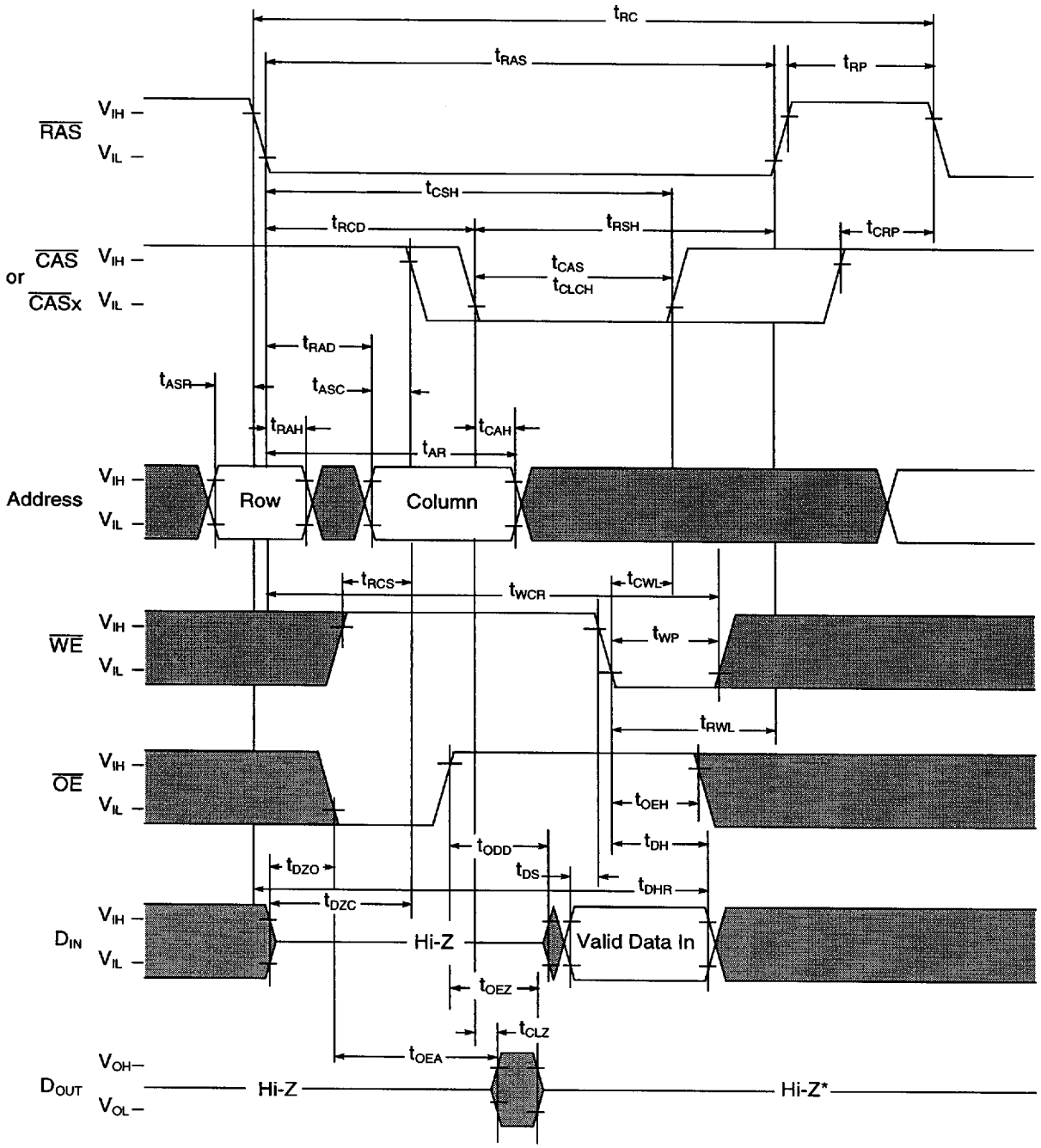
Read Cycle



Write Cycle (Early Write)

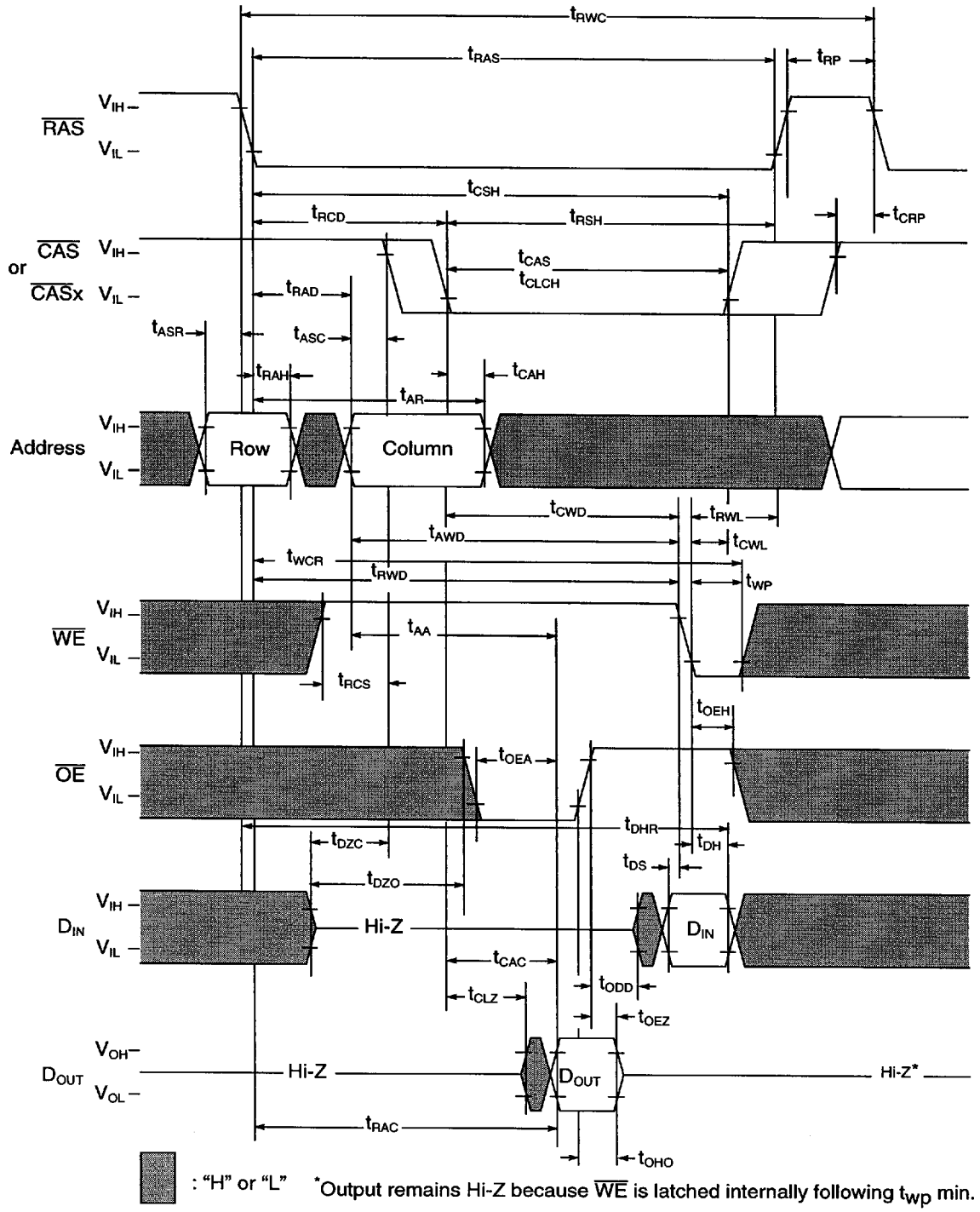


Write Cycle (Late Write)

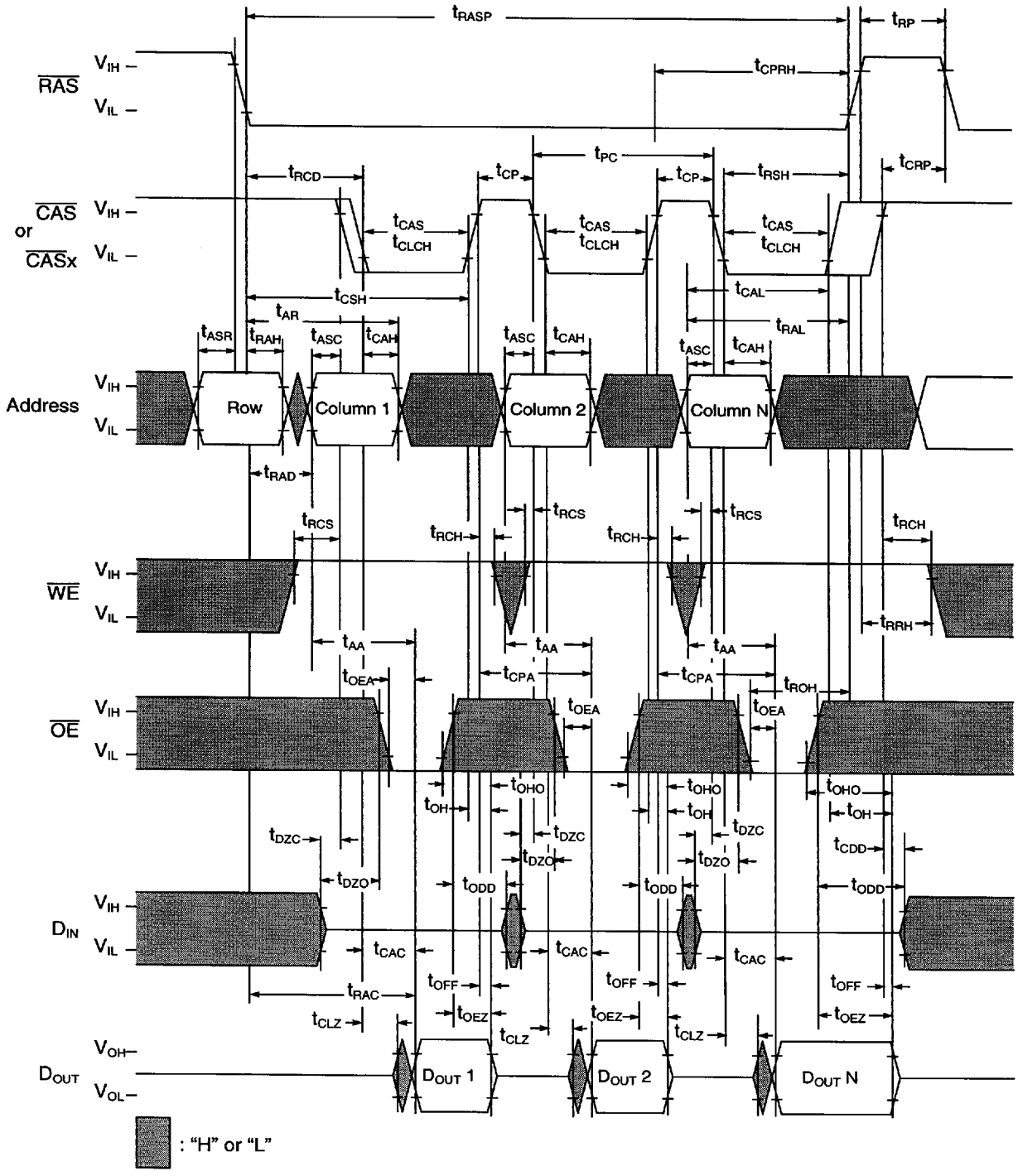


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{WP} min.

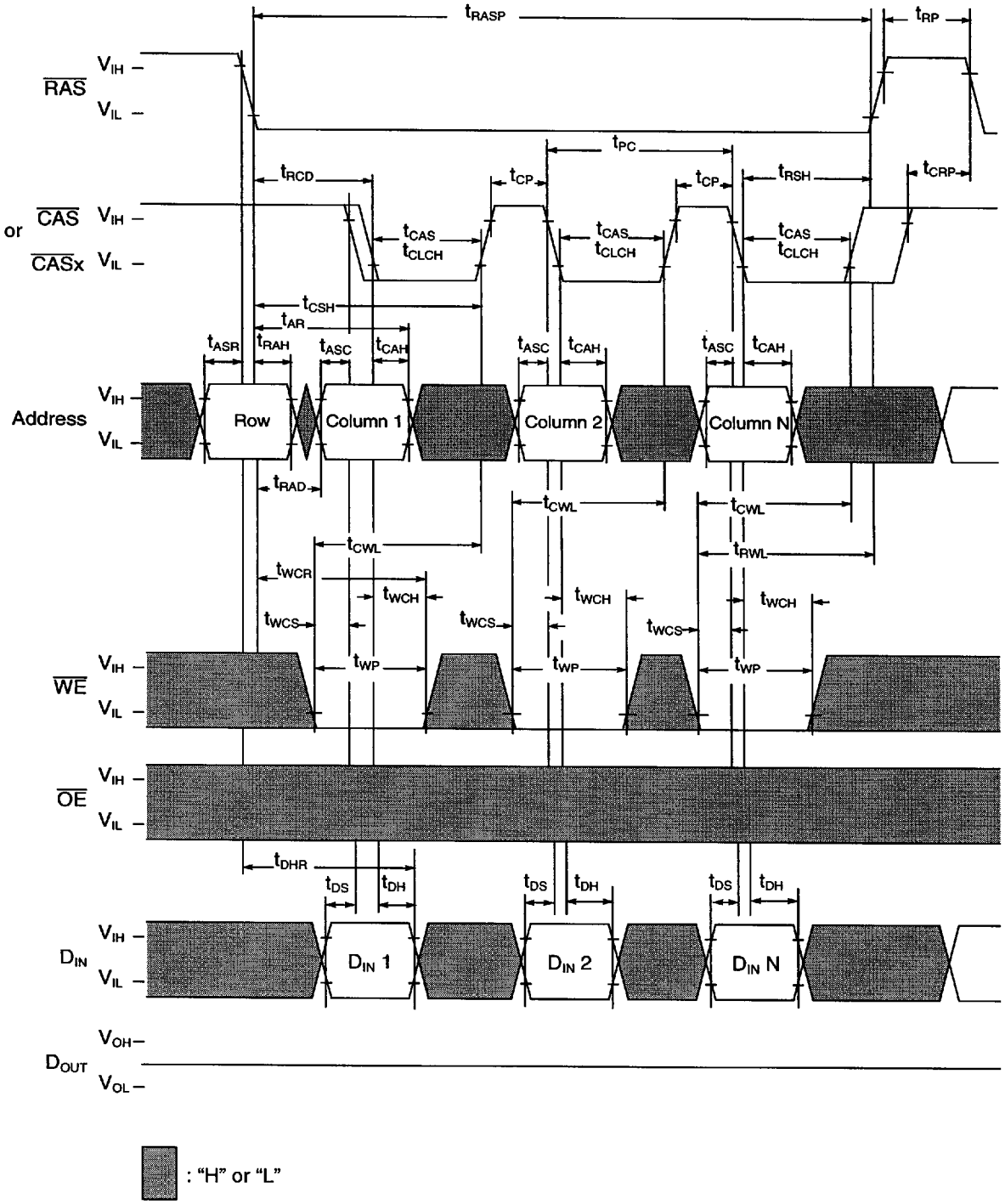
Read-Modify-Write-Cycle



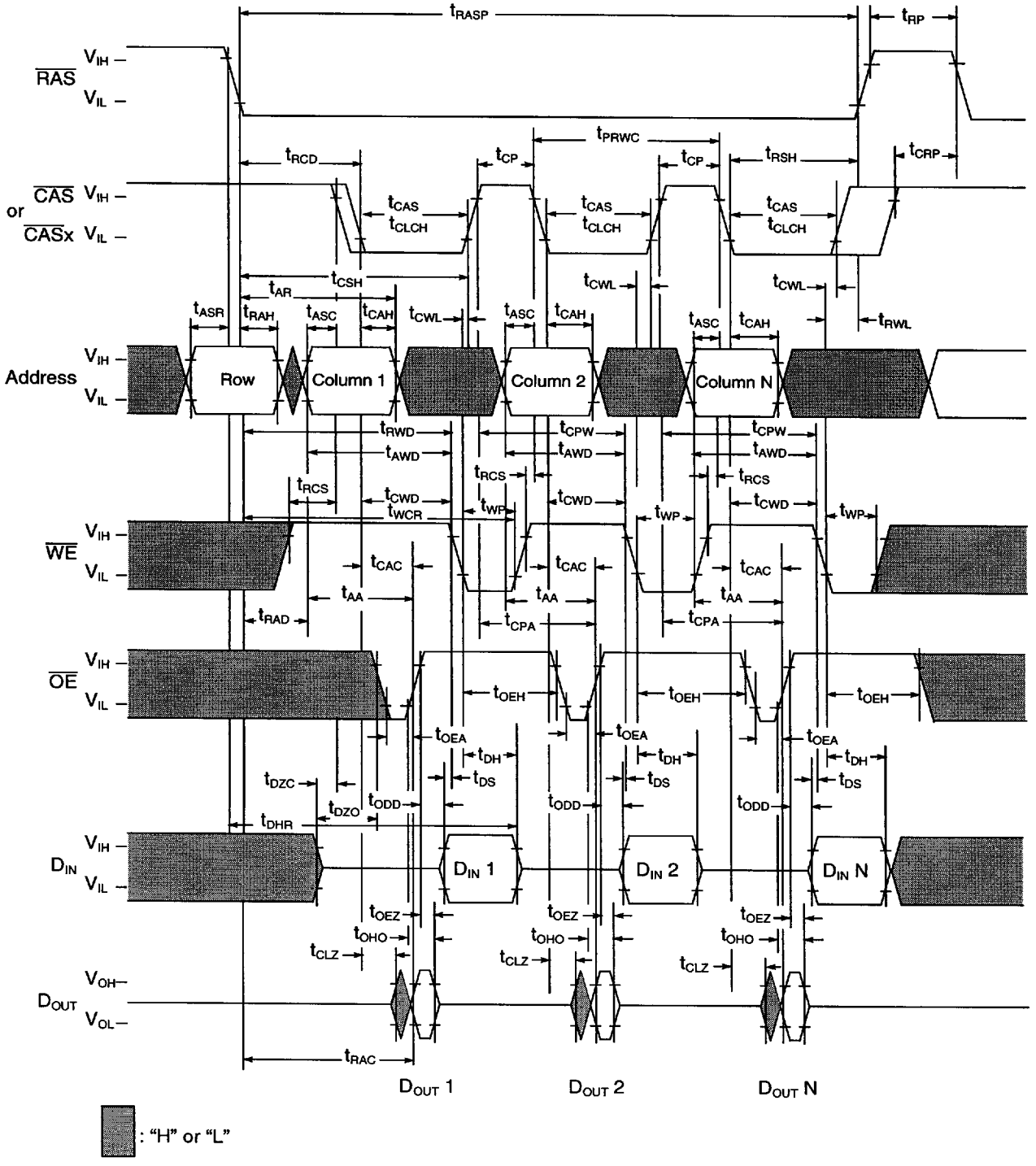
Fast Page Mode Read Cycle



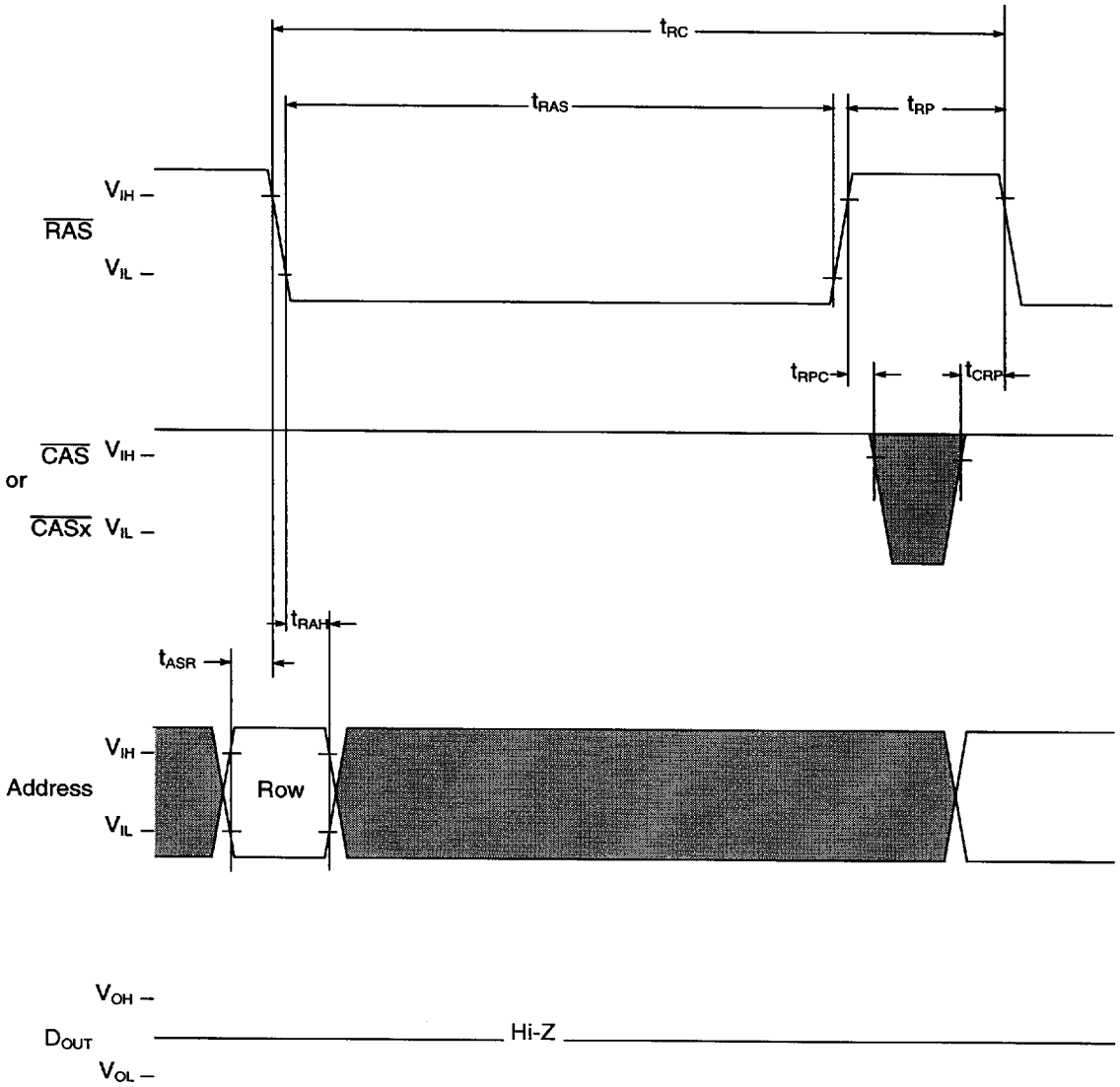
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle



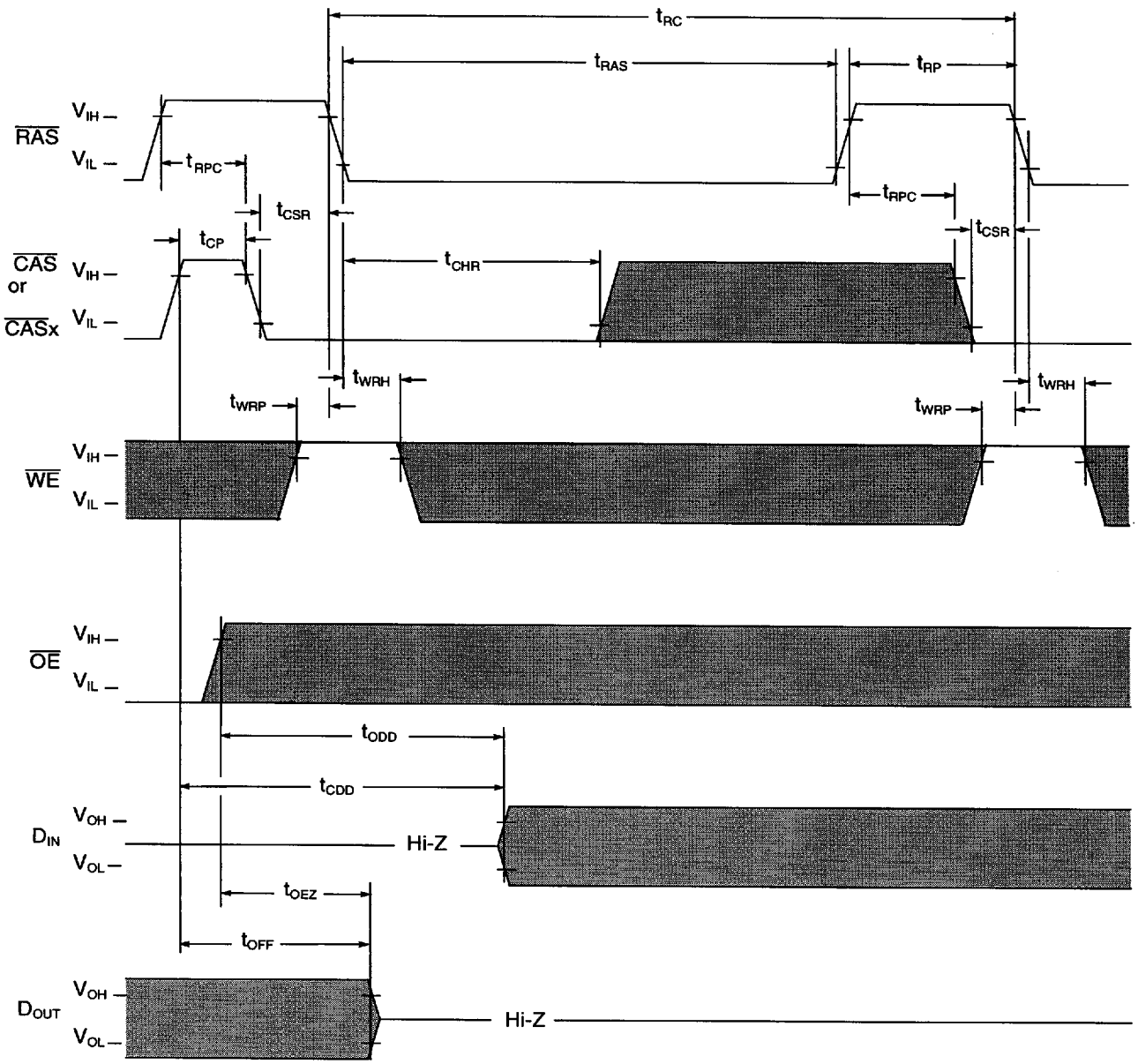
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

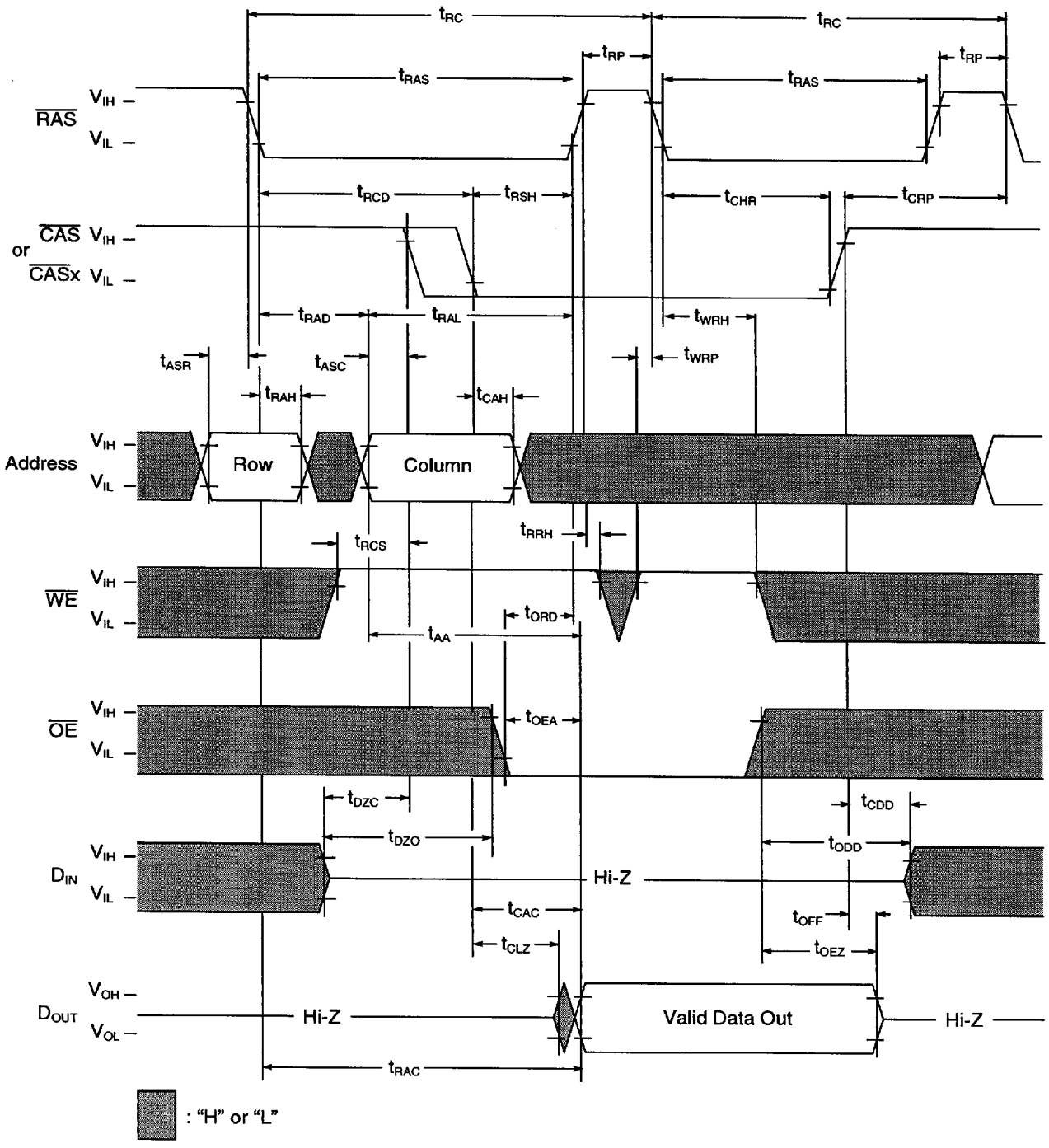
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



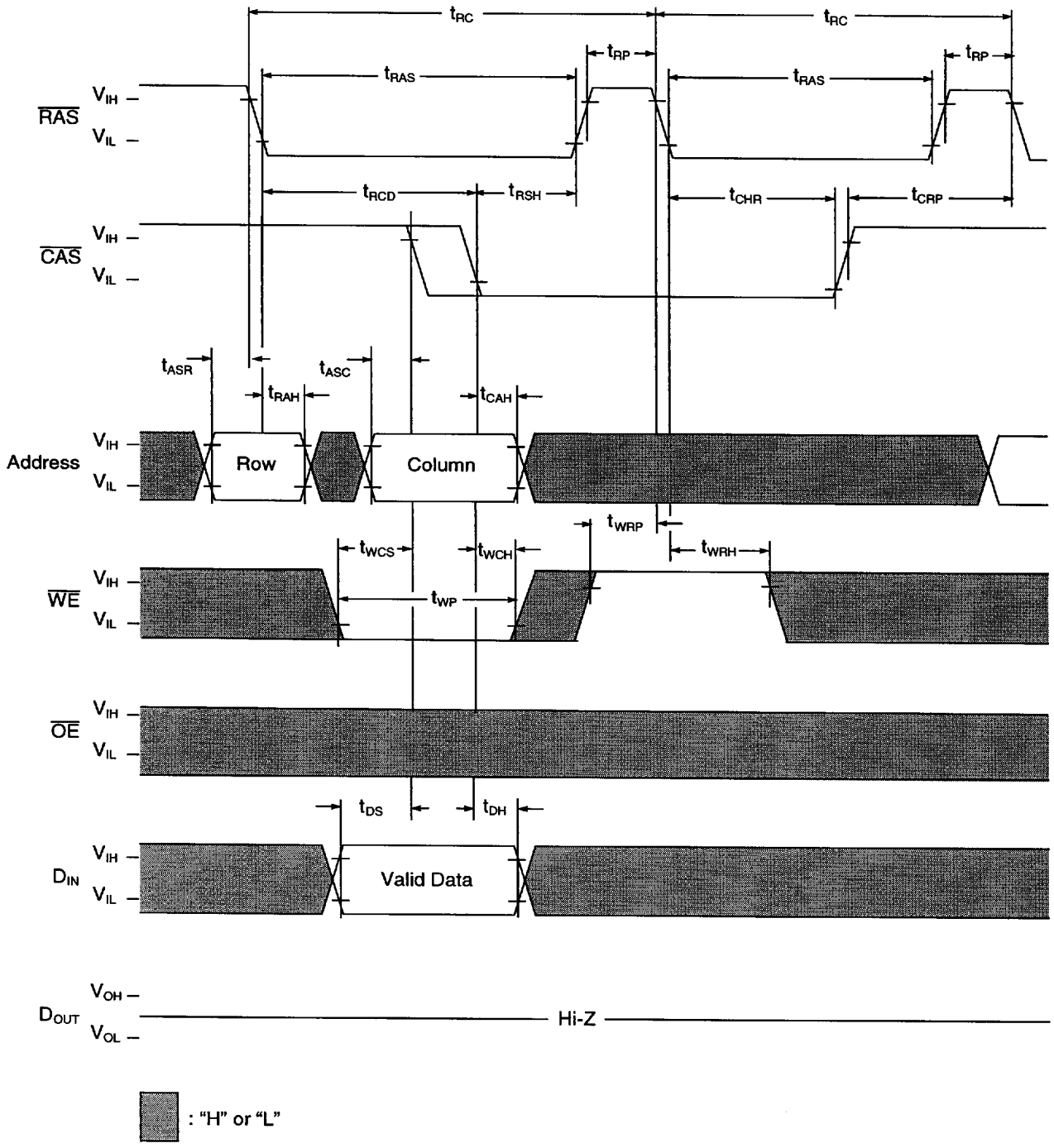
: "H" or "L"

NOTE: Address is "H" or "L"

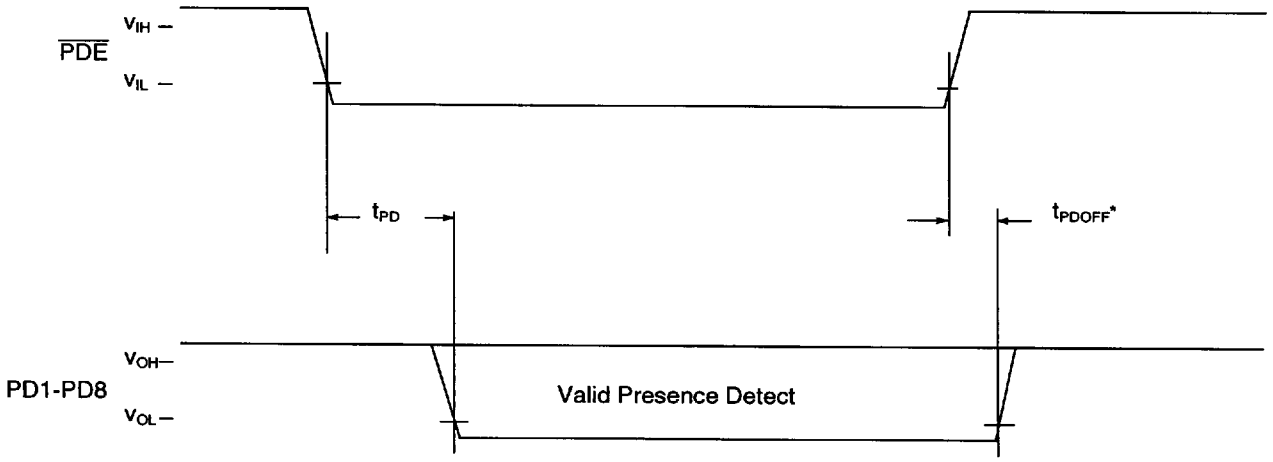
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)

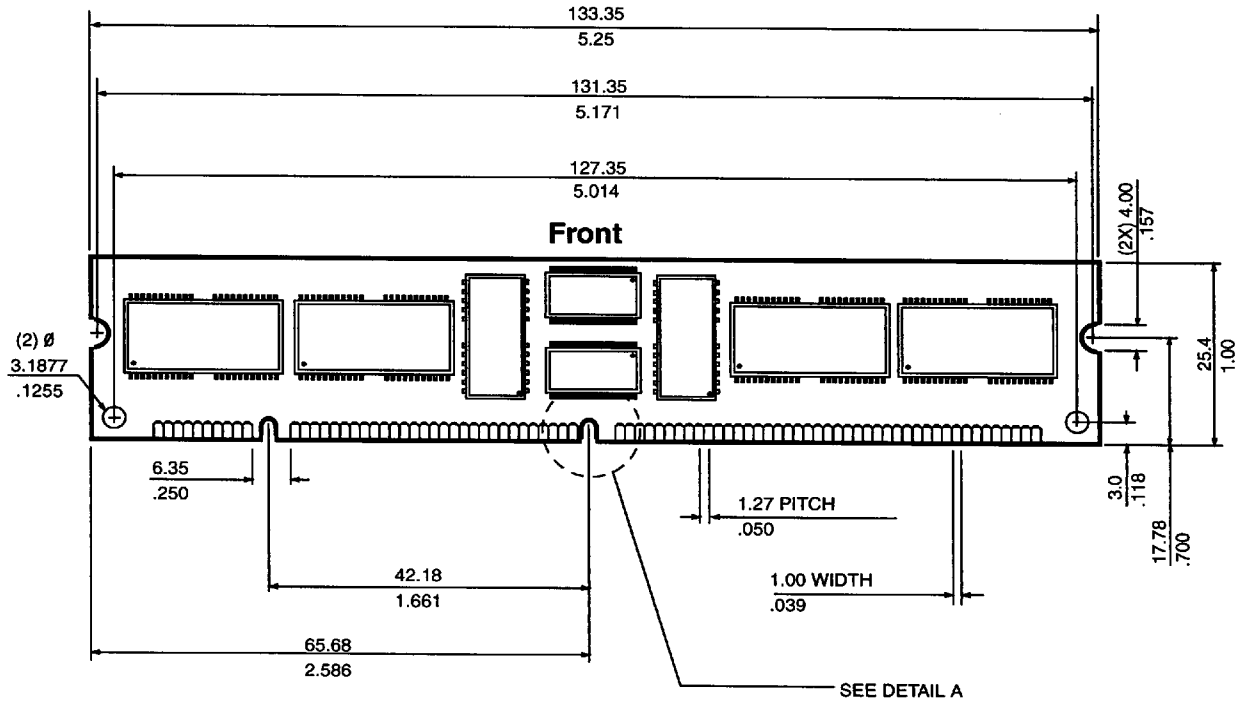


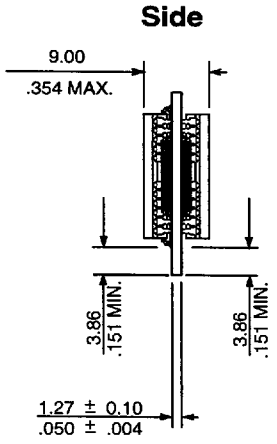
Presence Detect Read Cycle

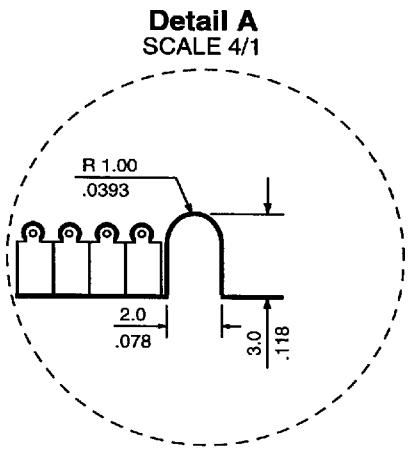


*PD pins must be pulled high at next level of assembly

Layout Drawing (TSOP/SOJ Version)

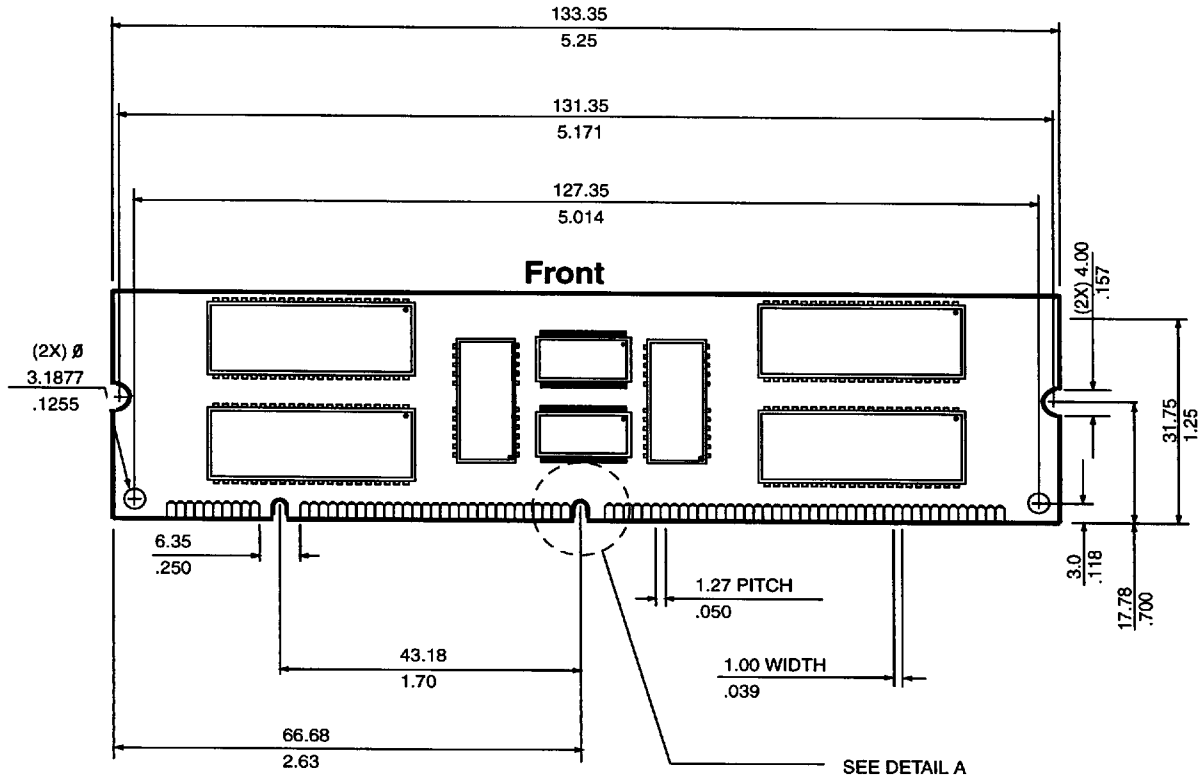


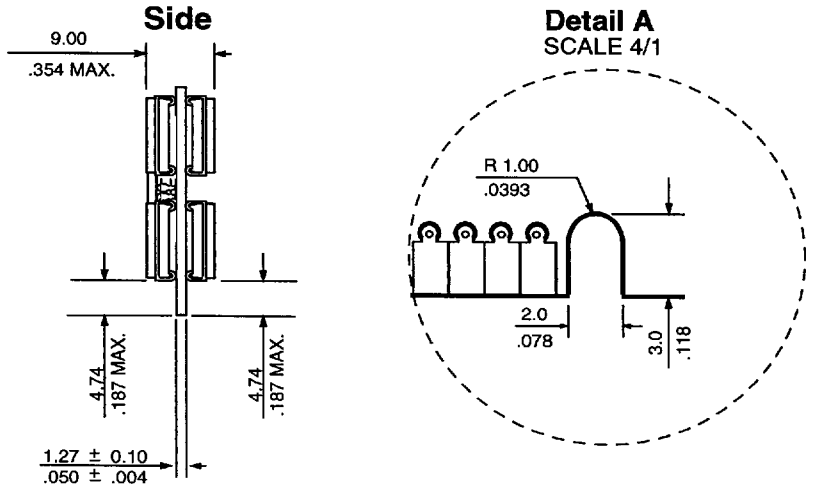




Note: All dimensions are typical unless otherwise stated. Millimeters / Inches

Layout Drawing (SOJ Version)





Note: All dimensions are typical unless otherwise stated. Millimeters / Inches

Revision Log

Rev	Contents of Modification
07/95	Initial release.
5/96	Updated ordering information Improved currents and power Added timings: t_{CAS}, t_{AR}, t_{WCR}, t_{DHR}, t_{ROH} Improved timings: t_{CAH}, t_{CRP}, t_{RRH}, t_{OEZ}, t_{OFF}, t_{OEH}, t_{CSR}, t_{CHR}