HARRIS

HPL-82C339

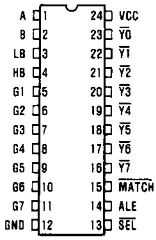
Programmable Chip Select Decoder (PCSD™)

Features

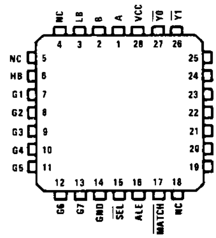
- Memory or I/O Chip Select Decoding, Replaces 3-7 ICs
- Superset of the Industry Standard 74138/74139
- Microprocessor Bus Oriented Interface
- Address "Match" Output Facilitates Bus Arbitration and "Wait-state" Timing Generation
- Harris Advanced Scaled SAJI IV CMOS Process
- Faster than Low-Power Schottky at CMOS Power Consumption
- 24 Pin Slimline DIP
- Wide Operating Temperature Ranges:
  - HPL-82C339-5 ....0°C to +75°C
  - HPL-82C339-9 .... -40°C to +85°C
  - HPL-82C339-8 .... -55°C to +125°C
- Simple Programming Algorithm
- Mask Programmable for Volume Users

Pinouts

TOP VIEW



LCC
TOP VIEW



Description

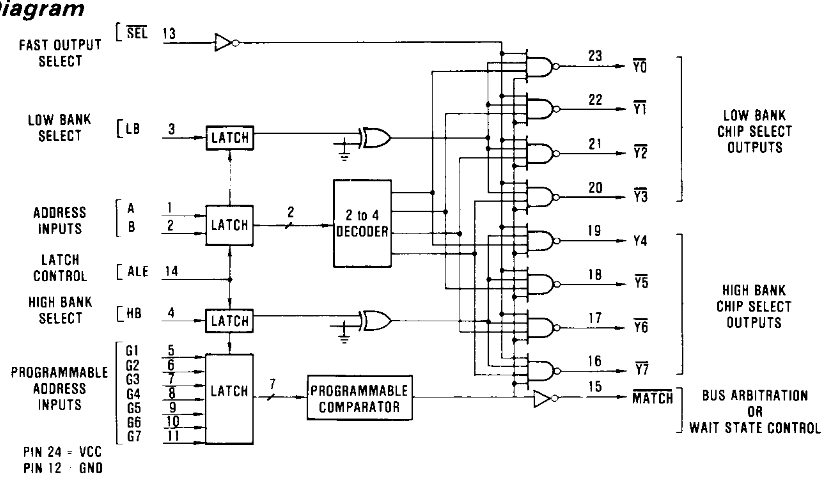
The HPL™-82C339 is a high performance Programmable Chip Select Decoder (PCSD) which is intended to be used for both memory and I/O chip select decoder applications. Utilizing the Harris advanced scaled SAJI IV CMOS process, this circuit provides bipolar speed with CMOS power consumption.

In a typical application, this circuit can replace a 24-pin Programmable Logic Device (PLD) and two octal latches. The associated reductions in board area, chip count and power consumption result in a substantial increase in system reliability and an attendant decrease in system cost.

The seven "Gx" inputs are field programmable for either high or low true address decoding. The High and Low Band (HB, LB) Select inputs are also programmable. This permits the PCSD to be optimized for either 8-bit or 16-bit microprocessor applications. The Harris fuse link technology used in this product provides a permanent fuse with stable storage characteristics over the full temperature ranges of 0°C to +75°C, -40°C to +85°C, and -55°C to +125°C.

Transparent latches are utilized on all address inputs which permits the PCSD to be used with both multiplexed and non-multiplexed address/data bus microprocessors.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage .... +7.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.3V to VCC +0.3V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation .... 1 Watt
θ_{jc} .... TBD°C/W (CERDIP Package), TBD°C/W (LCC Package)
θ_{ja} .... TBD°C/W (CERDIP Package), TBD°C/W (LCC Package)
Gate Count .... 500 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range
HPL-82C339-5 .... 0°C to +70°C
HPL-82C339-9 .... -40°C to +85°C
HPL-82C339-8 .... -55°C to +125°C

D.C. Electrical Specifications
(Operating)

HPL-82C339-5 (VCC = 5.0V ± 10%, TA = 0°C to +75°C)
HPL-82C339-9 (VCC = 5.0V ± 10%, TA = -40°C to +85°C)
HPL-82C339-8 (VCC = 5.0V ± 10%, TA = -55°C to +125°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
IIH IIL	Dedicated "1" Input Current "0"		+1 -1	μA μA	VIH = VCC MAX VIL = 0V VCC = VCC MAX
VIH VIL	Input Threshold "1" "1" Voltage "0"	2.0 2.2	 0.8	V V V	VCC = VCC MAX HPL-82C339-5/-9 VCC = VCC MAX HPL-82C339-8 VCC = VCC MIN
VOH1 VOH2 VOL	Output Voltage "1" "1" Output Voltage "0"	3.0 VCC-0.4	 0.4	V V V	IOH1 = -5mA IOH2 = -1mA VCC MIN, VIL MAX, VIH MIN IOL = +5mA
ICCSB*	Standby Power Supply Current		50	μA	VIH = VCC MAX IF = 0.0μA, VCC = VCC MAX
ICCOP*	Operating Power Supply Current		2	mA/MHz	VI = VCC or GND IF = 0.0μA, VCC = VCC MAX

* ICCSB, ICCOP specifications are achieved only after complete programming of the device. These specifications are sampled and guaranteed but not 100% tested. While testing these specifications, output pins should be left open circuit.

A.C. Switching Specifications
(Operating)

HPL-82C339-5 (VCC = 5.0V ± 10%, TA = 0°C to +75°C)
HPL-82C339-9 (VCC = 5.0V ± 10%, TA = -40°C to +85°C)
HPL-82C339-8 (VCC = 5.0V ± 10%, TA = -55°C to +125°C)

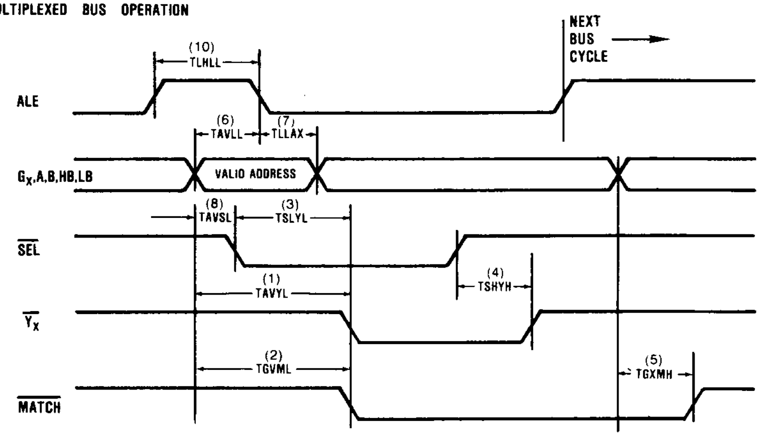
SYMBOL	PARAMETER	HPL-82C339-5		HPL-82C339-9		HPL-82C339-8		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
(1) TAVYL	Propagation delay A, B, LB, HB, or G to Output Low	—	50	—	50	—	50	ns
(2) TGVML	Propagation delay G to Match Output Low	—	50	—	50	—	50	ns
(3) TSLYL	Select Access Time to Output Low	—	35	—	35	—	35	ns
(4) TSHYH	Select Access Time to Output High	—	35	—	35	—	35	ns
(5) TGXMH	Match De-Select Propagation Delay	—	50	—	50	—	50	ns
(6) TAVLL	Address Set-Up to ALE Trailing Edge	15	—	15	—	15	—	ns
(7) TLLAX	Address Hold From ALE Trailing Edge	15	—	15	—	15	—	ns
(8) TAVSL	Address Set-Up to SEL Low (Glitch-Free Operation)	15	—	15	—	15	—	ns
(9) TSHAX	Address Hold From SEL High (Glitch-Free Operation)	15	—	15	—	15	—	ns
(10) TLHLL	ALE Pulse Width	15	—	15	—	15	—	ns

Capacitance: T_A +25°C (NOTE: Sampled and guaranteed - but not 100% tested.)

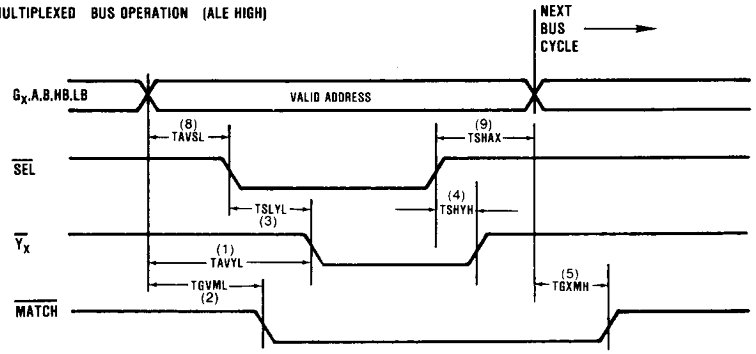
SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance	5	pF	VI = VCC or GND, f = 1 MHz
CO	Output Capacitance	10	pF	VO = VCC or GND, f = 1 MHz

Switching Time Definitions

MULTIPLEXED BUS OPERATION

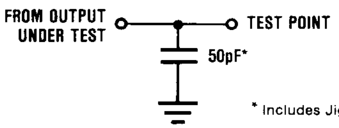


DEMULTIPLEXED BUS OPERATION (ALE HIGH)



NOTES: 1. In order to ensure glitch-free operation of the $\overline{Yx}$ outputs, set-up and hold times should be observed.
2. The $\overline{SEL}$ input controls the $\overline{Yx}$ outputs only and has no effect on the $\overline{MATCH}$ output.
3. AC switching characteristics are measured with inputs switching between GND and 3.0V. t_r, t_f = 5ns (10%–90%).

A.C. Test Load



* Includes Jig and Probe Total Capacitance.

Programming

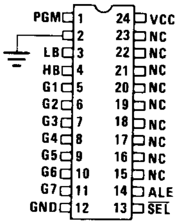
Following is the programming procedure which is used for the HPL-82C339 programmable logic device. This device is manufactured with all fuses intact. Any desired fuse can be programmed by following the simple procedure shown on the following page. One may build a programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which meets these specifications. Please contact Harris for a list of approved programmers.

Programming Specifications

TABLE 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNITS
VCCP	VCC Voltage During Programming		11.50	12.00	12.00	V
VCCV	VCC Voltage During Verify		4.75	5.00	5.25	V
ICCP	ICC Limit During Programming		—	100	200	mA
VNEG	Edit Enable & Mode Select Voltage		-6.00	-6.00	-7.00	V
INEG	Edit Enable & Mode Select Current		—	—	-5.00	mA
VIL VIHV VIHP	Input Voltage Low Input Voltage High Input Voltage High	 verify ① programming ①	0.00 VCCV-2 VCCP-2	0.00 VCCV VCCP	0.80 VCCV VCCP	V V V
IILP IIHV IIHP	Input Current Low Input Current High Input Current High	VIL = 0.0V verify programming	— — —	0 0 0	1 1 1	μA μA μA
PWP TD tr1 tr2 tf1 tf2	Programming Width Pulse Seq. Delay Signal Rise Time VCC Rise Time Signal Fall Time VCC Fall Time	 10% to 90% 10% to 90% 90% to 10% 90% to 10%	4.5 1 0.01 0.01 0.01 0.01	5.0 1 0.1 0.1 0.1 0.1	5.5 — 1 5 1 5	msec μsec μsec μsec μsec μsec
TPP FL	Programming Period Fuse Attempts/Link		— 1	5.1 1	— 2	msec cycles

① Inputs defined as logic "1" (VIHV or VIHP) must track the VCC power supply when the supply is raised or lowered. The input levels should never exceed the level on the VCC Pin.



NOTE: While programming the CMOS HPL device, no input pins should be left floating. Output pins (15-23) should be left unconnected. It is suggested that a 0.1μF capacitor be placed between VCC and GND to minimize VCC voltage spikes.

FIGURE 1. HPL-82C339 EDIT MODE PINOUT

Programming Procedure

Set Up:

a. During programming or operation, no input pins should be left floating.

b. No input pin voltage should ever be greater than the voltage applied to the device VCC pin.

c. The device should be decoupled with a 0.1μF or greater capacitor located at the device socket and placed between the VCC and GND pins.

Power up:

a. Initially, all input pins including power supply pins should be at ground potential.

b. Normally, the input pins (pins 3-11, 13, 14) are driven with an open collector driver with a pull-up resistor to the VCC pin (pin 24) so that these inputs automatically track the voltage on the VCC pin when they are set to the high state. This prevents the voltage level on the input pins from exceeding the voltage applied to the VCC pin.

c. Ramp the VCC pin (pin 24) to VCCV and the input pins (pins 3-11, 13, 14) to VIHV.

Programming Sequence

a. After a delay TD, the programming mode is entered by taking the programming enable pin (pin 1) to VNEG. Pin 1 must remain at VNEG throughout the entire programming sequence.

b. Wait TD and raises pin 24 to VCCP and pins 3-11, 14 to VIHP. At the same time, the $\overline{SEL}$ input (pin 13) is set to either VIHP or VIL in order to select the desired polarity of the input which is to be programmed. When $\overline{SEL}$ is at VIHP, the input will be programmed high true. When $\overline{SEL}$ is at VIL, the input will be programmed low true.

c. Wait TD and pulse the input to be programmed to ground for PWP milliseconds. It should be noted that only one input should be programmed at a time.

d. After a delay TD, return pin 24 to VCCV and pins 3-11, 14 to VIHV.

e. Repeat steps b), c), and d) until pins 3-11 have been programmed with the appropriate polarity.

f. When all inputs have been programmed as explained above, wait TD and return the programming enable pin (pin 1) to VIL.

Fuse Integrity Testing

a. Correct programming of the device should be verified by applying test vectors to the input pins.

b. Fuse integrity is tested by applying VCC to the device and measuring the static power consumption of the device. With all inputs at VCC or GND and the output pins unloaded, the measured ICCSB of the device should be less than 50 μA at VCC = 5V and T = 25°C. This guarantees that all fuses have been blown to a final state which is not marginal and will not create a reliability problem over the life of the device. NOTE: Any device which fails this test should be rejected even if it passes functional testing in order to ensure no future reliability problems associated with marginally blown fuses.

IMPORTANT: All nine inputs must be programmed regardless of desired high or low input polarity. The advanced design of the fuse select circuitry (Patent Pending) provides for ultra-low post programming ICCSB and requires that one fuse on each input be programmed.

Programming Waveforms