

HM5116400 Series

T-46-23-18

Product Preview

4,194,304-Word x 4-Bit Dynamic Random Access Memory

HITACHI/ LOGIC/ARRAYS/MEM

■ DESCRIPTION

The Hitachi HM5116400 is a CMOS dynamic RAM organized 4,194,304 words x 4 bits. It employs the most advanced CMOS technology for high performance and low power. The HM5116400 offers Fast Page Mode as a high speed access mode.

■ FEATURES

- Single 5V ($\pm 10\%$)
- High Speed
 - Access Time 60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
 - Active Mode 495 mW/440 mW/385 mW/330 mW (max)
 - Standby Mode 11 mW (max)
- Fast Page Mode Capability
- Long Refresh Period
 - 4096 Refresh Cycles (64 ms)
- 3 Variations of Refresh
 - RAS Only Refresh
 - CAS Before RAS Refresh
 - Hidden Refresh

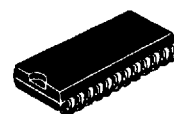
■ ORDERING INFORMATION

Part No.	Access Time	Package
HM5116400J-6	60 ns	400 mil 24-pin Plastic SOJ (CP-24D)
HM5116400J-7	70 ns	
HM5116400J-8	80 ns	
HM5116400J-10	100 ns	
HM5116400Z-6	60 ns	475 mil 24-pin Plastic ZIP (ZP-24)
HM5116400Z-7	70 ns	
HM5116400Z-8	80 ns	
HM5116400Z-10	100 ns	

■ PIN DESCRIPTION

Pin Name	Function
A ₀ -A ₁₁	Address Input
A ₀ -A ₁₁	Refresh Address Input
I/O ₀ -I/O ₄	Data Input/Data Output
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
V _{CC}	Power (+5V)
V _{SS}	Ground
NC	No Connection

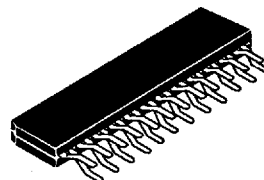
HM5116400J Series



3DCP24D

(CP-24D)

HM5116400Z Series

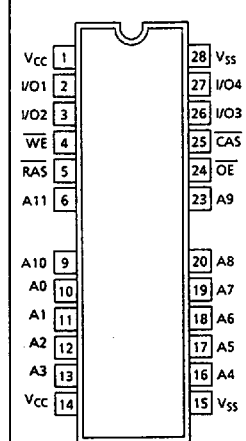


3DZP24

(ZP-24)

■ PIN OUT

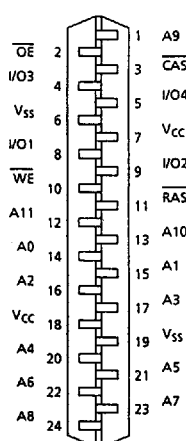
HM5116400J Series



D101-1

(Top View)

HM5116400Z Series



D101-2

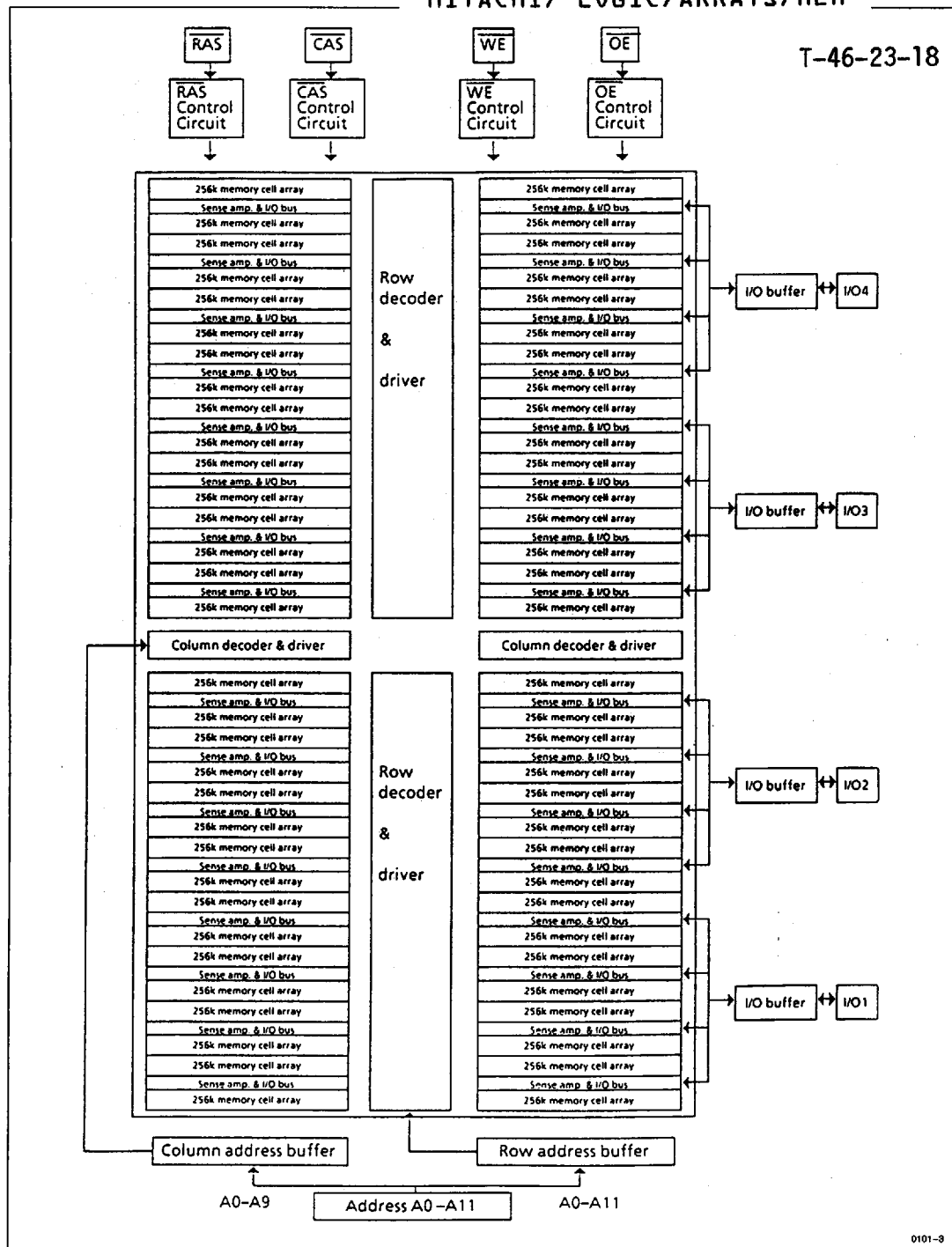
(Bottom View)



BLOCK DIAGRAM

HITACHI/ LOGIC/ARRAYS/MEM

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0101-3



■ ABSOLUTE MAXIMUM RATINGS

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Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions ($T_A = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	-1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS} .• DC Electrical Characteristics ($T_A = 0$ to +70°C, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$)

Parameter	Symbol	HM5116400J/Z								Unit	Test Conditions	Notes
		-6		-7		-8		-10				
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I _{CC1}	—	90	—	80	—	70	—	60	mA	t _{RC} = Min	1, 2
Standby Current	I _{CC2}	—	2	—	2	—	2	—	2	mA	TTL Interface RAS, CAS = V _{IH} D _{out} = High-Z	
		—	1	—	1	—	1	—	1	mA	CMOS Interface RAS, CAS ≥ V _{CC} - 0.2V D _{out} = High-Z	
RAS Only Refresh Current	I _{CC3}	—	90	—	80	—	70	—	60	mA	t _{RC} = Min	2
Standby Current	I _{CC5}	—	5	—	5	—	5	—	5	mA	RAS = V _{IH} CAS = V _{IL} D _{out} = Enable	1, 4
CAS Before RAS Refresh Current	I _{CC6}	—	90	—	80	—	70	—	60	mA	t _{RC} = Min	4
Fast Page Mode Current	I _{CC7}	—	70	—	60	—	50	—	45	mA	t _{PC} = Min	1, 3
Input Leakage Current	I _{LI}	-10	10	-10	10	-10	10	-10	10	μA	0V ≤ V _{IN} ≤ 7V	
Output Leakage Current	I _{LO}	-10	10	-10	10	-10	10	-10	10	μA	0V ≤ V _{out} ≤ 7V D _{out} = Disable	
Output High Voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High I _{out} = -5 mA	
Output Low Voltage	V _{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I _{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.4. Clock voltages ($\overline{RAS}$ and $\overline{CAS}$) must be applied simultaneously with or prior to applying supply voltage.

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- **Capacitance** ($T_A = 25^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	C_O	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{CAS} = V_{IH}$ to disable D_{out} .

- **AC Characteristics** ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$) 1, 2, 3, 19, 20

Read, Write Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t _{RC}	110	—	130	—	150	—	180	—	ns	
RAS Precharge Time	t _{RP}	40	—	50	—	60	—	70	—	ns	
CAS Precharge Time	t _{CP}	10	—	10	—	10	—	10	—	ns	
RAS Pulse Width	t _{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
CAS Pulse Width	t _{CAS}	15	10000	18	10000	20	10000	25	10000	ns	
Row Address Setup Time	t _{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	10	—	10	—	10	—	10	—	ns	
Column Address Setup Time	t _{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	15	—	15	—	15	—	15	—	ns	
RAS to CAS Delay Time	t _{RCD}	20	45	20	52	20	60	20	75	ns	4
RAS to Column Address Delay Time	t _{RAD}	15	30	15	35	15	40	15	55	ns	5
RAS Hold Time	t _{RSH}	15	—	18	—	20	—	25	—	ns	
CAS Hold Time	t _{CSH}	60	—	70	—	80	—	100	—	ns	
CAS to RAS Precharge Time	t _{CRP}	5	—	5	—	5	—	5	—	ns	
OE to Din Delay Time	t _{OED}	15	—	18	—	20	—	25	—	ns	6
OE Delay Time from Din	t _{DZO}	0	—	0	—	0	—	0	—	ns	7
CAS Delay Time from Din	t _{DZC}	0	—	0	—	0	—	0	—	ns	7
Transition Time (Rise and Fall)	t _T	3	30	3	30	3	30	3	30	ns	8

Read Cycle

Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from RAS	t _{RAC}	—	60	—	70	—	80	—	100	ns	9, 10, 21
Access Time from CAS	t _{CAC}	—	15	—	18	—	20	—	25	ns	10, 11, 21
Access Time from Address	t _{AA}	—	30	—	35	—	40	—	45	ns	10, 12, 21
Access Time from OE	t _{OEA}	—	15	—	18	—	20	—	25	ns	10, 21
Read Command Setup Time	t _{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to CAS	t _{RCH}	0	—	0	—	0	—	0	—	ns	13
Read Command Hold Time to RAS	t _{RRH}	5	—	5	—	5	—	5	—	ns	13
Column Address to RAS Lead Time	t _{RAL}	30	—	35	—	40	—	45	—	ns	
Column Address to CAS Lead Time	t _{CAL}	30	—	35	—	40	—	45	—	ns	
CAS to Output in Low-Z	t _{CLZ}	0	—	0	—	0	—	0	—	ns	



Read Cycle (continued)

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-40-

Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Output Data Hold Time	t _{OH}	3	—	3	—	3	—	3	—	ns	
Output Data Hold Time from $\overline{OE}$	t _{OH0}	3	—	3	—	3	—	3	—	ns	
Output Buffer Turn-off Time	t _{OFF}	—	15	—	18	—	20	—	25	ns	14
Output Buffer Turn-off Time to $\overline{OE}$	t _{OEZ}	—	15	—	18	—	20	—	25	ns	14
$\overline{CAS}$ to Din Delay Time	t _{CDD}	15	—	18	—	20	—	25	—	ns	6

Write Cycle

Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	tWCS	0	—	0	—	0	—	0	—	ns	15
Write Command Hold Time	tWCH	15	—	15	—	15	—	15	—	ns	
Write Command Pulse Width	tWP	15	—	15	—	15	—	15	—	ns	
Write Command to RAS Lead Time	tRWL	15	—	18	—	20	—	25	—	ns	
Write Command to CAS Lead Time	tCWL	15	—	18	—	20	—	25	—	ns	
Data-in Setup Time	tDS	0	—	0	—	0	—	0	—	ns	16
Data-in Hold Time	tDH	15	—	15	—	15	—	20	—	ns	16

Read-Modify-Write Cycle

Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t _{RWC}	150	—	176	—	200	—	245	—	ns	
RAS to $\overline{WE}$ Delay Time	t _{RWD}	80	—	93	—	105	—	135	—	ns	15
CAS to $\overline{WE}$ Delay Time	t _{CWD}	35	—	41	—	45	—	60	—	ns	15
Column Address to $\overline{WE}$ Delay Time	t _{AWD}	50	—	58	—	65	—	80	—	ns	15
$\overline{OE}$ Hold Time from $\overline{WE}$	t _{OEH}	15	—	18	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
CAS Setup Time (CBR Refresh Cycle)	t _{CSR}	10	—	10	—	10	—	10	—	ns	
CAS Hold Time (CBR Refresh Cycle)	t _{CHR}	20	—	20	—	20	—	20	—	ns	
$\overline{WE}$ Setup Time (CBR Refresh Cycle)	t _{WRP}	10	—	10	—	10	—	10	—	ns	
$\overline{WE}$ Hold Time (CBR Refresh Cycle)	t _{WRH}	10	—	10	—	10	—	10	—	ns	
RAS Precharge to $\overline{CAS}$ Hold Time	t _{RPC}	0	—	0	—	0	—	0	—	ns	



Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t _{PC}	40	—	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{\text{RAS}}$ Pulse Width	t _{RASP}	—	100000	—	100000	—	100000	—	100000	ns	17
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	35	—	40	—	45	—	50	ns	18, 21
$\overline{\text{WE}}$ Delay Time from $\overline{\text{CAS}}$ Precharge	t _{CPW}	55	—	63	—	70	—	85	—	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{CPRH}	35	—	40	—	45	—	50	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Read-Modify-Write Cycle Time	tPRWC	80	—	91	—	100	—	110	—	ns	

Test Mode Cycle

Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Test Mode $\overline{\text{WE}}$ Setup Time	t _{WTS}	10	—	10	—	10	—	10	—	ns	
Test Mode $\overline{\text{WE}}$ Hold Time	t _{WTH}	10	—	10	—	10	—	10	—	ns	

Counter Test Cycle

Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
CAS Precharge Time in Counter Test Cycle	tCPT	TBD	—	TBD	—	TBD	—	TBD	ns		

Refresh ($T_J = 85^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$)

Parameter	Symbol	Max	Unit	Note
Refresh Period	t _{REF}	64	ms	4096 Cycles



Notes: 1. AC measurements assume $t_T = 5$ ns.

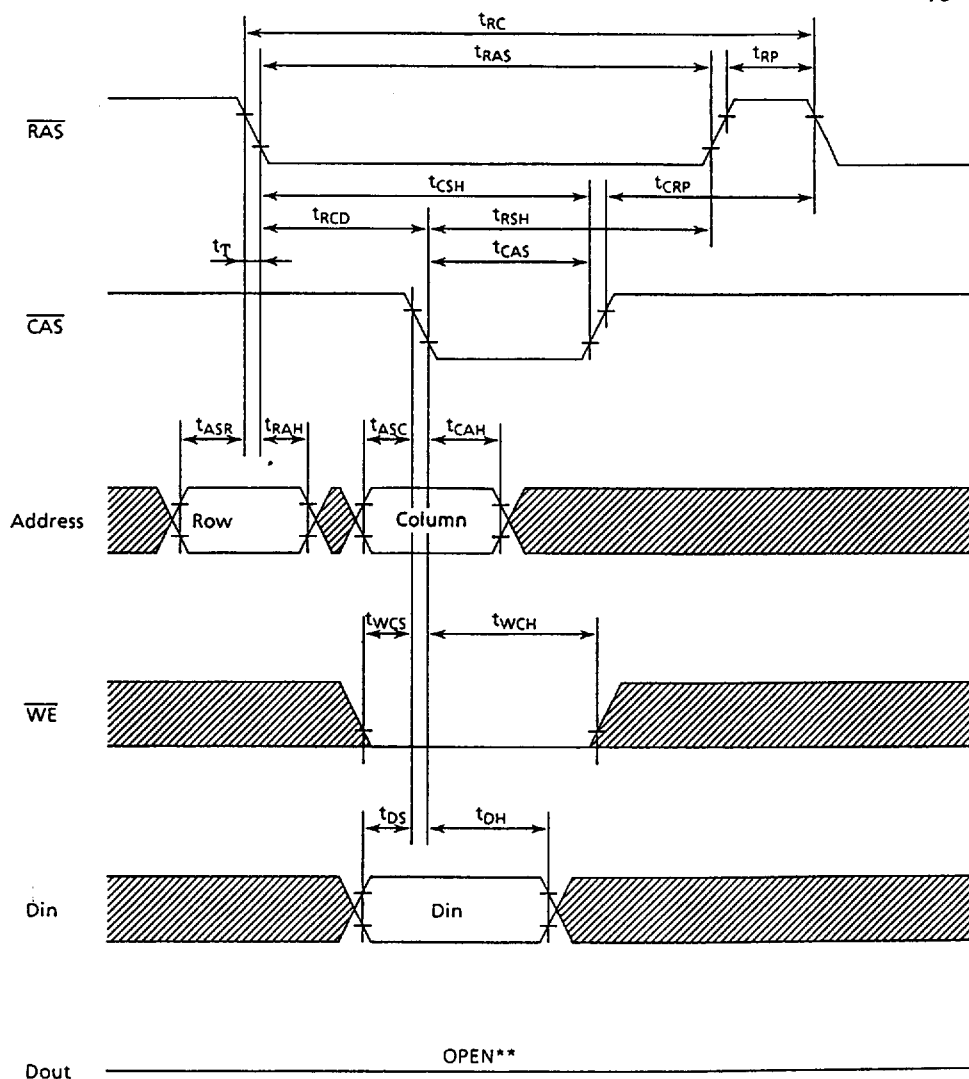
2. An initial pause of 100 μ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ only Refresh or $\overline{CAS}$ before $\overline{RAS}$ Refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
3. Only row address is indispensable on address A10 and A11.
4. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
5. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
6. Either t_{ODD} or t_{CDD} must be satisfied.
7. Either t_{DZO} or t_{DZC} must be satisfied.
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
9. Assumes that $t_{RCD} < t_{RCD}$ (max) and $t_{RAD} < t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
10. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
12. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
13. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
14. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
15. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min) the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
16. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
17. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
18. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA} .
19. In delay write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
20. Test mode operation specified in this data sheet is 16 bits test function controlled by compression addresses ... CA0 and CA1. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of four test bits on each I/O accord with each other, the state of the output data on the I/O is high level. When the state of four test bits on the I/O do not accord with each other, the state of the output data on the I/O is low level. Data input and output pins are I/O₁-I/O₄. If any refresh cycle is occurred, the test mode is reset.
21. In a test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} and t_{CPA} is delayed by 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.



• Early Write Cycle

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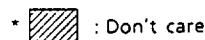
* $\overline{OE}$: Don't care

** : Don't care

*** $tw_{CS} \geq tw_{CS}(\min)$

0101-5



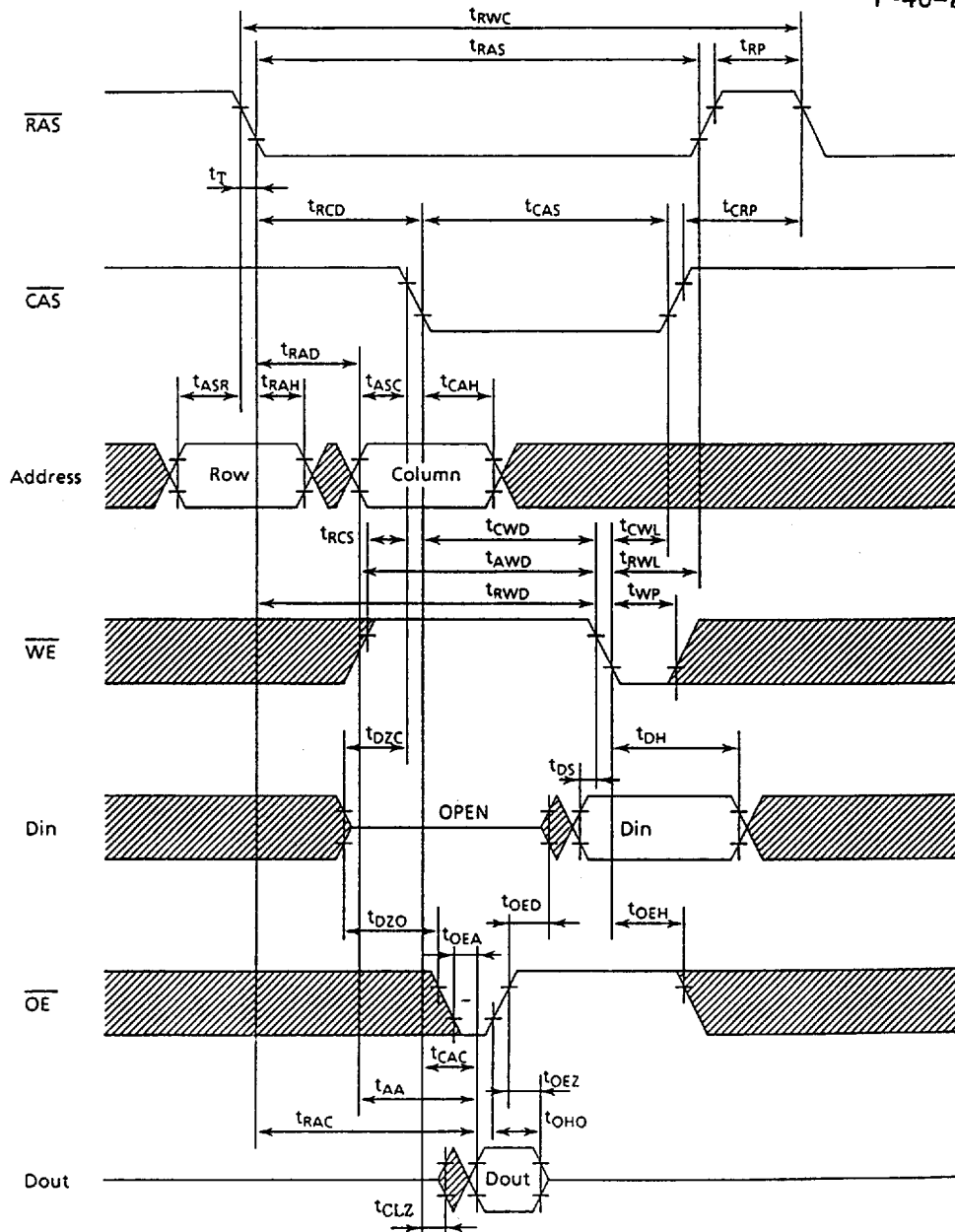


0101-8

- **Read-Modify-Write Cycle**

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*  : Don't care

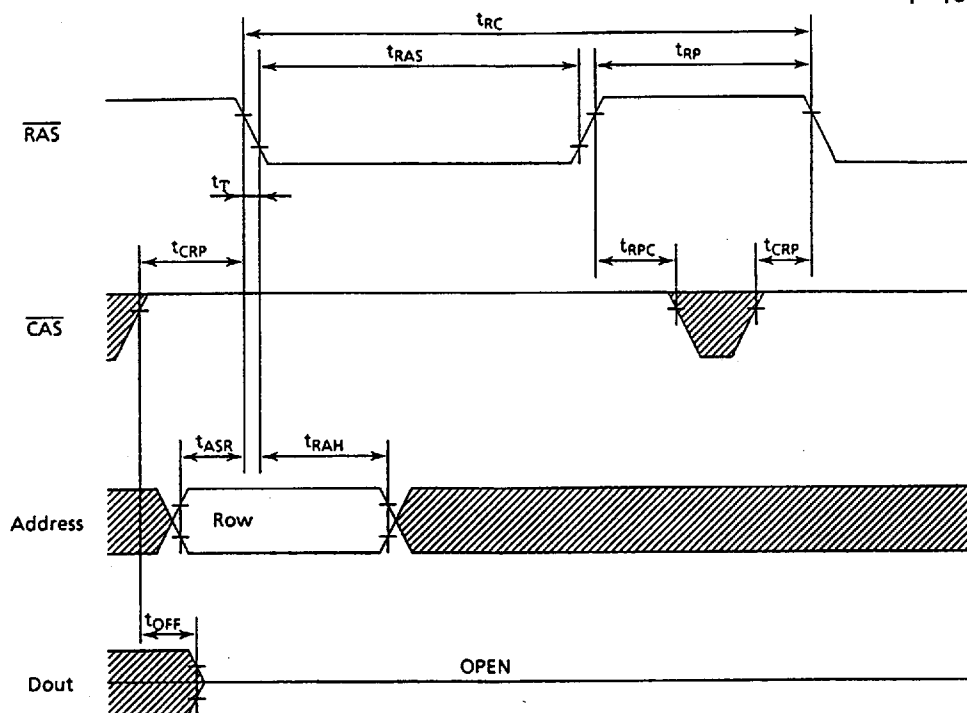
0101-15



• RAS Only Refresh Cycle

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- * $\overline{\text{OE}}, \overline{\text{WE}}$: Don't care
- **  : Don't care
- *** Refresh address : A0 - A11 (RA0 - RA11)

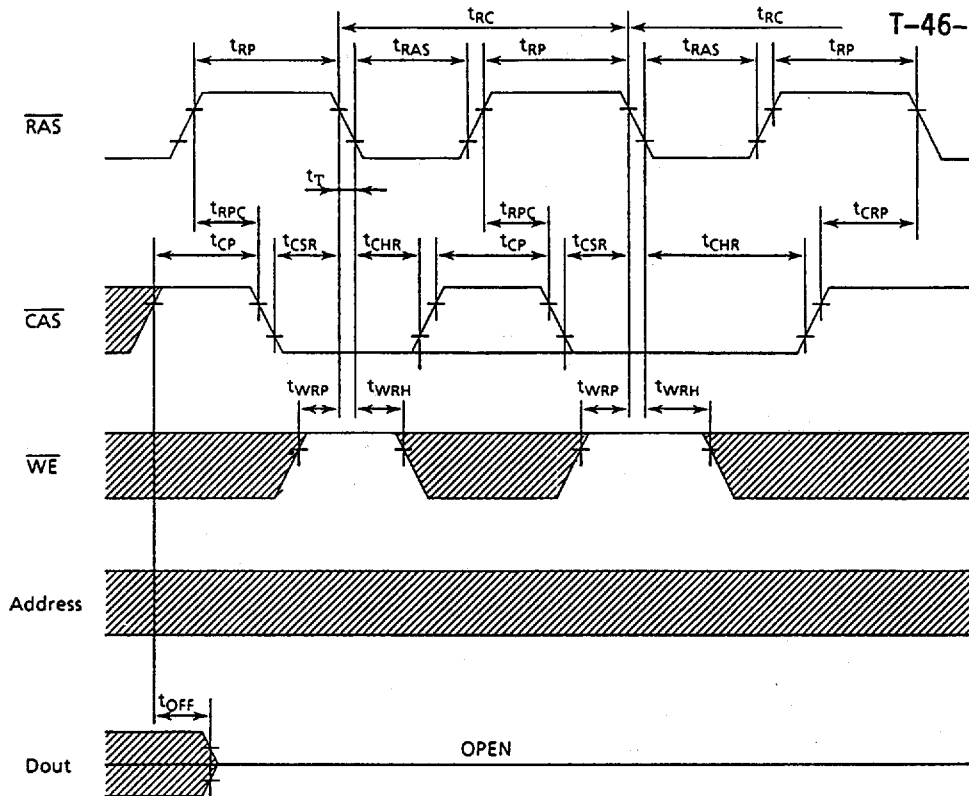
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• $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle

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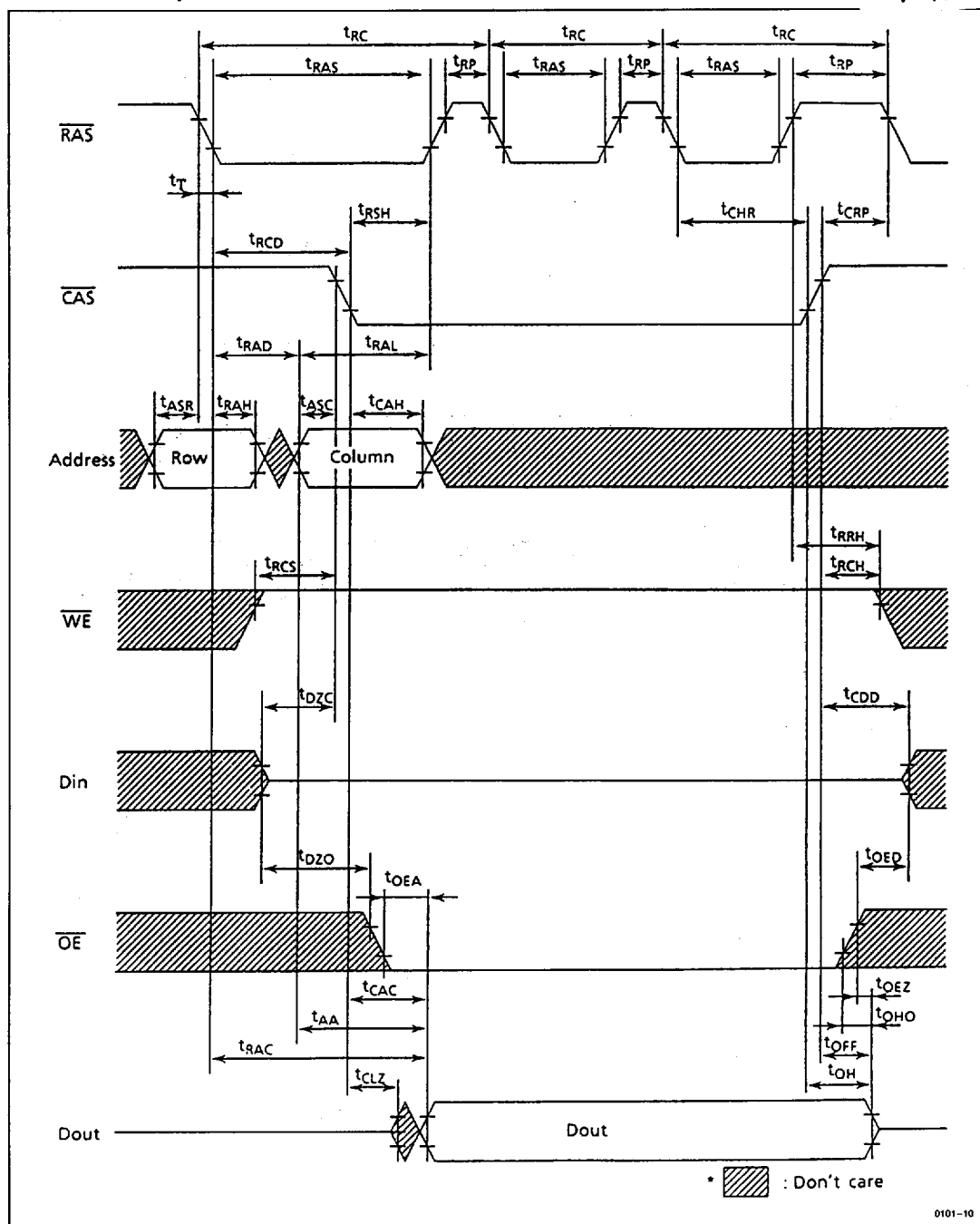
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* $\overline{\text{OE}}$: Don't care
 **  : Don't care

0101-8

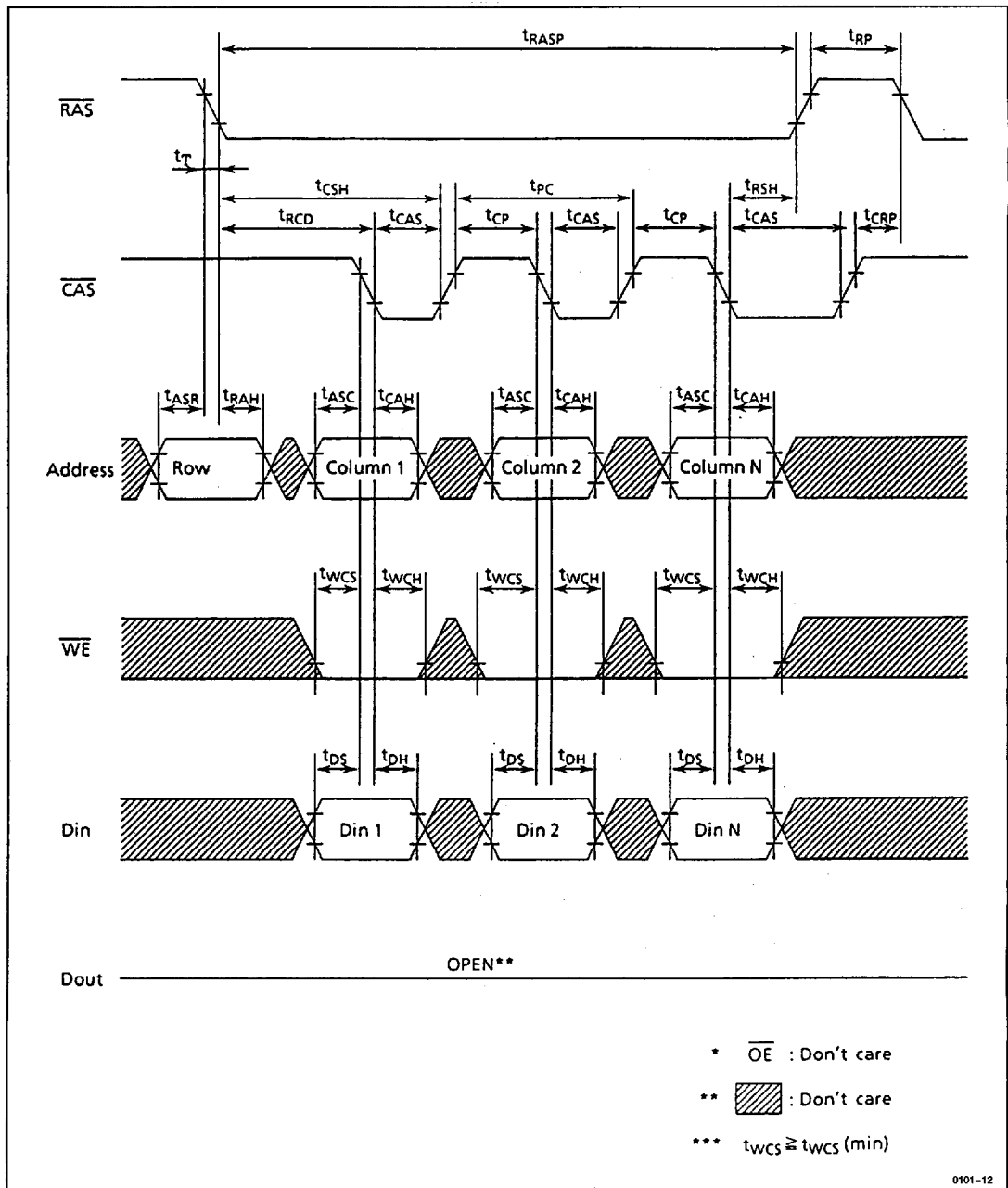




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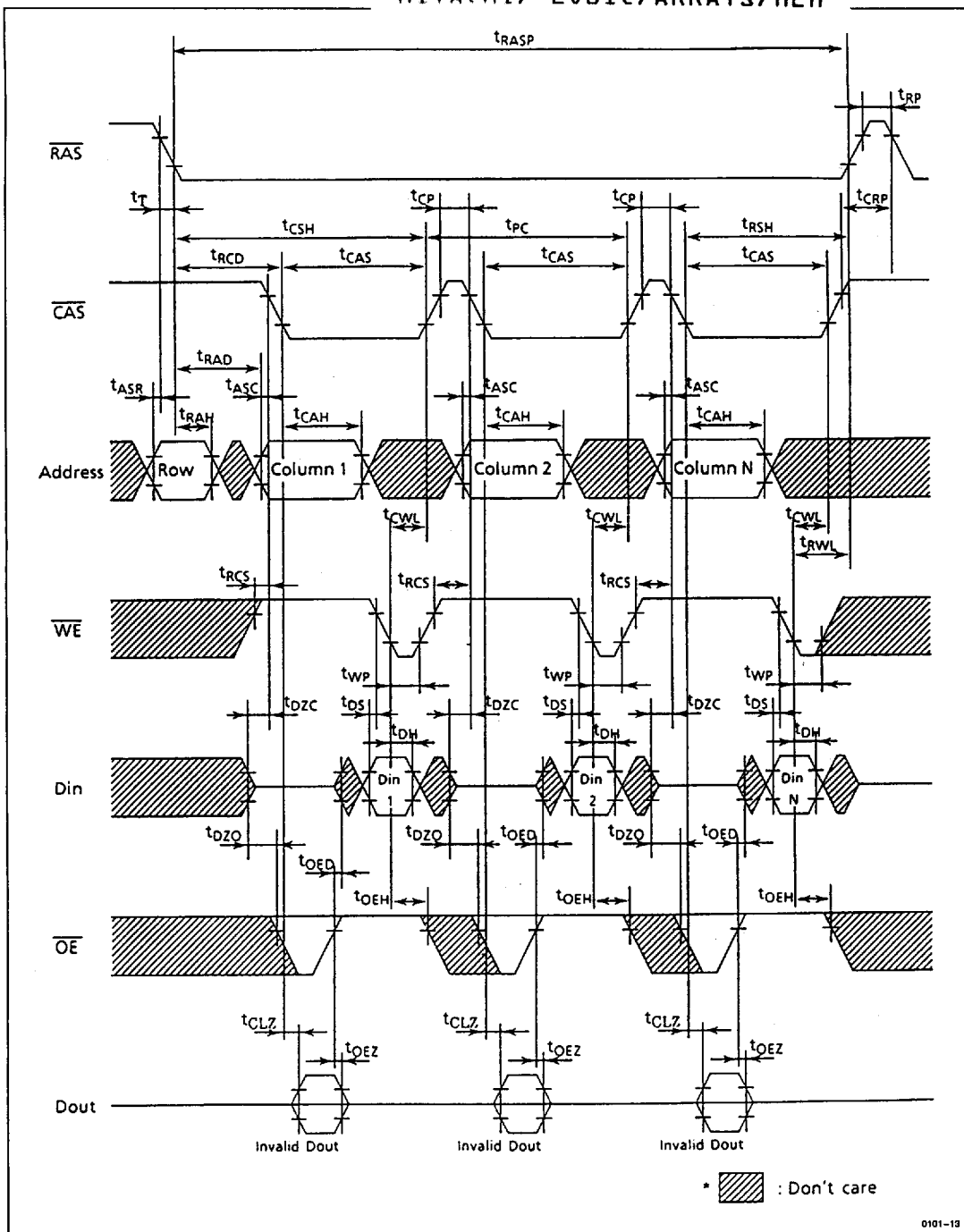


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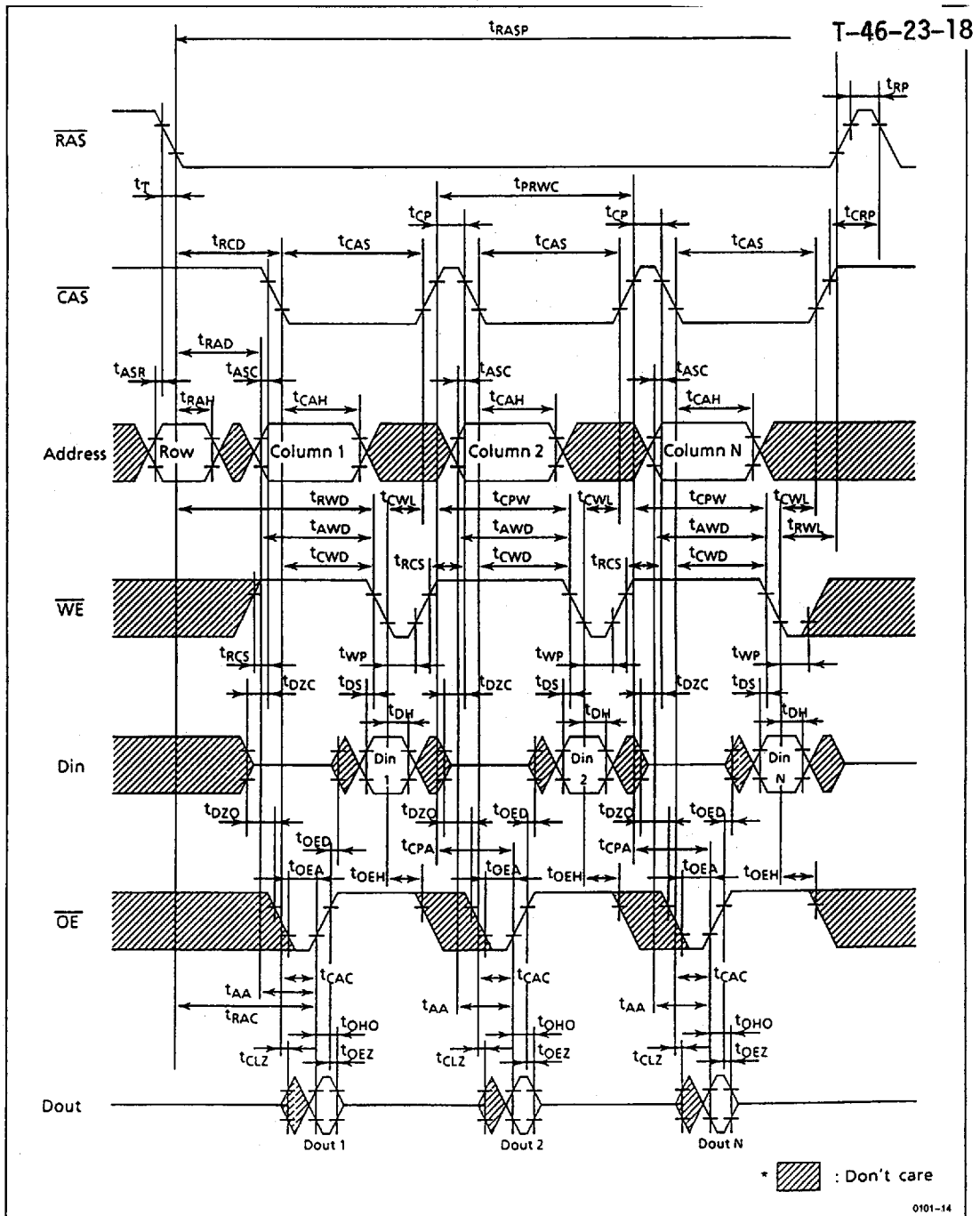
• Fast Page Mode Delayed Write Cycle

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0101-13

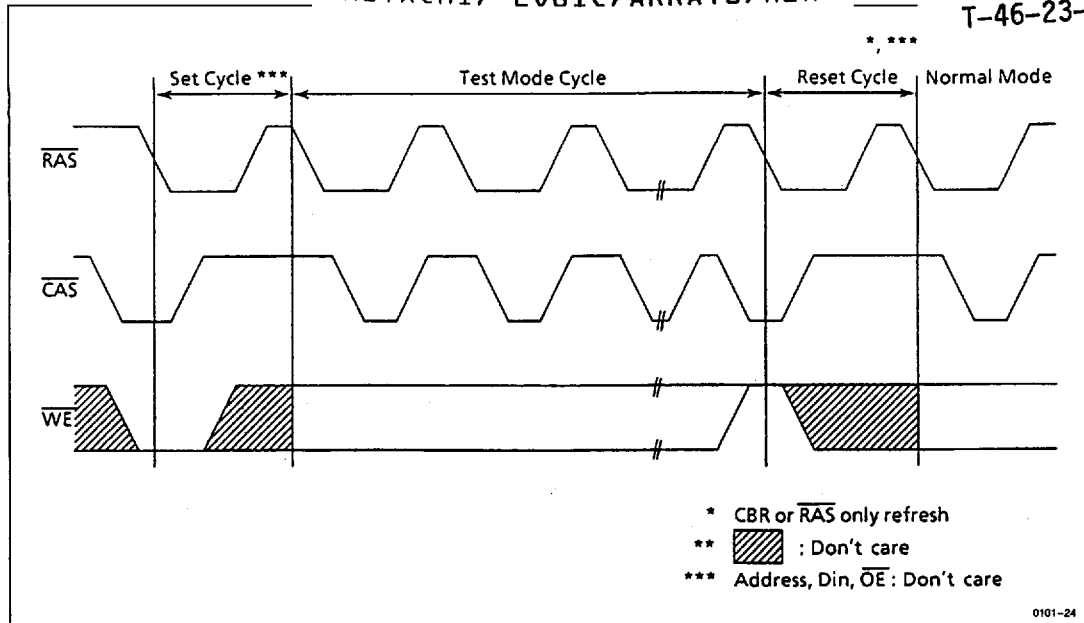




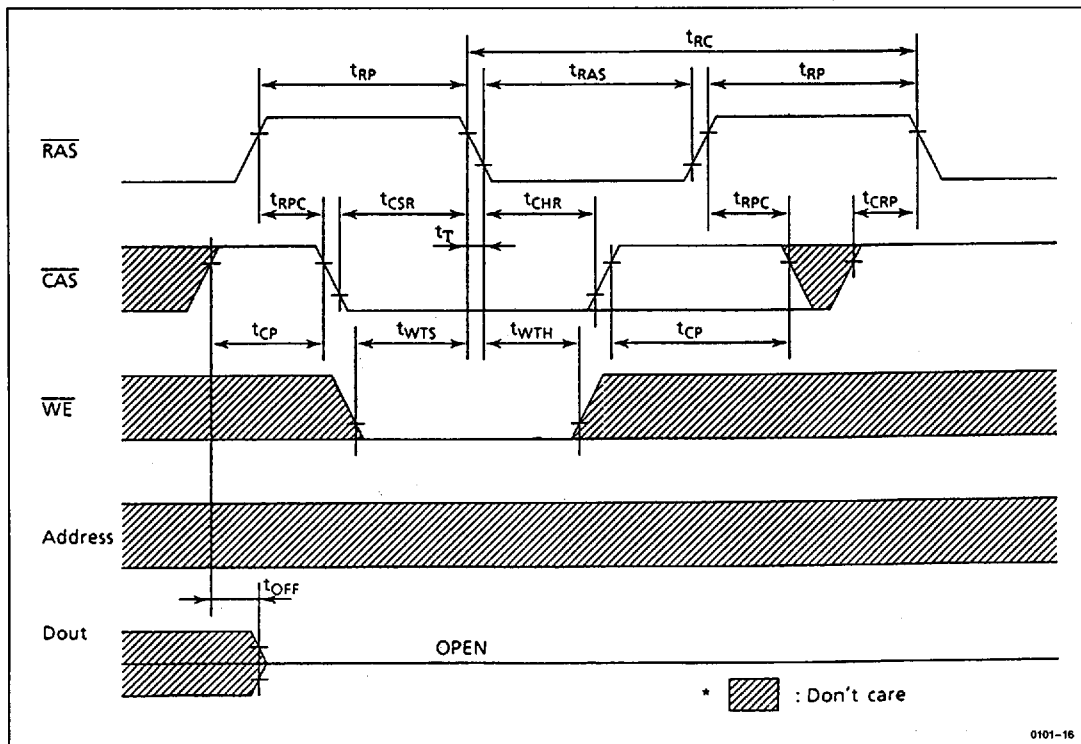
• Test Mode Cycle

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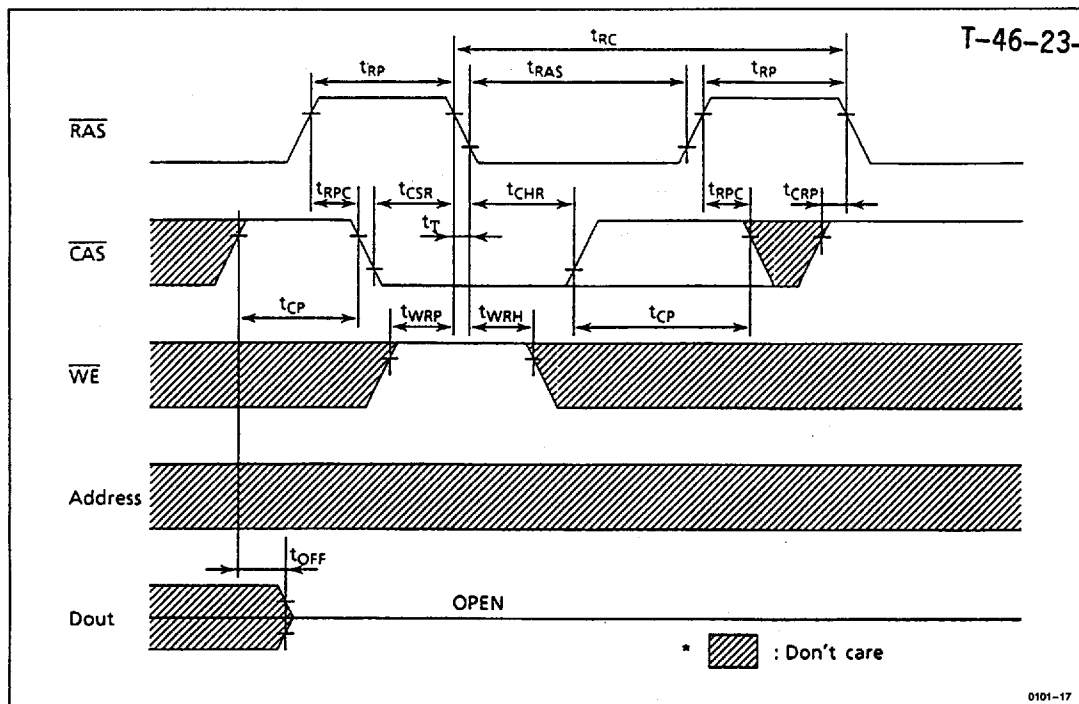
• Test Mode Set Cycle



• Test Mode Reset Cycle
CAS Before RAS Refresh Cycle

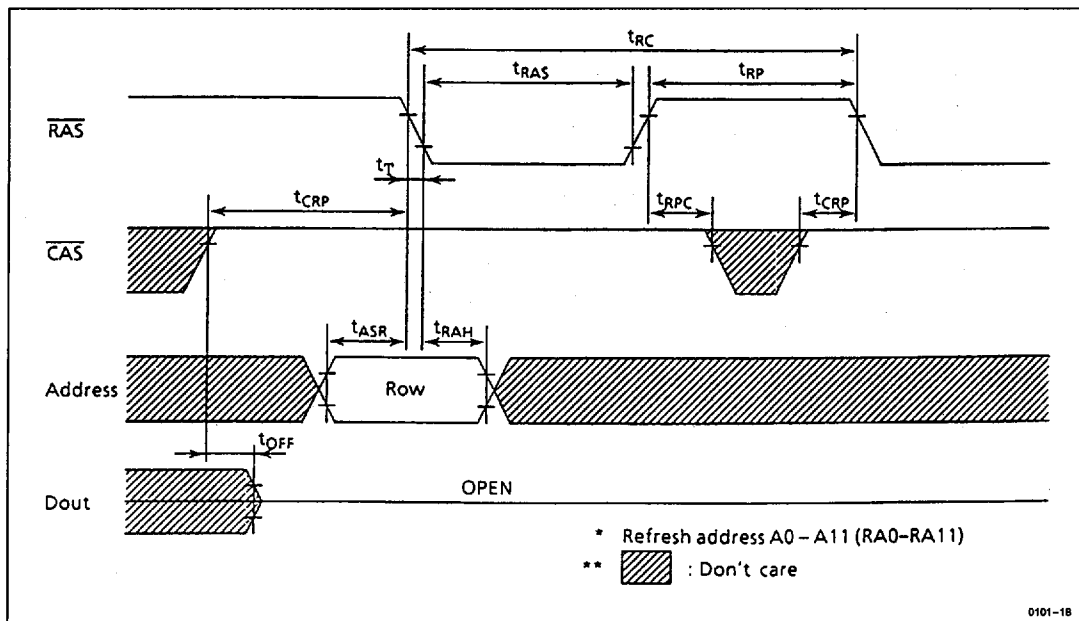
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0101-17

RAS Only Refresh Cycle



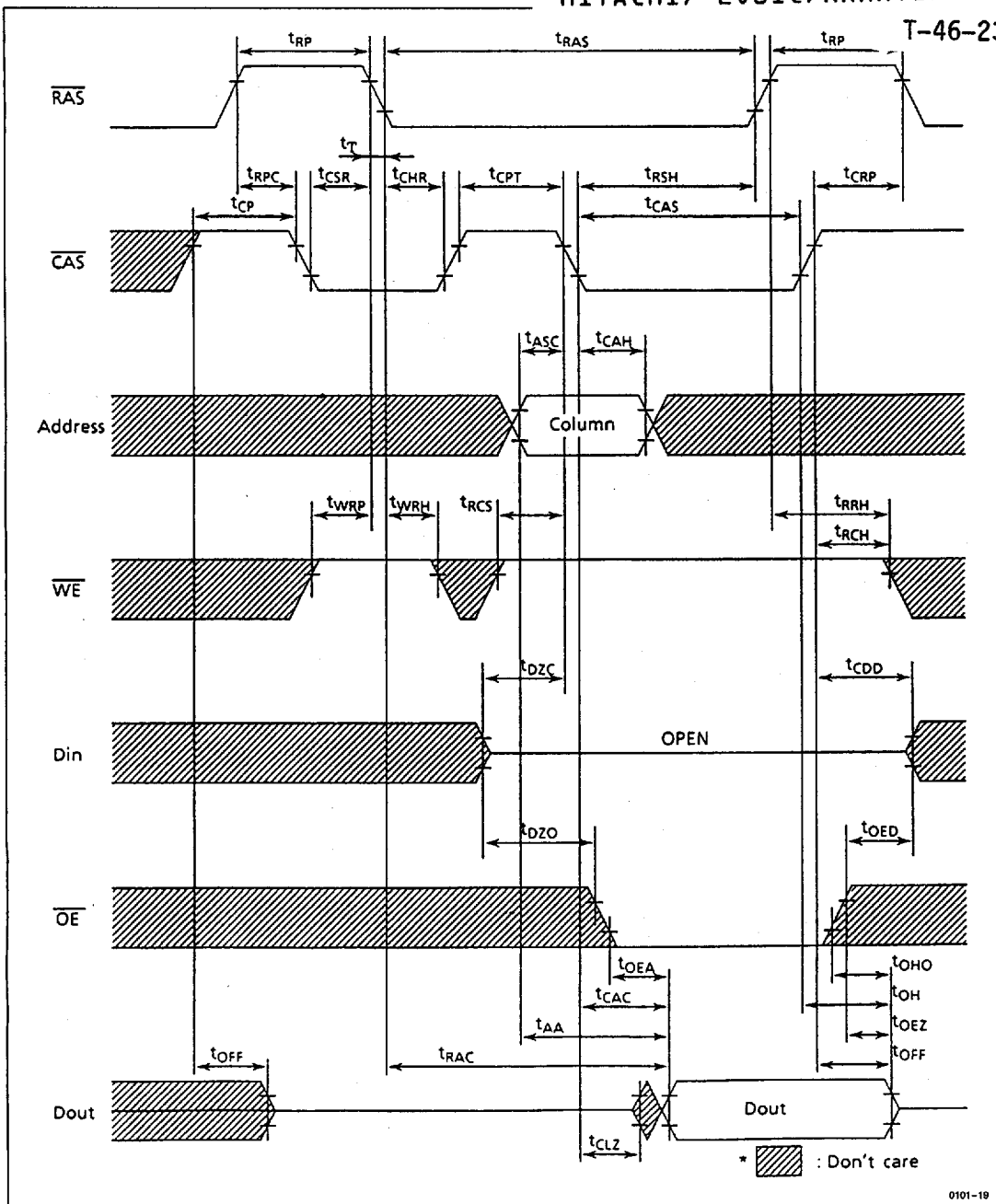
0101-18



CAS Before RAS Refresh Counter Check Cycle (Read)

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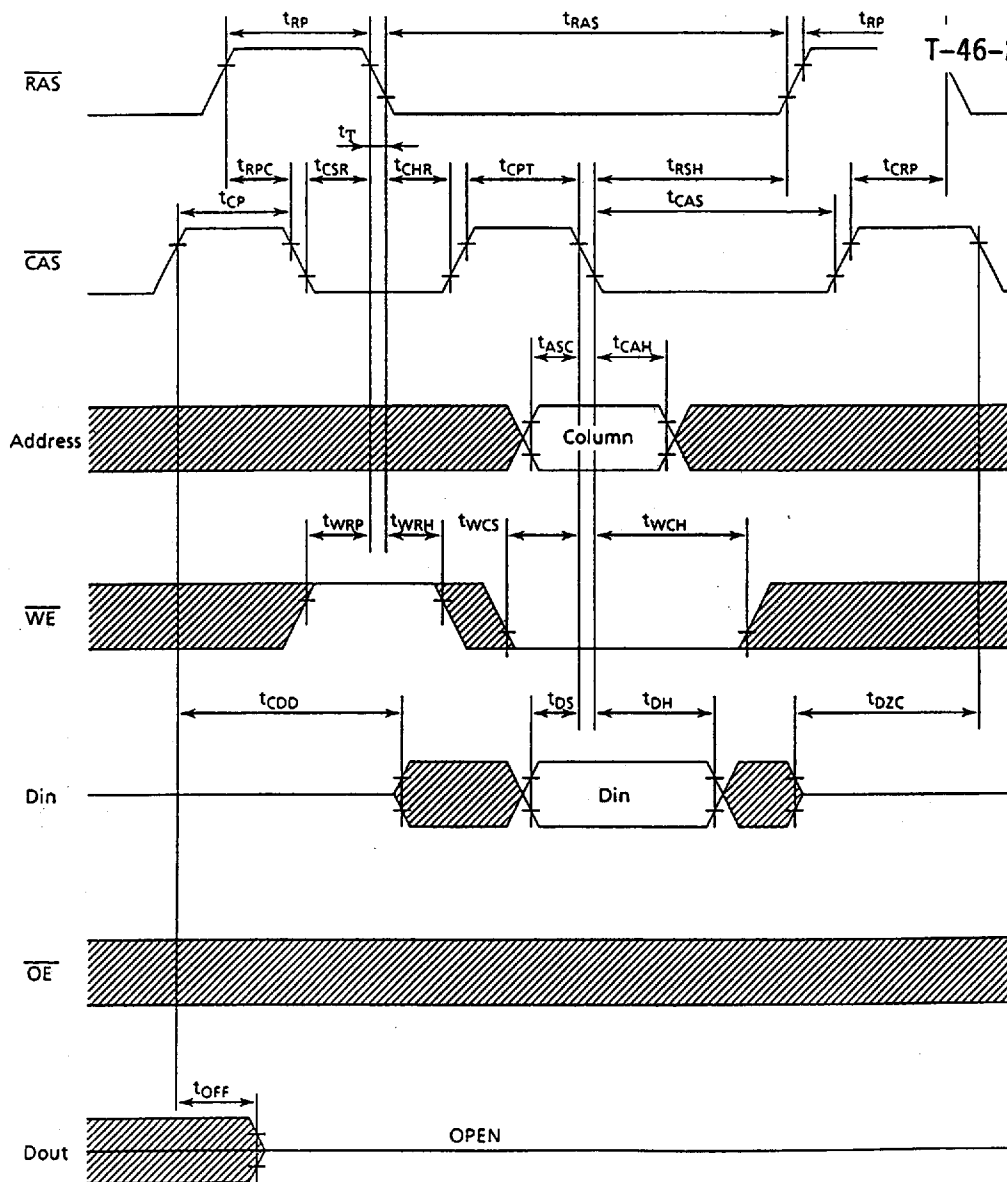
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0101-19



T-46-23-18

*  : Don't care

0101-20

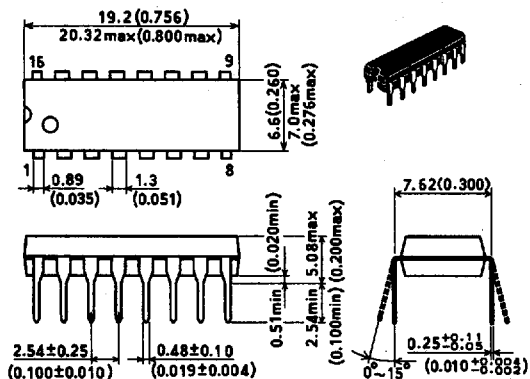


T-90-20

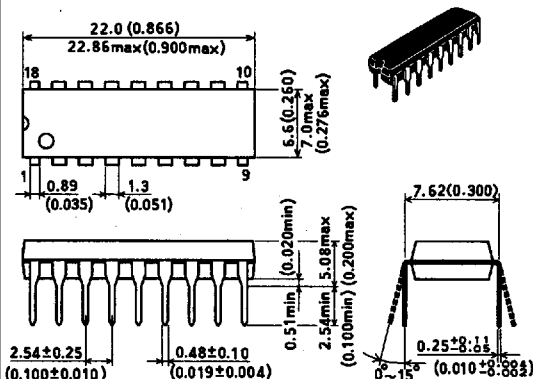
Unit: mm (inch) Scale 3/2

• Dual-in-line Plastic

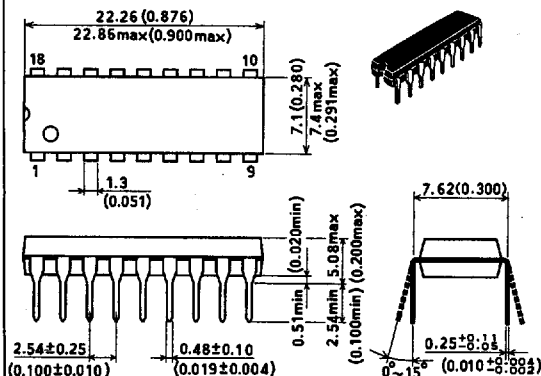
• DP-16B



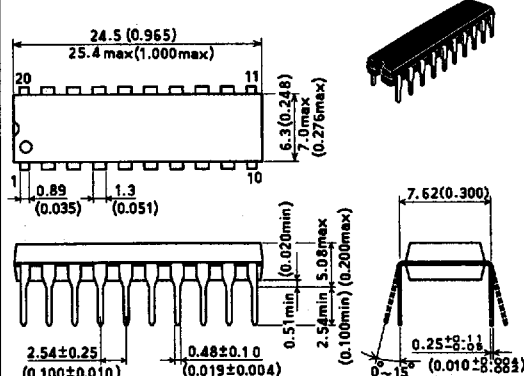
• DP-18B



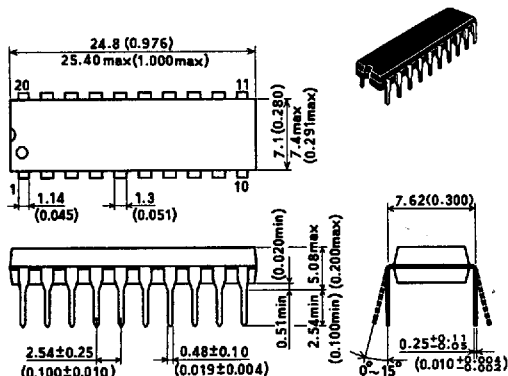
• DP-18C



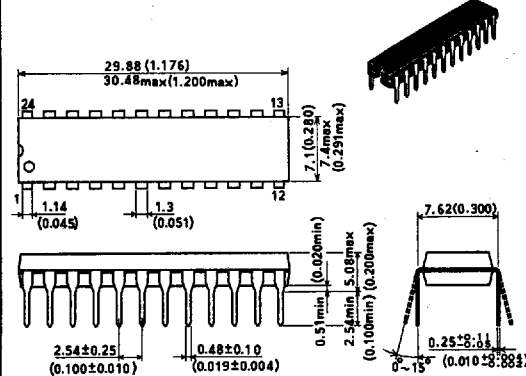
• DP-20N



• DP-20NA



• DP-20NC

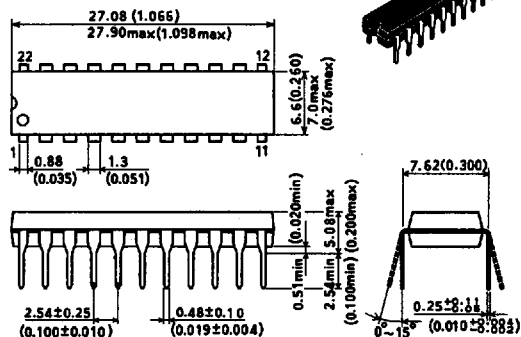


• Dual-In-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

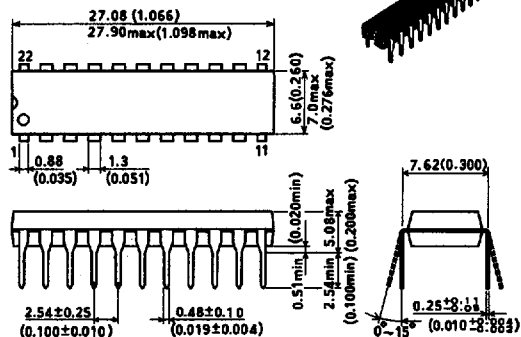
Unit: mm (inch) Scale 3/2

• DP-22N

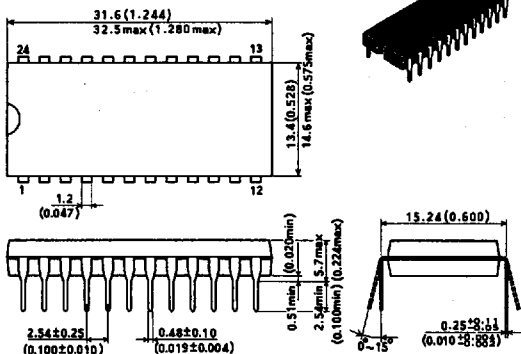


• DP-22NB

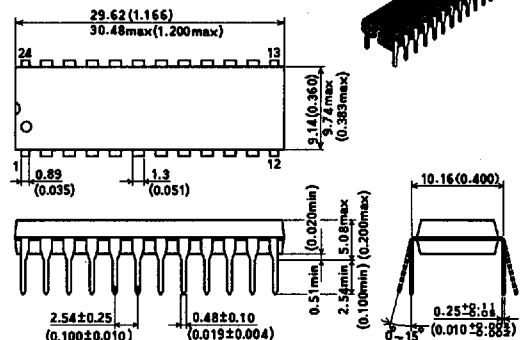
T-90-20



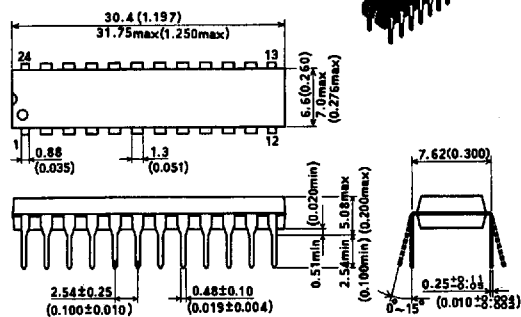
• DP-24



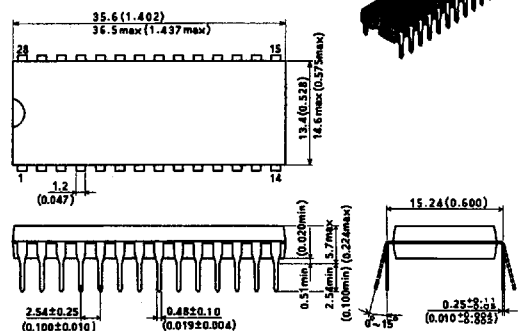
• DP-24A



• DP-24N



• DP-28

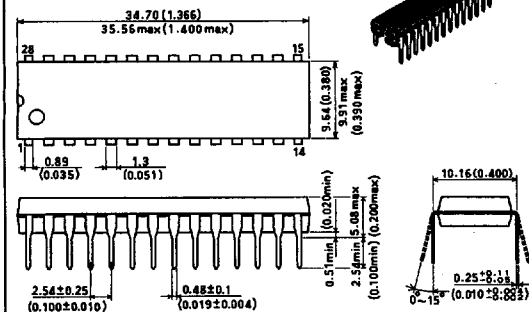


• Dual-in-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

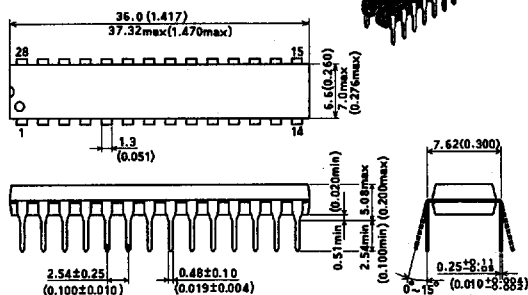
Unit: mm (inch) Scale 3/2

• DP-28C

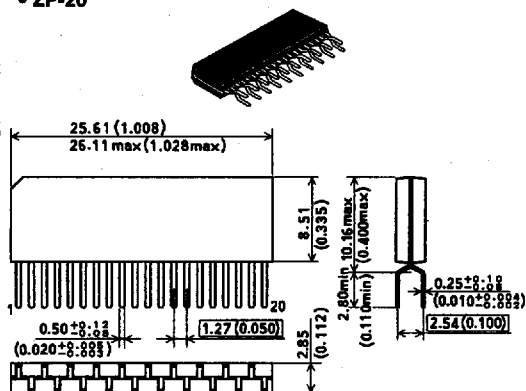


• DP-28N

T-90-20

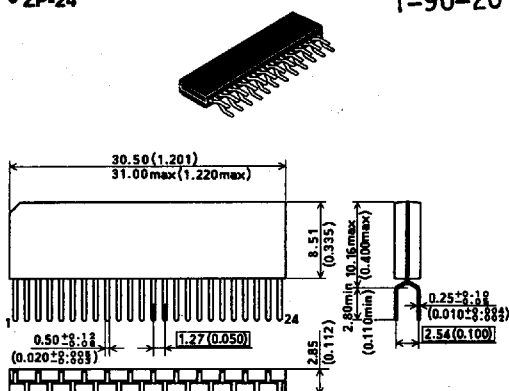


• ZP-20

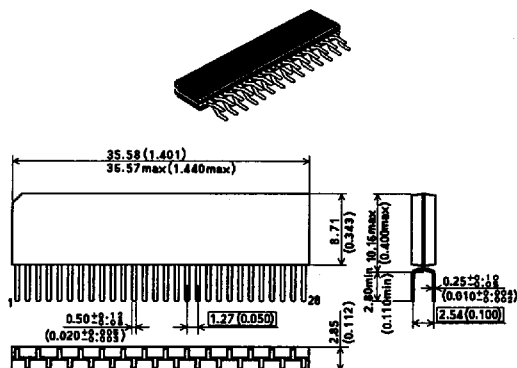


• ZP-24

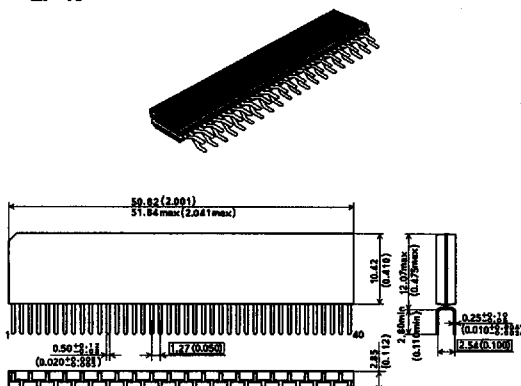
T-90-20



• ZP-28



• ZP-40



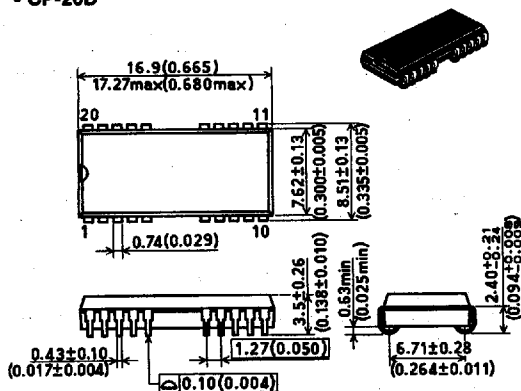
• Flat Package (J-bend Leads)

HITACHI/ LOGIC/ARRAYS/MEM

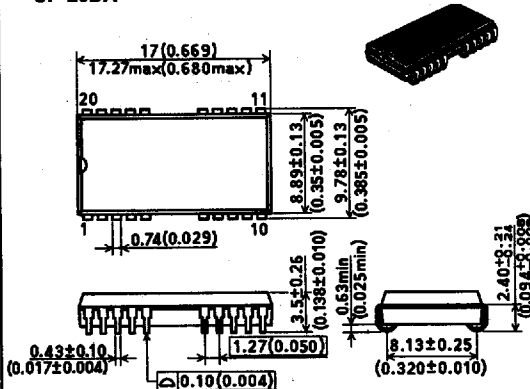
Unit: mm (inch) Scale 3/2

T-90-20

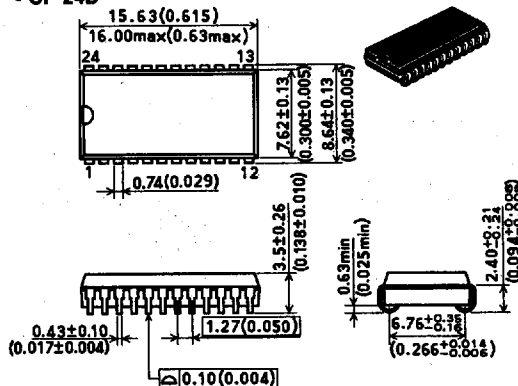
• CP-20D



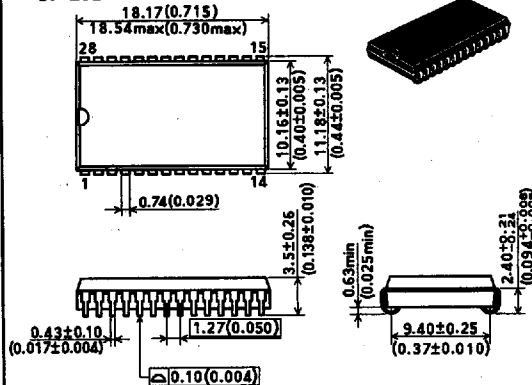
• CP-20DA



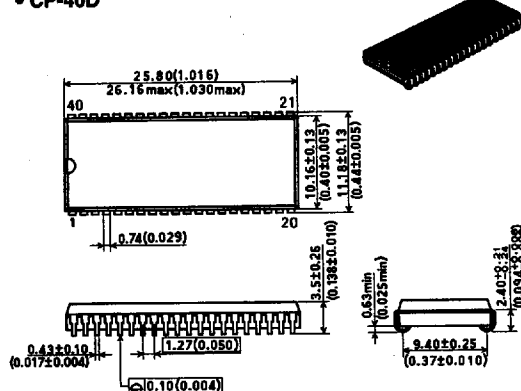
• CP-24D



• CP-28D



• CP-40D

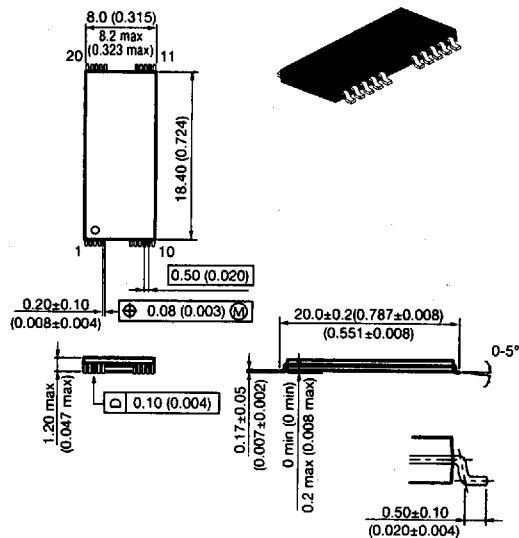


• TSOP (Thin Small Outline Package)

HITACHI/ LOGIC/ARRAYS/MEM

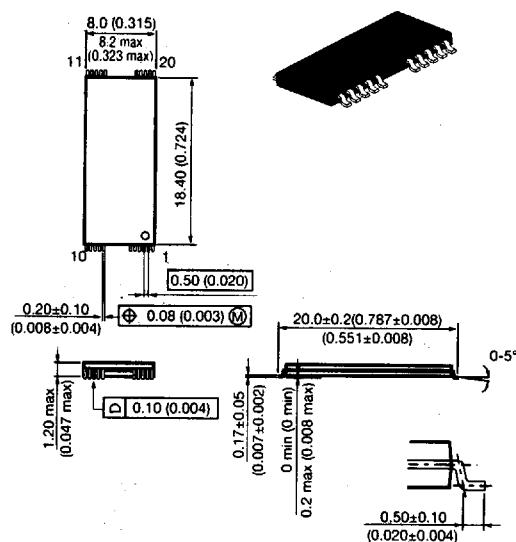
Unit: mm (inch) Scale 3/2

• TFP-20DA

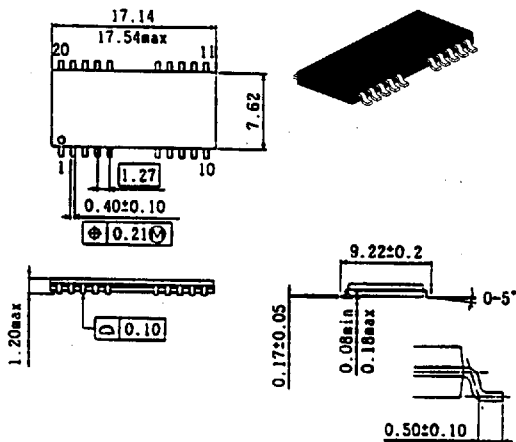


• TFP-20DAR

T-90-20



• TTP-20D



• TTP-20DR

