# TEMIC

MATRA MHS

# HM 65790

## 16 K × 4 High Speed CMOS SRAM Separate I/O

## Introduction

The HM 65790 is a high speed CMOS static RAM organized as 16384 × 4 bits. It is manufactured using MHS's high performance CMOS technology.

Access times as fast as 15 ns are available with maximum power consumption of only 633 mW.

The HM 65790 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 85 % when the circuit is deselected.

Easy memory expansion is provided by two active low chip select ($\overline{CS1}$, $\overline{CS2}$), an active low output enable ($\overline{OE}$) and three state drivers.

All inputs and outputs of the HM 65790 are TTL compatible and operate from single 5 V supply thus simplifying system design.

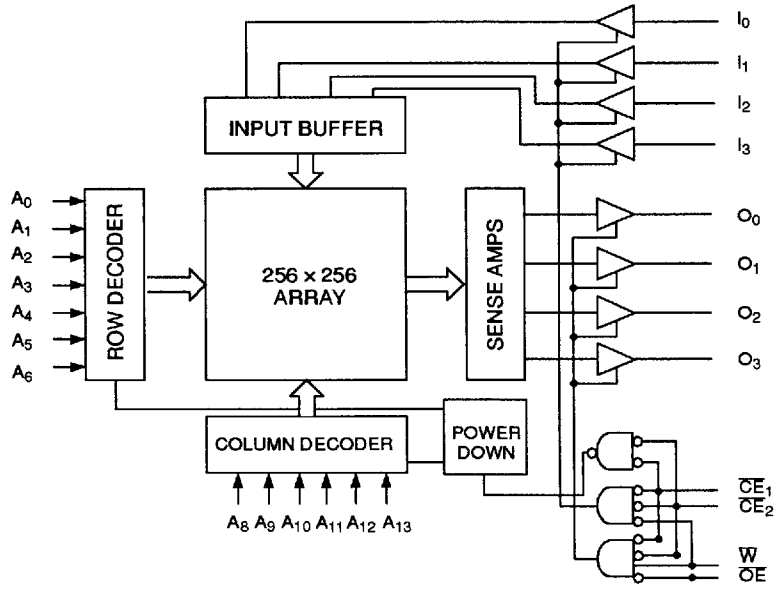
The HM 65790 is 100 % processed following the test methods of MIL STD 883 and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

## Features

- Fast access time
  Commercial : 15/20/25/35/45 ns (max)
  Military : 20/25/35/45 ns (max)
- Low power consumption
  Active : 267 mW (typ)
  Standby : 75 mW (typ)
- Wide temperature range :
  -55°C to + 125°C
- 300 mils width package
- TTL compatible inputs and outputs
- Asynchronous
- Capable of withstanding greater than 2000 V electrostatic discharge
- Single 5 volt supply
- Separate inputs/outputs
- Output enable

## Interface

### Block Diagram



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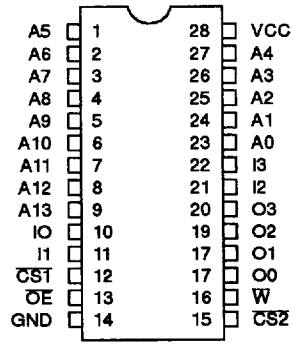
# HM 65790

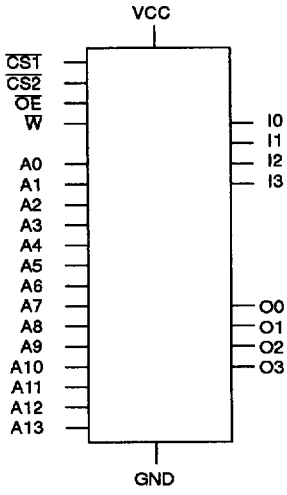
## Pin Configuration

Plastic 300 mils, 28 pins, DIL
Ceramic 300 mils, 28 pins, DIL
SOIC 300 mils, 28 pins




**Pinout DIL 28 pins (top view)**

## Logic Symbol




## Pin Names

| | | | |
|---|---|---|---|
| A0–A13: Address inputs | | $\overline{CS1}$–$\overline{CS2}$ | : Chip Select |
| I0–I3 | : Inputs | $\overline{OE}$ | : Output enable |
| O0–O3 | : Outputs | $\overline{W}$ | : Write enable |
| VCC | : Power | GND | : Ground |

## Truth Table

| $\overline{CS}$ | $\overline{OE}$ | $\overline{W}$ | DATA-IN | DATA-OUT | MODE |
|---|---|---|---|---|---|
| H | X | X | Z | Z | Deselect |
| L | L | H | Z | Valid | Read |
| L | X | L | Valid | Z | Write |

L = Low - H = High, X = H or L, Z = High impedance.



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# Electrical Characteristics

## Absolute Maximum Ratings

Supply voltage to GND potential : ..... -0.5 V to +7.0 V
DC input voltage : ..... -3.0 V to +7.0 V
DC output voltage in high Z state : ..... -0.5 V to +7.0 V

Storage temperature : ..... -65°C to +150°C
Output current into outputs (low) : ..... 20 mA
Electro Static Discharge Voltage ..... > 2001 V
(MIL STD 883C METHOD 3015-2)

## Operating Range

| | OPERATING VOLTAGE | OPERATING TEMPERATURE |
|---|---|---|
| Military (- 2) | 5 V ± 10 % | - 55°C to + 125°C |
| Commercial (- 5) | 5 V ± 10 % | 0°C to + 70°C |

## Recommended DC Operating Conditions

| PARAMETER | DESCRIPTION | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| Vcc | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| Gnd | Ground | 0.0 | 0.0 | 0.0 | V |
| VIL | Input low voltage | - 3.0 | 0.0 | 0.8 | V |
| VIH | Input high voltage | 2.2 | - | VCC | V |

## Capacitance

| PARAMETER | DESCRIPTION | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| Cin (1) | Input capacitance | - | - | 5 | pF |
| Cout (1) | Output capacitance | - | - | 7 | pF |

**Note :** 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.

## DC Parameters

| PARAMETER | DESCRIPTION | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| IIX (2) | Input leakage current | - 10.0 | - | 10.0 | µA |
| IOZ (3) | Output leakage current | - 10.0 | - | 10.0 | µA |
| IOS (3) | Output short circuit current | - | - | - 350.0 | mA |
| VOL (4) | Output low voltage | - | - | 0.4 | V |
| VOH (5) | Output high voltage | 2.4 | - | - | V |

**Note :** 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = -4.0 mA.



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## Consumption for Commercial (-5) Specification

| SYMBOL | | PARAMETER | 65790 E-5 | 65790 F-5 | 65790 H-5 | 65790 K-5 | 65790 M-5 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|---|---|
| ICCSB | (6) | Standby supply current | 20 | 40 | 30 | 30 | 30 | mA | max |
| ICCSB1 | (7) | Standby supply current | 20 | 20 | 20 | 20 | 20 | mA | max |
| ICCOP | (8) | Dynamic operating current | 115 | 100 | 100 | 100 | 100 | mA | max |

## Consumption for Military (-2) Specification

| SYMBOL | | PARAMETER | 65790 F-2 | 65790 H-2 | 65790 K-2 | 65790 M-2 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|---|
| ICCSB | (6) | Standby supply current | 40 | 40 | 30 | 30 | mA | max |
| ICCSB1 | (7) | Standby supply current | 20 | 20 | 20 | 20 | mA | max |
| ICCOP | (8) | Dynamic operating current | 115 | 100 | 100 | 100 | mA | max |

**Note :** 6. $\overline{CS} \geq$ VIH min duty cycle = 100 %, a pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values above.
7. $\overline{CS}$ = Vcc - 0.3 V Iout = 0 mA.
8. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.
* Preliminary.

# AC Parameters

## AC Conditions

Input pulse levels : ..... Gnd to 3.0 V
Input rise : ..... 5 ns
Input timing reference levels : ..... 1.5 V
Output loading IOL/IOH *(see figure 1a and 1b)* : ..... +30 pF

## AC Test Loads and Waveforms

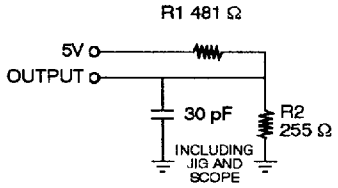



**Figure 1 a**

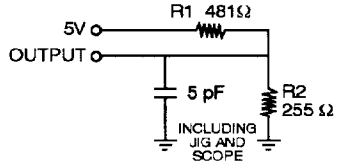



**Figure 1 b**

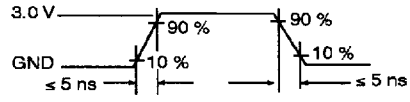
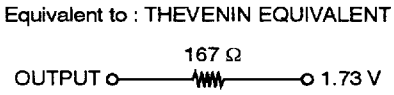



**Figure 2**



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## Write Cycle : Commercial (-5) Specification

| SYMBOL | PARAMETER | 65790 E-5 | 65790 F-5 | 65790 H-5 | 65790 K-5 | 65790 M-5 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|---|
| TAVAV | Write cycle time | 15 | 20 | 20 | 25 | 40 | ns | min |
| TAVWL | Address set-up time | 0 | 0 | 0 | 0 | 0 | ns | min |
| TAVWH | Address valid to end of write | 12 | 15 | 20 | 25 | 30 | ns | min |
| TDVWH | Data set-up time | 10 | 10 | 10 | 15 | 15 | ns | min |
| TELWH | $\overline{CS}$ low to write end | 12 | 15 | 20 | 25 | 30 | ns | min |
| TWLQZ | Write low to high Z | 7 | 7 | 7 | 10 | 15 | ns | max |
| TWLWH | Write pulse width | 12 | 15 | 15 | 20 | 20 | ns | min |
| TWHAX | Address hold from end of write | 0 | 0 | 0 | 0 | 0 | ns | min |
| TWHDX | Data hold time | 0 | 0 | 0 | 0 | 0 | ns | min |
| TWHQX (8) | Write high to low Z | 5 | 5 | 5 | 5 | 5 | ns | min |

## Write Cycle : Military (-2) Specification

| SYMBOL | PARAMETER | 65790 F-2 | 65790 H-2 | 65790 K-2 | 65790 M-2 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|
| TAVAV | Write cycle time | 20 | 20 | 25 | 40 | ns | min |
| TAVWL | Address set-up time | 0 | 0 | 0 | 0 | ns | min |
| TAVWH | Address Valid to end of write | 15 | 20 | 25 | 30 | ns | min |
| TDVWH | Data set-up time | 10 | 10 | 15 | 15 | ns | min |
| TELWH | $\overline{CS}$ low to write end | 15 | 20 | 25 | 30 | ns | min |
| TWLQZ(8) | Write low to high Z | 7 | 7 | 10 | 15 | ns | max |
| TWLWH | Write pulse width | 15 | 15 | 20 | 20 | ns | min |
| TWHAX | Address hold from end of write | 0 | 0 | 0 | 0 | ns | min |
| TWHDX | Data hold time | 0 | 0 | 0 | 0 | ns | min |
| TWHQ (8) | Write high to low Z | 5 | 5 | 5 | 5 | ns | min |

**Note :** 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.



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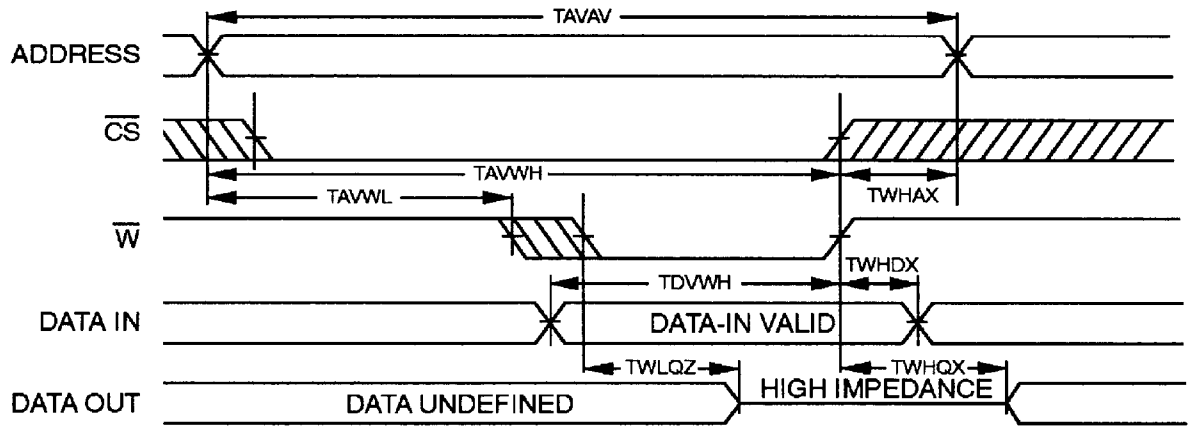
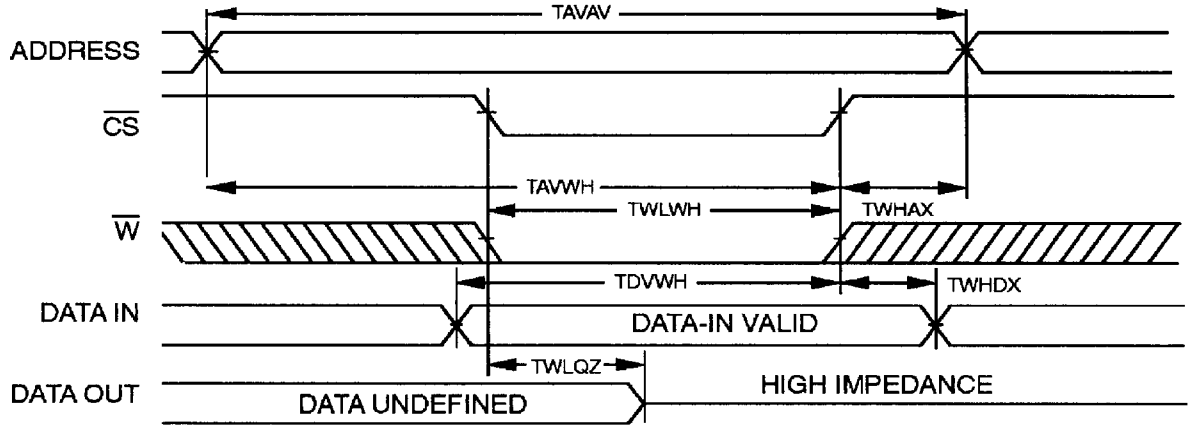
### Write Cycle 1 $\overline{W}$ Controlled




### Write Cycle 2 $\overline{CS}$ controlled



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## Read Cycle : Commercial (-5) Specification

| SYMBOL | PARAMETER | 65790 E-5 | 65790 F-5 | 65790 H-5 | 65790 K-5 | 65790 M-5 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|---|
| TAVAV | Read cycle time | 15 | 20 | 25 | 35 | 45 | ns | min |
| TAVQV | Address access time | 15 | 20 | 25 | 35 | 45 | ns | max |
| TAVQX | Address valid to low Z | 3 | 3 | 3 | 3 | 3 | ns | min |
| TELQV | Chip-select access time | 15 | 20 | 25 | 35 | 45 | ns | max |
| TELQX | $\overline{CS}$ low to low Z | 5 | 5 | 5 | 5 | 5 | ns | min |
| TEHQZ | $\overline{CS}$ high to high Z | 8 | 8 | 10 | 12 | 15 | ns | max |
| TELIC | $\overline{CS}$ low to power up | 0 | 0 | 0 | 0 | 0 | ns | min |
| TEHICL | $\overline{CS}$ high to power down | 15 | 20 | 20 | 20 | 25 | ns | max |
| TGLQV | Output enable access time | 10 | 10 | 12 | 15 | 20 | ns | max |
| TGLQX | $\overline{OE}$ low to low Z | 3 | 3 | 3 | 3 | 3 | ns | min |
| TGHQZ | $\overline{OE}$ high to high Z | 15 | 15 | 15 | 15 | 15 | ns | max |

## Read Cycle : Military (-2) Specification

| SYMBOL | PARAMETER | 65790 F-2 | 65790 H-2 | 65790 K-2 | 65790 M-2 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|
| TAVAV | Read cycle time | 20 | 25 | 35 | 45 | ns | min |
| TAVQV | Address access time | 20 | 25 | 35 | 45 | ns | max |
| TAVQX | Address valid to low Z | 3 | 3 | 3 | 3 | ns | min |
| TELQV | Chip-select access time | 20 | 25 | 35 | 45 | ns | max |
| TELQX | $\overline{CS}$ low to low Z | 5 | 5 | 5 | 5 | ns | min |
| TEHQZ | $\overline{CS}$ high to high Z | 8 | 10 | 12 | 15 | ns | max |
| TELIC | $\overline{CS}$ low to power up | 0 | 0 | 0 | 0 | ns | min |
| TEHICL | $\overline{CS}$ high to power down | 20 | 20 | 20 | 25 | ns | max |
| TGLQV | Output enable access time | 10 | 12 | 15 | 20 | ns | max |
| TGLQX | $\overline{OE}$ low to low Z | 3 | 3 | 3 | 3 | ns | min |
| TGHQZ | $\overline{OE}$ high to high Z | 15 | 15 | 15 | 15 | ns | min |



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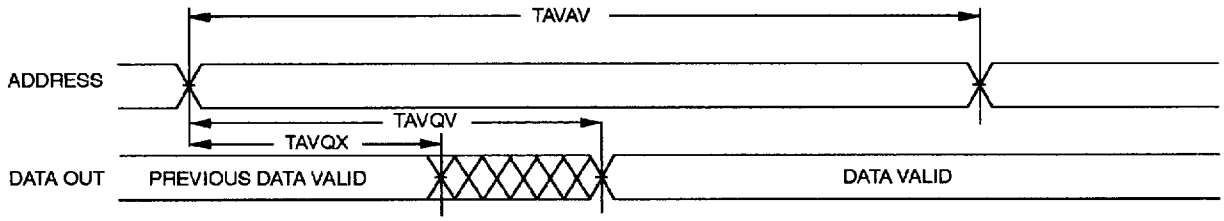
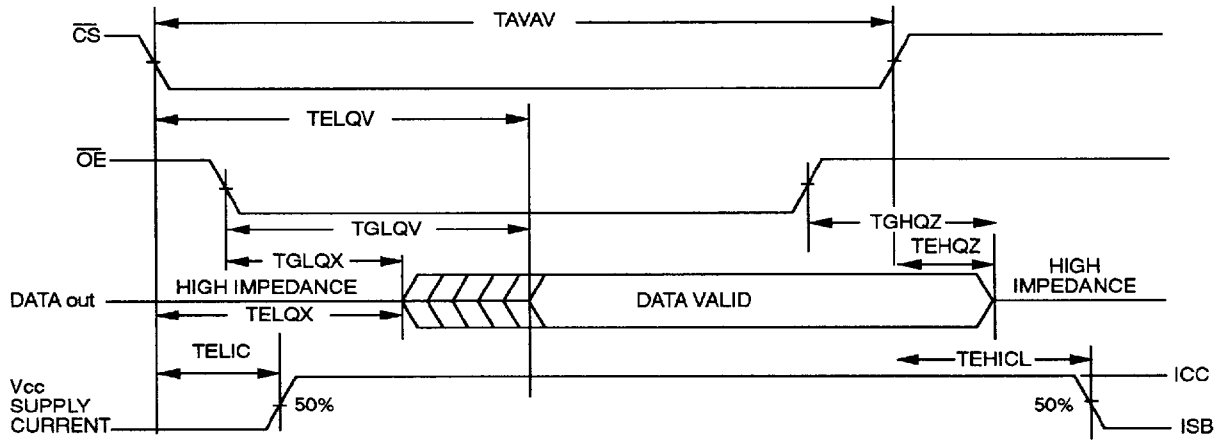
## Read Cycle nb 1 (notes 9, 10)




## Read Cycle nb 2 (notes 9, 11)




**Notes :** 9. $\overline{W}$ is high for read cycle.
10. Device is continuously selected, $\overline{CS}_1$, $\overline{CS}_2$ = VIL.
11. Address valid prior to or coincider with $\overline{CS}_1$, $\overline{CS}_2$ transition low.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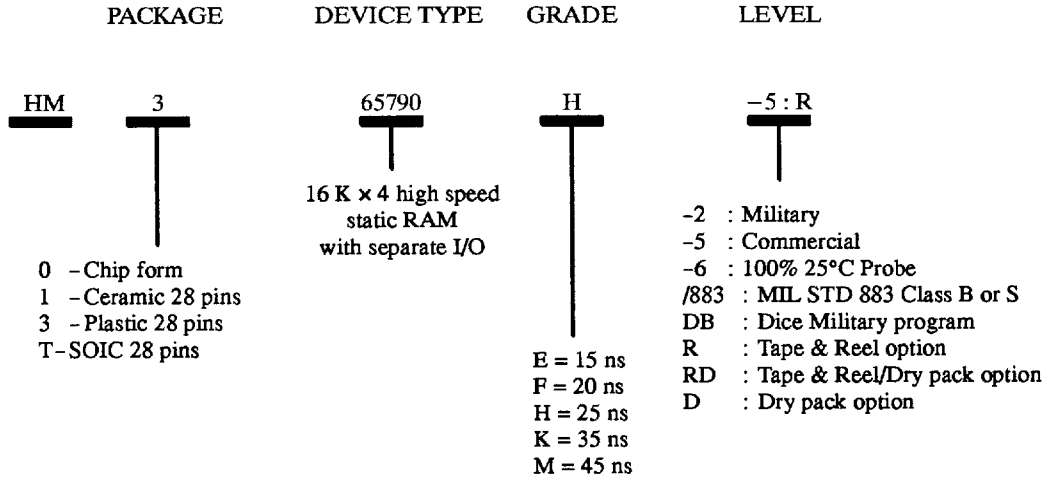
## Ordering Information

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