

T-75-45-05

DS75150 Dual Line Driver

General Description

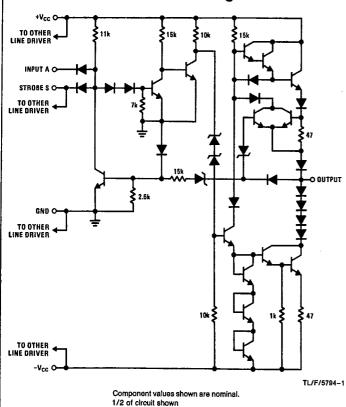
The DS75150 is a dual monolithic line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500 pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and LS families. Operation is from -12V and +12V power supplies.

Features

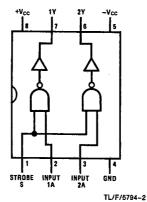
- Withstands sustained output short-circuit to any low impedance voltage between -25V and +25V
- \blacksquare 2 μ s max transition time through the -3V to +3V transition region under full 2500 pF load
- Inputs compatible with most TTL and LS families
- Common strobe input
- inverting output
- Slew rate can be controlled with an external capacitor at the output
- Standard supply voltages

± 12V

Schematic and Connection Diagrams



Dual-In-Line Package



Top View Positive Logic $C = \overline{AS}$

Order Number DS75150J-8, DS75150M or DS75150N See NS Package Number J08A, M08A or N08E

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Range (TA)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage + V_{CC} 15V Supply Voltage - V_{CC} Input Voltage 15V Applied Output Voltage +25V Storage Temperature Range -65°C to +150°C

Maximum Power Dissipation* at 25°C

1133 mW Cavity Package 1022 mW Molded DIP Package 655 mW SO Package 260°C Lead Temperature (Soldering, 4 sec.)

*Derate cavity package 7.6 mW/*C above 25°C; derate molded DIP package 8.2 mW/*C above 25°C. Derate SO package 8.01 mW/*C above 25°C.

| Operating Condition | s T | T-75-45-05 | | | |
|------------------------------------|-------|------------|-------|--|--|
| GP 37 37 37 3 | Min | Max | Units | | |
| Supply Voltage (+V _{CC}) | 10.8 | 13.2 | ٧ | | |
| Supply Voltage ($-V_{CC}$) | -10.8 | -13.2 | ٧ | | |
| Input Voltage (V _I) | 0 | +5.5 | ٧ | | |
| Output Voltage (VO) | | ±15 | ٧ | | |
| Operating Ambient Temperature | | | | | |
| Range (T _A) | 0 | +70 | °C | | |

DC Electrical Characteristics (Notes 2.2.4 and 5)

| Symbol | Parameter | Conditions | | Min | Тур | Max | Units |
|---------------------|---|---|----------------------|----------|-----|------|-------|
| VIH | High-Level Input Voltage | (Figure 1) | | 2 | | | ٧ |
| VIL | Low-Level Input Voltage | (Figure 2) | | | | 0.8 | ٧ |
| V _{OH} | High-Level Output Voltage | $+V_{CC} = 10.8V, -V_{CC} = -13.2V, V_{IL} = 0.8V,$ $R_{L} = 3 kΩ$ to 7 kΩ (Figure 2) | | 5 | 8 | | ٧ |
| V _{OL} | Low-Level Output Voltage | $+V_{CC} = 10.8V, -V_{CC} = -10.8V, V_{IH} = 2V,$ $R_L = 3 kΩ$ to 7 kΩ (Figure 1) | | | -8 | -5 | ٧ |
| lін | High-Level Input Current | $+V_{CC} = 13.2V, -V_{CC} = -13.2V,$ V ₁ = 2.4V, (Figure 3) | Data Input | | 1 | 10 | μΑ |
| | | +V _{CC} = 13.2V, -V _{CC} = -13.2V, V ₁ = 2.4V, (<i>Figure 3</i>) | Strobe Input | | 2 | 20 | μА |
| l _{IL} | Low-Level Input Current | $+V_{CC} = 13.2V, -V_{CC} = -13.2V,$ $V_1 = 0.4V, (Figure 3)$ | Data Input -1 | 1.6 | mA | | |
| | | +V _{CC} = 13.2V, -V _{CC} = -13.2V, V _i = 0.4V, (Figure 3) | Strobe Input | | -2 | -3.2 | mA |
| I _{OS} Sho | Short-Circuit Output Current | Short-Circuit Output Current $+V_{CC} = 13.2V, -V_{CC} = -13.2V,$ | V _O = 25V | | 2 | 5 | mA |
| | | | $V_O = -25V$ | <u> </u> | -3 | -6 | mA |
| | | | $V_O = 0V, V_I = 3V$ | | 15 | 30 | mA |
| | · | | $V_O = 0V, V_I = 0V$ | | -15 | -30 | mA |
| +Іссн | Supply Current From +V _{CC} , High-Level Output | $+V_{CC} = 13.2V, -V_{CC} = -13.2V, V_{I} = 0V,$ $R_{L} = 3 k\Omega, T_{A} = 25^{\circ}C, (Figure 5)$ | | | 10 | 22 | mA |
| —łссн | Supply Current From -V _{CC} , High-Level Output | $+V_{CC} = 13.2V, -V_{CC} = -13.2V, V_{I} = 0V,$ $R_{L} = 3 \text{ k}\Omega, T_{A} = 25^{\circ}\text{C}, (Figure 5)$ | | | -1 | -10 | mA |
| + lccr | Supply Current From +V _{CC} , Low-Level Output | $+V_{CC} = 13.2V, -V_{CC} = -13.2V, V_I = 3V,$ $R_L = 3 \text{ k}\Omega, T_A = 25^{\circ}\text{C}, (Figure 5)$ | | | 8 | 17 | mA |
| -I _{CCL} | Supply Current From -V _{CC} , Low-Level Output | $+V_{CC} = 13.2V, -V_{CC} = -13.2V, V_{I} = 3V,$ $R_{L} = 3 k\Omega, T_{A} = 25^{\circ}C, (Figure 5)$ | | | -9 | -20 | mA |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75150. All typical values are TA = 25°C and +V_{CC} = 12V, $-V_{CC} = -12V$.

Note 3: All current into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when -5V is the maximum, the typical value is more-negative voltage.

 $C_L = 15 \text{ pF}, R_L = 7 \text{ k}\Omega$, (Figure 6)

| | | | | | _ |
|---|----|----|----|----|---|
| Т | -7 | 5 | 15 | Λ | C |
| | _, | J- | TU | -0 | J |

| $(+V_{CC} = 12V, -V_{CC} = -12V, T_A = 25^{\circ}C)$ | | T-75-45-05 | | | |
|--|-------------------|-----------------------------------|---|--|--|
| Min | Тур | Max | Units | 2/5/50 | |
| 0.2 | 1.4 | 2 | μs | | |
| 0,2 | 1.5 | 2 | με | | |
| | 40 | | ns | | |
| | 20 | | ns | | |
| | 60 | | ns | | |
| | Min 0.2 | Min Typ 0.2 1.4 0.2 1.5 40 20 | Min Typ Max 0.2 1.4 2 0.2 1.5 2 40 20 | Min Typ Max Units 0.2 1.4 2 μs 0.2 1.5 2 μs 40 ns ns 20 ns | |

DC Test Circuits

t_{THL}

^tPLH

t_{PHL}

Level Output

Level Output

Transition Time, High-to-Low

Propagation Delay Time

Low-to-High Level Output Propagation Delay Time

High-to-Low Level Output

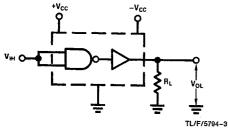
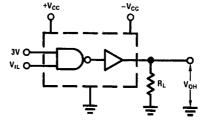


FIGURE 1. VIH, VOL

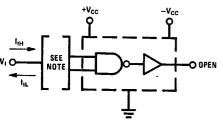


Each input is tested separately.

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ns

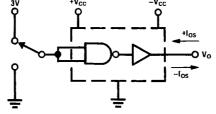
FIGURE 2. VIL, VOH



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Note: When testing $I_{\parallel H_1}$ the other input is at 3V; when testing $I_{\parallel L_1}$ the other input is open.

FIGURE 3. I_{IH}, I_{IL}



TL/F/5794-6

TL/F/5794-6 los is tested for both input conditions at each of the specified output conditions.

FIGURE 4. IOS

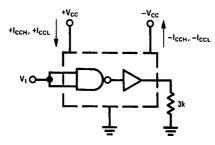


FIGURE 5. I_{CCH+}, I_{CCH-}, I_{CCL+}, I_{CCL-}

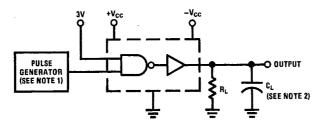
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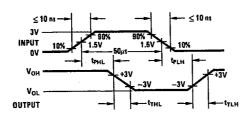
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AC Test Circuit and Switching Waveforms

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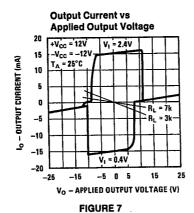
TL/F/5794-9

Note 1: The pulse generator has the following characterstics: duty cycle \leq 50%, Z_{OUT} \cong 50 $\!\Omega.$

Note 2: CL includes probe and jig capacitance.

FIGURE 6

Typical Performance Characteristics



TL/F/5794-10