



Digital Audio Clock Generator

Features

- Supports clock frequencies for digital audio applications
- On-chip loop filters for clock generation
- Low, short-term and long-term phase jitters
- Comes in miniature foot print package, while providing all PC audio clock requirements
- CMOS technology in 8-pin PDIP (300 mil) and SOIC (150 mil)
- 5V or 3.3V supply

Description

CH9420 is a dual PLL clock generator designed for digital audio applications. Four buffered fixed-frequency clocks are generated: a 14.318 MHz reference clock, a 33.868 MHz clock for the Yamaha OPL series music synthesizers, a 24.576 MHz clock, and a 16.934 MHz clock for stereo audio codecs, such as the CH6357.

Other digital audio applications include audio CD, DAT, and CD-ROM, as well as audio effects processors. CH9420 uses high performance, low power CMOS technology available in 8-pin PDIP and SOIC packages.

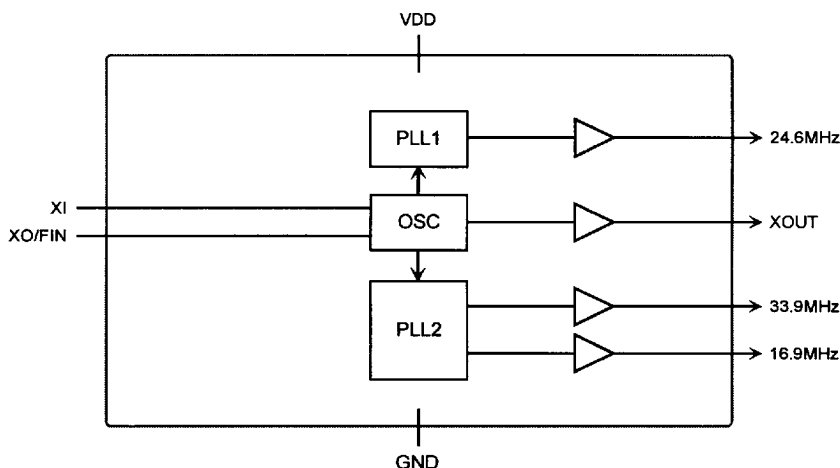


Figure 1: Block Diagram

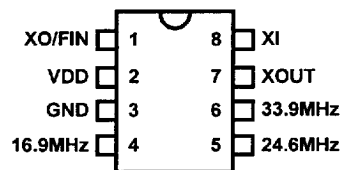


Figure 2: CH9420A

Table 1 • Pin Description CH9420A

Pin	Type	Symbol	Description
1	Out / In	XO / FIN	Crystal output or external FREF input
2	Power	VDD	5V or 3.3V supply
3	Power	GND	Ground
4	Out	16.9 MHz	16.934 MHz clock output
5	Out	24.6 MHz	24.576 MHz clock output
6	Out	33.9 MHz	33.868 MHz clock output
7	Out	XOUT	Buffered reference (14.318 MHz) clock output
8	In	XI	Crystal input

Table 2 • Absolute Maximum Ratings

Symbol	Description	Value	Unit
VDD	Power supply voltage with respect to GND	−0.5 to +7.0	V
VIN	Input voltage on any pin with respect to GND	−0.5 to VDD+0.5	V
TSTOR	Storage temperature	−55 to +150	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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Table 3 • DC Specifications (Operating Conditions: $T_A = 0^{\circ}\text{C} - 70^{\circ}\text{C}$, $V_{DD} = 5\text{V} \pm 5\%$)

Symbol	Description	Test Condition @ $T_A = 25^{\circ}\text{C}$	Min	Typ	Max	Unit
VOH	Output high voltage	$V_{DD} = 4.75\text{V}$, $I_{OH} = 4\text{mA}$	2.4			V
VOL	Output low voltage	$V_{DD} = 4.75\text{V}$, $I_{OL} = 8\text{mA}$			0.4	V
VIH	Input high voltage		2.0			V
VIL	Input low voltage				0.8	V
ILK	Input leakage current	Pin XI	−10		10	μA
CI	Input capacitance	Pins XO / FIN, XI		20		pF
IDD	Operating current	$V_{DD} = 5\text{V}$, No load		20		mA

Table 4 • AC Specifications (Operating Conditions: $T_A = 0^{\circ}\text{C} - 70^{\circ}\text{C}$, $V_{DD} = 5\text{V} \pm 5\%$)

Symbol	Description	Test Condition @ $T_A = 25^{\circ}\text{C}$	Min	Typ	Max	Unit
FXTAL	Crystal frequency			14.318		MHz
FIN	Input frequency		1	14.318	32	MHz
TIR	Input clock rise time				20	ns
TIF	Input clock fall time				20	ns
TR	Output clock rise time	15 pF load, $V_{OUT} = 0.8\text{V}$ to 2.0V			3	ns
TF	Output clock fall time	15 pF load, $V_{OUT} = 0.8\text{V}$ to 2.0V			3	ns
TDC	Duty cycle	15 pF load	40	50	60	%
TJCC	Jitter, cycle to cycle			50	150	ps
TPU	Power up time	From OFF to clocks stable		15		ms

Table 5 • DC Specifications (Operating Conditions: $T_A = 0^{\circ}\text{C} - 70^{\circ}\text{C}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Description	Test Condition @ $T_A = 25^{\circ}\text{C}$	Min	Typ	Max	Unit
V_{OH}	Output high voltage	$V_{DD} = 3.0\text{V}$, $I_{OH} = 1\text{mA}$	$V_{DD} - 0.5$			V
V_{OL}	Output low voltage	$V_{DD} = 3.0\text{V}$, $I_{OL} = 2\text{mA}$			0.5	V
V_{IH}	Input high voltage		2.0			V
V_{IL}	Input low voltage				0.8	V
I_{LK}	Input leakage current	Pin XI	-10		10	μA
CI	Input capacitance	Pins XO / FIN, XI		20		pF
I_{DD}	Operating current	$V_{DD} = 3.3\text{V}$, No load		15		mA

Table 6 • AC Specifications (Operating Conditions: $T_A = 0^{\circ}\text{C} - 70^{\circ}\text{C}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Description	Test Condition @ $T_A = 25^{\circ}\text{C}$	Min	Typ	Max	Unit
FXTAL	Crystal frequency			14.318		MHz
FIN	Input frequency		1	14.318	20	MHz
TIR	Input clock rise time				20	ns
TIF	Input clock fall time				20	ns
TR	Output clock rise time	15 pF load, $V_{OUT} = 0.8\text{V}$ to 2.0V			3	ns
TF	Output clock fall time	15 pF load, $V_{OUT} = 0.8\text{V}$ to 2.0V			3	ns
TDC	Duty cycle	15 pF load	40	50	60	%
TJCC	Jitter, cycle to cycle			50	150	ps
TPU	Power up time	From OFF to clocks stable		15		ms

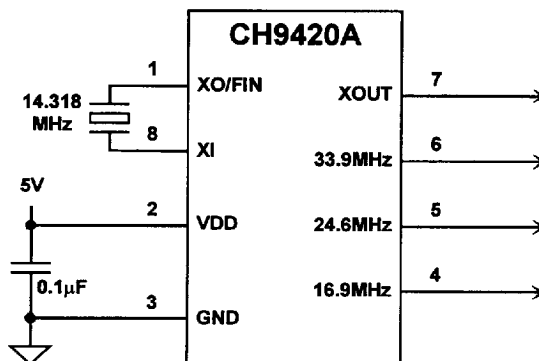


Figure 3: Application Schematic

ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH9420A-N	300 mil PDIP	8	5V
CH9420A-S	150 mil SOIC	8	5V
CH9420A-N-L	300 mil PDIP	8	3.3V
CH9420A-S-L	150 mil SOIC	8	3.3V