

December 1992

DESCRIPTION

The SSI 32P3030 is a low power pulse detector and servo demodulator designed for use in low power applications requiring +5V only power supplies. This device has a fully integrated bipolar circuit that detects and validates amplitude peaks in the output from a disk drive read amplifier, as well as detecting embedded servo information to provide position error signals used for read head positioning.

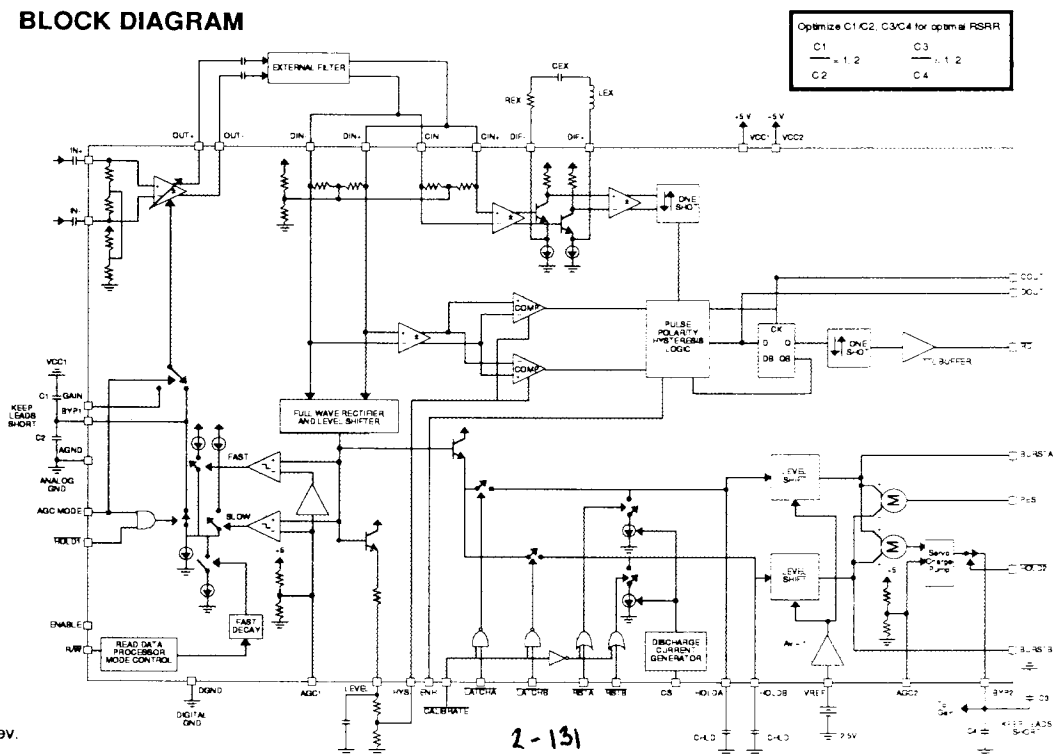
Time and amplitude qualification are used to provide a TTL compatible output that accurately duplicates the time position of input signal peaks. An AGC control loop, using a dual rate charge pump, provides a constant input amplitude for the level qualifier. Level qualification with or without hysteresis can be implemented as a fixed threshold or a constant percentage that tracks signal amplitude that enhances qualification during AGC loop transients.

(Continued)

FEATURES

- +5V only power supplies
- Wide bandwidth AGC Input amplifier
- Fast and slow AGC attack and decay regions for fast transient recovery
- Embedded servo channel provides servo burst capture and difference circuits
- Local sampled servo AGC provided based on servo burst output amplitude sum
- Write to Read transient suppression
- Dual mode pulse qualification with/without pulse polarity hysteresis for read/servo data retrieval.
- 24 Mbit/s operation

BLOCK DIAGRAM



1292 - rev.

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DESCRIPTION (Continued)

The Servo Demodulator consists of two peak detector channels that capture rectified servo data peaks. Buffered individual channel outputs are provided along with a difference output. Servo channel gain can be controlled by a sampled AGC signal based on maintaining the amplitude of the sum of both channels.

CIRCUIT OPERATION

READ MODE (R/\overline{W} pin high or open)

In Read Mode the SSI 32P3030 is used to process either data or servo signals. In the Data Read Mode the input signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks. In the Servo Read Mode the input signal is amplified and rectified and an error signal based on amplitude comparison is made available. Two servo burst channels are available that provide A & B burst levels.

DATA READ MODE (AGCMODE pin high or open)

An amplified head output signal is AC coupled to the $IN+$ and $IN-$ pins of the AGC amplifier. Gain control is accomplished by full wave rectifying and amplifying the $[(DIN+) - (DIN-)]$ voltage level and comparing it to a reference voltage level at the AGC1 pin.

The SSI 32P3030 contains a dual rate attack charge pump. The value of the attack current is dependent on the instantaneous level at $DIN\pm$. For signal levels above 125% of the desired level a fast attack mode is invoked that supplies a 1.4 mA charge current to the network on the $BYP1$ pin. Between 125% and 100% of the desired level the circuit enters a slow attack mode and supplies 0.18 mA of charge current to the $BYP1$ pin. This allows the AGC to rapidly recover during a write to read transition but reduces distortion once the AGC amplifier is within range.

Two decay modes are available and are automatically controlled within the device.

Upon a switch to write mode (R/\overline{W} pin low), the device will hold the gain at its previous value, and the AGC input stage is switched into a low impedance state. When the device is then switched back to read mode the AGC holds the gain and stays in the low impedance

state for 0.9 μs . It then switches into a fast/slow attack mode if the new gain required is less than the previously held gain or a fast decay mode if the gain required is more than its previous value. The fast decay current is 0.12 mA and stays on 0.9 μs . After the 0.9 μs time period the device stays in a steady state slow attack, slow decay mode. The slow decay discharge current is 4.5 μA .

The AGC1 pin is internally biased so that the target differential voltage input at $DIN\pm$ is 1.0 Vpp at nominal conditions. The voltage on this pin can be modified by tying a resistor between AGC and AGND or VCC1. A resistor to AGND decreases the voltage level, while a resistor to VCC1 increases it. The resulting AGC voltage level is shown in Figure 1;

Where:

V = Voltage at AGC1 with pin open (2.3V, nom.)

R_{int} = AGC1 pin input impedance (6.5 k Ω , typ.)

R_x = External resistor.

The new $DIN\pm$ input target level is nominally $(V_{AGC1} - 0.75) \cdot 0.64$ Vpp

The maximum AGC amplifier output swing is 2.6 Vpp at $OUT\pm$ which allows for up to 6 dB loss in any external filter between $OUT\pm$ and $DIN\pm$.

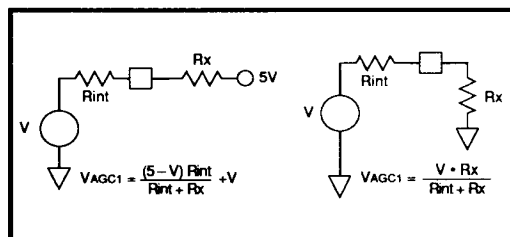


FIGURE 1: AGC Voltage

AGC gain is a linear function of the BYP1/Gain-pin voltage (VBYP1) as shown in Figure 2.

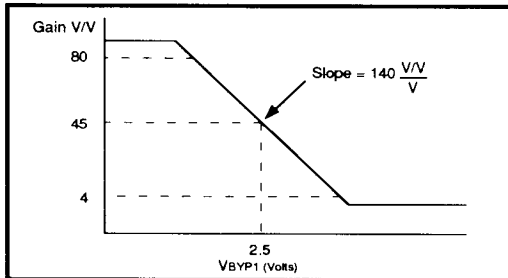


FIGURE 2: AGC Gain

The AGC amplifier has emitter follower outputs and can sink 4.0 mA.

One filter for both amplitude (DIN± input) and time (CIN± input) channels, or a separate filter for each may be used. If two filters are used, attention must be paid to time delays so that each channel is timed properly. A multi-pole Bessel filter is typically used for its linear phase or constant group delay characteristics.

In the amplitude channel the signal is sent to a hysteresis comparator. The hysteresis threshold level is set so that it will be tripped only by valid signal pulses and not by baseband noise. It can be a fixed level or a fraction of the DIN± voltage level.

The latter approach is accomplished by using an external filter/network between the LEVEL and HYS pins. This allows setting the AGC slow attack and decay times slow enough to minimize time channel distortion and setting a shorter time constant for the hysteresis level. The LEVEL pin output is a rectified and amplified version of DIN±, 1.0 Vpp at DIN± results in 1.0 Vop nominally, at the LEVEL pin. A voltage divider is used from LEVEL to ground to set the Hysteresis threshold at a percentage of the peak DIN± voltage. For example, if DIN± is 1.0 Vpp, then using an equal valued resistor divider will result in 0.5 Vop at the HYS pin. This will result in a nominal ±0.18V threshold or a 36% threshold of a ±0.5V DIN± input. The capacitor, from the LEVEL pin to GND, is chosen to set an appropriate time constant. This "feed forward" technique speeds up transient recovery by allowing qualification of the input pulses while the AGC is still settling. This helps in the two critical areas of write to read and head change

recovery. Some care in the selection of the hysteresis level time constant must be exercised so as to not miss pattern (resolution) induced lower amplitude signals. Note that there is a built in 50mV threshold (ie., 10% of ± 0.5V DIN± input) for level qualification even when the HYS pin is grounded. This is to prevent false triggering by baseband noise during a DC erase gap, (e.g., address mark). The output of the hysteresis comparator is the "D" input of a D-type flip-flop. The DOUT pin is a comparator output signal for testing purposes only. When testing, it requires an external 3-6 kΩ pull-down resistor to ground. If no testing is necessary, the DOUT pin can be pulled up to Vcc (+5V) to save power.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes. It also requires an external 3-6 kΩ pull down resistor for testing.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from CIN± to the comparator input (not DIF±) is:

$$A_v = \frac{-2000 C_s}{L C s^2 + C(R + 92) s + 1}$$

Where: C, L, R are external passive components

$$20 \text{ pF} < C < 150 \text{ pF}$$

$$s = j\omega = j2\pi f$$

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the CIN± input. Two qualification modes exist to determine peaks. The first mode, qualification with pulse polarity hysteresis, (ENH = High), is exactly the same as the qualification on the SSI 32P541. In this mode, the D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak. In the second mode, qualification without pulse polarity hysteresis, (ENH = Low), the polarity of the peaks is ignored. In this mode, the D input to the flip-flop changes state whenever the DIN± input exceeds the threshold regardless of polarity. This is accomplished, (see figure 3), by clocking the toggle flip-flop whenever the threshold is exceeded in either direction at the same time that the comparator detects a zero

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crossing. It may be advantageous to use this mode of pulse qualification for retrieving certain kinds of servo patterns.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched. The D flip-flop output triggers a one-shot that sets the \overline{RD} output pulse width.

SERVO READ MODE

A position error signal (PES) is generated based on the relative amplitude of two servo signals, A and B. Rectified servo signal peaks are captured on hold capacitors at the $\overline{HOLDA/B}$ pins. This is accomplished by pulling \overline{LATCHA} or \overline{LATCHB} low for a sample period. Additionally, a default hold capacitor discharge current of 1.5 mA can be turned on by pulling \overline{RSTA} or \overline{RSTB} low. This default 1.5 mA discharge current can be modified by tying a resistor between CS and GND or VCC1. A resistor to GND increases the discharge current, while a resistor to VCC1 decreases it. The equation for increasing the discharge current is:

$$I_{CS} = 22.5V \cdot \left(\frac{15k + R_{CS}}{15k \cdot R_{CS}} \right), \quad R_{CS} \geq 15 \text{ k}\Omega$$

For decreasing the discharge current, the equation is:

$$I_{CS} = 22.5V \cdot \left(\frac{R_{CS} - 22.5k}{15k \cdot R_{CS}} \right), \quad R_{CS} \geq 22.5 \text{ k}\Omega$$

Outputs $\overline{BURSTA/B}$ & PES are referenced to an external reference applied to the VREF pin.

In servo read mode (see Figure 4) the $\overline{BYP2}$ pin is connected to the GAIN pin and the servo channel gain is determined by the read channel gain as controlled by the sum of the A and B amplitudes. In this case a current is sourced/sunk to/from the capacitor on the $\overline{GAIN/BYP2}$ pin whenever the $\overline{HOLD2}$ pin is pulled high. The current magnitude and direction is determined by:

$$I_C = K_4[(K_5 \cdot V_{AGC2}) - V_a(\overline{DIN})_{pp} - V_b(\overline{DIN})_{pp}]$$

Where:

V_{AGC2} = AGC2 pin voltage = 2.3V with pin open.

K_4 = 640 $\mu A/V_{pp}$

K_5 = 0.50 V/V

$V_a/b(\overline{DIN})_{pp}$ = peak to peak A or B servo pattern signal voltages at \overline{DIN}

WRITE MODE

In Write Mode the SSI 32P3030 Pulse Detector section is disabled and preset for the following Read Mode. The digital circuitry is disabled, the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced to about 250 Ω .

Holding the AGC amplifier gain and reducing input impedance shortens system Write to Read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 32P3030 and a head preamplifier such as the SSI 32R4610AR. Write to read timing is controlled to maintain the reduced impedance for 0.9 μs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

MODE CONTROL

The device circuit mode is controlled by the \overline{ENABLE} , $\overline{R/W}$, $\overline{AGCMODE}$, $\overline{HOLD1}$ and $\overline{HOLD2}$ pins as shown in Table 1.

DATA READ MODE

AGC active and controlled by data, Digital section active.

DATA READ MODE, HOLD

AGC gain held constant, Digital section active. Gain will drift higher or lower at a rate determined by C_{BYP1} and Hold mode leakage current.

SERVO READ MODE I (See Figures 4 & 5)

The $\overline{BYP2}$ and GAIN pins are tied together. Read amplifier AGC control voltage developed from sum of Servo signal levels. $\overline{HOLD2}$ is toggled to update the control voltage after each Servo frame.

CALIBRATE MODE

A low level on $\overline{CALIBRATE}$ shall force \overline{LATCHA} and \overline{LATCHB} low and \overline{RSTA} and \overline{RSTB} high to measure the offset of the entire servo \overline{BURSTA} , \overline{BURSTB} , and PES channel.

WRITE

Read amplifier input impedance reduced. AGC gain held constant, \overline{RD} stays high.

POWER DOWN

Circuit switched to a low current disabled mode.

Note: When AGCMODE is switched to a low state the voltage at the BYP1 pin will be held constant subject to Hold mode leakage current induced drift. So, when returning to Data Read Mode, the channel gain will be the same as it was prior to AGCMODE switching or slightly higher/lower.

TABLE 1: SSI 32P3030 Circuit Mode Control

ENABLE	R/W	AGC MODE	HOLD1	HOLD2	READ PATH MODES
1	1	1	1	X	Data Read Mode
1	1	1	0	X	Data Read Mode Hold
1	1	0	X	1	Servo Read Mode - Sample
1	1	0	X	0	Servo Read Mode - Hold
1	0	X	X	X	Write
0	X	X	X	X	Power Down

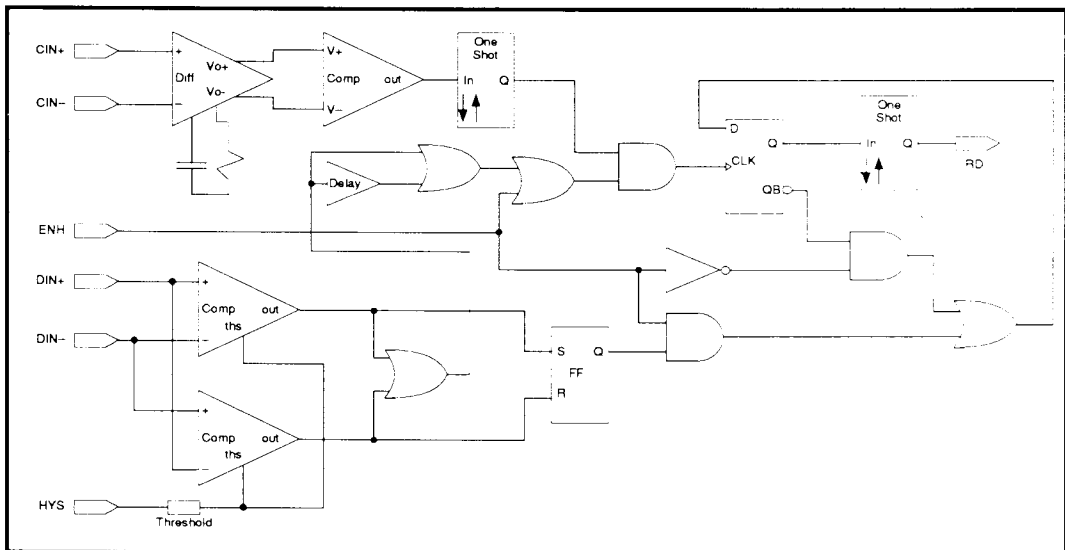


FIGURE 3: ENH Provides Two Pulse Qualification Modes.

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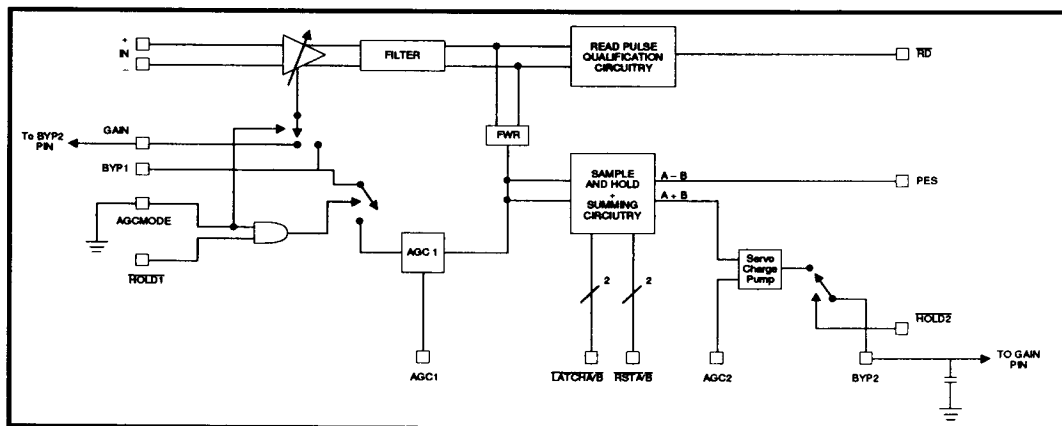


FIGURE 4: Servo Read Mode

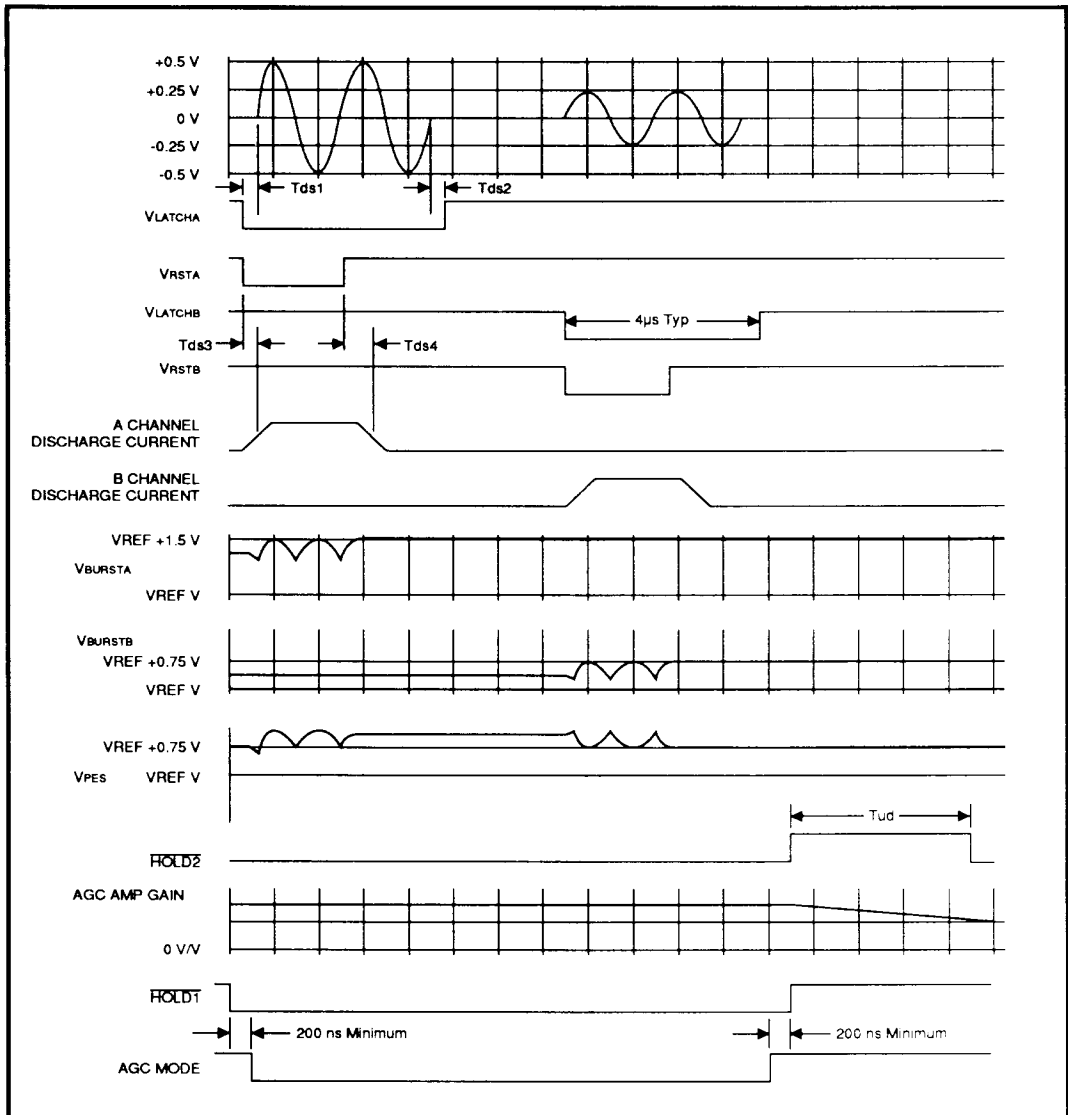


FIGURE 5: Servo Read Mode 1

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PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VCC1	I	Analog (+5V) power supply for pulse detector.
AGND	I	Analog ground pin for pulse detector block.
VCC2	I	Digital (+5V) supply pin for data synchronizer block.
DGND	I	Digital ground pin.
IN+, IN-	I	Analog signal input pins.
OUT+, OUT-	O	Read path AGC Amplifier output pins.
DIN+, DIN-	I	Analog input to the amplitude channel.
CIN+, CIN-	I	Analog input to the time channel.
DIF+, DIF-	I/O	Pins for external differentiating network.
COUT	O	Test point for monitoring the flip-flop clock input, pull-down resistor required.
DOUT	O	Test point for monitoring the flip-flop D-input, pull-down resistor required.
BYP1, BYP2	I/O	An AGC timing capacitor or network is tied between each pin and GND. BYP1 is for read data. BYP2 is for servo data.
AGC1, AGC2	I	Reference input voltage for the read data AGC loop. (AGC1) and sampled servo AGC loop (AGC2).
LEVEL	O	Output from fullwave rectifier that may be used for input to the hysteresis comparator.
HYS	I	Hysteresis level setting input to the hysteresis comparator.
HOLD1, HOLD2	I	TTL compatible pin that holds the AGC gain when pulled low.
LATCHA, LATCHB	I	TTL compatible inputs that switch channel A or B into peak acquisition mode when low.
RSTA, RSTB	I	TTL compatible input that enables the discharge of channels A & B hold capacitors when held low.
CS	I	Hold capacitor discharge current magnitude is controlled by a resistor from this pin to GND or VCC1. If left open the default current is 1.5 mA.
HOLDA, HOLDB	I/O	Peak holding capacitors are tied from each of these pins to AGND.
VREF	O	Reference voltage for Servo outputs.
BURSTA, BURSTB	O	Buffered hold capacitor voltage outputs.
PES	O	Position error signal, A minus B output.
R/W	I	TTL compatible Read/Write control pin. A low input selects write mode.
Enable	I	TTL compatible power up control. A low input selects a low power state.
AGCMODE	I	TTL compatible pin that selects the AGC loop control input. A high selects BYP1, a low selects GAIN.
Gain	I	A voltage at the pin may be used to control AGC gain.
RD	O	TTL compatible read output, a falling edge corresponds to a detected peak.
CALIBRATE	I	Used to measure servo offset.
ENH	I	TTL compatible pulse qualification control pin. A low input selects modes which ignore polarity of peaks.

ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING	UNIT
5V Supply Voltage, VCC1, VCC2	6.5	V
Pin Voltage (Analog pins)	.3 to VCC1 + .3	V
Pin Voltage (Digital pins)	.3 to VCC2 + .3 or +12 mA	V
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering 10 sec.)	260	°C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage (VCC1, VCC2)		4.5	5.0	5.5	V
Tj Junction Temperature		-		135	°C
Ambient Temperature	ENABLE = High or Low	0		80	°C

POWER SUPPLY

IVCC1,2 Supply Current	Outputs unloaded; ENABLE = high or open		76	110	mA
Pd Power dissipation	Ta = 25°C, outputs unloaded		380	570	mW
	ENABLE = Low		140	210	mW

LOGIC SIGNALS

VIL Input Low Voltage		-0.3		0.8	V
VIH Input High Voltage		2.0		VCC+0.3	V
IIL Input Low Current	VIL = 0.4V	0.0		-0.4	mA
IIH Input High Current	VIH = 2.4V			100	μA
VOL Output Low Voltage	IOL = 4.0 mA			0.5	V
VOH Output High Voltage	IOH = -400 μA	2.4			V

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MODE CONTROL

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Enable to/from Disable Transition Time	Settling time of external capacitors not included, ENABLE pin high to/from low			20	μ s
Read to Write Transition Time	R/ \overline{W} pin high to low			1.0	μ s
Write to Read Transition Time	R/W pin low to high AGC setting not included	0.4	0.9	1.6	μ s
AGC on to/from AGC off transition time	AGC mode pin high to/from low			2.0	μ s
HOLD1 ON to/from HOLD1 OFF transition time	HOLD1 pin high to/from low			1.0	μ s
HOLD2 ON to/from HOLD2 OFF	HOLD2 pin high to/from low			1.0	μ s

READ MODE (R/ \overline{W} is High)

AGC AMPLIFIER

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN \pm . OUT \pm are loaded differentially with 800 Ω , and each side is loaded with < 10 pF to AGND, and AC coupled to DIN \pm . A 900 pF capacitor is connected between BYP1/BYP2 and AGND. An 1100 pF capacitor is connected between BYP1/BYP2 and VCC1. AGC1/AGC2 pin is open.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Minimum Gain Range	1.0 Vp-p \leq (OUT+) - (OUT-) \leq 2.6 Vp-p	4		80	V/V
AGC Input Range		25		250	mVpp
Output Offset Voltage Variation	Over entire gain range	-500		+500	mV
Maximum Output Voltage Swing	Set by BYP1 pin	2.6			Vpp
Differential Input Resistance	(IN+) - (IN-) = 100 mVp-p @ 2.5 MHz	4	5.4	7.5	k Ω
Differential Input Capacitance	(IN+) - (IN-) = 100 mVp-p @ 2.5 MHz		4	10	pF
Single-Ended Input Impedance	R/ \overline{W} = high, IN+ or IN-	2	2.7	3.8	k Ω
	R/ \overline{W} = low, IN+ or IN-		160	250	Ω
Input Noise Voltage	Gain set to maximum, RS = 0, BW = 15 MHz		5	15	nV/ $\sqrt{\text{Hz}}$
Bandwidth	-3 dB bandwidth at maximum gain	30			MHz
OUT+ & OUT- Pin Current	No DC path to AGND	\pm 2.5	\pm 4.0		mA
CMRR (Input Referred)	(IN+) = (IN-) = 100 mVp-p @ 5 MHz, gain set to max	40			dB

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AGC AMPLIFIER (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT	
PSRR (Input Referred)	VCC1, 2 = 100 mVp-p @ 5 MHz, gain set to max	30			dB	
(DIN+) - (DIN-) Input Swing vs. AGC1 Input	K2 K1	25 mVp-p ≤ (IN+) - (IN-) ≤ 250 mVp-p, HOLD = high, 0.5 Vp-p ≤ (DIN+) - (DIN-) ≤ 1.5 Vp-p	.54 0.5	.64 0.75	.74 1.0	Vp-p/V V
(DIN+) - (DIN-) = (V _{AGC1} -K1) • K2						
(DIN+) - (DIN-) Input Voltage Swing Variation	25 mVp-p ≤ (IN+) - (IN-) ≤ 250 mVp-p			5.0	%	
AGC1 Voltage	AGC1 open	1.8	2.2	2.7	V	
AGC1 Pin Input Impedance		4.8	6.5	9.5	kΩ	
Slow AGC Discharge Current	(DIN+) - (DIN-) = 0V	2.8	4.5	6.5	μA	
Fast AGC Discharge Current	Starts at 0.9 μs after R/W goes high, stops at 1.8 μs	0.07	0.12	0.18	mA	
BYP1 Leakage Current	HOLD1 = low, 10 ≤ Gain ≤ 80	-0.2		+0.2	μA	
Gain Pin Leakage Current	HOLD2 = low, 10 ≤ Gain ≤ 80	-0.2		+0.2	μA	
Slow AGC Charge Current	(DIN+) - (DIN-) = .563 VDC, V _{AGC1} = 2.3 V	-0.11	-0.18	-0.27	mA	
Fast AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, V _{AGC1} = 2.3 V	-0.9	-1.4	-2.1	mA	
Fast to Slow Attack Switchover Point	$\frac{[(DIN+) - (DIN-)]}{[(DIN+) - (DIN-)]_{FINAL}}$	110		140	%	
Gain Decay Time (Td)	(IN+) - (IN-) = 250 mVp-p to 125 mVp-p @ 2.5 MHz, (OUT+) - (OUT-) to 90% final value	12	20	36	μs	
	(IN+) - (IN-) = 50 mVp-p to 25 mVp-p at 2.5 MHz (OUT+) - (OUT-) to 90% final value	38	60	110	μs	
Gain Attack Time	R/W low to high (IN+) - (IN-) = 250 mVp-p @ 2.5 MHz, (OUT+) - (OUT-) to 110% final value	.8	2	3.6	μs	

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HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC coupled, 1.0 Vp-p, 2.5 MHz sine wave. 0.5 VDC is applied to the HYS pin. R/W pin is high.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vp-p
Differential Input Resistance	(DIN+) - (DIN-) = 100 mVp-p @ 2.5 MHz	8	10	14	kΩ
Differential Input Capacitance	(DIN+) - (DIN-) = 100 mVp-p @ 2.5 MHz		3.0	5.0	pF
Single-Ended Input Impedance	DIN+ or DIN-	4	5	7	kΩ
Slope of Level Gain	Calculated from $0.6 < \text{DIN}_{\pm} < 1.5 \text{ Vppd}$.85	1	1.2	V/Vp-p
Intercept of Level Gain	$\text{DIN}_{\pm} = 0 \text{ Vppd}$	0	0.13	0.26	V
Level Gain		Slope + (Intercept / DIN ppd)			
Level Pin Output Impedance	$\text{I}_{\text{LEVEL}} = 0.2 \text{ mA}$	100	200	300	Ω
Level pin Maximum Output Current		1.5			mA
Slope of Hysteresis Gain	Calculated from $0.3\text{V} < \text{HYS} < 1.0\text{V}$	0.32	0.36	0.44	V/V
Intercept of Hysteresis Gain	$\text{HYS} = 0$	-0.04	-0.025	0	V
Hysteresis Gain		Slope + (Intercept / HYS Voltage)			
HYS Pin Current	$0.3\text{V} < \text{HYS} < 1.0\text{V}$	0.0		-5	μA
Tracking Hysteresis Threshold Tolerance		-15		+15	%
DOUT Pin Output Low Voltage	5 kΩ from DOUT to GND	VCC -2.5	VCC -2.0	VCC -1.35	V
DOUT Pin Output High Voltage	5 kΩ from DOUT to GND	VCC -2.0	VCC -1.6	VCC -1.1	V

ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input (CIN+) - (CIN-) is an AC-coupled, 1.0 Vp-p, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

Input Signal Range				1.5	Vp-p
Differential Input Resistance	(CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz	8	10	14	kΩ
Differential Input Capacitance	(CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz		3.0	5.0	pF
Single-Ended Input Impedance	CIN+ or CIN-	4	5	7	kΩ
Voltage Gain From CIN± to DIF±	(DIF+ to DIF-) = 2 kΩ		1		V/V
DIF+ to DIF- Pin Current	Differentiator impedance must be set so as to not clip the signal for this current level	±0.7			mA

ACTIVE DIFFERENTIATOR (Continued)

Unless otherwise specified, recommended operating conditions apply. Input (CIN+) - (CIN-) is an AC-coupled, 1.0 Vp-p, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
COUT Pin Output Low Voltage	5 kΩ from COUT to GND	VCC -2.5	VCC -2.0	VCC -1.35	V
COUT Pin Output High Voltage	5 kΩ from COUT to GND	VCC -2.0	VCC -1.6	VCC -1.1	V
COUT Pin Output Pulse Width		22	35	52	ns

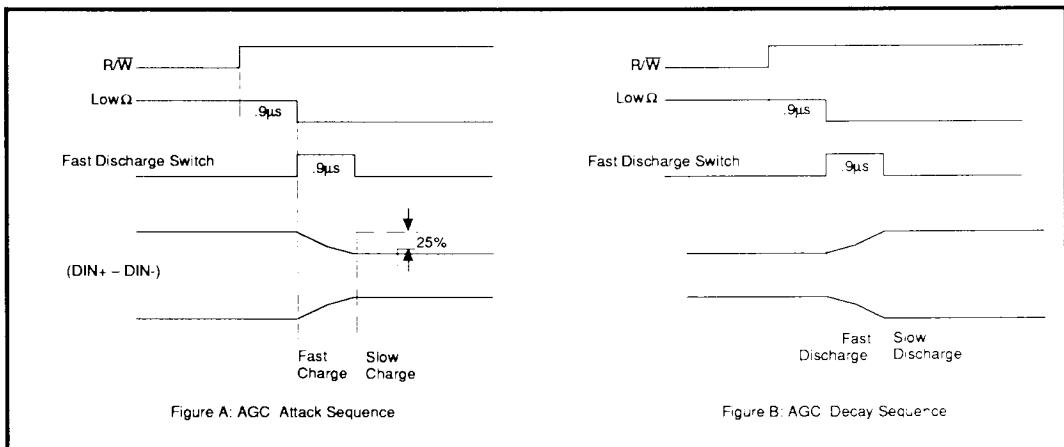


FIGURE 6: AGC Timing Diagram

OUTPUT DATA CHARACTERISTICS (See Figure 7)

Unless otherwise specified, recommended operating conditions apply. Inputs (CIN+) - (CIN-) and (DIN+) - (DIN-) are in-place as an AC coupled, 1.0 Vp-p, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin. \overline{RD} is loaded with a 4 kΩ resistor to VCC and a 10 pF capacitor to DGND. ENABLE and R/W pins are high.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Td1 D Flip-Flop Set Up Time	Minimum allowable time delay from (DIN+) - (DIN-) exceeding hysteresis point to (DIF+) - (DIF-) hitting a peak value.	0			ns
Td3 Propagation Delay			15	40	ns
Td3-Td4 Pulse Pairing	2.5 MHz sine wave input			1.5	ns
Td3-Td4 Pulse Pairing	4 MHz sine wave input			1.0	ns
Td5 Output Pulse Width		22	35	52	ns

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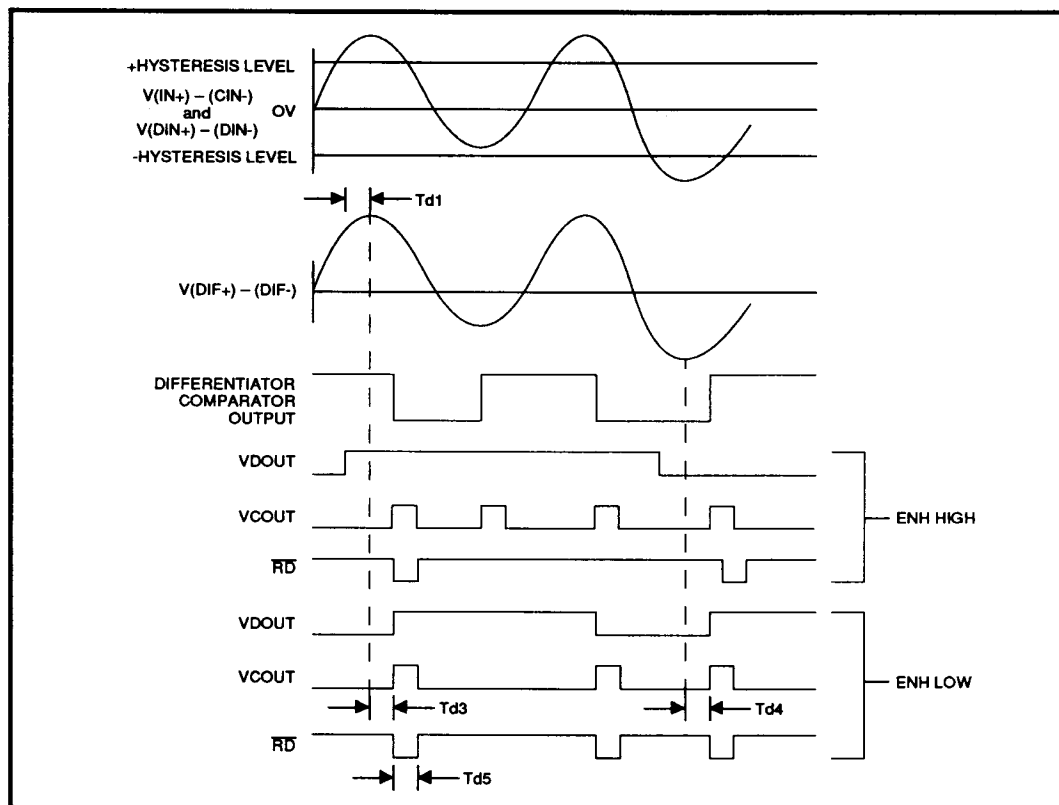


FIGURE 7: Read Mode Digital Section Timing Diagram

SERVO SECTION (Unless otherwise specified, recommended operating conditions apply.), LATCH A/B = Low, RST A/B = High, CS Pin Open

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VREF Voltage Range		2.25	2.5	2.75	V
VREF Pin Input Impedance		30			k Ω
AGC2 Pin Voltage	AGC2 Pin Open,	1.8	2.3	2.7	V
AGC2 Pin Input Impedance		4.8	6.5	9.5	k Ω
BURSTA/B pin Output Voltage vs (DIN+) - (DIN-)	LATCH A/B = Low $\frac{V_{BURSTA/B} - V_{REF}}{(DIN+) - (DIN-)} = 1.5V/V_{p-p}$	-20		+10	%

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SERVO SECTION (Continued)

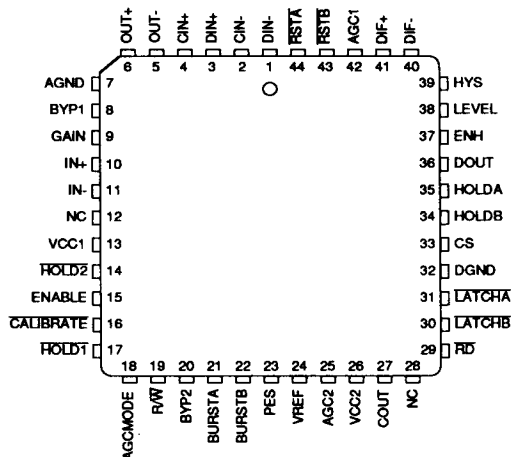
PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
BURSTA/B Output Offset Voltage $V_{BURST} - V_{REF}$	$I(HOLDA) = I(HOLDB) = -20 \mu A$, $LATCHA, \bar{B} = Low$ CS pin open (DIN+) = (DIN-)	-150		+150	mV
BURSTA - BURSTB Output Offset Match	$LATCHA/\bar{B} = low$ (DIN+) = (DIN-)	-15		+15	mV
Maximum PES Pin Output Voltage	Controlled by AGC2			$V_{CC1} - 1.5$	Vpp
PES Pin Output Offset Voltage	$V_{PES} - V_{REF}$, (DIN+) = (DIN-) $LATCHA/\bar{B} = Low$	-15		+15	mV
Output Resistance, BURSTA/B & PES pins	$I_{LOAD} \pm 500 \mu A$			50	Ω
Hold A/B Charge Current	$LATCHA/\bar{B} = Low$	8			mA
HOLDA/B Discharge Current Tolerance	$\bar{RSTA}/\bar{B} = Low$, CS pin open	0.8	1.5	2.2	mA
	$\bar{RSTA}/\bar{B} = High$, $LATCHA/\bar{B} = High$	-0.2		+0.2	μA
Load Resistance BURSTA/B, PES pins	Resistors to GND	10.0			k Ω
Load Capacitance BURSTA/B, PES pins				20	pF
$LATCHA/\bar{B}$ pin set up time	(Tds1 in Figure 5)	150			ns
$LATCHA/\bar{B}$ pin Hold Time	(Tds2 in Figure 5)	150			ns
Channel A/B Discharge Current Turn On time	(Tds3 in Figure 5)			150	ns
Channel A/B discharge Current Turn Off time	(Tds4 in Figure 5)			150	ns
BYP2 Pin Leakage Current	$HOLD2 = Low$	-0.2		+0.2	μA
BYP2 Pin Charge/Discharge Current $I_C = K_4[(K_5 \cdot V_{AGC2}) -$ $V_A(DIN)_{pp} - V_B(DIN)_{pp}]$	$K_4, \bar{HOLD2} = High$	400	640	880	$\mu A/V_{pp}$
	$K_5, \bar{HOLD2} = High$	0.4	0.5	0.7	V/V
Maximum BYP2 pin charge/discharge current		190	300	450	μA
V_{PES} pp vs. V_{AGC2}	$V_{PES} pp/V_{AGC2}$	1.18	1.33	1.5	V_{pp}/V
	V_{PES} pp Swing $AGC2 = Open$	2.4	3	3.6	Vpp

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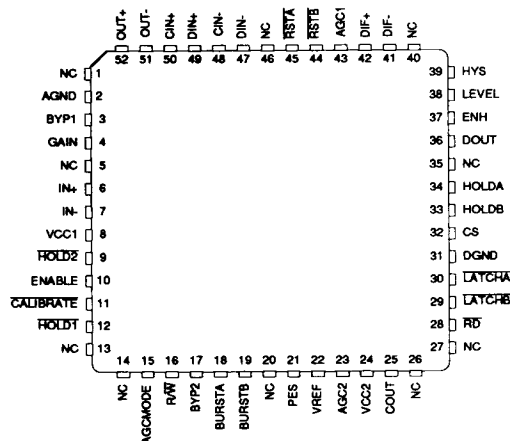
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PACKAGE PIN DESIGNATION (Top View)

CAUTION: Use handling procedures necessary
for a static sensitive component.



44-Pin PLCC



52-Pin QFP

THERMAL CHARACTERISTICS: θ_{JA}

44-Pin PLCC	60° C/W
52-Pin QFP	75° C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32P3030 44-Pin PLCC	32P3030-CH	32P3030-CH
SSI 32P3030 52-Pin QFP	32P3030-CG	32P3030-CG

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