ABRIDGED VERSION

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SSI 34P3201

Pulse Detector & Data Synchronizer, 250K to 8.0 Mbit/s

Preliminary Data

December 1993

DESCRIPTION

The SSI 34P3201 is a high performance pulse detector and data synchronizer integrated circuit. This device is designed for use in high density floppy storage applications. The pulse detection portion of this device detects and validates amplitude peaks output from a disk drive read amplifier. The data synchronization portion is a 1,7 RLL or MFM data synchronizer with window shift. The SSI 34P3201 supports a Sleep mode for minimal power dissipation in non-operational periods.

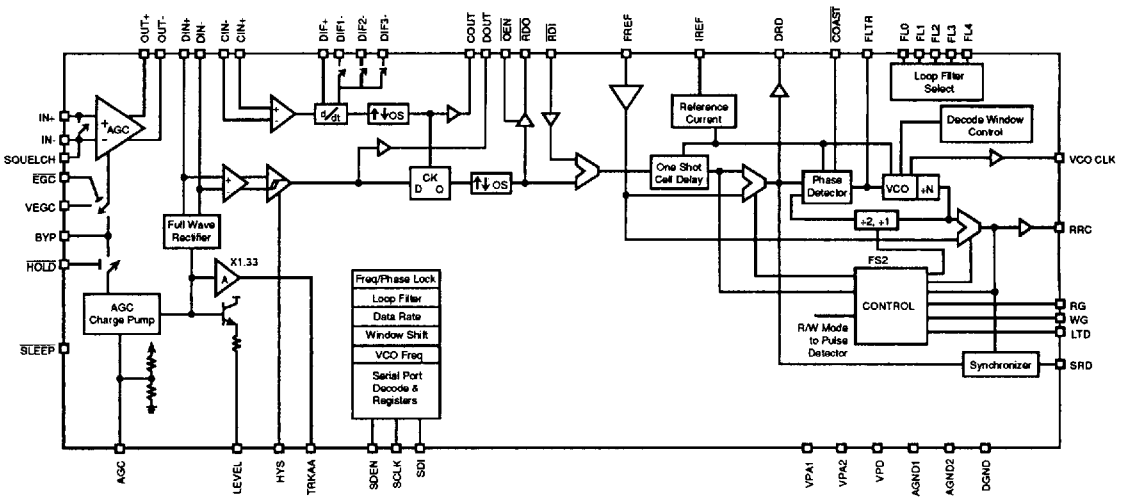
The SSI 34P3201 features a 3-pin serial port for easy selection of data rate and operating configurations.

The SSI 34P3201 is available in a 52-lead QFP package.

FEATURES

- **Highly Integrated Pulse Detector & Data Synchronizer**
- **Ideal for High Density Floppy Storage Applications**
- **Operating Data Rate: 250K to 8.0M NRZ bits per second selectable through the serial port**
- **Supports 1,7 RLL, MFM, FM, and GCR Encoding Format**
- **3-Pin Serial Port Programming: Data Rate Selection, Window Shift & Test Mode**
- **Fast Acquisition Phase Lock Loop & Zero Phase Restart Technique**
- **5V Operation only**
- **Low Operating Power**
- **Sleep Mode**

BLOCK DIAGRAM



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SSI 34P3201
Pulse Detector & Data Synchronizer, 250K to 8.0 Mbit/s

FUNCTIONAL DESCRIPTION

The SSI 34P3201 is a pulse detector and data synchronizer circuit. Its two main functions are:

- Validate and time-position preserve the analog pulses (IN±) from a read-write preamplifier.
- Extract the encoded data bit and its corresponding clock signal.

The SSI 34P3201 major functional blocks are:

- AGC amplifier & AGC control
- Pulse qualifier
- Data synchronizer
- Window shift
- Serial port decode & registers

AGC AMPLIFIER & AGC CONTROL

The AGC amplifier is to provide signal amplification prior to pulse qualification. The amplifier gain is a linear function of a gain control voltage, Figure 1. The gain control voltage is either the BYP voltage when $\overline{EGC}$ = logic high, or the VEGC voltage when $\overline{EGC}$ = logic low.

In the normal Read mode, i.e., with the AGC active, the DIN± input signal is regulated to a nominal level which is set by the voltage at the AGC pin. With the AGC pin open, the nominal DIN± level is 1 Vppd (peak-to-peak differential). This nominal DIN± level can be adjusted with an external resistor tied from the AGC pin to either VPA1 or AGND1, as shown in Figure 2. The DIN± voltage level is nominally 1.0 Vppd/V x V_{AGC}.

The AGC actions are current charging and discharging the external BYP integrating capacitor. They are described as follows:

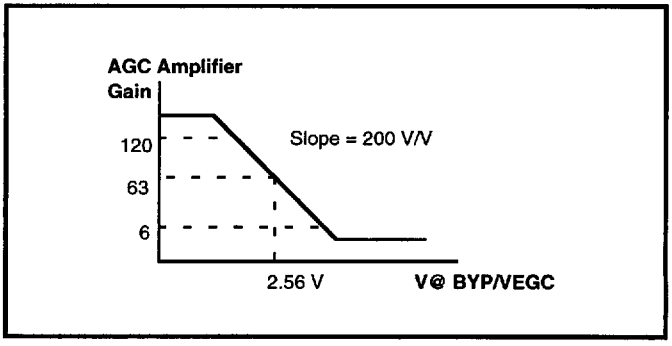

FIGURE 1: AGC Amplifier Gain vs. BYP/VEGC Voltage

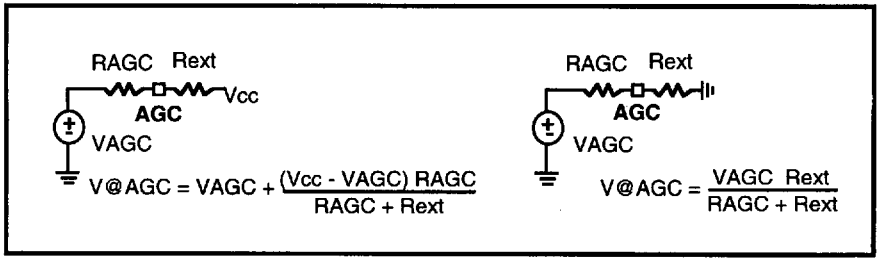

FIGURE 2: AGC Loop Reference Adjustment

Slow Decay 1 (R4, bit 0 = 0)

When the instantaneous DIN± signal is below the nominal level, a slow decay current, 4.5 µA, discharges the BYP capacitor. The AGC amplifier gain is increased slowly.

Slow Decay 2 (R4, bit 0 = 1)

When the instantaneous DIN± signal is below the nominal level, a slow decay current, 0.1 mA, discharges the BYP capacitor. The AGC amplifier gain is increased.

Slow Attack

When the instantaneous DIN± signal exceeds the nominal level but is below 125% of the nominal level, a slow attack current, 0.18 mA, charges the BYP capacitor. The AGC amplifier gain is decreased.

Fast Attack

When the instantaneous DIN± signal exceeds 125% of the nominal level, the device enters a Fast Attack mode. A fast attack current, 1.3 mA, charges the BYP capacitor. The AGC amplifier gain is quickly lowered.

Write-to-Read Recovery

With a logic high to logic low transition of the WG, the SSI 34P3201 enters the Write-to-Read Recovery mode except while SQUELCH is set to high. The input impedance remains in the low impedance state for 0.9 µs for fast input DC coupling recovery. The device then restores to high input impedance state, and enters into a Fast Decay mode for 0.9 µs. In the Fast Decay mode, a continuous 0.1 mA current discharges the BYP capacitor. The AGC amplifier gain is increased very quickly. This additional Fast Decay mode current is disabled when the Slow Decay 2 mode is active. Figure 3 shows the nominal write-to-read AGC action timing.

The AGC input impedance is also controlled by the SQUELCH pin. When SQUELCH is asserted high, the AGC input impedance becomes low impedance.

The above AGC actions, except that of write-to-read recovery, can be suspended with the $\overline{\text{HOLD}}$ = logic low. The AGC amplifier gain is then held constant, except for leakage effect.

With $\overline{\text{EGC}}$ = logic low, the AGC amplifier gain is determined by the VEGC voltage. With a fixed external DC voltage, or a second AGC control loop at the VEGC pin, the AGC amplifier gain is set independent of the on-chip AGC control loop, such as when read signal is over a servo demodulation field.

The AGC amplifier outputs are emitter follower outputs.

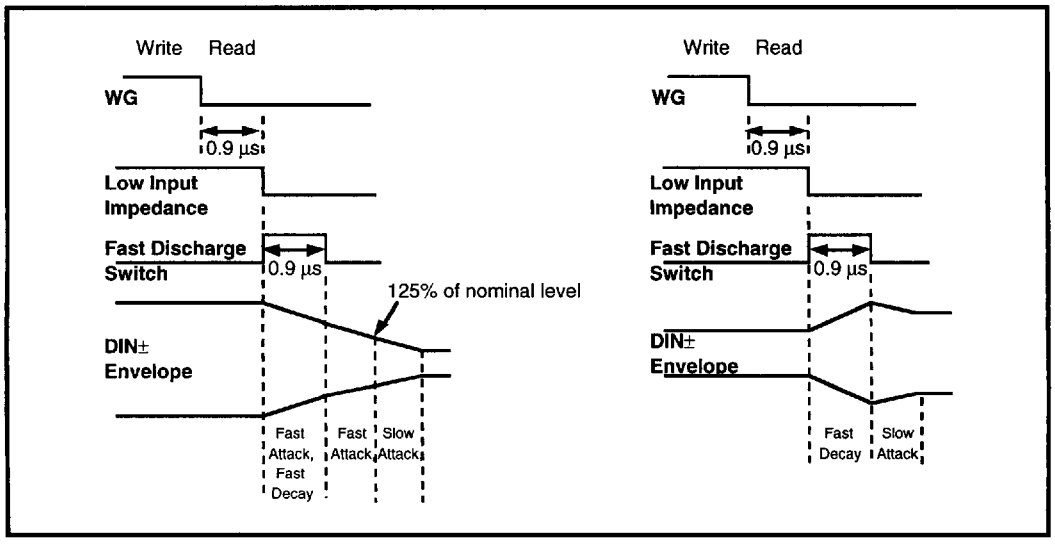

FIGURE 3: AGC Action Timing in Write-to-Read Recovery

FUNCTIONAL DESCRIPTION (continued)

PULSE QUALIFIER

The pulse qualifier validates each DIN± peak by a combination of level qualification and time qualification. In level qualification, a hysteresis comparator eliminates errors due to low level additive noise. In time qualification, the AGC amplifier output is time differentiated to locate the signal peaks in time.

Level Qualification

The level qualification is accomplished by comparing the DIN± signal with a set threshold. The SSI 34P3201 allows two ways of setting the thresholds: fixed threshold or DIN± tracking threshold. Fixed threshold can be simply set by a DC voltage at the HYS pin, such as a resistor from VPA1 to ground. The threshold at the comparator can be computed as: Hysteresis Gain x V@HYS. For high performance system application, however, DIN± tracking threshold is recommended.

DIN± tracking threshold has the advantage of shorter write-to-read recovery time and lower probability of error with input amplitude drop out. The threshold is designed as a percentage of the DIN± peak voltage. This technique can be implemented by feeding the LEVEL output, through a resistor divider, to the HYS pin. The LEVEL output, amplified peak capture of DIN± signal, can be computed as: Level Gain x DIN±ppd. With the resistor divider, a fraction of the LEVEL output is presented at the HYS pin. The threshold, as a function of DIN±, can be summarized as: Level Gain x Resistor Dividing Ratio x Hysteresis Gain x DIN±ppd. For a typical case of 1 Vppd DIN± signal, assume equal value resistors in the divider network, the threshold is 1 x 0.5 x 0.38 x 1 = 0.19V. This represents 38% threshold on a 1 Vppd signal. While both the Level Gain and the Hysteresis Gain bear a moderate tolerance due to typical process variation, they inversely track each other to yield a much tighter threshold accuracy in a closed loop.

While the external resistor divider ratio determines the qualification setting, the total resistance and the peak capture capacitor should be optimized for the system data rate. The RC time constant must be small enough to allow good response to changing DIN± peak, but large enough to provide a constant threshold after a long duration of input absence.

Time Qualification

Time qualification is used to locate DIN± peaks. With time differentiation, each DIN± peak is translated into a zero crossing, which clocks an on-chip flip-flop in the pulse qualifier. The SSI 34P3201 supports on-chip or off-chip differentiation.

ON-CHIP DIFFERENTIATION

The on-chip differentiation is accomplished by connecting an external RLC network across the DIF± pins. The DIF1-, DIF2-, and DIF3- pins are provided for wide code rate variation. These differentiators are selected by Register 4, bits 1 and 2. The DIN+ and CIN+ pins should be tied together, as well as the DIN- and CIN- pins.

OFF-CHIP DIFFERENTIATION

For constant density recording applications, a differentiation function with a low pass cut-off frequency tracking data rate can maximize the signal-to-noise ratio performance. A time differentiated input can be applied at the CIN± pins, separated from the DIN± pins. A 1.2 kΩ resistor should be placed across the DIF± pins.

This function can best be supported by the Silicon Systems programmable filters, such as the SSI 32F8030 and the SSI 32F8130/8131. The filters feature both a normal low pass output and a differentiated low pass output. The low pass cut-off frequency is programmable by the user to track the data rate. The signal delays of the two signal paths are well matched.

Qualified Read Data

Upon level and time qualification, a one-shot data pulse is generated for every validated peak of the DIN± signal. This read data pulse can be monitored at the $\overline{RDO}$ pin, when $\overline{OEN}$ = logic low. In high speed normal Read mode, it is recommended that the $\overline{RDO}$ output be disabled for lower noise performance with $\overline{OEN}$ = logic high. The pulse detector read data can be used as input to the data synchronizer. Alternately, external input at the $\overline{RDI}$ pin can be used as input to the data synchronizer.

Figure 4 summarizes the pulse detector function.

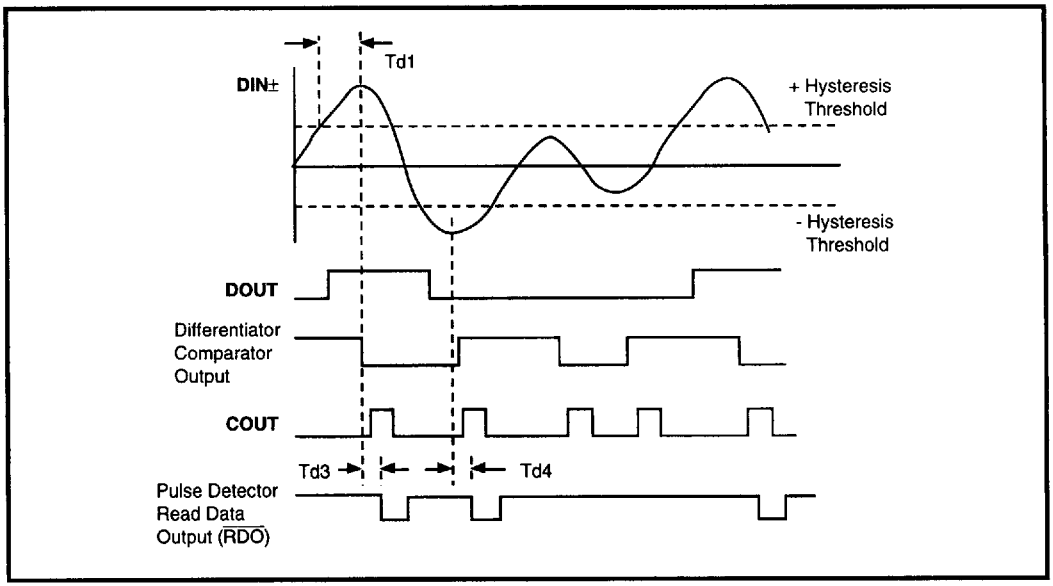

FIGURE 4: Read Mode Pulse Detector Timing Diagram

DATA SYNCHRONIZER

The data synchronizer is used to extract the clock and the encoded data signals from the read data signal. The input source to the data synchronizer can be from the pulse qualifier or from an external source via the $\overline{RDI}$ pin.

The SSI 34P3201 is designed to perform data synchronization for operating data rates of 250K to 8.0M NRZ bits per second. Data rates are selected through a combination of serial port register R0 for ÷N and serial port register R2 for VCO center frequency. The following is a partial list of possible data rates:

NRZ Data Rate	Encoding Format	VCO Freq	÷N	Code Clk (MHz)
8 Mbit/s	1,7 RLL	12	1	12.0
6 Mbit/s	MFM	12	1	12.0
4 Mbit/s	1,7 RLL	12	2	6.0
3.429 Mbit/s	1,7 RLL	10.286	2	5.143
3.2 Mbit/s	1,7 RLL	9.6	2	4.8
3.0 Mbit/s	1,7 RLL	9.0	2	4.5
2.667 Mbit/s	1,7 RLL	8.0	2	4.0
2.4 Mbit/s	MFM	9.6	2	4.8
1.6 Mbit/s	1,7 RLL	9.6	4	2.4
1.2 Mbit/s	MFM	9.6	4	2.4
1.0 Mbit/s	MFM	8.0	4	2.0
600 Kbit/s	MFM	9.6	8	1.2
500 Kbit/s	FM	8.0	8	1.0

DATA SYNCHRONIZER (continued)

For the 1,7 RLL format, the encoded bit rate, as well as the data synchronizer clock, is at 1.5 times the NRZ data rate. For the MFM encoding format, the encoded bit rate, as well as the data synchronizer clock, is at twice the NRZ data rate. Thus, the required data synchronizer clock rate is from 0.5 to 12 MHz.

To accommodate the wide data rate dynamic range, the SSI 34P3201 employs a novel data synchronizer phase locked loop (PLL) architecture (see Block Diagram). While the voltage controlled oscillator (VCO) operates only between 6 MHz to 12 MHz, a divide-down function is used to generate the lower frequency clocks.

With the serial register R0 programmed for a specific divide-down factor and serial register R2 programmed for a specific VCO center frequency, the SSI 34P3201 would decode the proper NRZ data rate. The 1/2 code cell delay duration is also set properly for each operating mode.

When the SSI 34P3201 is in the Idle mode, the VCO should lock to an external reference clock, FREF, which needs to be the same frequency as the VCO divided by N for proper operation.

The SSI 34P3201 employs a dual mode phase detector: Phase Lock mode and Frequency Lock mode. In the Read mode, the mode of the phase detector is programmable. With Fast Sync = logic low, the phase detector operates in the Phase Lock mode whereby the phase detector updates the PLL with each occurrence of a read data pulse from the pulse qualifier. With Fast Sync = logic high, the phase detector operates in the Frequency Lock mode. In the Write and Idle modes, the Frequency Lock mode phase detector is continuously enabled, thus maintaining both phase and frequency lock. Figure 5 shows the phase detector transfer function. By acquiring both phase and frequency lock to the FREF and utilizing a zero phase restart technique, false lock to the pulse detector read data is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. The charge pump gain during the PLL acquisition phase in the preamble area is controlled by LTD as shown in Figure 6. The selection of Frequency Lock mode (Fast sync 2: FS2) or Phase Lock mode (Fast sync 1: FS1) during preamble area is controlled through the serial port. The phase detector and charge pump output (high Z) are disabled when $\overline{\text{COAST}}$ is low.

Because of the wide data rate dynamic range, the SSI 34P3201 provides five high impedance/low impedance switchable nodes, FL0-4, for external loop filter component switching. The impedance of these FL0-4 nodes are controlled by register 2 bit 0 and register 3 bit 0-3. When the node is in high impedance state, the external component connected to this node is switched out. When the node is in low impedance state, the external component is included in the loop filter network.

The various operating modes of the data synchronizer are discussed in the Operation Modes section.

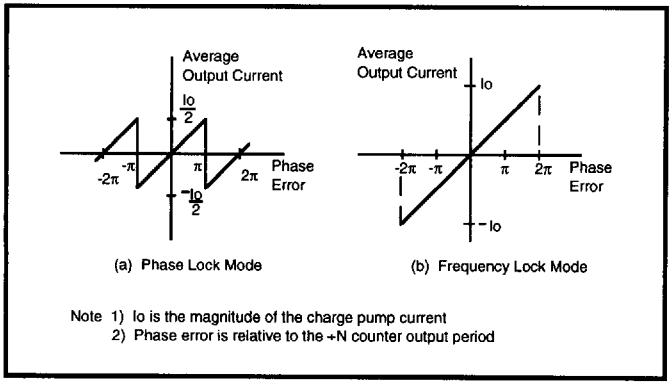

FIGURE 5: Phase Detector Transfer Function

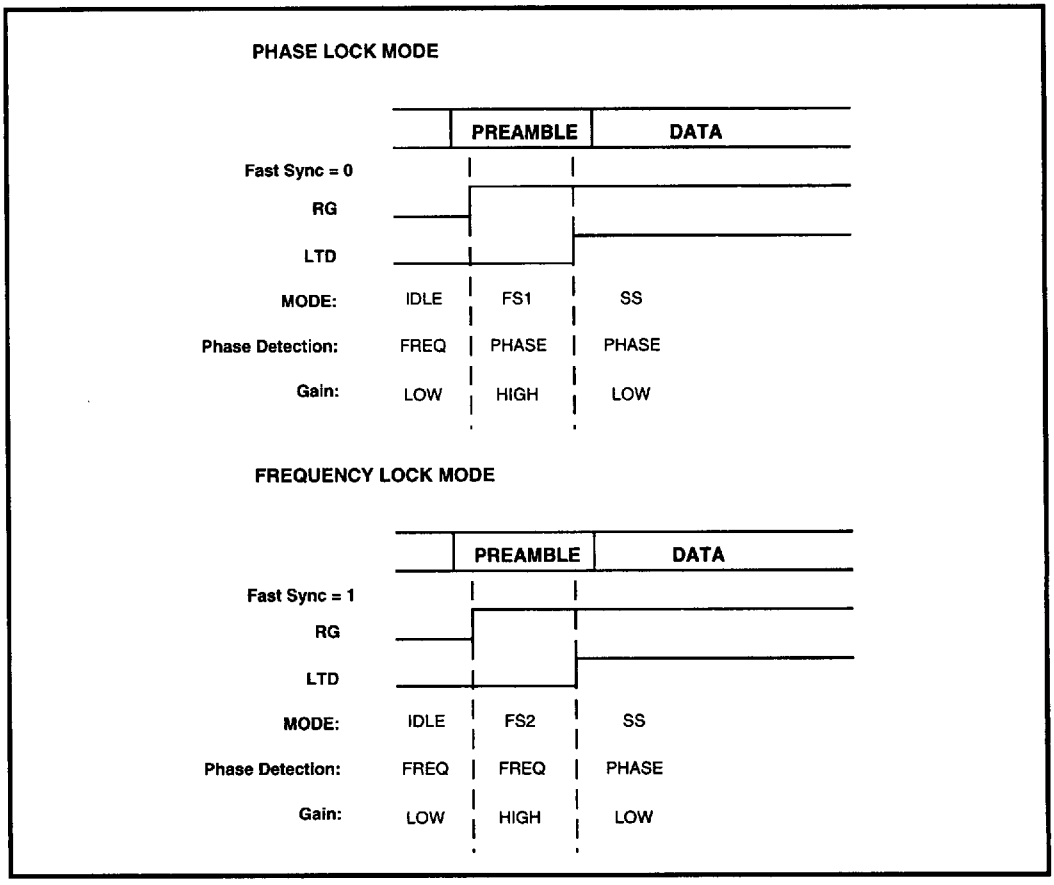

FIGURE 6: PLL Acquisition Mode During Preamble

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FUNCTIONAL DESCRIPTION (continued)

WINDOW SHIFT

To enhance the data decode function, the SSI 34P3201 supports a window shift function for code rates 3 Mbit/s and above. Shifting the pulse width of the ½ code cell delay output shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability, supported through serial register R1, easily facilitates defect mappings, automatic calibration, window margin testing, error recovery, and systematic error cancellation.

The window shift can be set to ±20%, ±30% or ±40% of the decode half window. Figure 7 defines the direction of the window shift. Refer to the Serial Port Decode & Registers section for serial port register assignment.

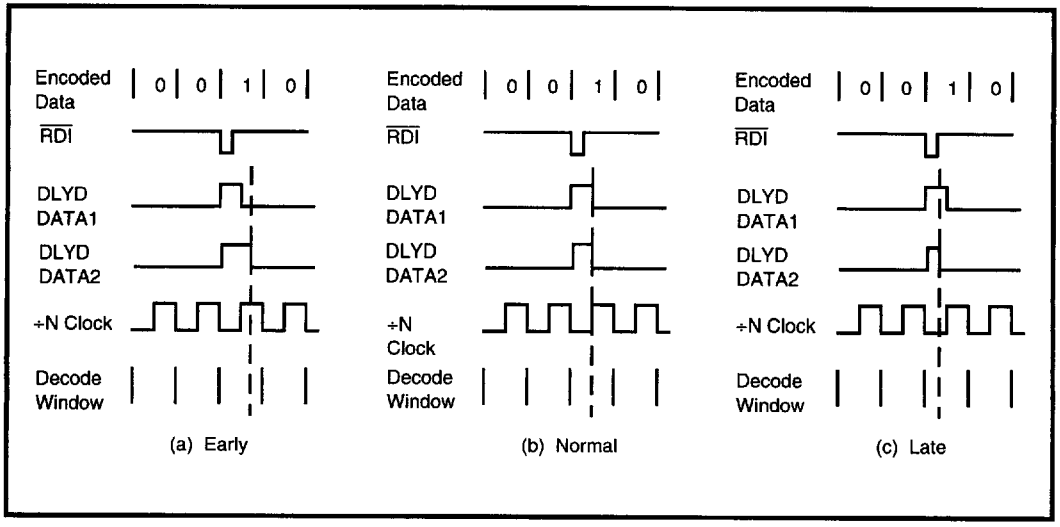

FIGURE 7: Decode Window & Window Shift Directions

SERIAL PORT DECODE & REGISTERS

The SSI 34P3201 provides a 3-pin serial port to facilitate the following digital controls:

- Phase/Frequency Lock mode (Register 0: Bit 3)
- N value (Register 0: Bits 2-0)
- Window shift (Register 1: Bits 3-0)
- VCO center frequency (Register 2: Bits 3-1)
- FL0-4 switch control (Register 2: Bit 0, Register 3: Bits 3-0)
- Data sychronizer input source (Register 4: Bit 3)
- DIF (Register 4: Bits 2 - 1)
- ISD (Register 4: Bit 0)

The 3 serial port pins are SDEN, SDI and SCLK. Figure 8 shows a timing diagram of the serial data transmission. Each data transmission consists of an 8-bit packet, Bit 7 being the most significant bit (MSB). The 8-bit packet is divided into two fields: Bit 7-4 address field, Bit 3-0 data field. All register bits are reset to 0 at power-up.

The register assignment is as follows:

Register 0 Address 0000

Bit 3 Fast Sync register

0 : Phase Lock mode (FS1)

1 : Freq Lock mode (FS2)

Bits 2, 1, 0 N register

0 0 0 : N = 1

0 0 1 : 2

0 1 0 : 4

0 1 1 : 8

1 X X : 16

Register 1 Address 0001 Window Shift

Bit 3

0 : Disable

1 : Enable

Bit 2

0 : Direction Early

1 : Direction Late

Bit 1, 0 Window shift magnitude

0 0 : 40% of half window

0 1 : 30% of half window

1 0 : 20% of half window

1 1 : 0% of half window

Register 2 Address 0010

Bits 3, 2, 1 VCO register

0 0 0 VCO center frequency = 6 MHz

0 0 1 VCO center frequency = 7 MHz

0 1 0 VCO center frequency = 8 MHz

0 1 1 VCO center frequency = 9 MHz

1 0 0 VCO center frequency = 10 MHz

1 0 1 VCO center frequency = 11 MHz

1 1 0 VCO center frequency = 12 MHz

1 1 1 VCO center frequency = 13 MHz

Bit 0 MSB of FL register

Register 3 Address 0011 FL0-4 Switch Control

Register 2	Register 3
Bit 0	Bits 3, 2, 1, 0
0	0 0 0 0 All off (All Hi Z)
x	x x x 1 FL0 on (FL0 : Low Z)
x	x x 1 x FL1 on (FL1 : Low Z)
x	x 1 x x FL2 on (FL2 : Low Z)
x	1 x x x FL3 on (FL3 : Low Z)
1	x x x x FL4 on (FL4 : Low Z)

Register 4 Address 0100 DIF and ISD Register

Bit 3 Data synchronizer input source

0 : From interanl pulse qualification output

1 : From the $\overline{\text{RDI}}$ pin

Bit 2, 1 DIF Register

0 0 : DIF1-

0 1 : DIF2-

1 0 : DIF3-

1 1 : Unused

Bit 0 ISD Register

0 : Slow Decay 1

1 : Slow Decay 2

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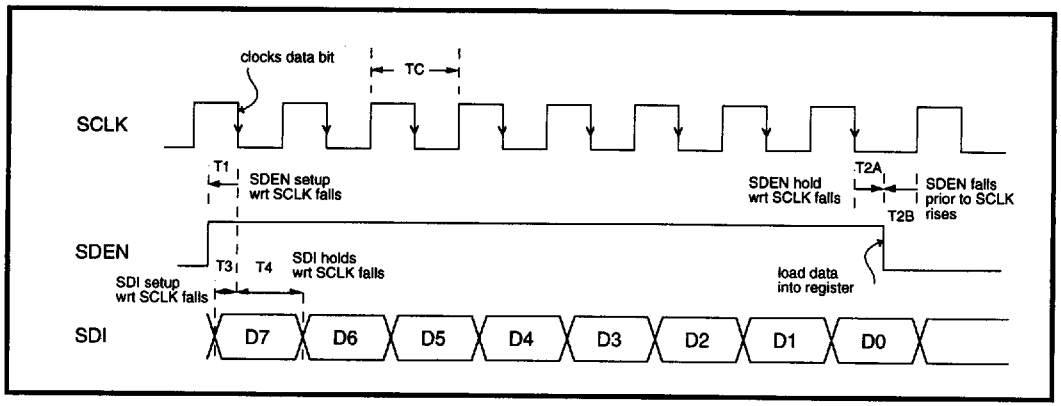

FIGURE 8: Serial Port Timing Diagram

OPERATION MODES

The SSI 34P3201 can support the following operating modes:

Mode	WG	RG	$\overline{\text{HOLD}}$	$\overline{\text{EGC}}$	$\overline{\text{SLEEP}}$	LTD
Idle VCO locked to FREF AGC active Frequency lock phase detection I charge pump X1 (KD2)	0	0	1	1	1	X
Idle VCO locked to FREF AGC gain held constant by BYP Frequency lock phase detection I charge pump X1 (KD2)	0	0	0	1	1	X
Idle VCO locked to FREF AGC gain held constant by VEGC Frequency lock phase detection I charge pump X1 (KD2)	0	0	X	0	1	X
Read VCO locked to Pulse Qualifier DLYD DATA AGC active Phase lock phase detection I charge pump X1 (KD2)	0	1	1	1	1	1

Mode	WG	RG	$\overline{\text{HOLD}}$	$\overline{\text{EGC}}$	$\overline{\text{SLEEP}}$	LTD
Read VCO locked to Pulse Qualifier DLYD DATA AGC gain held constant by BYP Phase lock phase detection I charge pump X1 (KD2)	0	1	0	1	1	1
Read VCO locked to Pulse Qualifier DLYD DATA AGC gain held constant by VEGC Phase lock phase detection I charge pump X1 (KD2)	0	1	X	0	1	1
Write AGC gain held constant by BYP Input impedance lowered VCO locked to FREF	1	X	X	1	1	X
Write AGC gain held constant by VEGC Input impedance lowered VCO locked to FREF	1	X	X	0	1	X
FS1 Serial port register 0, bit 3 = 0 VCO locked to preamble Phase lock phase detection I charge pump X3 (KD1)	0	1	X	X	1	0
FS2 Serial port register 0, bit 3 = 1 VCO locked to preamble Frequency lock phase detection I charge pump X3 (KD1)	0	1	X	X	1	0
Power Shutdown	X	X	X	X	0	X

OPERATION MODES (continued)

READ MODE

In the Read mode, the rising edge of DLYD DATA enables the phase detector while the falling edge is phase compared to the rising edge of the ÷N counter. As depicted in Figure 9, DLYD DATA is ½ code cell wide (TVCO / 2 / N) pulse whose leading edge is defined by the leading edge of Read Data. RRC is generated from the rising edge of the ÷N counter output. The accuracy of the ½ code cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of RRC.

In the Non-Read modes, the PLL is locked to FREF. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When RG transitions, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment in this manner (phase error ≤ 0.5 rads), the acquisition time is substantially reduced.

With the PLL in lock, the encoded data bit is re-synchronized before output to the SRD pin. Figure 10 shows the Read mode timing.

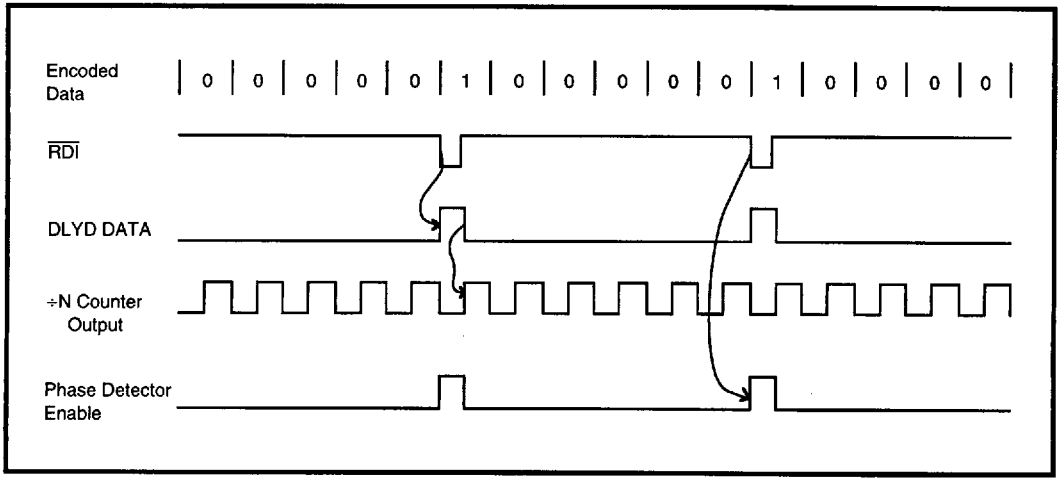

FIGURE 9: Data Synchronizer Timing

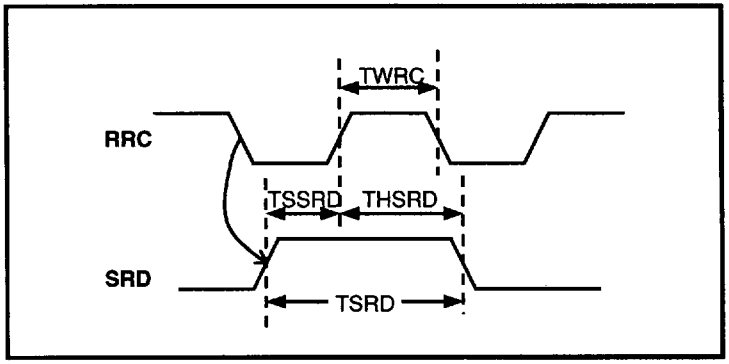

FIGURE 10: Read Mode Timing

WRITE MODE

In the Write mode, the SSI 34P3201 pulse detector is disabled and preset for the subsequent Read mode. The digital circuitry is disabled, the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced.

Holding the AGC amplifier gain and reducing input impedance shortens system write-to-read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 34P3201 and a head preamplifier such as the SSI 34R1203R. Write-to-read timing is controlled to maintain the reduced impedance for 0.9 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

POWER SHUTDOWN

For reduced power dissipation during non-operational periods, the SSI 34P3201 can be switched into a Sleep mode. The serial port registers will remain powered up during Sleep mode. Therefore no reprogramming is required following a logic low to logic high $\overline{\text{SLEEP}}$ transition.

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PIN DESCRIPTION

ANALOG INPUT PINS

NAME	TYPE	DESCRIPTION
IN+, IN-	I	AGC amplifier inputs.
DIN+, DIN-	I	Data inputs to hysteresis comparator and full-wave rectifier.
CIN+, CIN-	I	Data inputs to time-channel qualification.
HYS	I	Hysteresis input to establish the hysteresis threshold of the data comparator.
AGC	I	The voltage at the AGC pin determines the nominal level at the DIN± pins.
BYP	I	The voltage at the BYP pin controls the AGC amplifier gain when $\overline{EGC}$ = logic high.
VEGC	I	The voltage at the VEGC pin controls the AGC amplifier gain when $\overline{EGC}$ = logic low.

DIGITAL INPUT PINS

FREF	I	TTL reference clock input to data synchronizer.
$\overline{OEN}$	I	TTL $\overline{RDO}$ Output Enable input: $\overline{RDO}$ enabled with $\overline{OEN}$ = logic low, $\overline{RDO}$ forced to high with $\overline{OEN}$ = logic high.
$\overline{RDI}$	I	TTL external input source to the data synchronizer.
RG	I	TTL Read Gate input.
WG	I	TTL Write Gate input. Enables Write mode.
LTD	I	TTL Lock to Data asynchronous input.
$\overline{SLEEP}$	I	TTL power shutdown control. The device is in Power Shutdown mode when $\overline{SLEEP}$ = logic low. The device is in normal operational state when $\overline{SLEEP}$ = logic high, or left open.
$\overline{HOLD}$	I	TTL input that holds the AGC gain constant when pulled low. When left open, this input is at logic high.
$\overline{EGC}$	I	TTL input. When $\overline{EGC}$ = logic low, the AGC amplifier gain is controlled by the voltage at VEGC. When $\overline{EGC}$ = logic high, or left open, the AGC amplifier gain is controlled by the voltage at BYP.
SQUELCH	I	TTL input. The AGC input impedance is reduced when SQUELCH = logic high. When SQUELCH = logic low, the AGC input impedance is normal.
$\overline{COAST}$	I	TTL input. When $\overline{COAST}$ = logic low, the phase detector and charge pump output are disabled (high Z).
SDI	I	TTL Serial Data Input.
SCLK	I	TTL Serial Clock. Negative edge triggered clock input for serial register.
SDEN	I	TTL Serial Data Enable. A high level enables data loading. The data is latched on the falling edge of SDEN.

ANALOG OUTPUT PINS

NAME	TYPE	DESCRIPTION
OUT+, OUT-	O	AGC amplifier emitter follower output pins.
LEVEL	O	Open emitter output from fullwave rectifier that may be used for input to the HYS pin.
TRKAA	O	Open emitter output from fullwave rectifier with an additional gain of 1.333 over LEVEL.
FL0-4	O	Loop filter connection pins. Either high impedance or low impedance state.

ANALOG CONTROL PINS

DIF+, DIF1-, DIF2-, DIF3-	O	Pins for external differentiating network. When off-chip differentiator is used, a 1.2 kΩ resistor should be tied across DIF+ and DIFX-.
IREF	O	Input reference current for VCO bias. A 7.5 kΩ resistor should be tied between IREF and VPA2.
FLTR	O	Loop filter pin.

DIGITAL OUTPUT PINS

$\overline{RDO}$	O	TTL output of the pulse detector read data. This output is enabled with $\overline{OEN}$ = logic low. It is forced high with $\overline{OEN}$ = logic high.
RRC	O	Read Reference Clock: a multiplexed TTL clock source used by the controller. In the Read mode, this clock is the encoded bit rate. In the Write mode, it is FREF. No short clock pulses are generated during a mode change.
SRD	O	Synchronized Read Data: a TTL read data that has been re-synchronized to read clock.
COUT	O	Time qualification one-shot test point: open emitter output which requires an external 1 kΩ pull down resistor when used.
DOUT	O	Data comparator test point: open emitter output which requires an external 1 kΩ pull down resistor when used.
DRD	O	Delay Read Data test point: open emitter output which requires an external 5 kΩ pull down resistor when used.
VCO CLK	O	VCO test point: open emitter output which requires an external 5 kΩ pull down resistor when used.

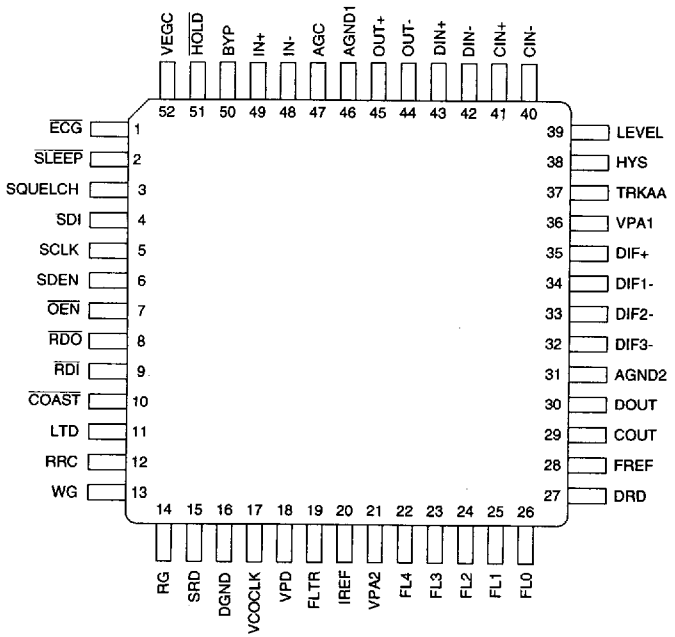
POWER & GROUND

VPA1	-	Analog supply to the pulse detector section.
VPA2	-	Analog supply to the data synchronizer section.
VPD	-	Digital supply.
AGND1	-	Analog ground to the pulse detector section.
AGND2	-	Analog ground to the data synchronizer section.
DGND	-	Digital ground.

SSI 34P3201
Pulse Detector & Data Synchronizer, 250K to 8.0 Mbit/s

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



52-Lead QFP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 34P3201 - 52-Lead QFP	34P3201-CG	34P3201-CG

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

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