SECTION 13

ELECTRICAL SPECIFICATIONS

This section contains the electrical specifications and associated timing information for the MC68HC11G5.

13.1 MAXIMUM RATINGS †

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	– 0.5 to 7.0	V
Input Voltage	V_{in}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Operating Temperature Range	T_A	T_L to T_H – 40 to 85	°C
Storage Temperature Range	T_{stg}	– 65 to 150	°C
Current Drain per Pin * Excluding V_{DD} and V_{SS}	I_D	25	mA

* One pin at a time, observing maximum power dissipation limits.

† This device contains protective circuitry against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (eg. either GND or V_{DD}).

13.2 THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Plastic	θ_{JA}	50	°C/W

13.3 POWER CONSIDERATIONS

The average chip junction temperature, T_J, in degrees Celsius can be obtained from the following equation:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A	=	Ambient temperature (°C)
θ_{JA}	=	Package thermal resistance, junction-to-ambient (°C/W)
P_D	=	$P_{INT} + P_{I/O}$
P_{INT}	=	Internal chip power = $I_{DD} \times V_{DD}$ (W)
$P_{I/O}$	=	Power dissipation on input and output pins (W) — user determined)

Note: For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) for any value of T_A.

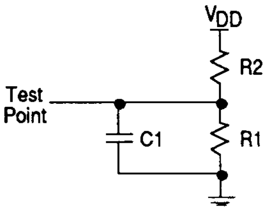
13.4 DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Output Voltage I_{Load} = ± 10.0µA (See Note 1)	All outputs All outputs except $\overline{RESET}$ and MODA	V_{OL} V_{OH}	— V_{DD} - 0.1	0.1 —	V
Output High Voltage I_{Load} = - 0.8mA, V_{DD} = 4.5V (See Note 1)	All outputs except $\overline{RESET}$, XTAL and MODA	V_{OH}	V_{DD} - 0.8	—	V
Output Low Voltage I_{Load} = 1.6mA	All outputs except XTAL	V_{OL}	—	0.4	V
Input High Voltage	$\overline{RESET}$ All inputs except $\overline{RESET}$	V_{IH} V_{IH}	0.8 x V_{DD} 0.7 x V_{DD}	V_{DD} V_{DD}	V
Input Low Voltage I_{Load} = 1.6mA	All Inputs	V_{IL}	—	0.8	V
I/O Ports, Three-state Leakage V_{in} = V_{IH} or V_{IL}	PA0-7, PC0-7, PD0-5, PG0-7, PH0-7, PJ0-3, MODA/$\overline{LIR}$, $\overline{RESET}$	I_{OZ}	—	±10	µA
Input Current V_{in} = V_{DD} or V_{SS}	All Inputs	I_{in}	—	±1.0	µA
RAM Standby Voltage	Powerdown	V_{SB}	2.0	V_{DD}	V
RAM Standby Current	Powerdown	I_{SB}	—	20	µA
Total Supply Current (See Note 2) RUN: Single-Chip Mode WAIT: (All Peripheral Functions Shut Down) Single-Chip Mode STOP: (No Clocks) Single-Chip Mode	 I_{DD}(run) I_{DD}(wait) I_{DD}(stop)	I_{DD}	 — — —	 30 15 100	 mA mA µA
Input Capacitance	$\overline{IRQ}$, $\overline{XIRQ}$, EXTAL MODA/$\overline{LIR}$, $\overline{RESET}$, all Ports except Port E	C_{in} C_{in}	— —	12 12	pF pF

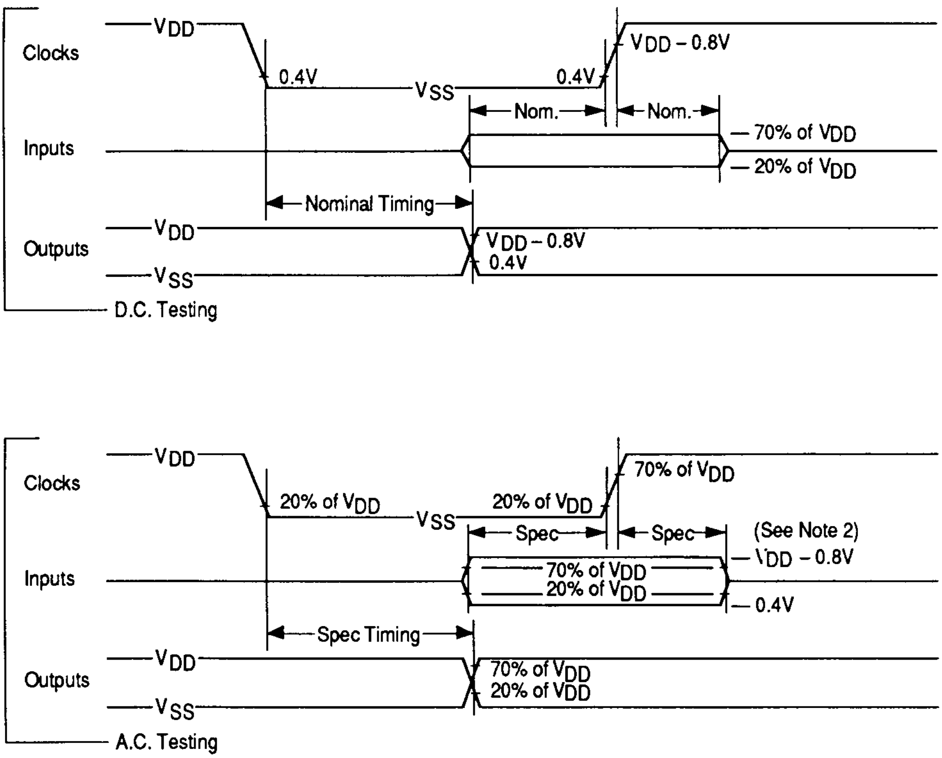
NOTES:

1. V_{OH} specification for $\overline{RESET}$ and MODA is not applicable because they are open-drain pins.
   V_{OH} specification is not applicable to ports C and D in wired-OR mode.
2. All ports configured as inputs,
   $V_{IL} \leq 0.2V$,
   $V_{IL} \geq V_{DD} - 0.2V$,
   No dc loads,
   EXTAL is driven with a square wave, and
   t_{cyc} = 476.5ns.



Equivalent Test Load [1]

Pins	R1	R2	C1
PA0-7, PB0-7, PC0-7, PD0, PD5, PF0-7, PG0-7, PH0-7, PJ0-3, E, R/$\overline{W}$	3.26kΩ	2.38kΩ	90pF
PD1-PD4	3.26kΩ	2.38kΩ	200pF



Notes: 1. Full test loads are applied during all DC electrical tests and AC timing measurements.

2. During AC timing measurements, inputs are driven to 0.4 volts and VDD – 0.8 volts while timing measurements are taken at the 20% and 70% of VDD points.

Figure 13-1. Test Methods

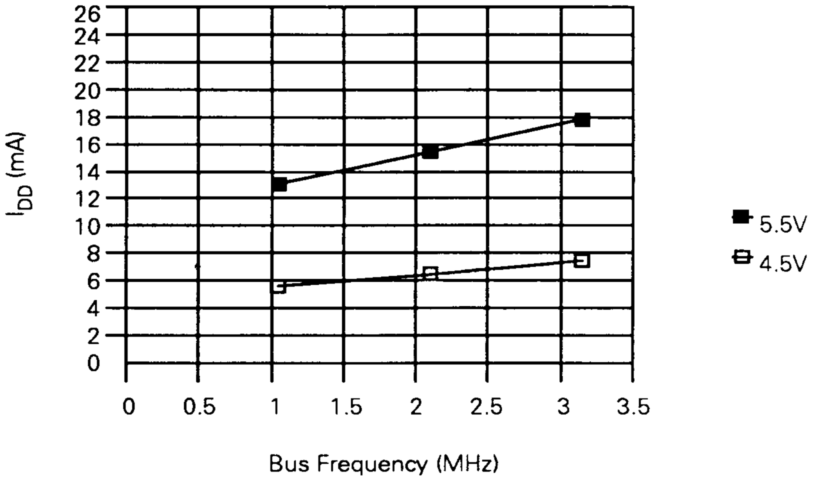


Figure 13-2. Run I_{DD} vs Bus Frequency (Single Chip Mode – 4.5V, 5.5V)

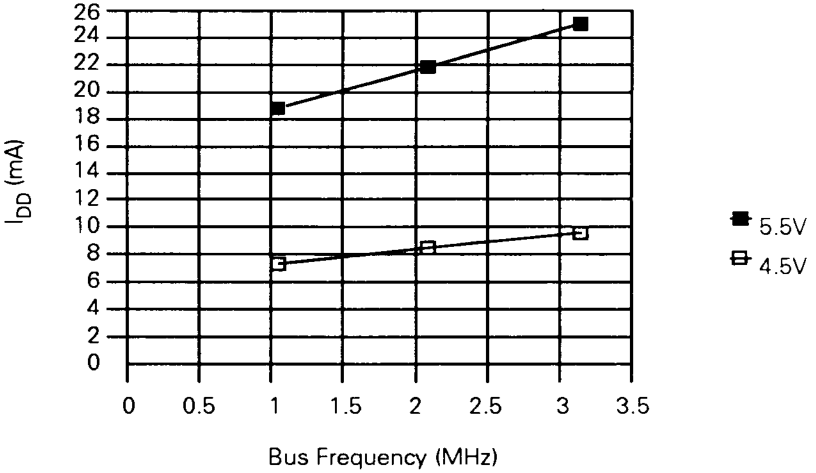


Figure 13-3. Run I_{DD} vs Bus Frequency (Expanded Mode – 4.5V, 5.5V)

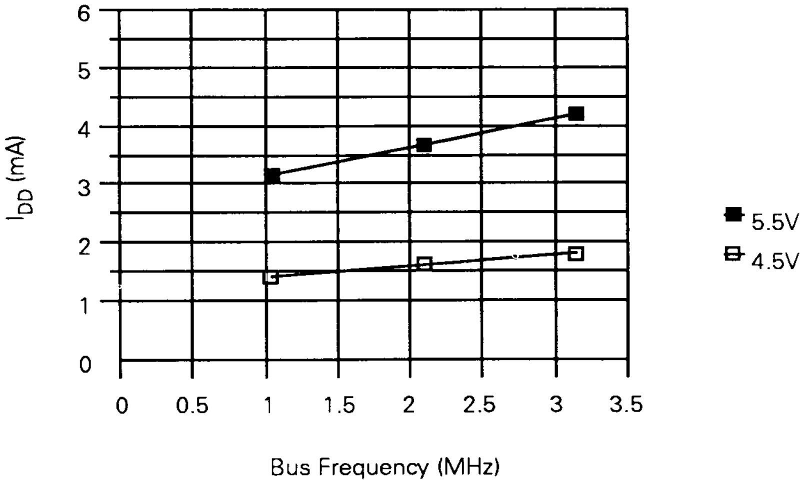


Figure 13-4. Wait I_{DD} vs Bus Frequency (Single Chip Mode – 4.5V, 5.5V)

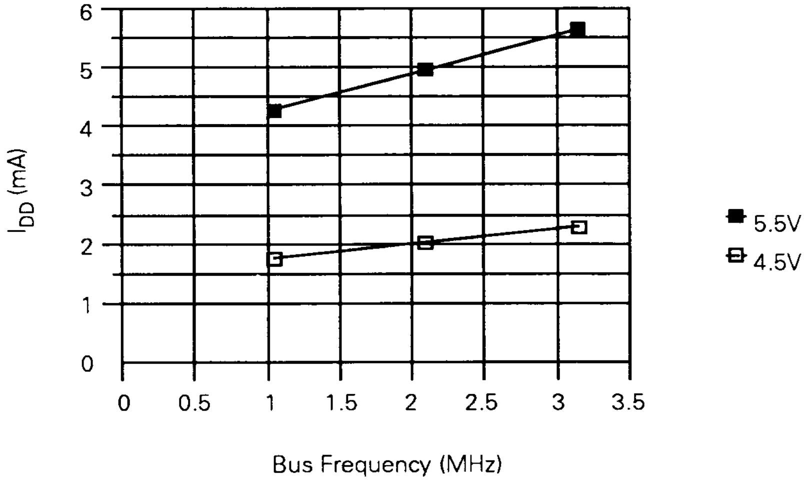


Figure 13-5. Wait I_{DD} vs Bus Frequency (Expanded Mode – 4.5V, 5.5V)

13.5 CONTROL TIMING

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
External Oscillator Frequency	Crystal option	f_{XTAL}	—	8.4	MHz
	External clock option	$4f_o$	DC	8.4	MHZ
Internal Operating Frequency	Crystal ($f_{XTAL}/4$)	f_o	—	2.1	MHz
	External clock	f_o	DC	2.1	MHZ
Cycle Time	All outputs except XTAL	t_{cyc}	476	—	ns
Crystal Oscillator Startup Time		t_{OXOV}	—	100	ms
Stop Recovery Startup Time	DLY = 0	t_{SRS}	—	4	t_{cyc}
	DLY = 1	t_{SRS}	—	4064	t_{cyc}
Wait Recovery Startup Time		t_{WRS}	—	4	t_{cyc}
Reset Input Pulse Width (See Note 1)		t_{RLRH}			t_{cyc}
	(To guarantee external reset vector)		8	—	
	(Minimum input time; may be pre-empted by internal reset)		1	—	
Mode Programming	Setup time	t_{MPS}	2	—	t_{cyc}
	Hold time	t_{MPH}	0	—	ns
Interrupt Pulse Width, $\overline{IRQ}$ Edge Sensitive Mode	$t_{ILIH} = t_{cyc}$ + 20ns	t_{ILIH}	496	—	ns
Interrupt Pulse Period		t_{ILIL}	Note 2	—	t_{cyc}
Processor Control					
$\overline{RESET}$, WAIT, $\overline{IRQ}$	(t_{PCS} = 1/4 t_{cyc} - 50ns)	t_{PCS}	69	—	ns
MRDY		t_{PCS}	50	—	ns
HALT	(t_{PCS} = 1/4 t_{cyc} + 20ns)	t_{PCS}	170	—	ns
Bus Tri State Enable	(t_{TSE} = 1/4 t_{cyc} + 40ns)	t_{TSE}	—	159	ns
Bus Tri State Disable		t_{TSD}	—	65	ns

NOTES:

1. $\overline{RESET}$ will be recognised during the first clock cycle it is held low. Internal circuitry then drives the pin low for four clock cycles, releases the pin, and samples the pin level two cycles later to determine the source of the interrupt.
2. The minimum period t_{ILIL} should not be less than the number of cycles it takes to execute the interrupt service routine plus 21 t_{cyc}.
3. All timing is shown with respect to 20% V_{DD} and 70% V_{DD} unless otherwise noted.

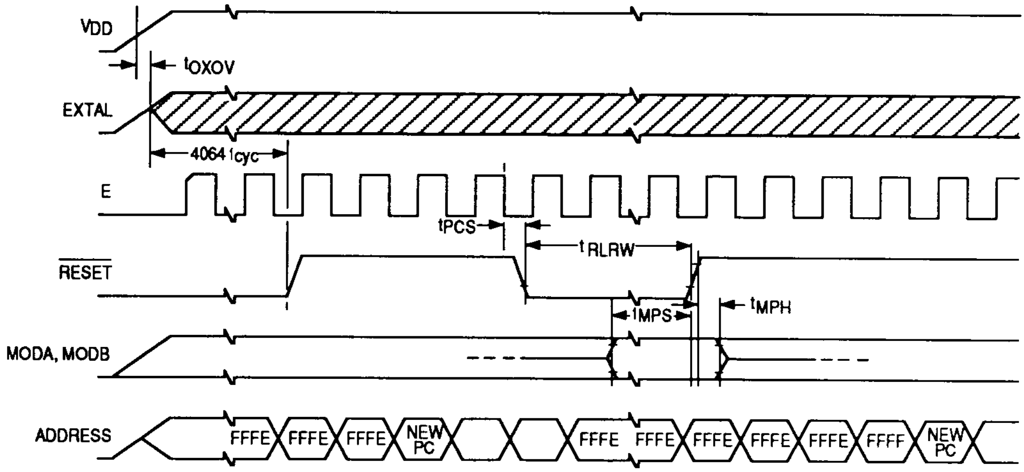


Figure 13-6. POR External RESET Timing Diagram

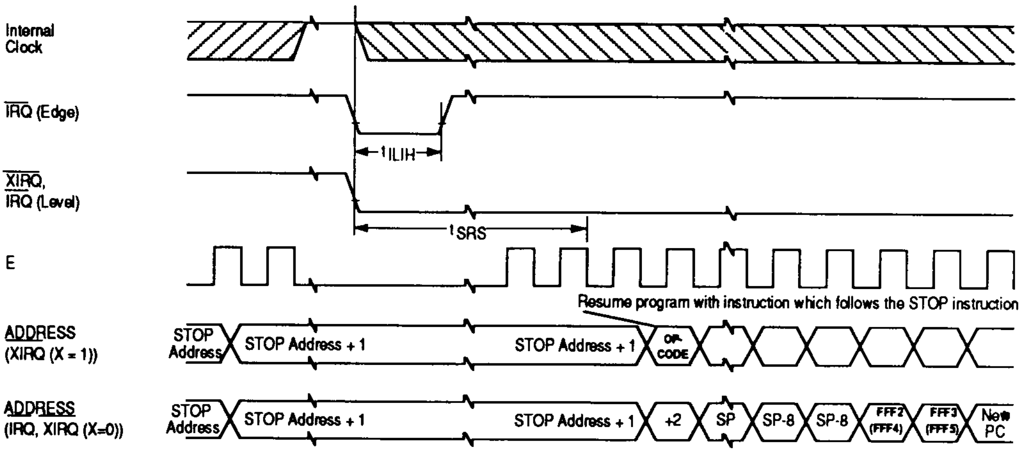


Figure 13-7. STOP Recovery Timing Diagram

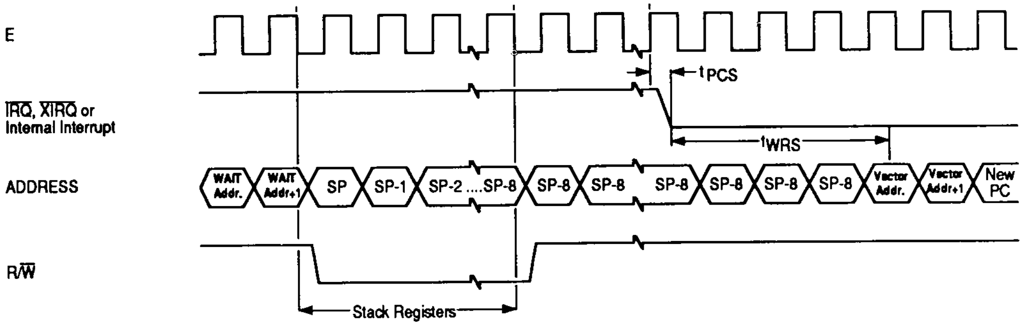


Figure 13-8. WAIT Recovery from Interrupt Timing Diagram

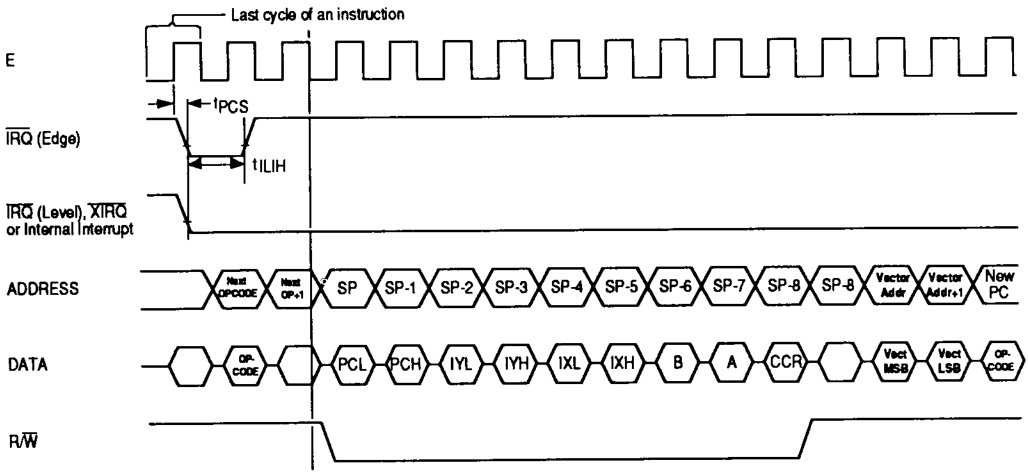


Figure 13-9. Interrupt Timing Diagram

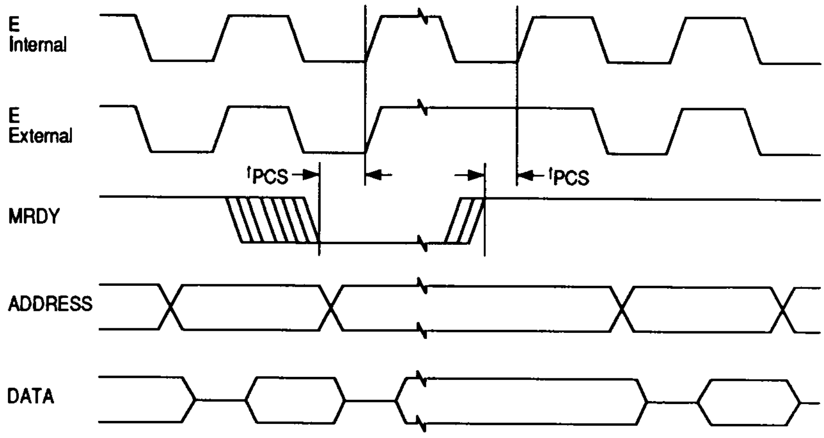


Figure 13-10. Memory Ready Timing Diagram

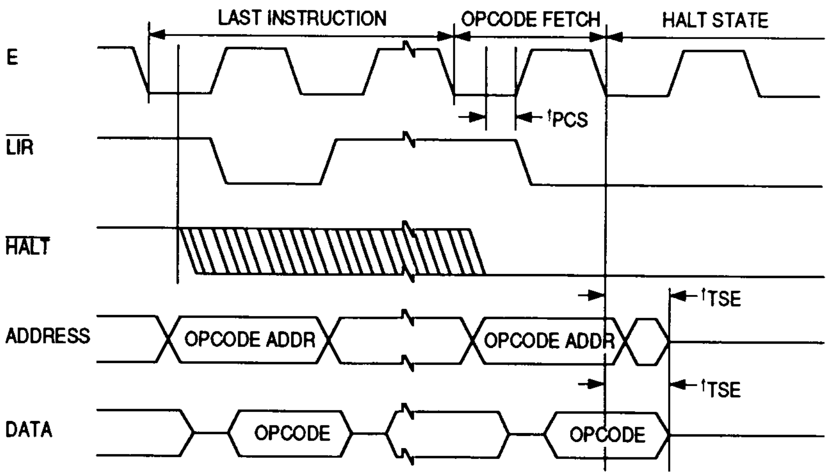


Figure 13-11. Entering HALT

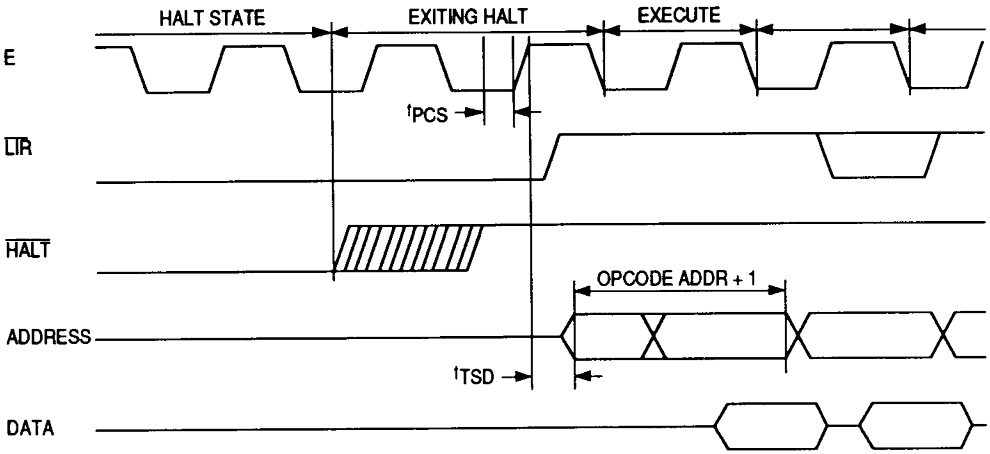


Figure 13-12. Exiting HALT

13.6 PERIPHERAL PORT CHARACTERISTICS

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation (E Clock)	f_o	—	2.1	MHz
E Clock Period	t_{cyc}	476	—	ns
Peripheral Data Setup Time				
Port A, C, D, J	t_{PDSU}	100	—	ns
Port E	t_{PDSU}	100	—	ns
Port G, H (t_{PDSU} = -1/4 t_{cyc} + 93ns)	t_{PDSU}	– 26	—	ns
Peripheral Data Hold Time				
Port A, C, D, J	t_{PDH}	80	—	ns
Port E	t_{PDH}	80	—	ns
Port G, H (t_{PDH} = 1/4 t_{cyc} + 130ns)	t_{PDH}	249	—	ns
Delay Time, Peripheral Data Write				
Port J1, J2, A3, A4, A5, A6, A7	t_{PWD}	—	150	ns
Port B, C, D, F, G, H, A0, A1, A2, J0, J3 (t_{PWD} = 1/4 t_{cyc} + 90ns)	t_{PWD}	—	209	ns

NOTES:

1. All timing is shown with respect to 20% V_{DD} and 70% V_{DD} unless otherwise noted.

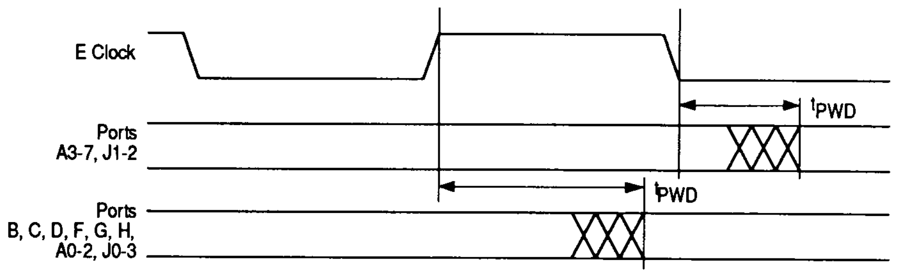


Figure 13-13. Port Write Timing Diagram

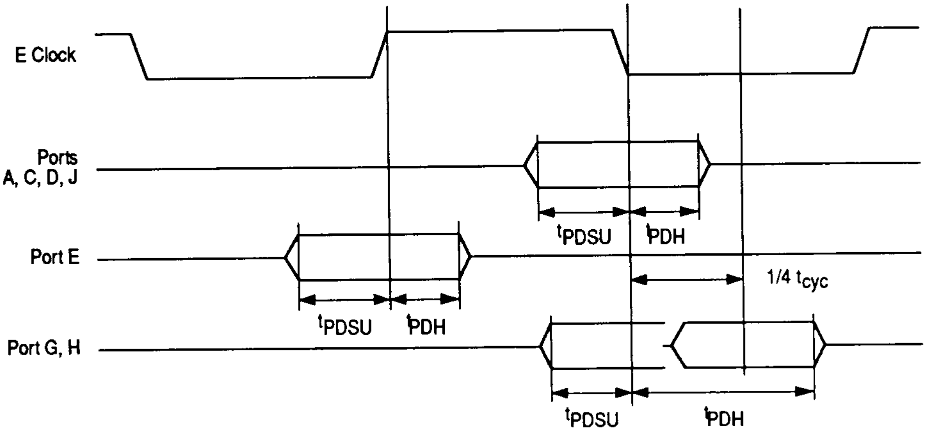


Figure 13-14. Port Read Timing Diagram

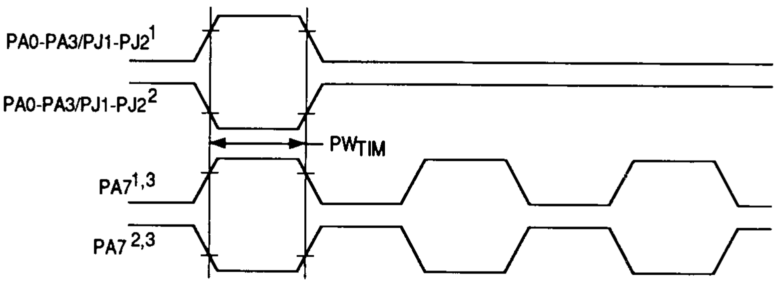
13.7 TIMER CHARACTERISTICS

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Timer Pulse Width Input Capture Pulse Accumulator Input (PW_{TIM} = t_{cyc} + 20ns)	PW_{TIM}	496	—	ns
Timer Output Compare High Valid	t_{OCH}	—	310	ns
Timer Output Compare Low Valid	t_{OCL}	—	295	ns
Timer Input Capture Response Delay Min = t_{cyc} + 20ns Max = 2 t_{cyc} + 220ns	t_{CAP}	496	1172	ns

NOTES:

1. All timing is shown with respect to 20% V_{DD} and 70% V_{DD} unless otherwise noted.



Notes:
1. Rising edge sensitive input.
2. Failing edge sensitive input.
3. Maximum pulse accumulator clocking rate is E frequency divided by 2.

Figure 13-15. Timer Inputs Timing Diagram

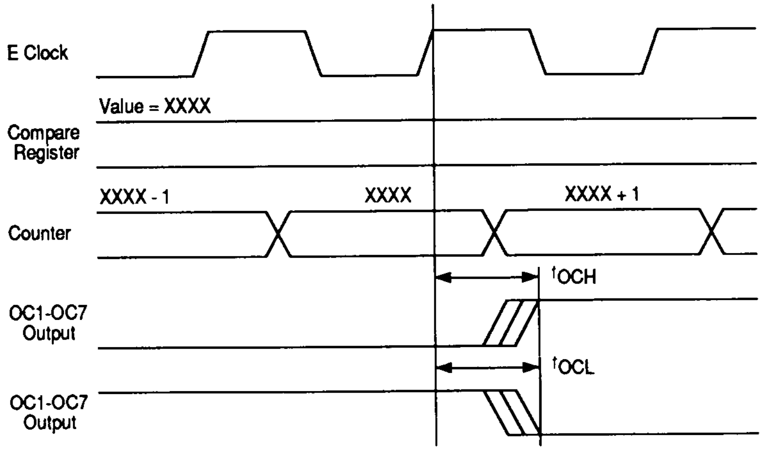


Figure 13-16. Output Compare Timing Diagram

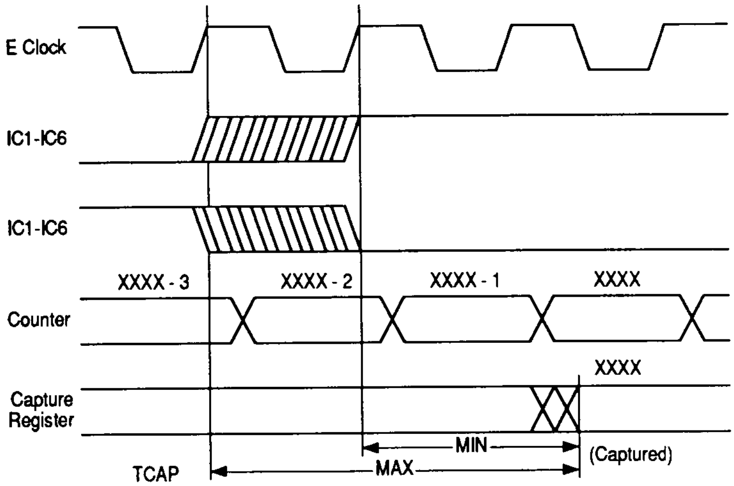


Figure 13-17. Input Capture Timing Diagram

13.8 A/D CONVERTER CHARACTERISTICS

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, E = 750kHz to 2.1MHz unless otherwise noted)

Characteristic	Parameter	Min	Absolute	Max	Unit
Resolution	Number of bits resolved by the A/D	10	—	—	Bits
Nonlinearity	Maximum deviation from the ideal A/D transfer characteristics	—	—	TBD	LSB
Zero Error	Difference between the output of an ideal and an actual A/D for zero input voltage	—	—	TBD	LSB
Full Scale Error	Difference between the output of an ideal and an actual A/D for full scale input voltage	—	—	TBD	LSB
Total Unadjusted Error	Maximum sum of Nonlinearity, zero error and full scale error	—	—	TBD	LSB
Quantization Error	Uncertainty due to converter resolution	—	—	±0.5	LSB
Absolute Accuracy (See Note 1)	Difference between the actual input voltage and the full scale weighted equivalent of the binary output code, all error sources included	—	—	TBD	LSB
Conversion Range (See Notes 3 and 4)	Analog input voltage range	V_{rl}	—	V_{rh}	V
V_{rh} (See Note 2)	Maximum analog reference voltage	V_{rl}	—	V_{DD} + 0.1	V
V_{rl} (See Note 2)	Minimum analog reference voltage	V_{SS} - 0.1	—	V_{rh}	V
Delta V_r (See Note 2)	Minimum difference between V_{rh} and V_{rl}	0	—	—	V
Conversion Time	Total time to perform a single analog to digital conversion: 1. E Clock 2. Internal RC Oscillator	 — —	 36 —	 — t_{cyc} + 24	 t_{cyc} µs
Monotonicity	Conversion result never decreases with an increase in input voltage and has no missing codes	Guaranteed			
Zero Input Reading (See Note 3)	Conversion result when $V_{in} = V_{rl}$	\$000	—	—	Hex
Full Scale reading (See Note 4)	Conversion result when $V_{in} = V_{rh}$	—	—	\$3FF	Hex
Sample Acquisition Time	Analog Input Acquisition sampling time: 1. E Clock 2. Internal RC Oscillator	 — —	 13 —	 — 8.7	 t_{cyc} µs
Sample Hold Capacitance	Input capacitance during sample PE0-PE7	—	35 (Typ)	—	pF
Input Leakage	Input leakage on A/D pins: PE0-PE7 V_{rl}, V_{rh}	 — —	 — —	 100 250	 nA µA

NOTES:

1. Source impedances greater then 10kΩ will adversely affect accuracy, due mainly to input leakage.
2. Performance verified down to 2.5V Delta V_r, but accuracy is tested and guaranteed at Delta V_r = 5V ± 10%.
3. Minimum analog input voltage should not go below V_{SS} - 0.3V.
4. Maximum analog input voltage should not exceed 1.125V_{rh}.

13.9 EXPANSION BUS TIMING

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H unless otherwise noted)

Num	Characteristic	Symbol	Min	Max	Unit
	Frequency of Operation (E-Clock)	f_o	—	2.1	MHz
1	Cycle Time	t_{cyc}	476	—	ns
2	Pulse Width E Low (1/2 t_{cyc} - 23ns)	t_{ELEH}	215	—	ns
3	Pulse Width E High (1/2 t_{cyc} - 28ns)	t_{EHEL}	210	—	ns
4	E Rise and Fall Time	t_R, t_F	—	20	ns
9	Address Hold Time (t_{AH} = 1/8 t_{cyc} - 29.5ns) (See Note 1(A))	t_{AH}	30	—	ns
12	Address Valid Time to E Rise (See Note 1(B))	t_{AV}	120	—	ns
17	Read Data Setup Time	t_{DSR}	30	—	ns
18	Read Data Hold Time	t_{DHR}	10	—	ns
19	Write Data Delay Time	t_{DDW}	—	80	ns
21	Write Data Hold Time	t_{DHW}	50	—	ns
29	MPU Address Access Time ($t_{ACCA} = t_{AV} + t_R + t_{EHEL} - t_{DSR}$ (See Note 1(A))	t_{ACCA}	320	—	ns

NOTES:

1. Input clock with duty cycle other than 50% will affect the bus performance. Timing parameters affected by the input clock duty cycle are identified by (A) and (B). To re-calculate approximate bus timing values, substitute the following expressions in place of 1/8 t_{cyc} in the above formulae where applicable:

   (A) (1-DC) x 1/4 t_{cyc}
   (B) DC x 1/4 t_{cyc}

   where DC is the decimal value of duty cycle percentage (High time).

2. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}.

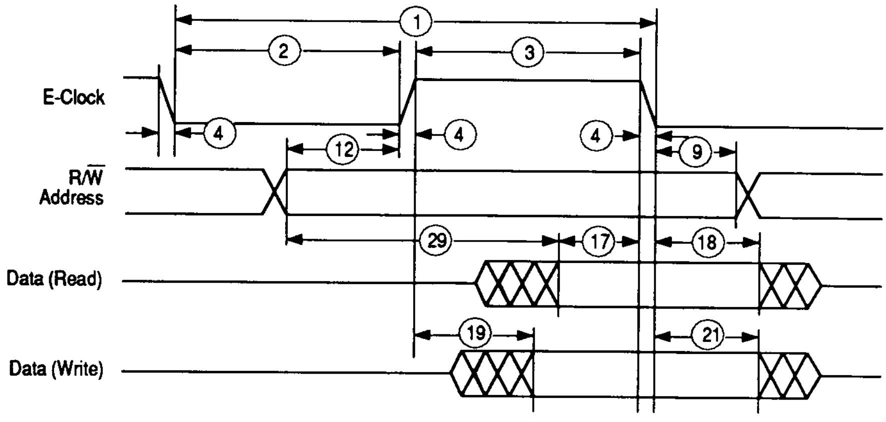


Figure 13-18. Non-multiplexed Expanded Bus

13.10 SERIAL PERIPHERAL INTERFACE (SPI) TIMING

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H unless otherwise noted)

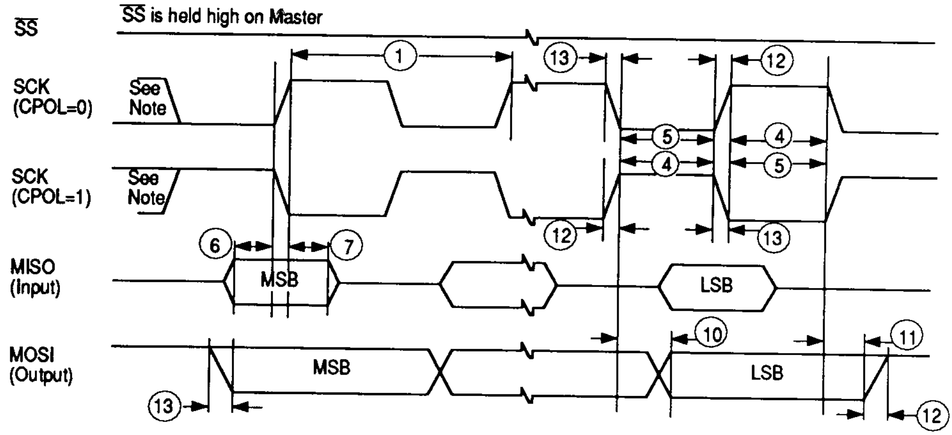
Num	Characteristic		Symbol	Min	Max	Unit
	Operating Frequency	Master Slave	$f_{op(m)}$ $f_{op(s)}$	dc dc	0.5 2.1	f_o MHz
1	Cycle Time	Master Slave	$t_{cyc(m)}$ $t_{cyc(s)}$	2.0 480	— —	t_{cyc} ns
2	Enable Lead Time	Master Slave	$t_{lead(m)}$ $t_{lead(s)}$	* 240	— —	ns ns
3	Enable Lag Time	Master Slave	$t_{lag(m)}$ $t_{lag(s)}$	* 240	— —	ns ns
4	Clock (SCK) High Time	Master Slave	$t_{w(SCKH)m}$ $t_{w(SCKH)s}$	340 190	— —	ns ns
5	Clock (SCK) Low Time	Master Slave	$t_{w(SCKL)m}$ $t_{w(SCKL)s}$	340 190	— —	ns ns
6	Data Setup Time	Master Slave	$t_{su(m)}$ $t_{su(s)}$	100 100	— —	ns ns
7	Data Hold Time	Master Slave	$t_{h(m)}$ $t_{h(s)}$	100 100	— —	ns ns
8	Access Time (Time to Data Active from High-Impedance State)	Slave	t_a	0	120	ns
9	Disable Time (Hold Time to High-Impedance State)	Slave	t_{dis}	—	240	ns
10	Data Valid (After Enable Edge)**		$t_{v(s)}$	—	240	ns
11	Data Hold Time (Outputs) (After Enable Edge)		t_{ho}	- 40	—	ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, C_L = 200pF) SPI Outputs (SCK, MOSI, MISO) SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)		 $t_{r(m)}$ $t_{r(s)}$	 — —	 100 2.0	 ns µs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200pF) SPI Outputs (SCK, MOSI, MISO) SPI Inputs (SCK, MOSI, MISO, $\overline{SS}$)		 $t_{f(m)}$ $t_{f(s)}$	 — —	 100 2.0	 ns µs

NOTES:

* Signal production depends on software.

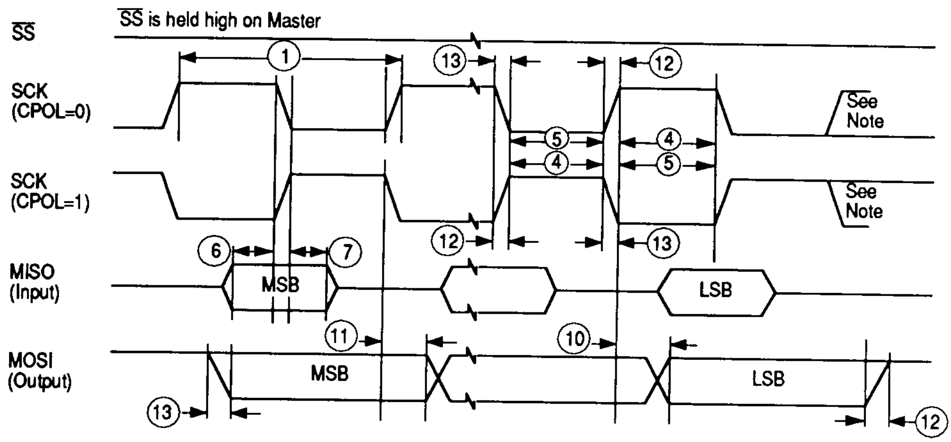
** Assumes 200 pF load on all SPI pins.

1. All timing is shown with respect to 20% V_{DD} and 70% V_{DD} unless otherwise noted.



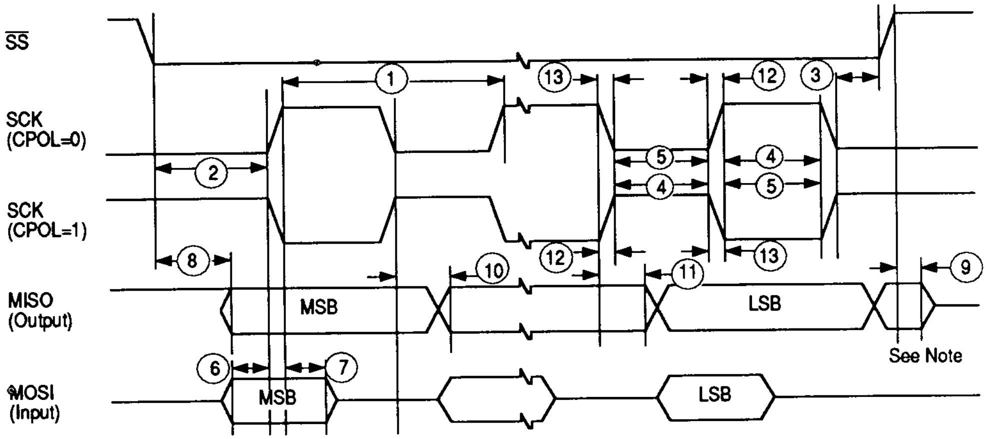
Note: This first edge is generated internally but is not seen at the SCK pin.

Figure 13-19. SPI Master Timing (CPHA = 0)



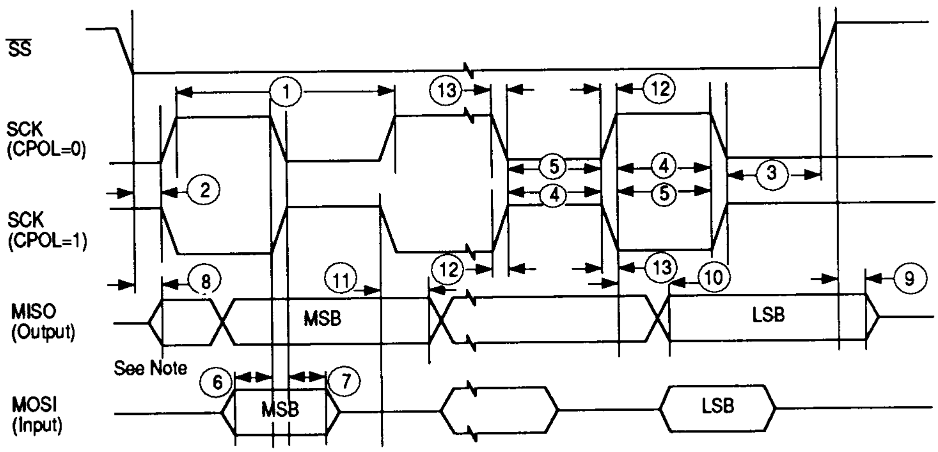
Note: This last edge is generated internally but is not seen at the SCK pin.

Figure 13-20. SPI Master Timing (CPHA = 1)



Note: Not defined but normally MSB of character just received.

Figure 13-21. SPI Slave Timing (CPHA = 0)



Note: Not defined but normally LSB of character previously transmitted.

Figure 13-22. SPI Slave Timing (CPHA = 1)

13.11 EVENT COUNTER CHARACTERISTICS

Table 13.1. Clock Input (Required Limit)

Clock Input (Required Limit)

Num	Characteristic	Symbol	Min	Max	Unit
1	Cycle Time of External Clock Input	t_{cycex}	$3xt_{cyc}$	—	ns
2	Clock High Time	t_{wckh}	$1.5xt_{cyc}$	—	ns
3	Clock Low Time	t_{wckl}	$1xt_{cyc}$	—	ns
4	Rise Time	t_{rck}	—	$0.25xt_{cyc}$	ns
5	Fall Time	t_{fck}	—	$0.25xt_{cyc}$	ns

Table 13.2. Clock Input (Guaranteed Limit)

Clock Input (Guaranteed Limit)

Num	Characteristic	Symbol	Min	Max	Unit
6	Propagation Delay External Clock Rise to EVO Valid	t_{ovr}	$1.5xt_{cyc}$	$2.5xt_{cyc}$ + 240	ns
7	Propagation Delay External Clock Fall to EVO Valid	t_{ovf}	$1.5xt_{cyc}$	$2.5xt_{cyc}$ + 240	ns

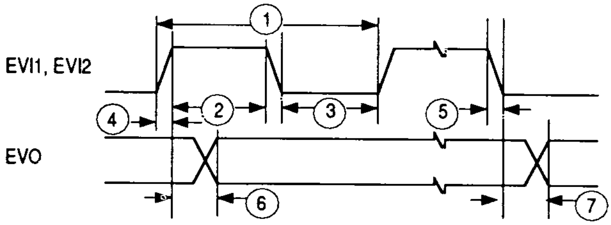


Figure 13-23. Event Counter Mode 1, 2, 3 – Clock Input Timing Diagram

Table 13.3. Clock Gate Input (Guaranteed Limit)

Clock Gate Input (Required Limit)

Num	Characteristic	Symbol	Min	Max	Unit
1	Gate Input Setup Time to E Fall	t_{gsu}	$0.25xt_{cyc}$	—	ns
2	Gate Input Hold Time to E Fall	t_{gh}	$0.5xt_{cyc}$	—	ns

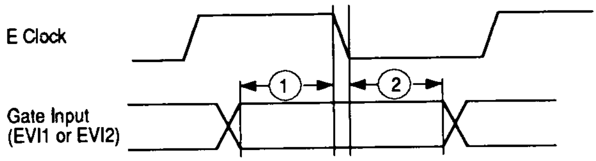


Figure 13-24. Event Counter Mode 1, 2, 3 – Clock Gate Input Timing Diagram