



## N-Channel 75-V (D-S) MOSFET with Sensing Diode

### PRODUCT SUMMARY

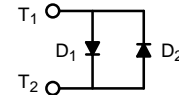
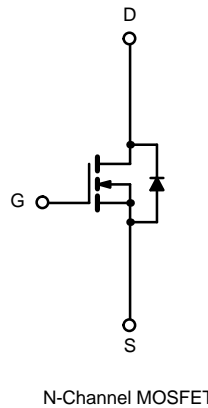
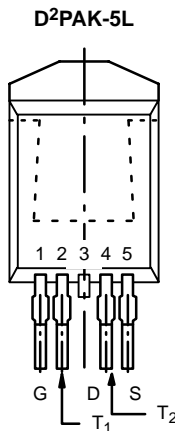
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
75	0.007 @ $V_{GS} = 10$ V	60 <sup>a</sup>

### FEATURES

- TrenchFET® Power MOSFET Plus Temperature Sensing Diode
- New Low Thermal Resistance Package

### APPLICATIONS

- Automotive
- Industrial



ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DS}$	75	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175^\circ\text{C}$ ) <sup>d</sup>	$T_C = 25^\circ\text{C}$	$I_D$	60 <sup>a</sup>	A
	$T_C = 100^\circ\text{C}$		60 <sup>a</sup>	
Pulsed Drain Current		$I_{DM}$	240	
Continuous Diode Current (Diode Conduction) <sup>d</sup>		$I_S$	60 <sup>a</sup>	
Avalanche Current		$I_{AR}$	60 <sup>a</sup>	
Repetitive Avalanche Energy <sup>b</sup>	$L = 0.1$ mH	$E_{AR}$	180	
Maximum Power Dissipation <sup>a</sup>	$T_C = 25^\circ\text{C}$	$P_D$	300 <sup>c</sup>	W
	$T_A = 25^\circ\text{C}$		3.75 <sup>d</sup>	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Limit	Unit
Junction-to-Ambient <sup>d</sup>	PCB Mount <sup>d</sup>	$R_{thJA}$	40	$^\circ\text{C}/\text{W}$
Junction-to-Case		$R_{thJC}$	0.5	

Notes

- a. Package limited.
- b. Duty cycle  $\leq 1\%$ .
- c. See SOA curve for voltage derating.
- d. When mounted on 1" square PCB (FR-4 material).

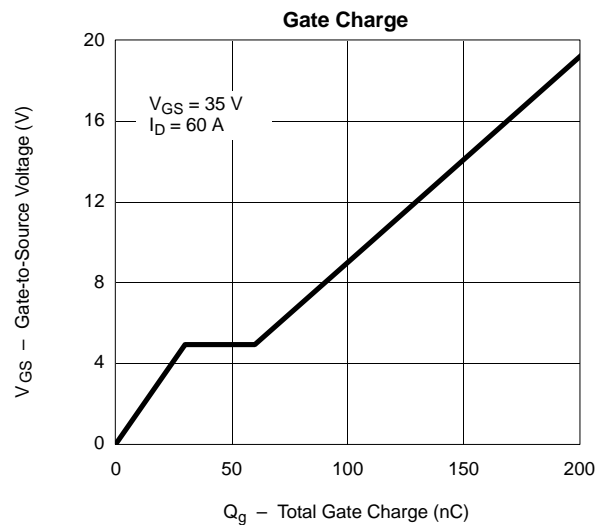
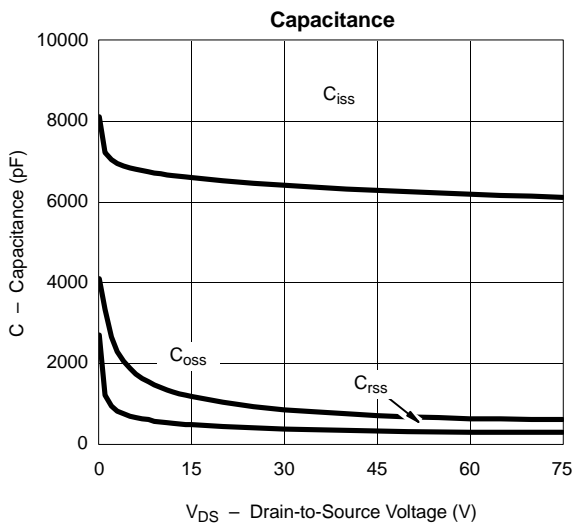
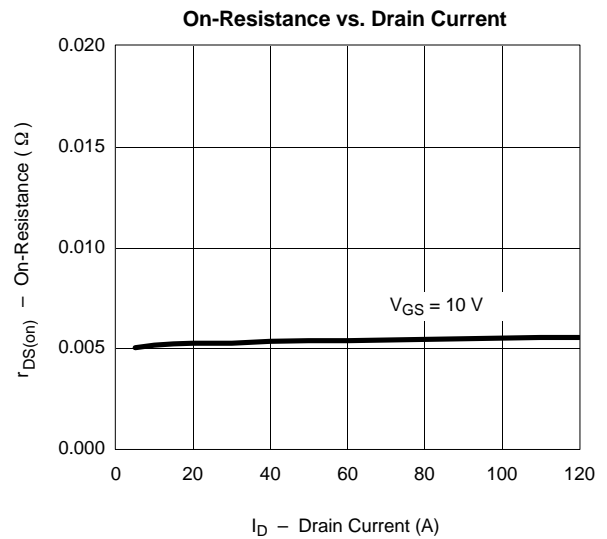
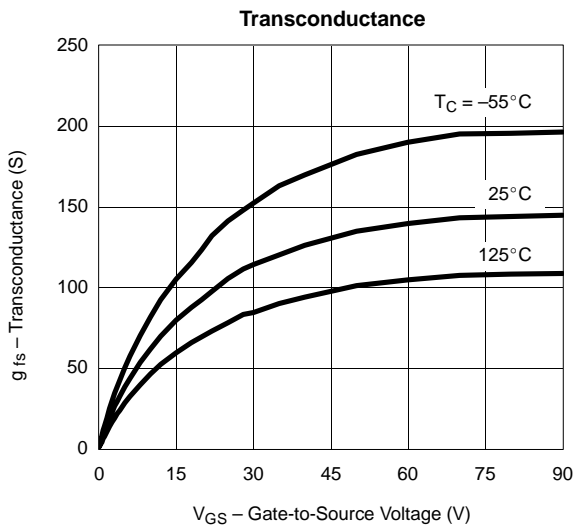
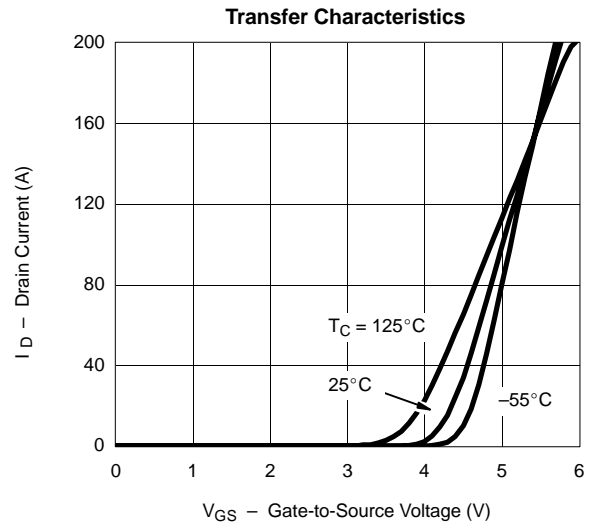
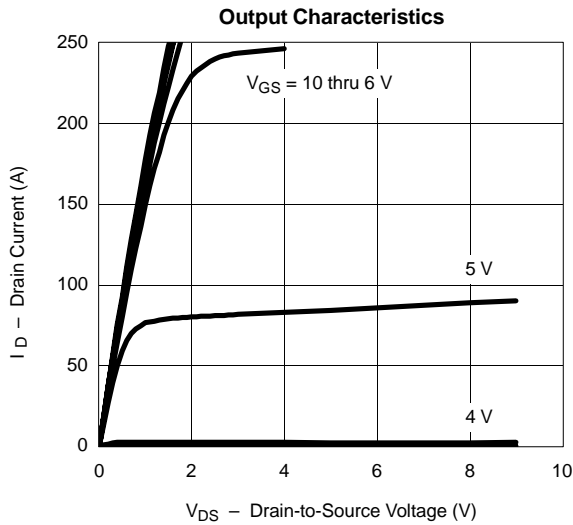
MOSFET SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	75			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>DS</sub> = 250 μA	2		4	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			500	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	120			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A		0.0054	0.007	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A, T <sub>J</sub> = 125 °C			0.010	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A, T <sub>J</sub> = 175 °C			0.013	
Sense Forward Voltage	V <sub>FD1</sub>	I <sub>F</sub> = 50 μA	710		770	mV
	V <sub>FD2</sub>	I <sub>F</sub> = 25 μA	640		700	
Sense Diode Forward Voltage Increase	ΔV <sub>F</sub>	From I <sub>F</sub> = 25 μA to I <sub>F</sub> = 50 μA	40		100	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A		100		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		6500		pF
Output Capacitance	C <sub>oss</sub>			920		
Reverse Transfer Capacitance	C <sub>rss</sub>			400		
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 35 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 60 A		110	150	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			30		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			30		
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 35 V, R <sub>L</sub> = 0.6 Ω I <sub>D</sub> = 60 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 2.5 Ω		15	20	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			130	200	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			75	115	
Fall Time <sup>c</sup>	t <sub>f</sub>			120	180	
<b>Source-Drain Diode Ratings and Characteristics (T<sub>C</sub> = 25 °C)<sup>b</sup></b>						
Continuous Current	I <sub>s</sub>				60	A
Pulsed Current	I <sub>SM</sub>				240	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 60 A, V <sub>GS</sub> = 0 V		1.0	1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 60 A, di/dt = 100 A/μs		75	115	ns
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>			3.5	5	A
Reverse Recovery Charge	Q <sub>rr</sub>			0.13	0.29	μC

Notes:

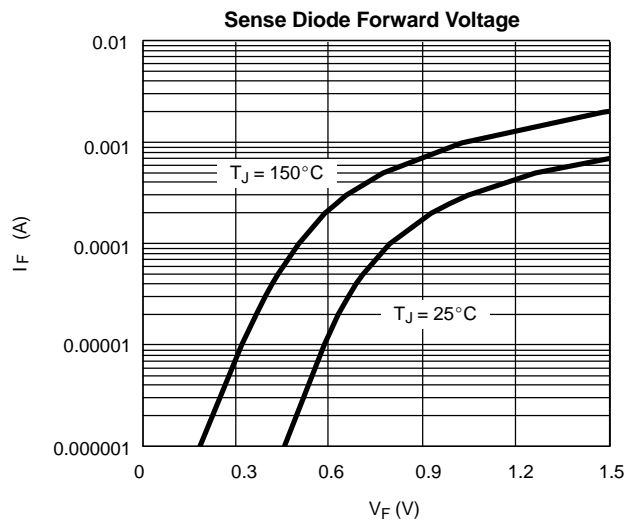
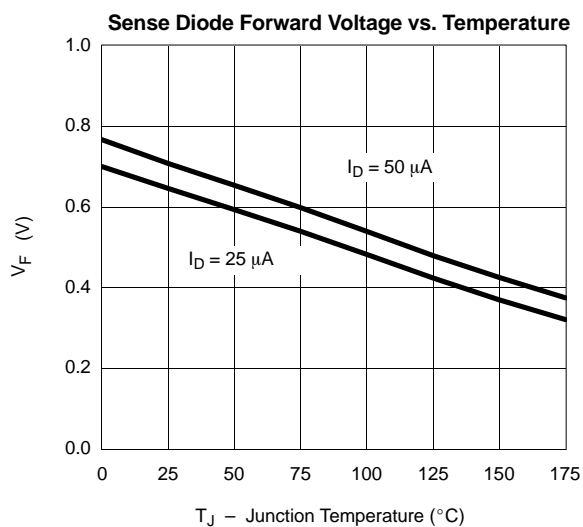
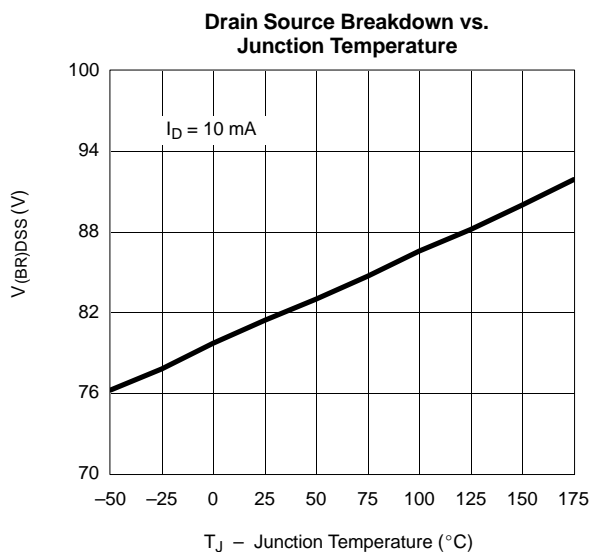
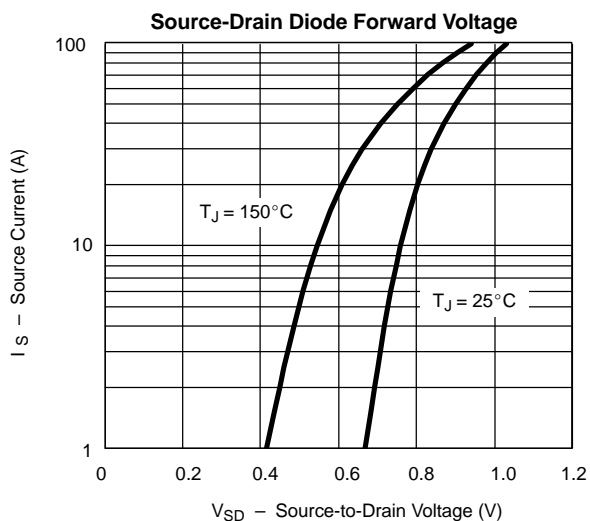
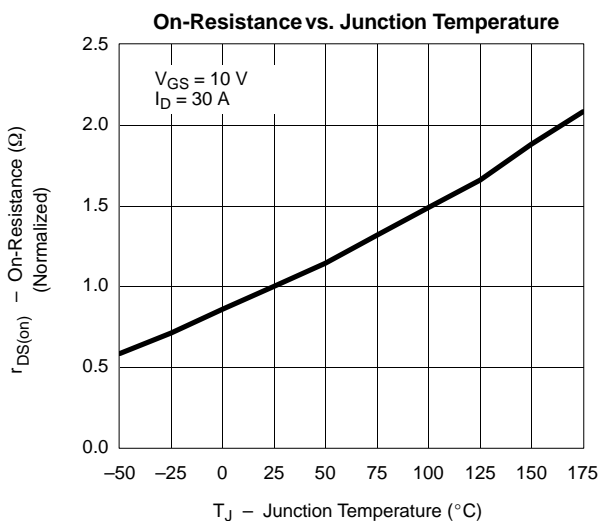
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



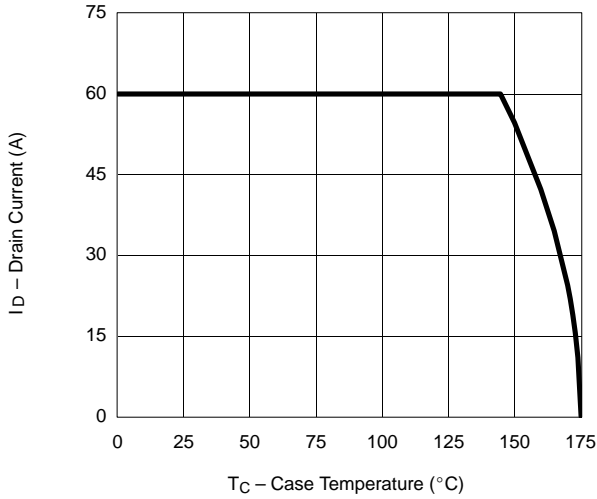
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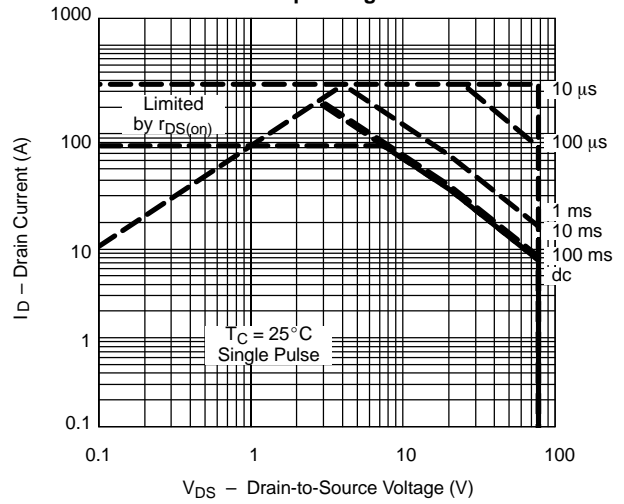


**THERMAL RATINGS**

Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

