REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
SHEET																								
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REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14									

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
22 SEPTEMBER 1989

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, FAST, CMOS, 8-BIT TRANSCEIVER WITH PARITY, TTL COMPATIBLE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89731

SHEET 1 OF 14

DESC FORM 193
SEP 87

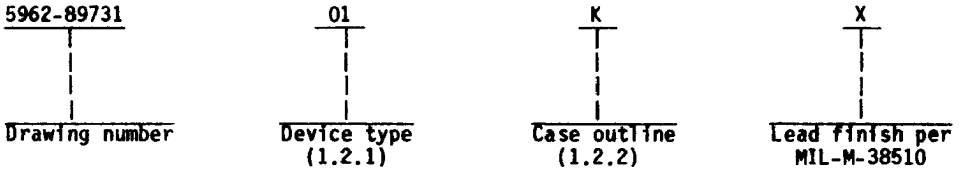
* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1430

SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54FCT833A	8-bit transceiver with parity, TTL compatible
02	54FCT833B	8-bit transceiver with parity, TTL compatible

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
K	F-6 (24 lead, .640" x .420" x .090"), flat package
L	D-9 (24 lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to V_{CC} + 0.5 V dc
Output voltage range	-0.5 V dc to V_{CC} + 0.5 V dc
DC input diode current (I_{IK})	-20 mA
DC output diode current (I_{OK})	-50 mA
DC output current	±100 mA
Maximum power dissipation (P_D) 2/	500 mW
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	+175°C
Lead temperature (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ All voltages referenced to GND.
2/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V dc ±10% unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.0 V	I_{OH} = -300 µA	All	1, 2, 3	4.3		V
			I_{OH} = -15 mA	All	1, 2, 3	2.4		
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.0 V	I_{OL} = 300 µA	All	1, 2, 3		0.2	V
			I_{OL} = 32 mA	All	1, 2, 3		0.5	
Input clamp voltage	V_{IK}	V_{CC} = 4.5 V, I_{IN} = -18 mA		All	1, 2, 3		-1.2	V
High level input current	I_{IH}	V_{CC} = 5.5 V, V_{IN} = 5.5 V		All	1, 2, 3		5.0	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = GND		All	1, 2, 3		-5.0	µA
Short circuit output current	I_{OS}	V_{CC} = 5.5 V 1/ V_O = GND		All	1, 2, 3	-60		mA
Quiescent power supply current (CMOS inputs)	I_{CCQ}	$V_{IN} \le 0.2$ V or $V_{IN} \ge 5.3$ V, V_{CC} = 5.5 V, f_I = 0 MHz		All	1, 2, 3		1.5	mA
Quiescent power supply current (TTL inputs)	ΔI_{CC}	V_{CC} = 5.5 V, V_{IN} = 3.4 V 2/		All	1, 2, 3		2.0	mA
Dynamic power supply current	I_{CCD}	V_{CC} = 5.5 V, outputs open, one input toggling, $V_{IN} \ge 5.3$ V or $V_{IN} \le 0.2$ V, $\overline{OE}_n$ = GND, 50% duty cycle		All	3/		0.25	mA/MHz

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5.0$ V dc ±10% unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Total power supply current	I_{CCT}	V_{CC} = 5.5 V, outputs open, f_I = 2.5 MHz, 50% duty cycle, one input toggling, f_{CP} = 10 MHz (CLK), $\overline{OE}_T$ = GND, $\overline{OE}_R$ = V_{CC} 4/	$V_{IN} \ge 5.3$ V or $V_{IN} \le 0.2$ V	All	1, 2, 3		3.4	mA
			V_{IN} = 3.4 V or V_{IN} = GND	All	1, 2, 3		5.4	mA
Input capacitance	C_{IN}	See 4.3.1c		All	4		10	pF
Output capacitance	C_{OUT}	See 4.3.1c		All	4		12	pF
Functional tests		See 4.3.1d		All	7, 8			
Propagation delay time, Rn to Tn, Tn to Rn	t_{PLH1}, t_{PHL1}	C_L = 50 pF, R_L = 500Ω, See figure 4 5/		01	9,10,11	1.5	14.0	ns
				02		1.5	10.0	
Propagation delay time, Rn to PARITY	t_{PLH2}, t_{PHL2}			01	9,10,11	2.0	20.0	
				02		2.0	14.0	
Propagation delay time, $\overline{CLR}$ to $\overline{ERR}$	t_{PLH3},			01	9,10,11	1.5	20.0	
				02		1.5	18.0	
Propagation delay time, CLK to $\overline{ERR}$	t_{PHL3},			01	9,10,11	2.0	16.0	
				02		2.0	11.0	
Propagation delay time, $\overline{OE}_R$ to PARITY	t_{PLH4}, t_{PHL4}			01	9,10,11	1.5	20.0	
				02		1.5	14.0	

See footnotes at top of next page.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5.0$ V dc ±10% unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Minimum setup time, Tn, PARITY to CLK	t_s	C_L = 50 pF, R_L = 500Ω, See figure 4	01	9,10,11	16.0		
			02		11.0		
Minimum hold time, Tn, PARITY to CLK	t_h		01	9,10,11	0.0		
			02		0.0		
Minimum pulse width, CLK	t_{w1}		01	9,10,11	9.5		
			02		7.0		
Minimum pulse width, $\overline{CLR}$	t_{w2}		01	9,10,11	9.5		
			02		7.0		
Minimum clear recovery time, $\overline{CLR}$ to CLK	t_{rec}		01	9,10,11	20.0		
			02		14.0		

1/ Not more than one output should be shorted at one time, and the duration of the short circuit condition should not exceed 1 second.

2/ TTL driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND.

3/ This parameter is not directly testable, but is derived for use in total power supply calculations.

4/ $I_{CC} = I_{CCQ} + (\Delta I_{CC} \times D_H \times N_T) + I_{CCD} \left(\frac{f_{CP}}{2} + f_I \times N_I \right)$ where:

D_H = Duty cycle for TTL inputs high
N_T = Number of TTL inputs at D_H
f_I = Input frequency in MHZ
N_I = Number of inputs at f_I

5/ The minimum limits for the propagation delay times are guaranteed, if not tested, to the limits specified in table I.

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Device types 01 and 02		
Case outlines	K, L	3
Terminal number	Terminal symbol	
1	$\overline{OE}_R$	NC
2	RO	$\overline{OE}_R$
3	R1	RO
4	R2	R1
5	R3	R2
6	R4	R3
7	R5	R4
8	R6	NC
9	R7	R5
10	$\overline{ERR}$	R6
11	$\overline{CLR}$	R7
12	GND	$\overline{ERR}$
13	CLK	$\overline{CLR}$
14	$\overline{OE}_T$	GND
15	PARITY	NC
16	T7	CLK
17	T6	$\overline{OE}_T$
18	T5	PARITY
19	T4	T7
20	T3	T6
21	T2	T5
22	T1	NC
23	TO	T4
24	V_{CC}	T3
25	---	T2
26	---	T1
27	---	TO
28	---	V_{CC}

FIGURE 1. Terminal connections.

ERROR FLAG TRUTH TABLE

Inputs		Internal to device	Outputs pre-state	Output	Function
$\overline{CLR}$	CLK	POINT "P"	$\overline{ERR}$ n-1	$\overline{ERR}$	
H	↑	H	H	H	Sample
H	↑	X	L	L	(1's capture)
H	↑	L	X	L	
L	X	X	X	H	Clear

$\overline{OE}_T$ is HIGH and $\overline{OE}_R$ is LOW

H = High voltage level
L = Low voltage level
X = Irrelevant
↑ = Transition from low to high

FUNCTION TABLE

Inputs						Outputs				Function
$\overline{OE}_T$	$\overline{OE}_R$	$\overline{CLR}$	CLK	Rn (Σ of H's)	Tn Incl PARITY (Σ of H's)	Rn	Tn	PARITY	$\overline{ERR}$ 1/	
L	H	X	X	H (Odd)	N/A	N/A	H	L	N/A	Transmit data from R Port to T Port with parity; receiving path is disabled
L	H	X	X	H (Even)	N/A	N/A	H	H	N/A	
L	H	X	X	L (Odd)	N/A	N/A	L	L	N/A	
L	H	X	X	L (Even)	N/A	N/A	L	L	N/A	
H	L	H	↑	N/A	H (Odd)	H	N/A	N/A	H	Receive data from T to R Port with parity resulting in flag; transmitting path is disabled
H	L	H	↑	N/A	H (Even)	H	N/A	N/A	L	
H	L	H	↑	N/A	L (Odd)	L	N/A	N/A	H	
H	L	H	↑	N/A	L (Even)	L	N/A	N/A	L	
X	X	L	X	X	X	X	N/A	N/A	H	Clear the state of error flag register
H	H	H	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode
H	H	L	X	X	X	Z	Z	Z	H	
H	H	H	↑	L (Odd)	X	Z	Z	Z	H	
H	H	H	↑	H (Even)	X	Z	Z	Z	L	
L	L	X	X	H (Odd)	N/A	N/A	H	H	N/A	Forced-error checking
L	L	X	X	H (Even)	N/A	N/A	H	L	N/A	
L	L	X	X	L (Odd)	N/A	N/A	L	H	N/A	
L	L	X	X	L (Even)	N/A	N/A	L	L	N/A	

H = High voltage level
L = Low voltage level
N/A = Not applicable
Z = High impedance
X = Irrelevant
* = Store the error state of the last receive cycle
↑ = Transition from low to high
Odd = Odd number of logic one's
Even = Even number of logic one's
n = 0, 1, 2, 3, 4, 5, 6, 7

1/ Output state assumes high output pre-state.

FIGURE 2. Truth tables.

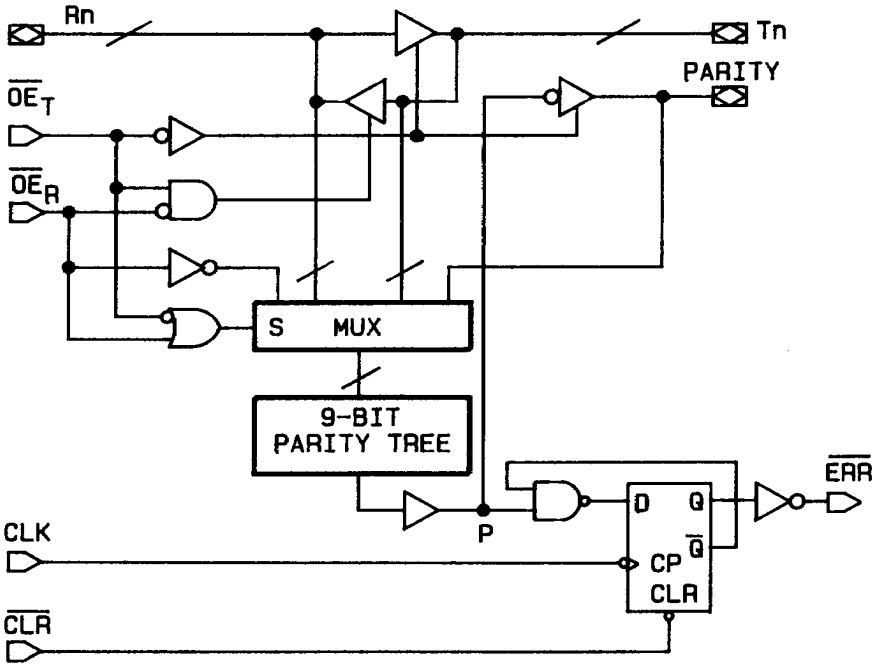
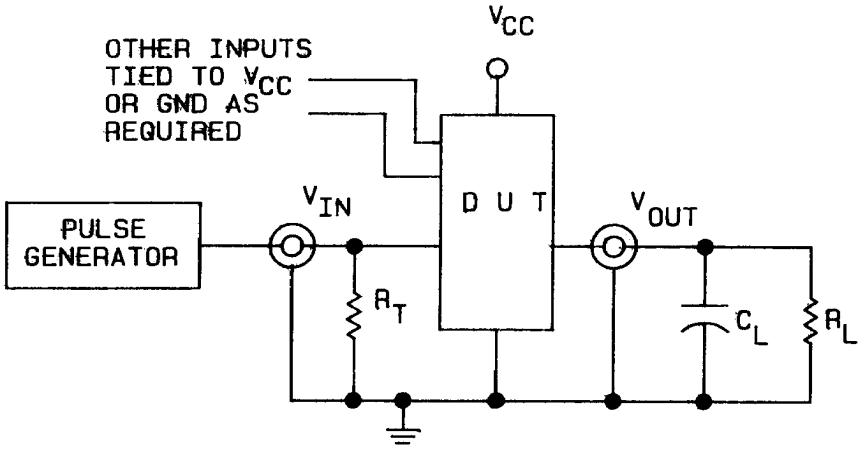


FIGURE 3. Logic diagram.



R_L = Load resistor (see ac characteristics for value).
C_L = Load capacitance includes jig and probe capacitance (see ac characteristics for value).
R_T = Termination should be equal to Z_{OUT} of pulse generators.

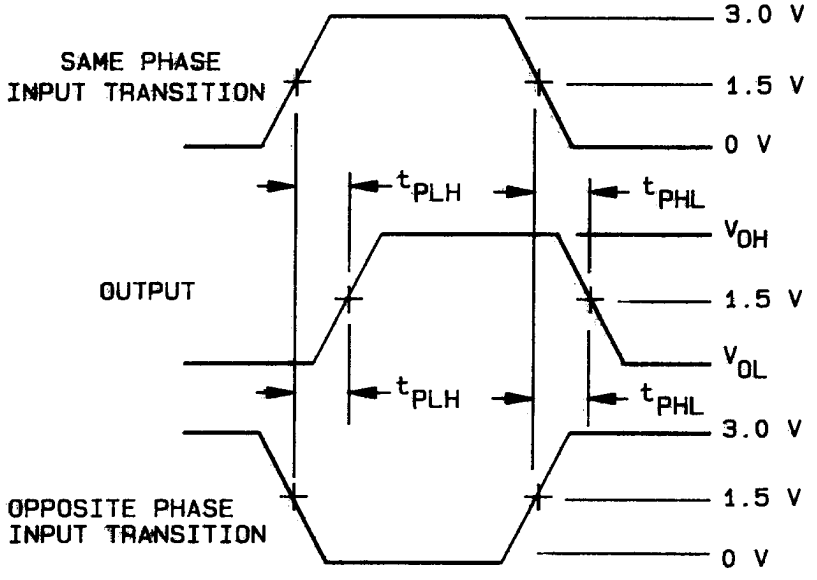
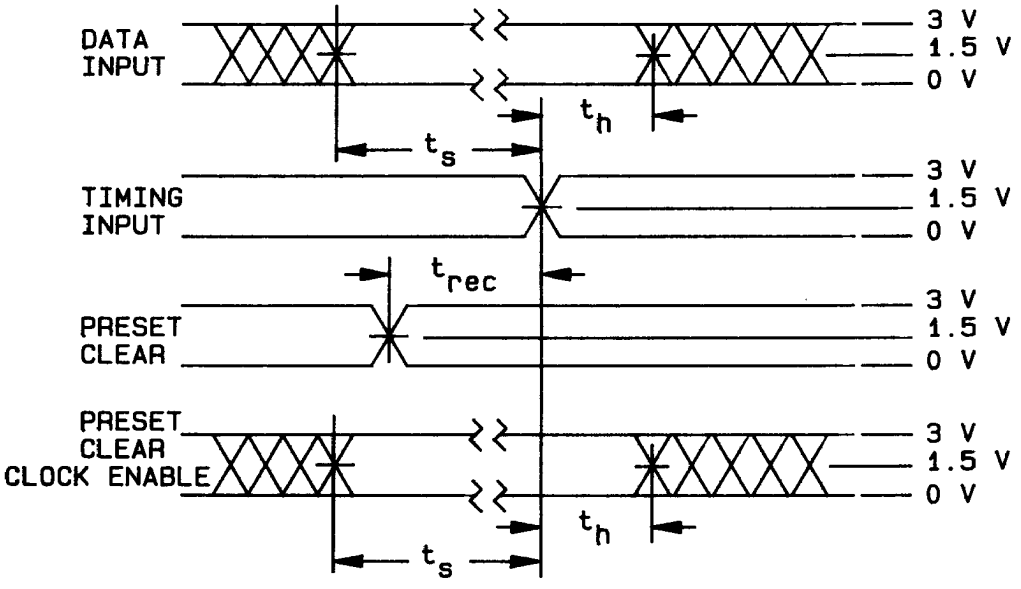


FIGURE 4. Switching waveforms and test circuit.



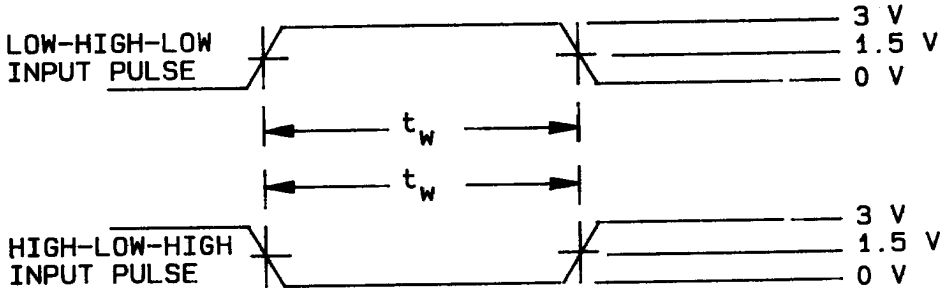


FIGURE 4. Switching waveforms and test circuit - Continued.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only initially and after process or design changes which may affect capacitance. Test all applicable pins on five devices with zero failures.

d. Subgroups 7 and 8 tests shall verify the truth table as specified on figure 2.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industry users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of the drawing covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513)296-6022).

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. An approved source of supply listed below is for information purposes only and is current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8973101KX	61772	IDT54FCT833AEB
5962-8973101LX	61772	IDT54FCT833ADB
5962-89731013X	61772	IDT54FCT833ALB
5962-8973102KX	61772	IDT54FCT833BEB
5962-8973102LX	61772	IDT54FCT833BDB
5962-89731023X	61772	IDT54FCT833BLB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
61772	Integrated Device Technology 3236 Scott Boulevard Santa Clara, CA 95052