R/W Preamplifier for 3 Terminal Recording Heads, 6 or 8 Channels

GENERAL DESCRIPTION

The XR-501 is a high speed, low noise head interface integrated circuit for hard disk drives, performing both read and write functions The XR-501 is compatible with 3 1/2" to 14" multiple platter drives and features low noise, large dynamic range, and high bandwidth. Several packaging options extend usefulness to applications requiring six or eight center-tapped read/write heads Multiple devices are easily cascaded for drives with more heads.

The XR-501 features a pinout with all head ports on one side of the circuit. This eases flex cable or PC board layout by eliminating crossovers. The XR-501R option includes internal damping resistors facilitating use in systems requiring minimum external circuit complexity.

XR-501, manufactured with a high speed bipolar process, operates on +5 V and +12 V. It is offered in a variety of packages, both surface mount and DIP.

FEATURES

Complete Head Interfacing Functions, Read and Write
Low Noise Preamplifier
High Dynamic Range and Bandwidth
Pinout Optimized for Easy Layout
Available in Six and Eight Head Versions
Easily Cascaded for Larger Systems
Full Featured Power Monitor
TTL Compatible Control Inputs

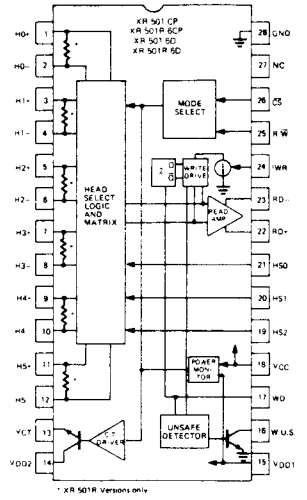
APPLICATIONS

Hard Disk Drives with MIG, ferrite or composite heads

ABSOLUTE MAXIMUM RATINGS

VDD	15V
VCC	6V
Digital Inputs	-0.3 V to VCC +0.3 V
Write Current	60 mA
Junction Temperature	150°C
Storage Temperature	-65°C to 150°C

PIN ASSIGNMENT



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-501-6CP	28 Pin Plastic DIP	0°C to 70°C
XR-501-6CJ	28 Pin PLCC	0°C to 70°C
XR-501-6D	28 Pin SO	0°C to 70°C
XR-501-8CP	40 Pin Plastic DIP	0°C to 70°C
XR-501-8CJ	44 Pin PLCC	0°C to 70°C
XR-501-8D	32 Pin SO	0°C to 70°C
XR-501R-6CP*	28 Pin Plastic DIP	0°C to 70°C
XR-501R-6CJ	28 Pin PLCC	0°C to 70°C
XR-501R-6D	28 Pin SO	0°C to 70°C
XR-501R-8CP*	40 Pin Plastic DIP	0°C to 70°C
XR-501R-8CJ	44 Pin PLCC	0°C to 70°C
XR-501R-8D	32 Pin SO	0°C to 70°C

Contact Factory for availability

SYSTEM DESCRIPTION

The XR-501 consists of a low noise preamplifier for reading from center tapped magnetic heads, a write current source for writing to the heads, a switching matrix to select one of eight heads, and associated control and monitoring functions. Less than 1.0 nV/ √Hz (typical) noise allows error free operation with small input signals. Over 50 mA of write current output (user adjustable) are available.

ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25°C V_{CC}=5V, V_{DD} =12 V, I_W = 40 mA, R_D =750Ω, C_L (R_{D+}, R_{D-}) ≤20 pF, Data Rate= 5 MHz, unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
I_{CC}	Supply Current			25	mA	V_{CC} = 5.5 V, Read or Idle Mode
				26	mA	V_{CC} = 5.5 V, Write Mode
I_{DD}	Supply Current			20	mA	V_{DD} = 13.2 V, Idle Mode
				40	mA	V_{DD} = 13.2 V, Read Mode
				20	mA	V_{DD} = 13.2 V, Write Mode, I_W = 0 mA
PD	Power Dissipation			400	mW	Idle Mode - V_{CC} = 5.5V, V_{DD} = 13.2V
				600	mW	Read Mode-V_{CC}=5.5V, V_{DD}=13.2V
				750	mW	I_W = 50 mA,,R_{CT}=160Ω
				1050	mW	I_W=50 mA, R_{CT} = 0Ω
VCT	Center Tap Voltage		4.5		V	Read Mode
			6.5		V	Write Mode
V_{PM}	Power Monitor Protection	3.7	4.0	4.4	V	V_{CC} to Disable Write
		8.5	9.6	10.5	V	V_{DD1} to Disable Write
DIGITAL CHARACTERISTICS						
WUS	Write Unsafe Output					
V_{OL}	Saturation Voltage		0.2	0.5	V	I_{OL} = 8 mA
I_{OH}	Leakage Current			100	µA	V_{OH}=5V
V_{IL}	Input Low Voltage			0.8	V	All digital inputs
V_{IH}	Input High Voltage	2.0		V		All digital inputs
I_{IL}	Input Low Current	-0.4		mA		All digital inputs, V_{IL} = 0.8V
I_{IH}	Input High Current			100	µA	All digital inputs, V_{IH} = 2.0V
WRITE CHARACTERISTICS						
	Write Current Accuracy	-7		7	%	Error from IW=140/RW
	Recommended Write Current Range	10		50	mA	
	Differential Head Voltage Swing	7.0	11		V	Peak(Inductive Load)
	Unselected Differential Head Current			85	µA	
	Unselected Transient Current			2	mA	Peak
	Differential Output Capacitance			15	pF	

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
WRITE CHARACTERISTICS (cont.)						
	Differential Output Resistance	10			KΩ	XR-501
		635	750	865	Ω	XR-501R
	WD Rate/Transistion Freq.	125	500		KHz	
K_I	Current Source Factor		20			$K_I = I_W/(\text{Current through } R_W)$
K	Write Current Constant	129	140	151	V	$I_W = K/R_W$
	Write Protection Leakage Current -200	-200		200	µA	Per Side, $V_{CC^-} \leq 3.7$ V, $V_{DD^-} \leq 8.7$V
V	Preamplifier Output Offset Voltage	-20		+20	mV	Write or Idle Mode
V_{CM}	Preamplifier Output Common Mode Voltage		5.3		V	Write or Idle Mode
	Preamplifier Output Leakage Current	-50		50	µA	Write or Idle Mode, $R_{D^+} = R_{D^-} = 6$ V
READ MODE						
A_V	Differential Voltage Gain	80		120	V/V	V_{IN} = 1 mVp-p at 300 kHz, $R_{L^+} = R_{L^-} = 1$ kΩ
	Dynamic Range	-3		+3		DC input voltage where gain drops 10%. $V_{IN} = V_i + 0.5$ mVp-p at 300 kHz.
R_{IN}	Differential Input Resistance	2	8		KΩ	XR-501
		530	650	790	Ω	XR-501R
C_{IN}	Differential Input Capacitance			23	pF	
e_{ni}	Input Noise Voltage		1.0	1.5	nV/√Hz	$L_h = 0$, $R_h = 0$, BW = 15 MHz
BW	Bandwidth	30	60		MHz	-3dB Point, $\lvert Z_s \rvert \leq 5\Omega V_{in}$ = 1 mVp-p
I_B	Input Bias Current		10	100	µA	
CMRR	Common Mode Rejection Ratio	50	60		dB	$V_{CM} = V_{CT}$ + 100 mVp-p at 5 MHz
PSRR	Power Supply Rejection Ratio	45	60		dB	100 mVp-p at 5 MHz Superimposed on V_{DD1}, V_{DD2} or V_{CC}
	Channel Separation	45	60			Unselected Channel: V_{IN} = 100 mVp-p at 5 MHz. Selected Channel V_{IN} = 0 V
	Output Offset Voltage	-480	±50	480	mV	
V_{CM}	Common Mode Output Voltage	5.0	6.2	7	V	
	Head Current Leakage	-200		200	µA	Per Side

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
READ MODE (cont.)						
R_O	Single Ended Output Resistance			30	Ω	f = 5 MHz
I_O	Output Current	2.1			mA	AC Coupled, Source or Sink
SWITCHING CHARACTERISTICS						
R/W	Read to Write		0.1	0.6	µs	Note 1
	Write to Read		0.1	0.6	µs	Note 1,3
CS	Start-up Delay		0.1	0.6	µs	Note 1,2
	Inhibit Delay		0.1	0.6	µs	Note 3
	Head Switching Delay		0.1	0.6	µs	Note 2, Switching between any heads.
WUS	Write Unsafe					
	Safe to Unsafe	1.6		8.0	µs	I_W = 50 mA, See Figure 1, TD1
	Unsafe to Safe		0.2	1	µs	I_W = 20 mA, See Figure 1, TD2
I_W	Head Current					
	Propagation Delay			30	ns	Note 4, See Figure 1, TD3
	Asymmetry			2	ns	Note 5
	Rise or Fall Time			20	ns	10% to 90% or 90% to 10% point

Note 1: Delay to 90% of I_W.
Note 2: Delay to 90% of 100 mVp-p 10 MHz Read Signal Envelope.
Note 3: Delay to 90% Decay of I_W.
Note 4: From 50% Points. L_h = 0H, R_h = 0Ω
Note 5: Write Data with 1 nS rise and fall times and 50% duty cycle.

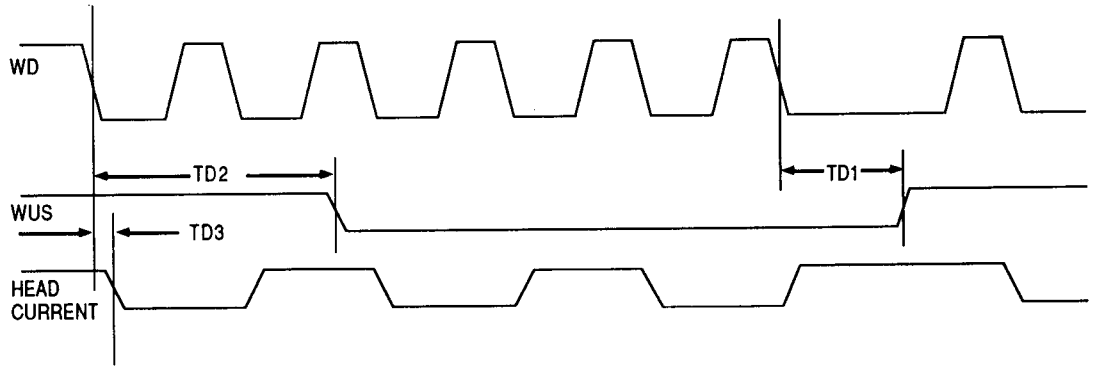


Figure 1. Write Mode Timing Diagram

A full-featured power monitor circuit disables the write mode during power-up and low operating voltage conditions, protecting data integrity.

CAUTION: This device may be damaged by electrostatic discharge. ESD precautions should be taken.

PRINCIPLES OF OPERATION

Write Mode

Before writing may begin, both chip select ($\overline{CS}$) and Read/Write ($R/\overline{W}$) must be pulled low. The desired head, selected by HS0 to HS2, is driven by a differential current sink of magnitude I_W, set by R_{IW}. Input data is applied to a falling edge triggered toggle flip-flop, which in turn selects the active side of the center tapped write head.

Current is sourced through the center tap driver, V_{CT}, which is "high" in the write mode. Write unsafe (W.U.S.) signals the disk controlier whenever one of six error conditions exist and writing should be discontinued. The six faults are: open head, open center tap, no write current, write data frequency too low, device unselected, and writing attempted while the device is in the read mode. The power supply monitor disables writing when V_{CC} drops below 4 V and/or V_{DD1} drops below 9 V.

Read Mode

Pulling R/W high enables the data readback mode. A low noise, high gain differential amplifier increases the weak read signal amplitude and provides low output impedance drive for the following stage (Pulse Detector).

APPLICATIONS INFORMATION

As with all high frequency, high gain systems, layout is critical. Lead lengths should be minimized and supplies should be well by passed. The XR-501 is available in small outline surface mount and PLCC packages, facilitating installation near the drive heads. The XR-501R option has 750Ω internal damping resistors across each head input, further aiding the goal of short lead lengths by eliminating the need for external resistors. The XR-501R option is especially convenient when the device is mounted on the flexible cable connecting the heads, as internal damping resistors reduce layout complexity, parts counts, and mass.

The high frequency characteristics of the XR-501 lead to a certain degree of electrostatic discharge (ESD) susceptability, so static reducing precautions should be taken.

Write Mode Design Considerations

Write current, I_W, typically between 20 mA and 50 mA, is determined by a single resistor, R_{IW}.

$$RIW = \frac{140{,}000}{I_W}$$

where I_W is in mA and R_{IW} is in Ohms.

Device power dissipation is reduced by a resistor, R_{CT}, connecting V_{DD2} to the +12 V supply. Some of the center tap driver voltage is then dropped across the resistor.

With the nominal 12 V supply, R_{CT}, is calculated as

$$R_{CT} = 130\left(\frac{55}{IW}\right)$$

where R_{CT} is in Ohms and IW is in milliamperes.

Internal dissipation reduction is primarily a consideration with high write current levels and small surface mount packages. All XR-501 packages are suitable for continuous operation under worst case conditions without requiring R_{CT}. If R_{CT} is not used, V_{DD2} is directly connected to V_{DD1}.

Write center tap circuitry is designed for higher stability than similar devices from other manufacturers. If extreme conditions exist, a ferrite bead around the V_{CT} line to the heads will reduce overshoot and ringing.

Write Unsafe Indicator (WUS)

Write unsafe (WUS) pulls high whenever one or more of six write error conditions exist. Four conditions; open head, open center tap, no write current and write data transition rate too low are detected with a differential capacitor charge/discharge circuit. Device unselected and read mode digital conditions also force WUS high.

After removal of the fault condition, two negative write data transitions are required to clear WUS This output is for indication only, intended for signaling a controller, and does not stop the write operation. A pull-up resistor of from 2 kΩ to 10 kΩ is necessary for operation of this open collector output.

Power Monitor Considerations

A power monitor circuit protects data integrity by preventing erroneous writing during power up and low voltage periods. The power monitor disables write current when V_{CC} is below about 4 V and/or V_{DD1} is below about 9 V. Hysteresis avoids unwanted toggling about the thresholds. At V_{CC} and V_{DD1} levels above these thresholds, operation is fully controllable,

Device operation at standard voltages (V_{CC} = 5 V ± 10%, V_{DD1} = 12 V 1 10%) is not affected in any way and is fully specified.

Read mode operation is not affected by the power monitor circuitry.

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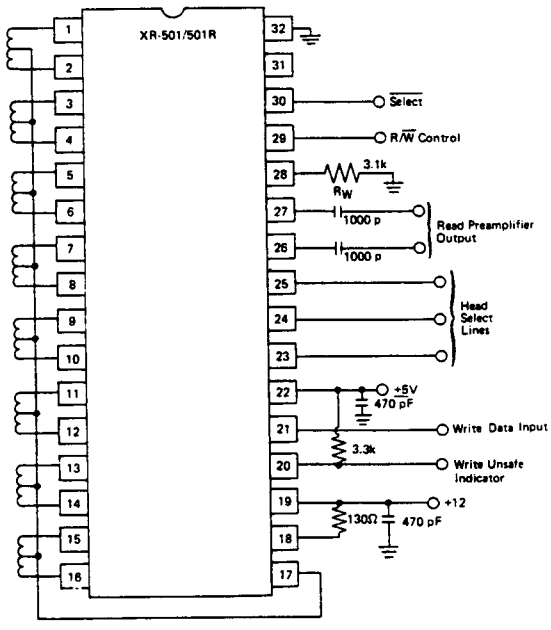
Read Mode Design Considerations

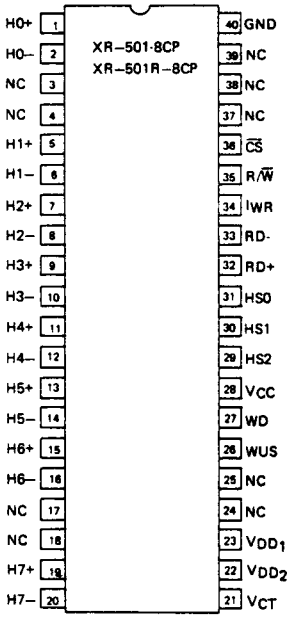
The read amp has a fully differential input and output and provides approximately 100 V/V gain. Its 60 MHz band- width and low noise characteristics (1.0 nV/ √Hz typical) provide substantial margins in most drives. The output should be AC coupled to delete the approximately 5.5 V output common mode voltage. Best results are obtained by limiting load capacitance to 20 pF and load current to 100 µA.

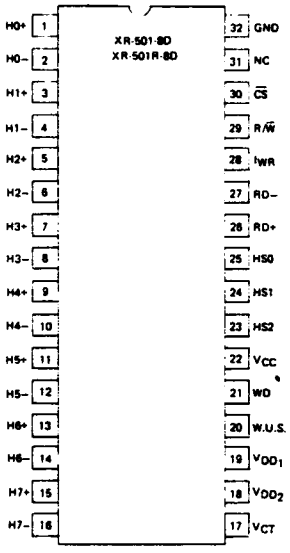
The XR-501 read preamplifier is specially designed to minimize output common mode voltage changes between write mode and read mode, thus reducing switching transients that slow write to read recovery time.

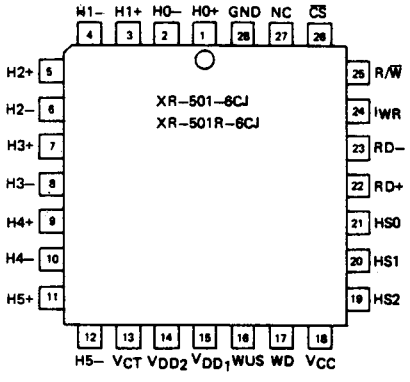


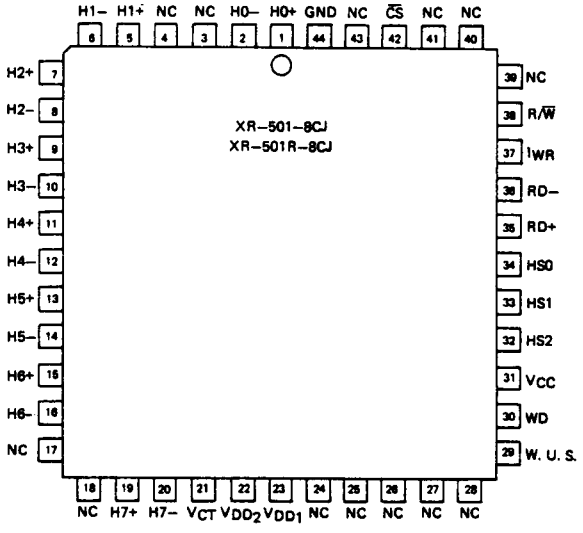
XR-501R Typical Application Circuit

NOTE: Non 'R' Versions Require External Damping Resistors









XR-501-6CP/501R-6CP/501-6D/501R-6D 28 Pin Package Pinout shown on front page.